CEPC Silicon Tracker Progress Report (19)

Qi Yan *on behalf of the Silicon Tracker Group*

Feb 11, 2025, IHEP

Progress on Silicon Tracker Ref-TRD

Chapter 5 Silicon Trackers

>90% of the content has been revised and completed.

We are working on the rest!

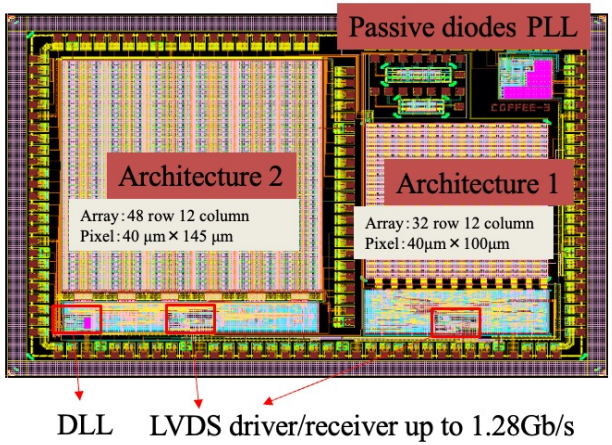
Remining Work on Silicon Tracker TDR

- <10% content needs to be completed and refined.
- Finish revision on the references and figure captions
- Finish silicon tracker group paper reading.

Thanks to Jingbo Ye for his TDR comments. We will take them into account properly.

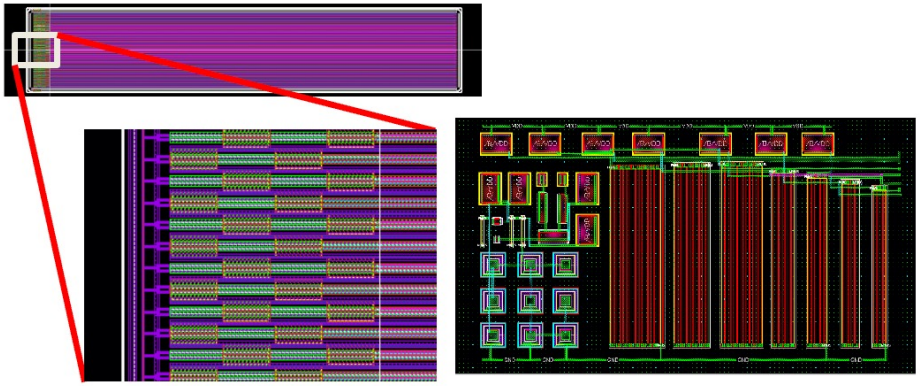
Sensor and ASIC R&D Plan

- HV-CMOS Pixels (COFFEE3):



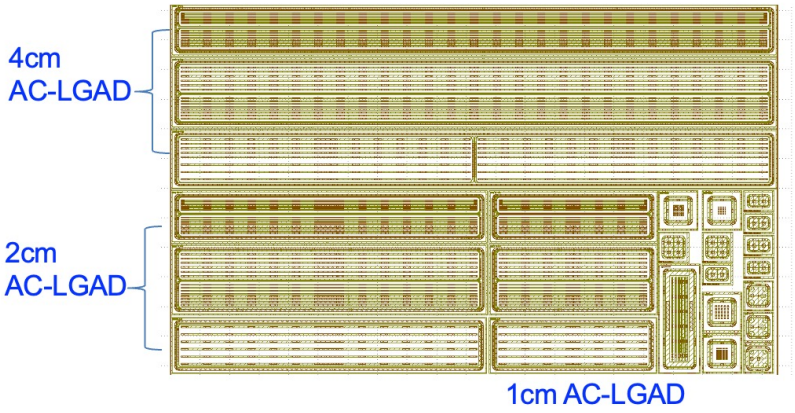
Submitted in 2025.1 and expected received in 2025.5

- CMOS Strips (CSC1):



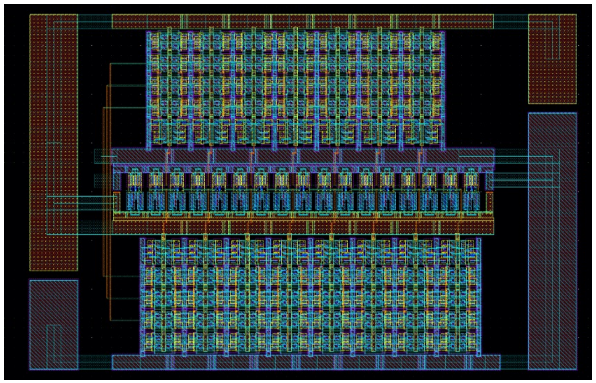
Scheduled for submission on March 5, 2025

- AC-LGAD Strips



Scheduled for submission in Feb 2025

- Pre-phototype for AC-LGAD ASIC (JuLoong, 烛龙)



Scheduled for submission in April 2025

Other R&D Plan

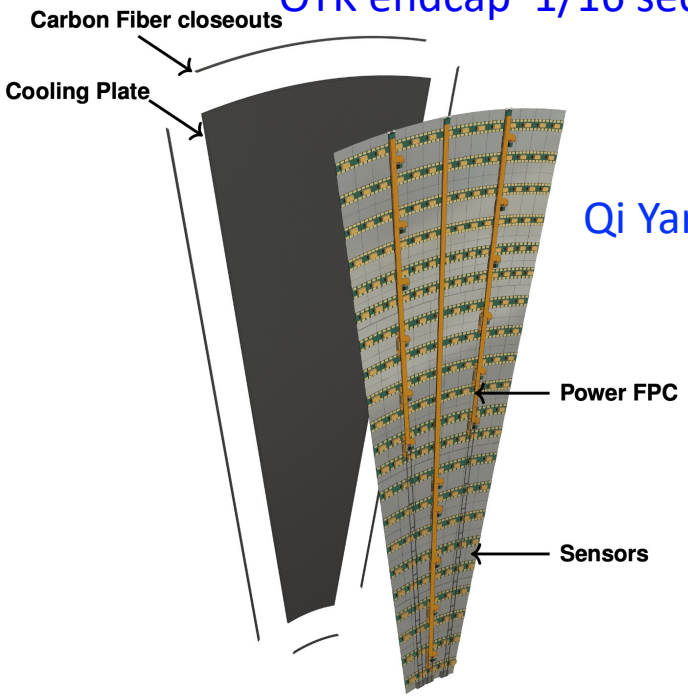
- Visit wafer foundries and semiconductor research institutions to explore direct collaboration and the development of sensor processes.

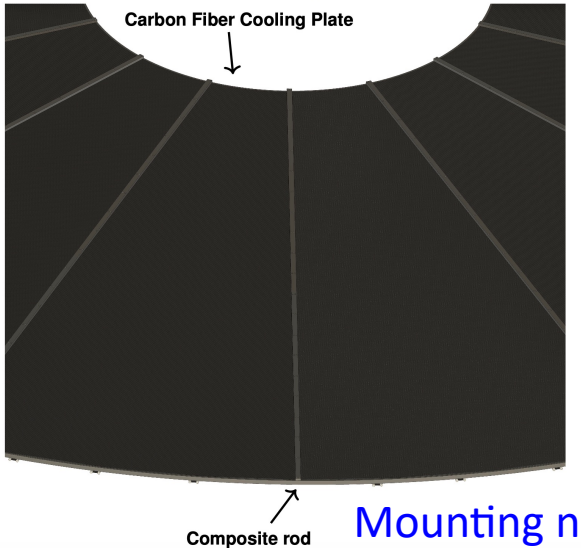
- Mechanical and cooling system development for the CEPC silicon trackers:
  - Collaborate with universities, especially their School of Energy and Power engineering, and industry partners to develop the system.
  - Build an STK mechanical and cooling laboratory at IHEP.
  - Partner with DRD8 and send young mechanical engineers for training at CERN in future (as pre-discussed with senior staff at CERN last year).

- Detector phototype module development.

Mechanical and Cooling Design for the OTK Endcap

OTK endcap 1/16 sector

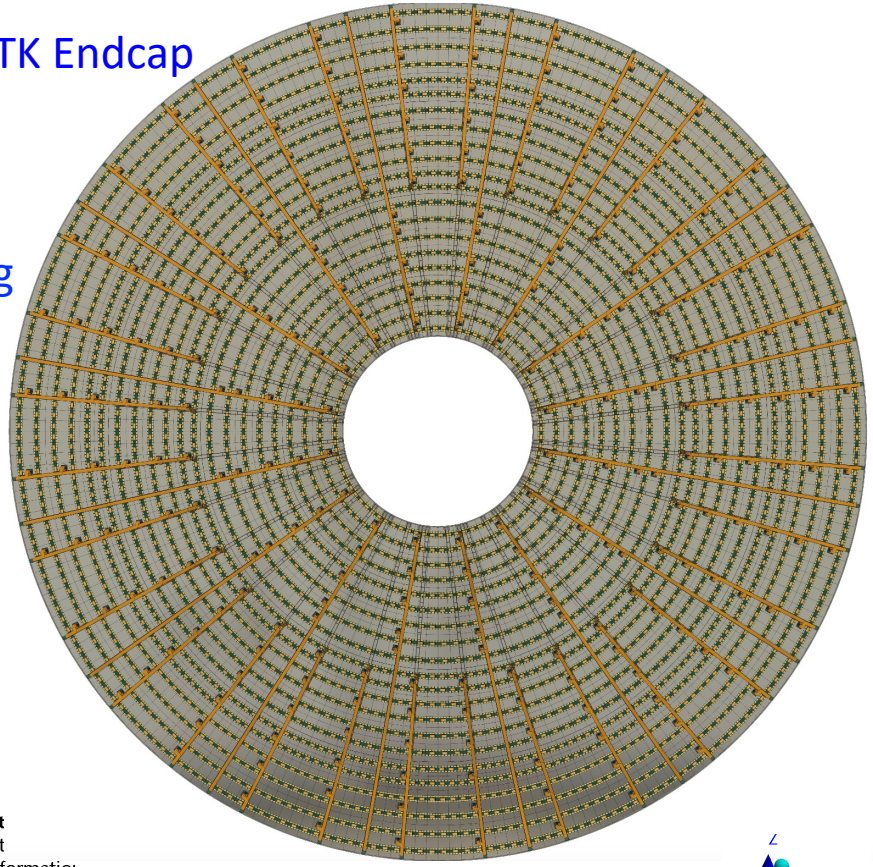


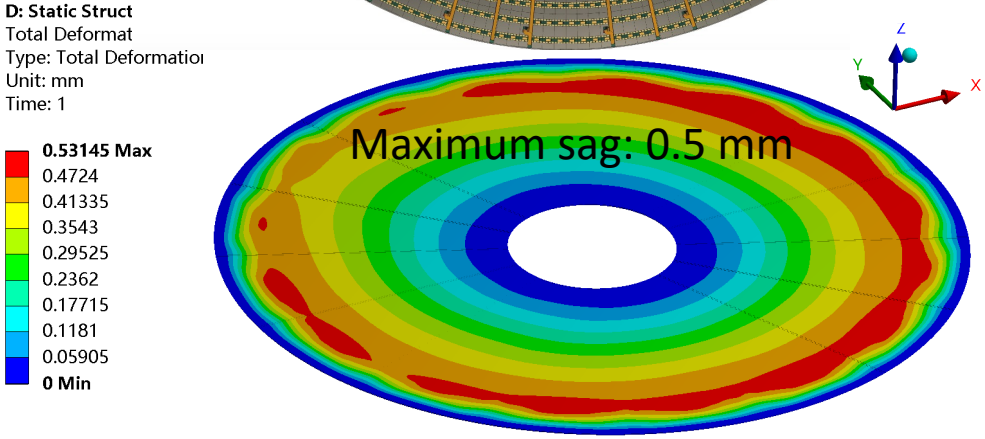


Mounting neighboring 1/16 sectors

Qi Yan *and* Yihan Zhang

OTK Endcap





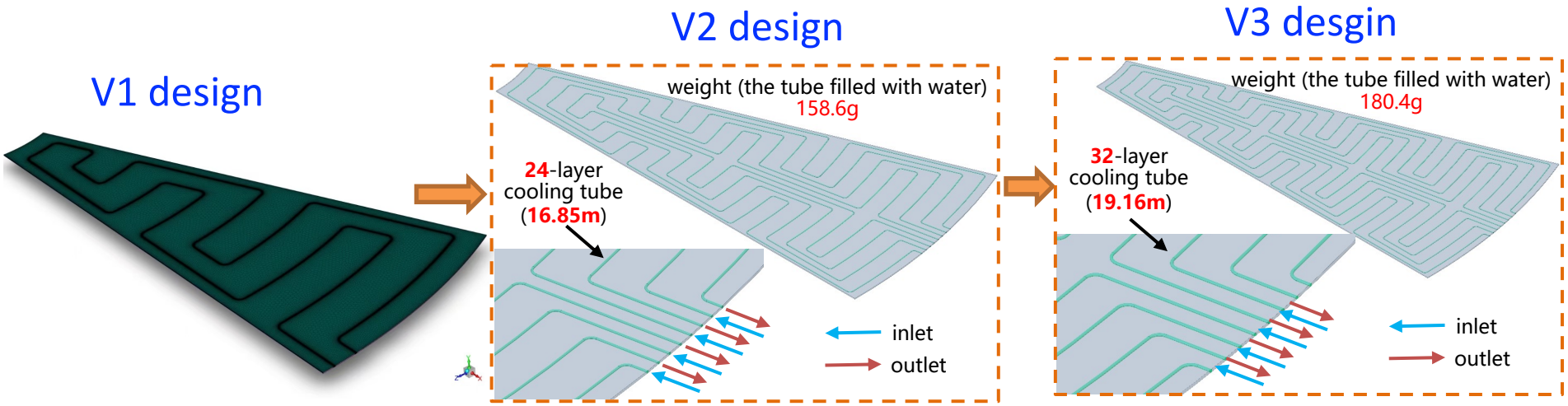
Yujie LI *and* Quan JI

Cooling Loop Design for the OTK Endcap

A few months ago, Quan Ji, Gang Li, and I visited Zhengzhou University of Light Industry, to explore ways to strengthen CEPC's R&D capabilities in mechanical and thermal systems.

The School of Energy and Power Engineering at Zhengzhou University of Light Industry has extensive experience and a strong focus on thermal system development, including CO_2 cooling. During our visit, we were highly impressed by their expertise in both thermal and mechanical engineering.

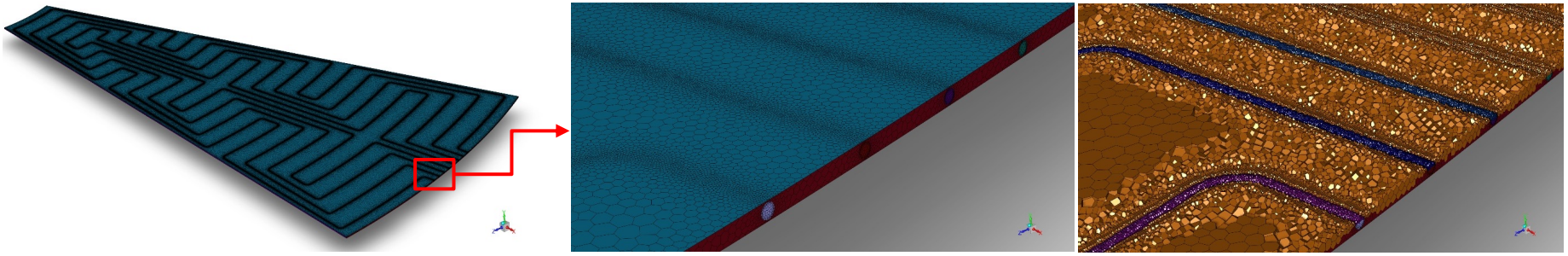
On Jan 10, the Dean of the School of Energy and Power Engineering, Professor Xuehong Wu, and his team, visited IHEP in return. They are now actively contributing to the design and analysis of the CEPC thermal system.



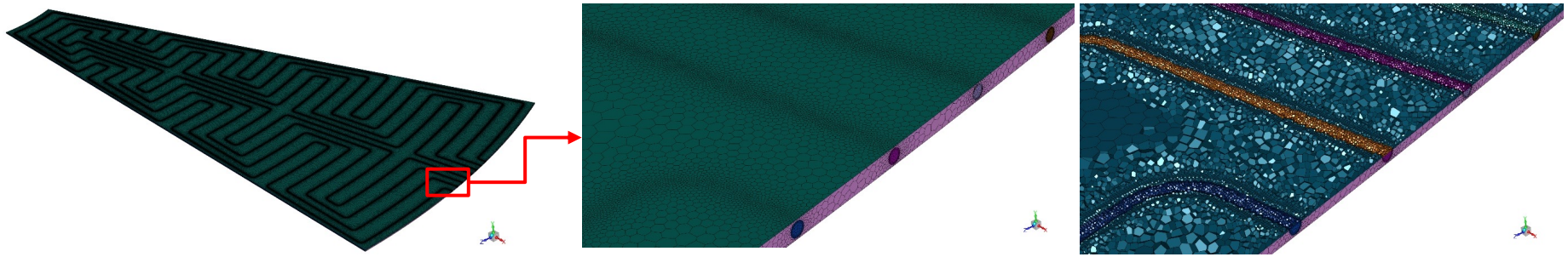
Cooling loops design and thermal analysis for the OTK endcap performed by Zhengzhou University of Light Industry（郑州轻工业大学）.

OTK Endcap Thermal Mesh Generation

ZHENGZHOU UNIVERSITY OF LIGHT INDUSTRY



24-layer cooling tube(16.85m, cell count 9356670，Orthogonal Quality≥0.5)



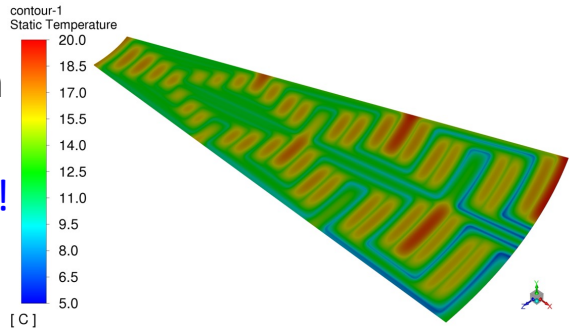
32-layer cooling tube(19.16m, cell count 10645946，Orthogonal Quality≥0.5)

- ✓ The mesh generation is performed for two different cooling tube arrangements, and numerical solutions are obtained using the finite volume method.
- ✓ The cooling performance of both arrangements is analyzed and compared.

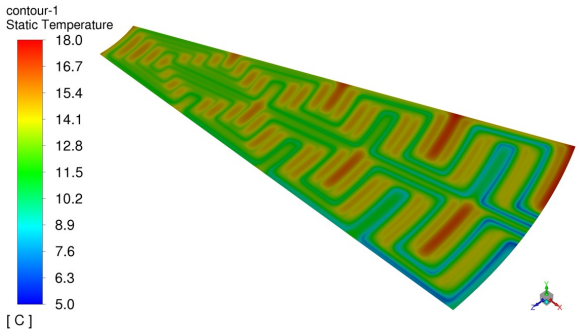
- Cooling tube diameter: 2.6 mm
- Water inlet velocity: 2.5m/s

Continuous optimization is ongoing!

Xuedong Wu, Yong Liu, ...
(郑州轻工业大学)



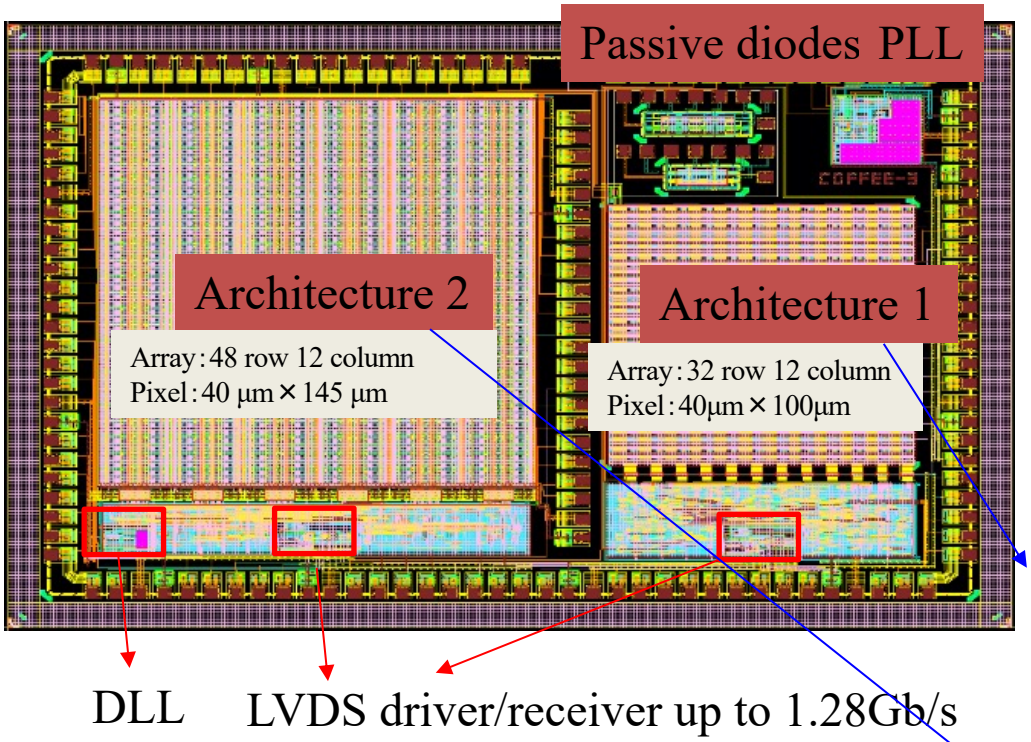
24-layer cooling tube



32-layer cooling tube

Progress on COFFEE3 Development and Submission

Submitted 2025.1/ expected received 2025.5



- In-pixel electronics;
- Pix matrix readout strategy;
- Periphery digital logics and functional IPs;
- Slow control & Fast control….
- Data/Power/CLK interfaces……

……

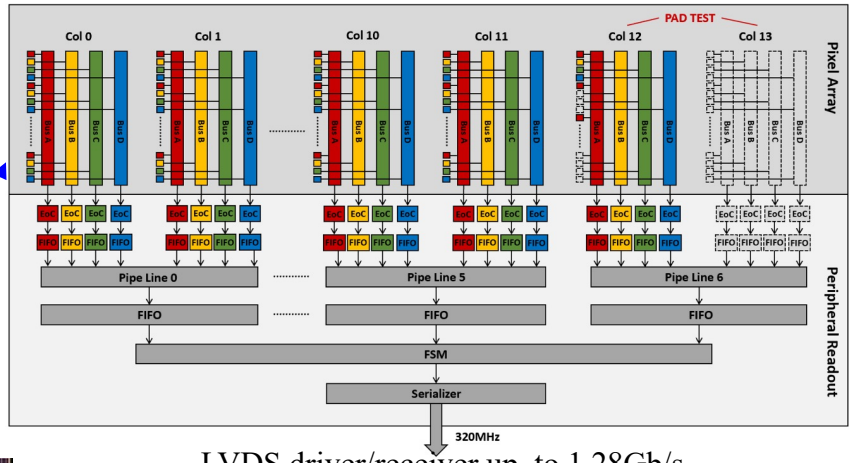
Two readout architectures:

Both include nearly a complete ASIC readout framework, and the solution can be extended to a full-size chip.

Each pixel can independently adjust its threshold through SPI (4-bit in-pixel DAC) and configure the mask.

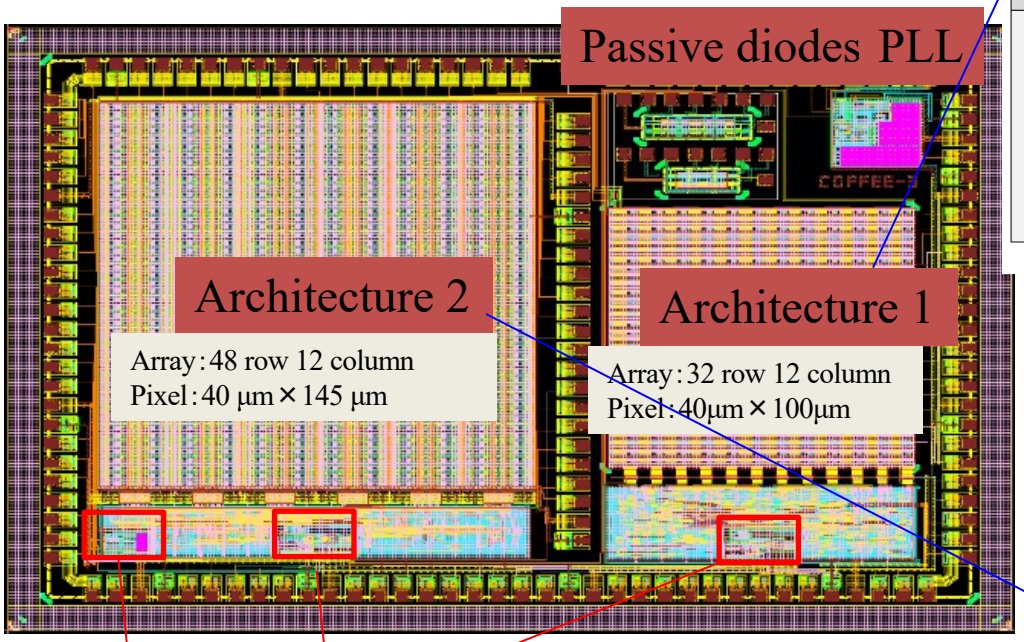
- **Architecture 1:** the optimized design framework based on current process conditions (Triple-well process);
- **Architecture 2:** an improved solution, while requires process modification. (Deep P-well required); fully utilize the advantages of the 55nm process node,.

Architecture 1: NMOS Pixel Array Schematic Diagram



LVDS driver/receiver up to 1.28Gb/s

COFFEE3 architecture 2:

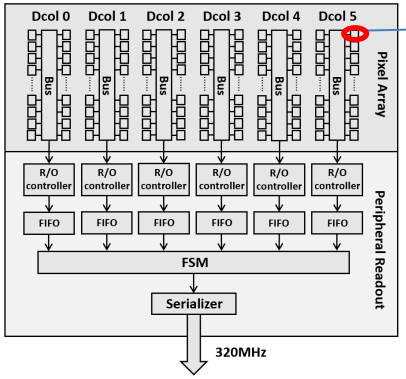


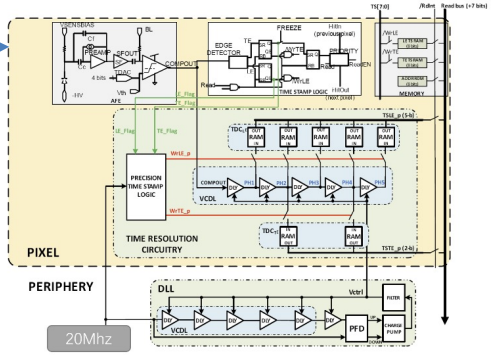
- In-pixel NMOS based comparator, in-pixel 4-bit DAC for threshold tuning;
- Time information (TOA, TOT…) and data formation in the end of each column;
- Improved capability to manage high incident conditions;

Architecture 2: an improved solution, fully utilize the advantages of the 55 nm process node

DLL

LVDS driver/receiver up to 1.28Gb/s





- In-pixel Coarse-fine TDC and 4-bit threshold tuning;
- ToA and ToT information are saved in each pixel;
- Data-driven readout;

LVDS driver/receiver up to 1.28Gb/s

Prototypes in 55 nm HV-CMOS Process

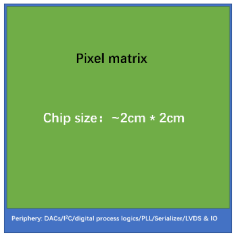
Several MPWs to reach the full-size full-function sensor

COFFEE

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

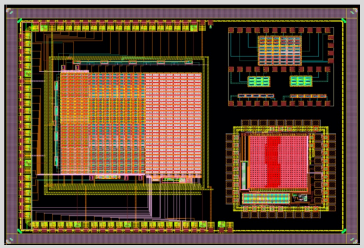
2023 → 2027 Time line

3×4 mm² | 3×4 mm² | ¼ of the full size

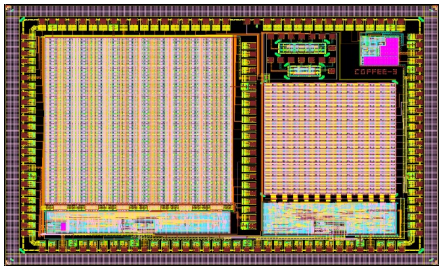


HV process

COFFEE2



COFFEE3

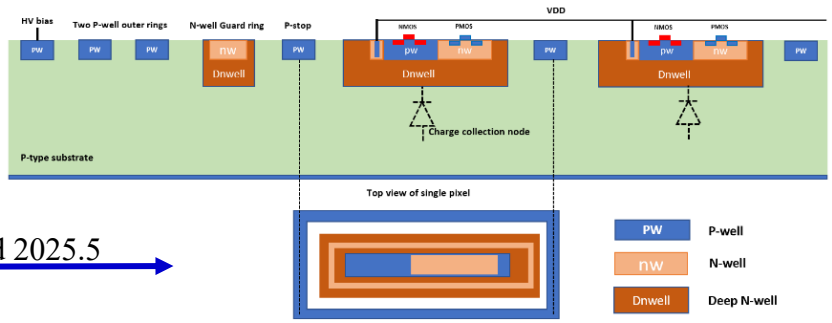


Submitted 2023.8/received 2023.12 Submitted 2025.1/ expected received 2025.5

Process characteristics & Technology validation

- In-pixel electronics;
- Pix matrix readout strategy;
- Periphery digital logics and functional IPs;
- Slow control & Fast control….
- Data/Power/CLK interfaces……

……

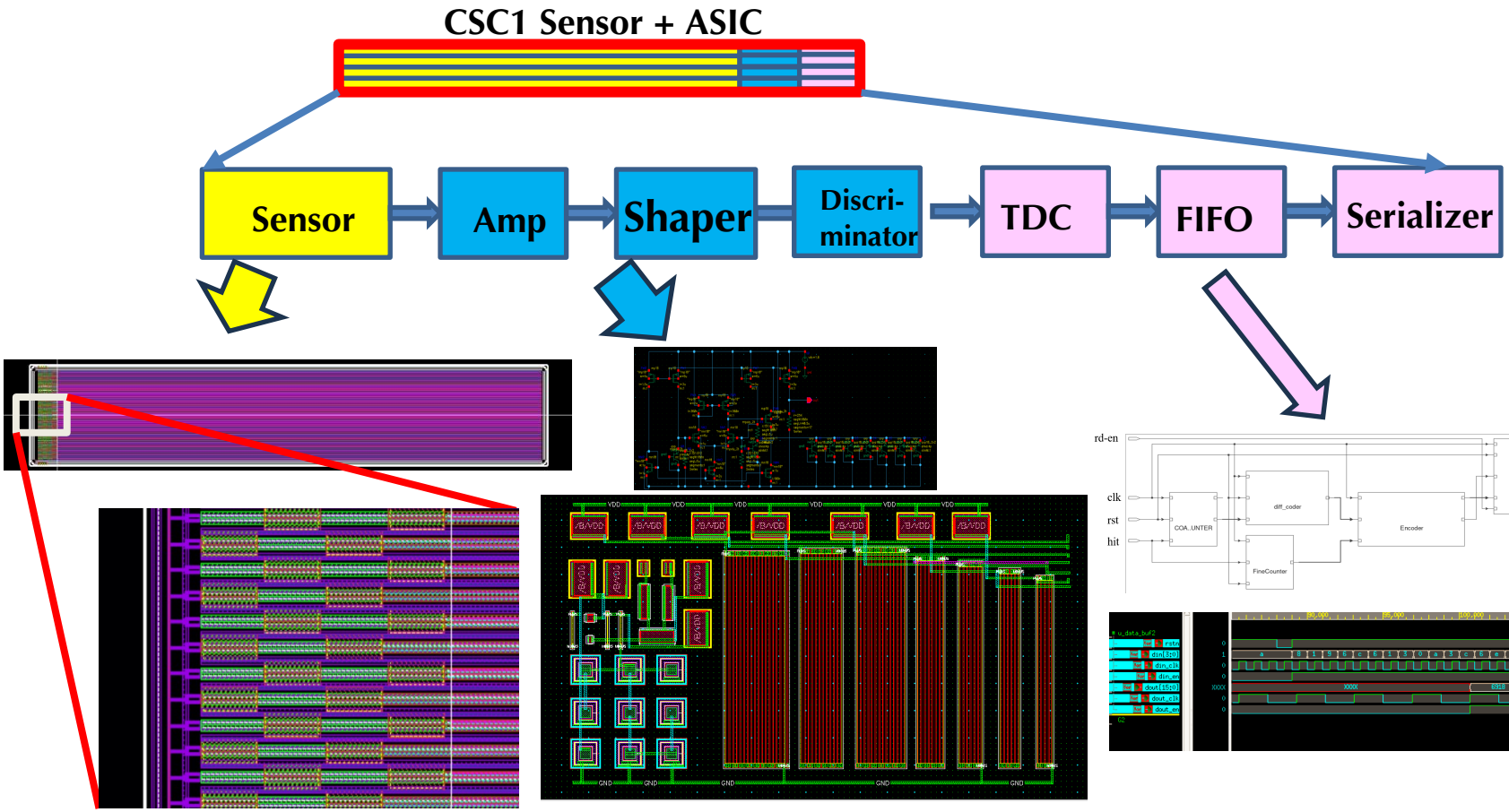


HV-CMOS process cross-section diagram showing the guard ring and pixel structure.

COFFEE3芯片设计团队：15 designers

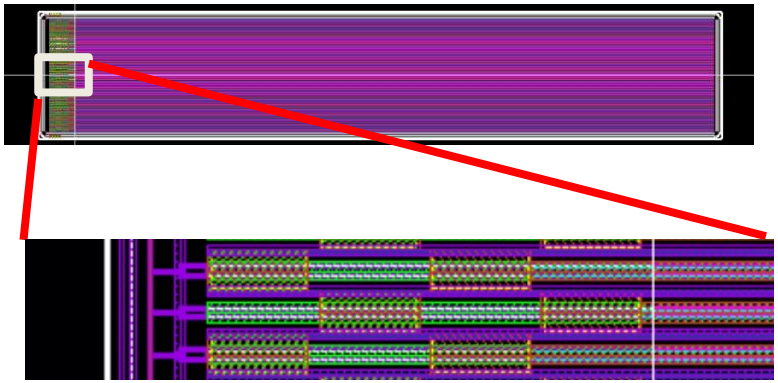
- **高能所**：李乐怡（山东大学/高能所）、张晓旭（南京大学/高能所）、赵梅、陆卫国、周扬；
- **西北工业大学**：吴慧敏、赵泽煊、赵宇、魏政、魏晓敏；
- **浙江大学**：邓建鹏、李鹏戍；
- **大连民族大学**：陈洋、王雨颉、施展；

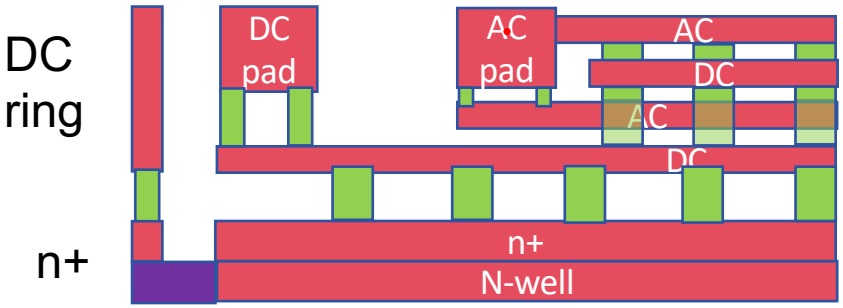
Progress on CMOS Strip Chip (CSC1) Development

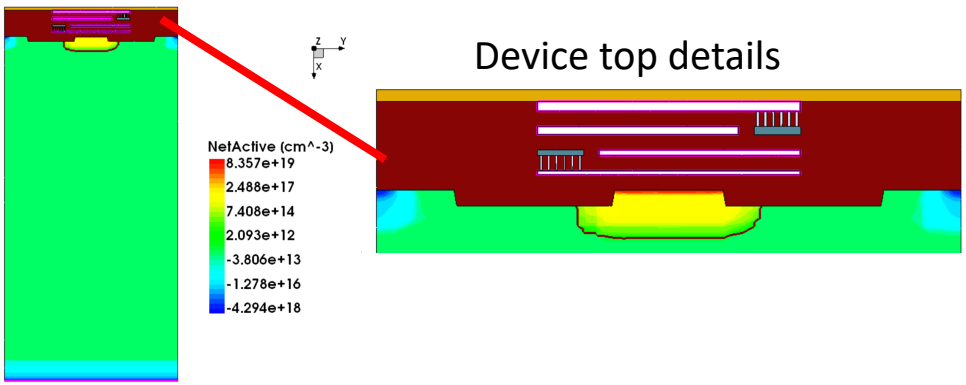


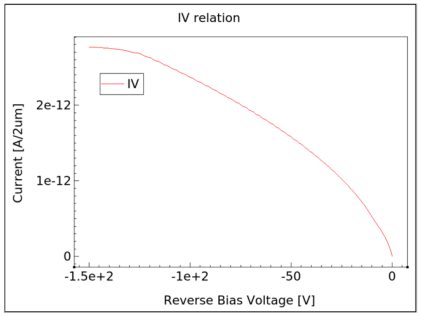
CMOS Strip Sensor Design and Simulation

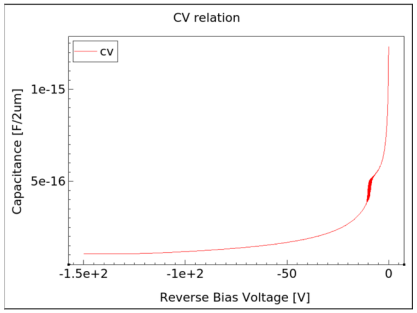
- Foundry: CSMC CMOS (1P4M)
- Sensor Size: 20.000 mm × 3.486 mm
- Strip length: 19.716 mm, pitch 75.5 μm
  - n-well:18 μm, n+: 15 μm
  - p-well: 4 μm, p+: 2 μm
- pad area: 75 μm × 180 μm
- Number of channels: 40
- n-well to bias ring via well-resister
- Two n+ guard rings
- Doping concentration









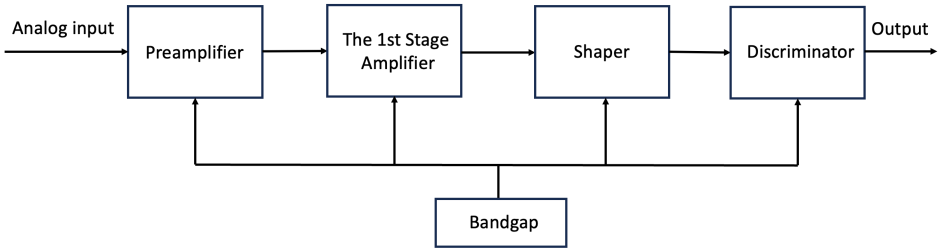


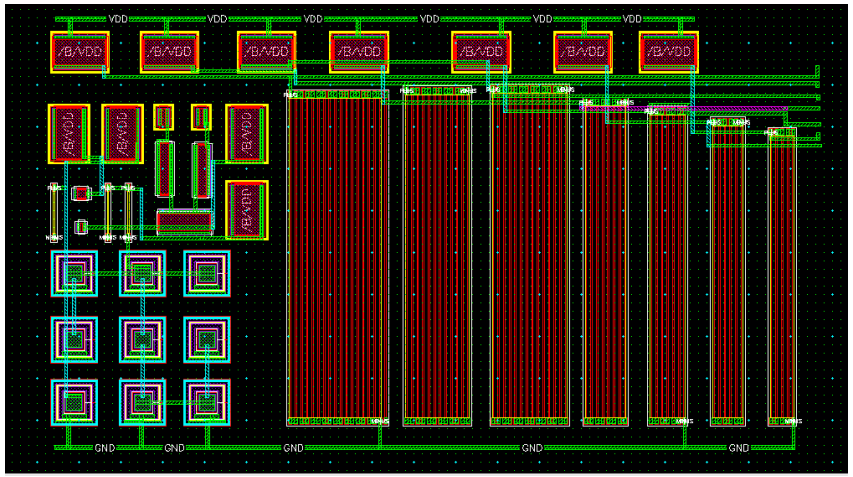
IV/CV results consistent with existing data*

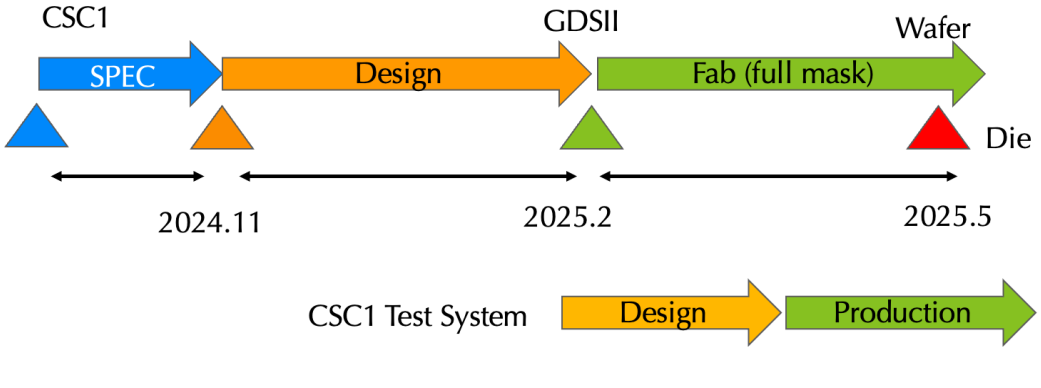
* Diehl et. al, Characterization of passive CMOS strip sensors, NIMA 1033 (2022) 166671

Analog Frontend Design Status and CSC1 Submission

- Completed the design of Analog Frontend (AFE): Preamplifier, the 1st stage amplifier, shaper, discriminator, and bandgap.
  - Circuit design, layout design, pre-simulation, and post-simulation
- Completed the overall Design Rule Checking (DRC), Layout Versus Schematics (LVS) checks.







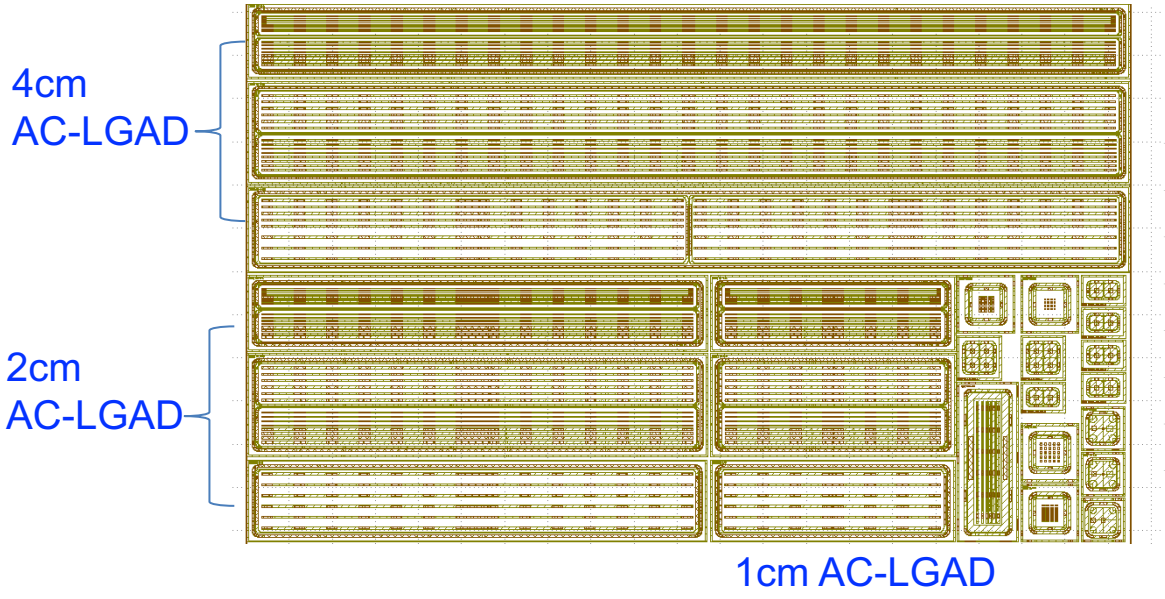
CSC1

- Working on the TDC
- Target for submission by February

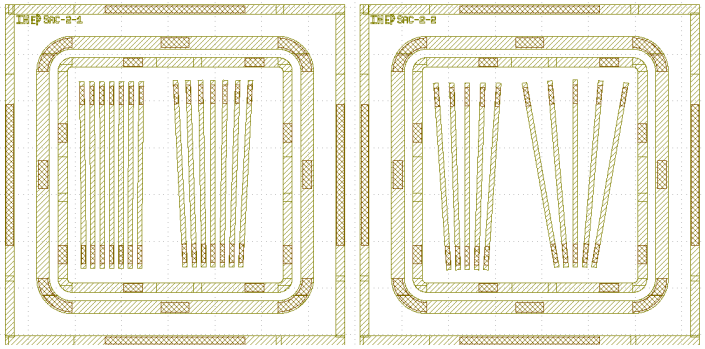
AC-LGAD Strip Sensor New R&D Design

New layout and design was done based on simulation. IHEP new AC-LGAD strip sensor prototype design for the CEPC OTK&TOF:

- Strip length： 1 cm, 2 cm, and 4 cm
- Strip pitch size: 100 μm, 200 μm, and 500 μm
- Optimized isolated structure design to reduce sensor capacitance
- Process design optimized for better spatial resolution (n+ layer dose)

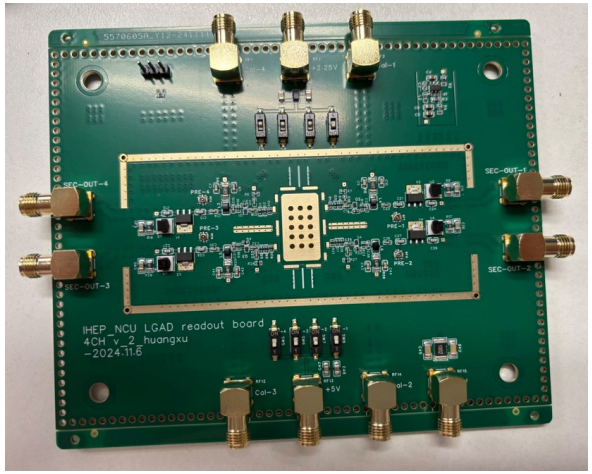


Sector shape AC-LGAD for endcap



AC-LGAD Sensor Readout Board Preparation

- 4-channels readout boards has been fabricated for AC-LGAD testing
- 2-stage amplifiers, Gain~70
- Signal shape has significantly improved, showing no oscillations.



AC-LGAD Strip Sensor Development Plan

Short term plan: 2024.12-2025.2

Simulation: ongoing

- Simulation of Strip length and its effect (signal shape)
- Simulation to reduce capacitance (isolation structure)
- Simulation of process parameters to optimize spatial resolution (AC coupling capacitor, n+ dose)

Testing:

- Multi-channel readout board with low noise design and fabrication (2 stages of amplifier) **done**
- Testing of short strip connected, radiation testing(TID) **ongoing**

Submission 1: 2025.2 (layout design is done, process simulation ongoing)

Strip AC-LGAD with different length and pad-pitch size: [1 cm, 2 cm, 4 cm] [100um, 200 um, 500 um]

- Strip AC-LGAD with different process parameters: n+ dose, dielectric material and thickness, …
- Strip AC-LGAD with different isolation structure →Capacitance
- Sensors with EPI layer of different thickness (50 um, 65 um, 80 um, 300 um)

Sensor Testing:

- clarify the sensors performance and requirement (include test beam and radiation test)
- Find out how to optimize the sensor performance (structure and process)

Submission 2: 2025.10

- Based on the results from first version and more simulation
- Sensors with strip length ~4cm

Sensor Testing: basic properties and test together with ASIC and BEE

Submission 3: 2026.6

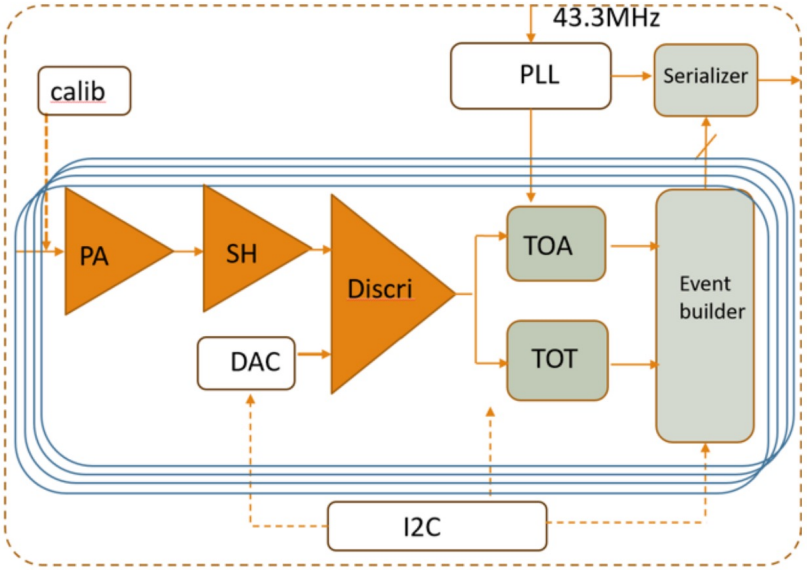
- large area sensor design and fabrication

Submission 4 if needed: 2027.2

- module: built sensor + ASIC module and test

OTK AC-LGAD Readout ASIC (JuLoong, 烛龙)

- Functions:
  - TOA (Time of arrival) for precise time and TOT (Time over threshold) for time walk correction and accurate position determination.
  - Each channel includes preamplifier, discriminator, and Time-to-Digital Converter (TDC).
- Requirements:
  - 128 channels, channel pitch less than 100 μm.
  - Single channel power consumption less than 20 mW.
  - Time resolution for TOA better than 30 ps.



JuLoong diagram

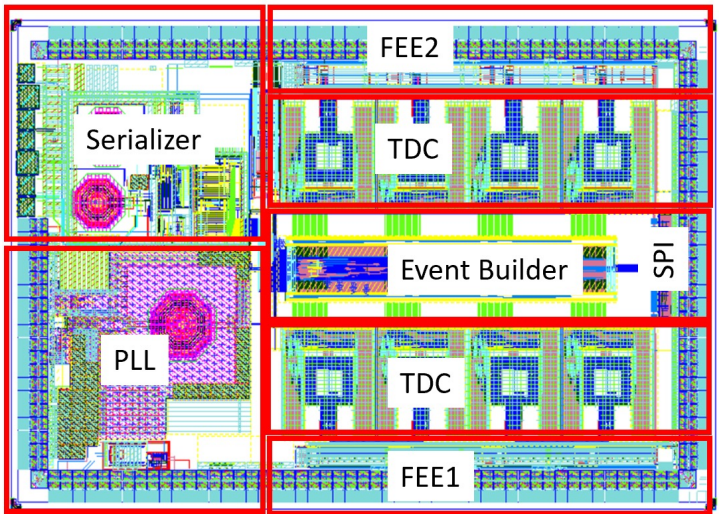
OTK AC-LGAD ASIC Development Progress

Several key cells are designed or verified:

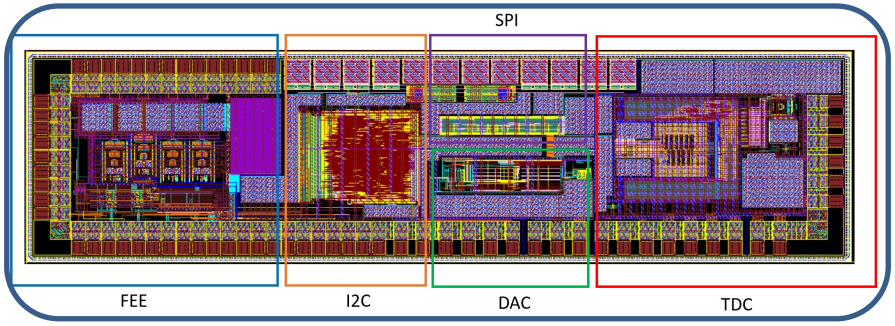
- FPMROC (10 ps) chip
  - FEE: Preamplifier+Discriminator

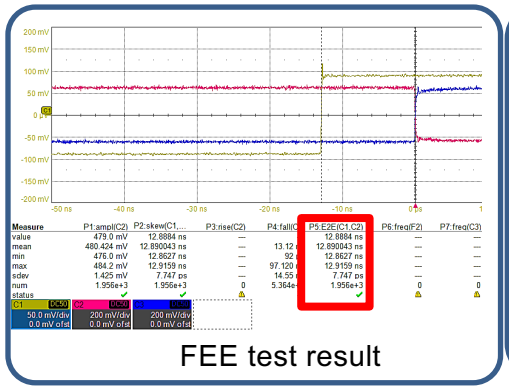
    jitter<7.8ps @ input 2.5mV, t_r=0.1ns, Cs=0 pF

    (need to be test with real LGAD sensor)
  - TDC core needs a new design
  - PLL, Serializer, SPI is verified but need to be simplified
- I2C Slave: ASIC parameter configuration
- 12-bit DAC: threshold and calibration

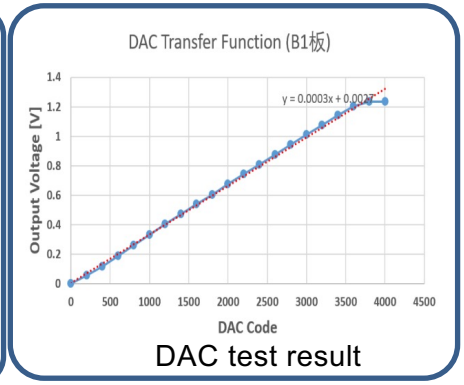


FPMROC





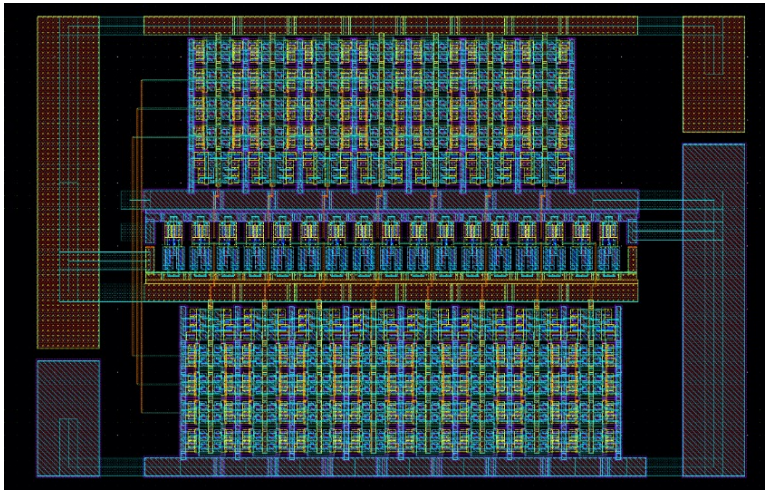
FEE test result



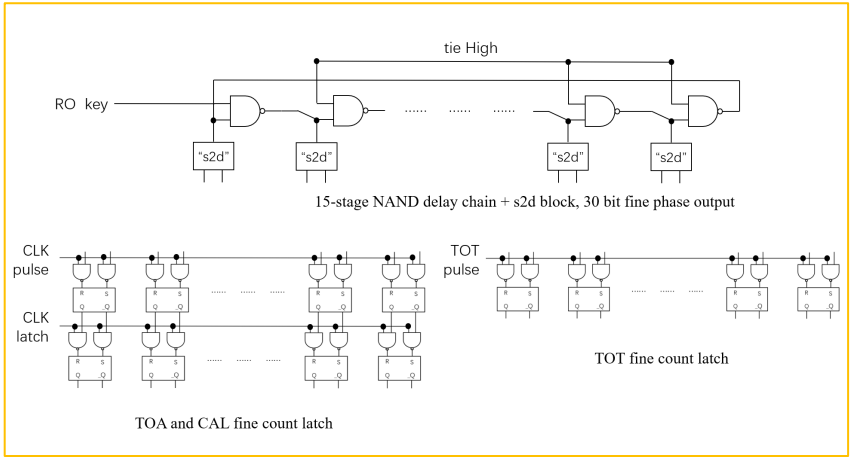
DAC test result

OTK AC-LGAD TDC Core Design

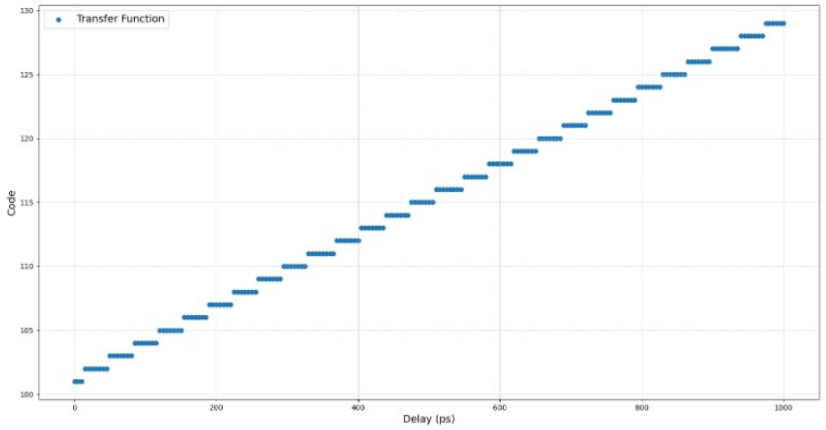
- Event driven delay line to reduce the power
- Real time Calibration for PVT (Process, Voltage, Temperature)
- LSB ~36 ps for preliminary layout post-simulation
- Power Consumption：
  - Average current for single event: 443 μA
  - Static current: < 5μA



Delay line layout



Single-Channel Delay Chain and Quantization Block Diagram



TOA transfer function curve (step=5 ps, TT27)

OTK AC-LGAD ASIC (JuLoong) Development Plan

- 2025.4: Design key components, including preamplifier, discriminator, and TDC, along with the design of the ASIC test system. Performance testing of the ASIC will be conducted by the end of the year, with radiation hardness testing for each component.
- 2025.7: Conduct components performance test.
- 2025.10: Refine components and complete the first version of multi-channel integration.
- 2026. 2: Performance test on the multi-channel ASIC, including radiation hardness testing.
- 2026. 6: Further refinement and integration of 128 channels.
- 2027.10: Performance testing of 128 channel ASIC will be conducted, integrated with LGAD sensor.
- 2027.12: Finalize the prototype and prepare for mass production of the chips.