Front End Electronics for Tracker

Yan Xiongbo

Content in TDR

ITK

5.3.3 Readout electronic

OTK

5.4.3 Readout electronic

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- 5.4.3.2 Concentrator Card and power distribution
- 5.4.3.4 Clock distribution

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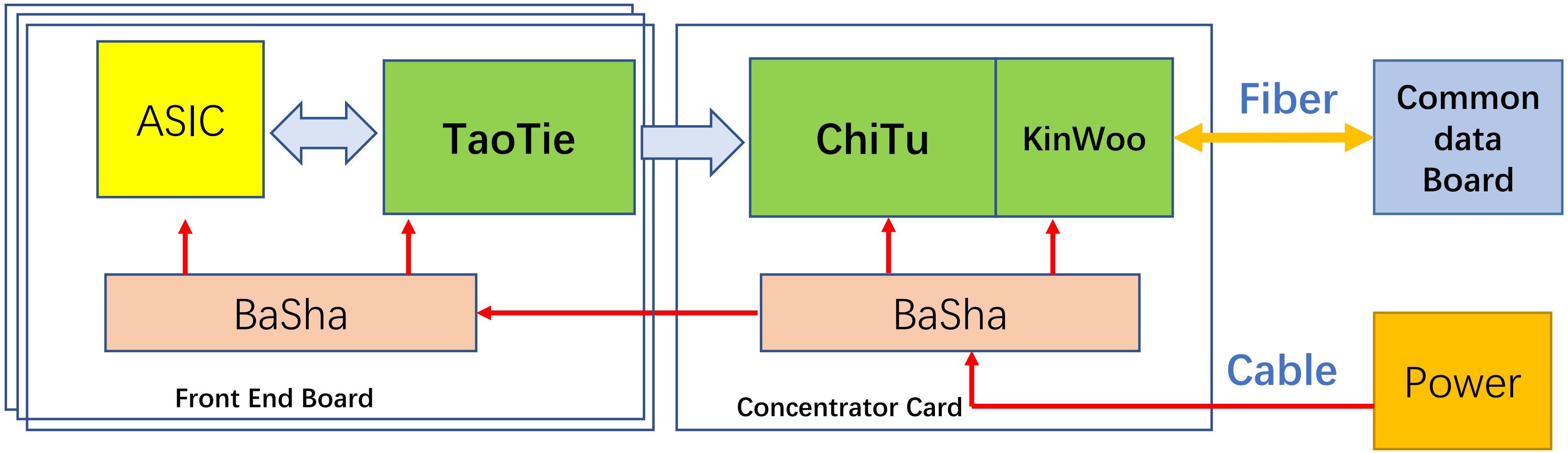
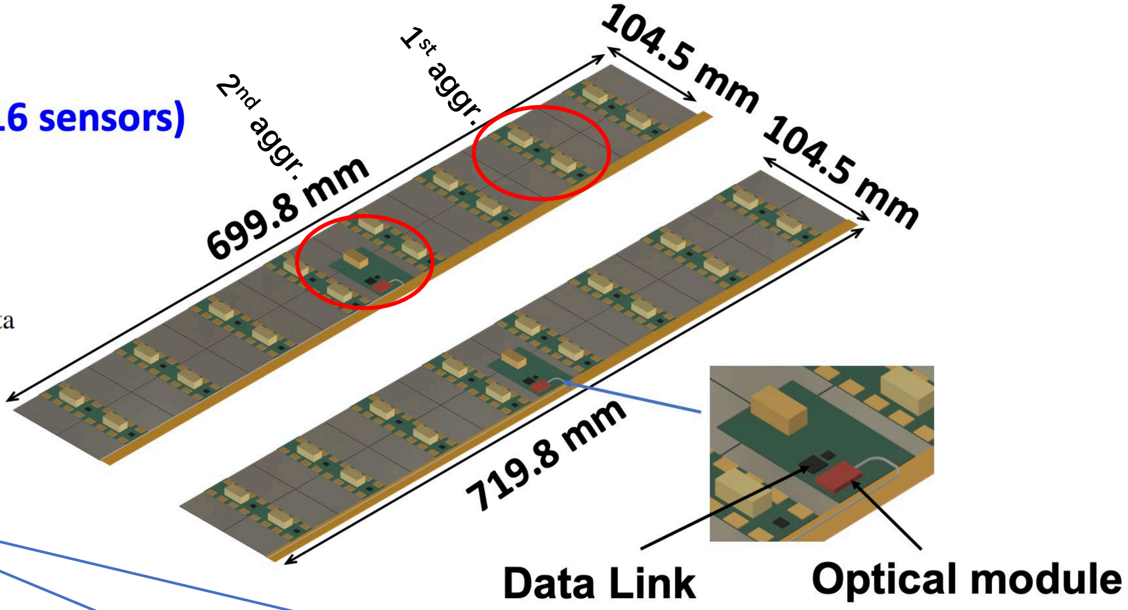
Section 5.4.3
OTK readout electronics



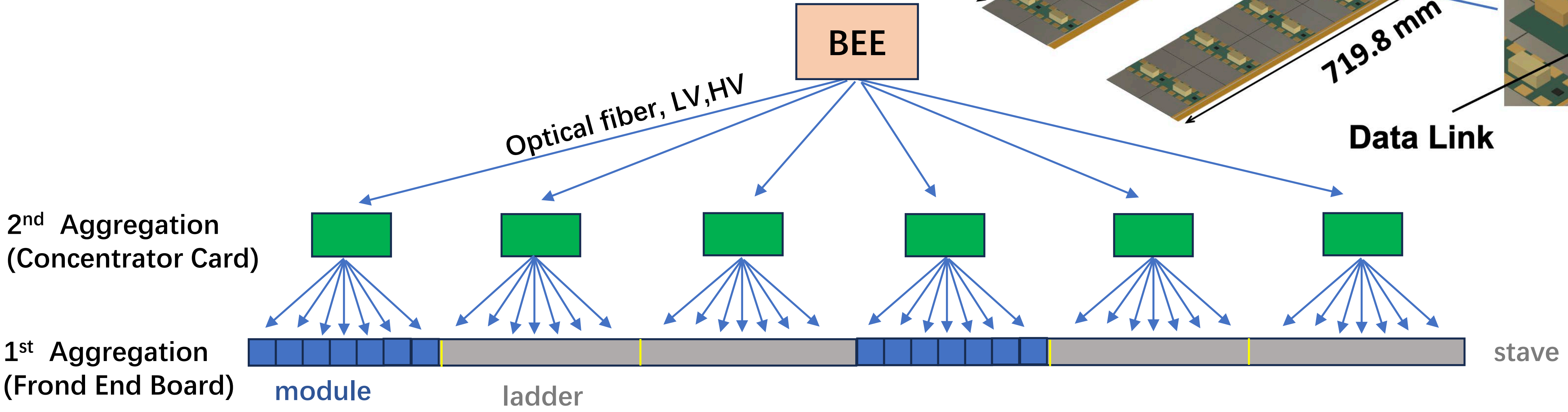
- 主要考虑探测器近端ASIC的供电方案和数据汇总方案
  - 电源采用层级降压，减少器件数量
  - 为提高传输效率，数据采用分级汇总，光纤输出
  - 光纤以后的电子学属于通用系统电子学

前端电子学整体层级架构

16 sensors)



In the OTK baseline design, each FE board interfaces to the Concentrator Card (CC), also referred to as the 2nd data aggregation boards (see Fig. 5.90 (a) or Fig. 5.94 (a)), transferring the following signals:



- 电源和数据均采用二级架构
  - 第一级：产生1.2V电压，针对module前端芯片数据初步汇总、传输
  - 第二级：产生12V电压，为module提供时钟和慢控，针对Ladder数据汇总、传输

Section 5.4.3.1
Data transmission for OTK

- Clock: ChiTu (GBTx-link) e-clocks (43.3 MHz) for OTKROC ASICs;
- Data readout:
  - For a barrel FE board, 2 uplink e-links (each with 346.67 Mbit/s) from 2 TaoTie chips connecting to ChiTu on the CC.

数据率按1.39Gbps根据32 ASICs 数量分配计算

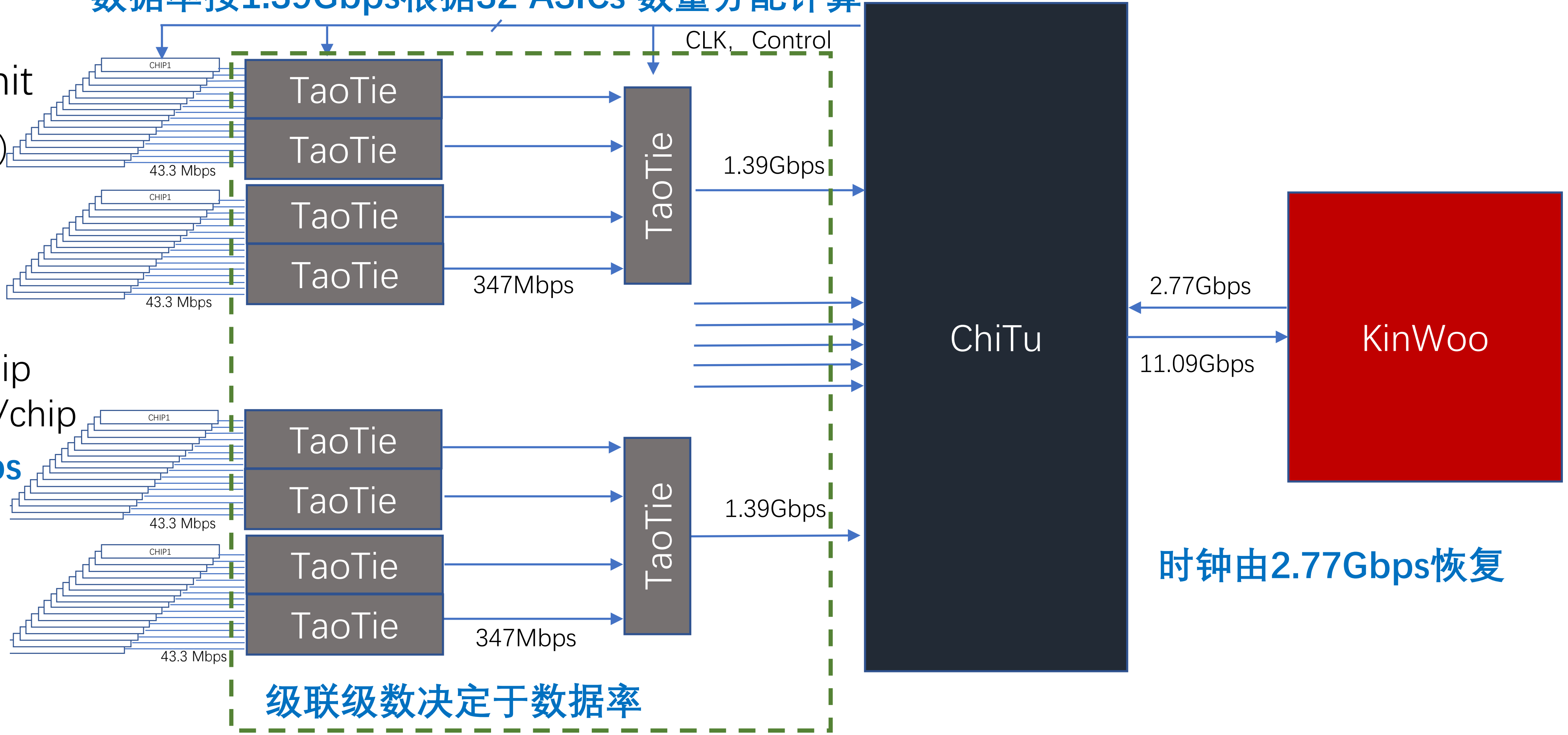
- Data rate： 40 bit/ hit

  17 bit (8 TOT, 9 TOA)
  + channel(7bit, 128)
  +bunch ID(8bit)
  + chip ID (5 bit)
- Hit rate：
  - Barrel: 90 KHz/chip
  - Endcap: 250 KHz/chip

数据率远小于43.3Mbps

Estimated Silicon Tracker Hit Rates [10^4 Hz/cm^2]	Low Lumi Z		Higgs		High Lumi Z	
	Average	Max	Average	Max	Average	Max
ITKB1	3.93	9.41	0.012	0.108		
ITKB2	2.04	5.26	0.019	0.202		
ITKB3	0.72	2.37	0.021	0.154		
OTKB	0.18	1.56	0.014	0.148		
ITKE1	10.63	58.70	0.151	1.052		
ITKE2	6.19	41.07	0.193	1.429		
ITKE3	2.45	24.80	0.166	1.427		
ITKE4	1.70	8.25	0.140	0.657		
OTKE	0.38	4.41	0.026	0.353		

Table 5.18: Estimated Silicon Tracker Hit Rates

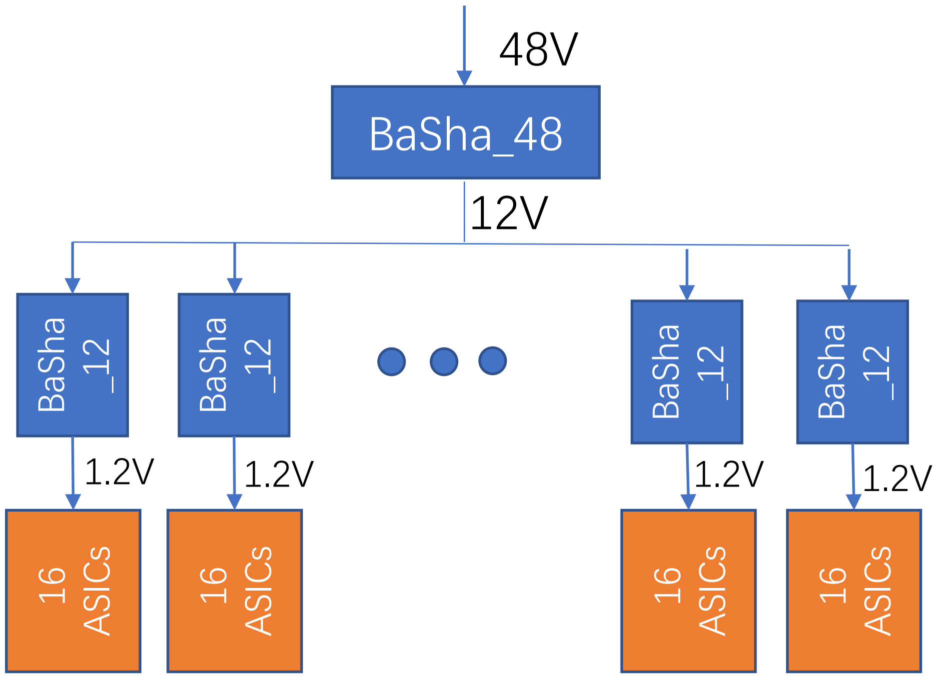


- TaoTie（可降频）
  - Input: 8 uplinks, 1 clk
  - Output: 1 uplink

- ChiTu
  - input： 7 uplinks （1.39Gbps）
  - Output： 16 downlinks， 16 clks

OTK Power Supply

- HV： 直接由机箱供电
- LV： 机箱供电48V
  - Basha_48: 48V->12V（10A）
  - Basha_12: 12V-1.2V（10A）/3.3V

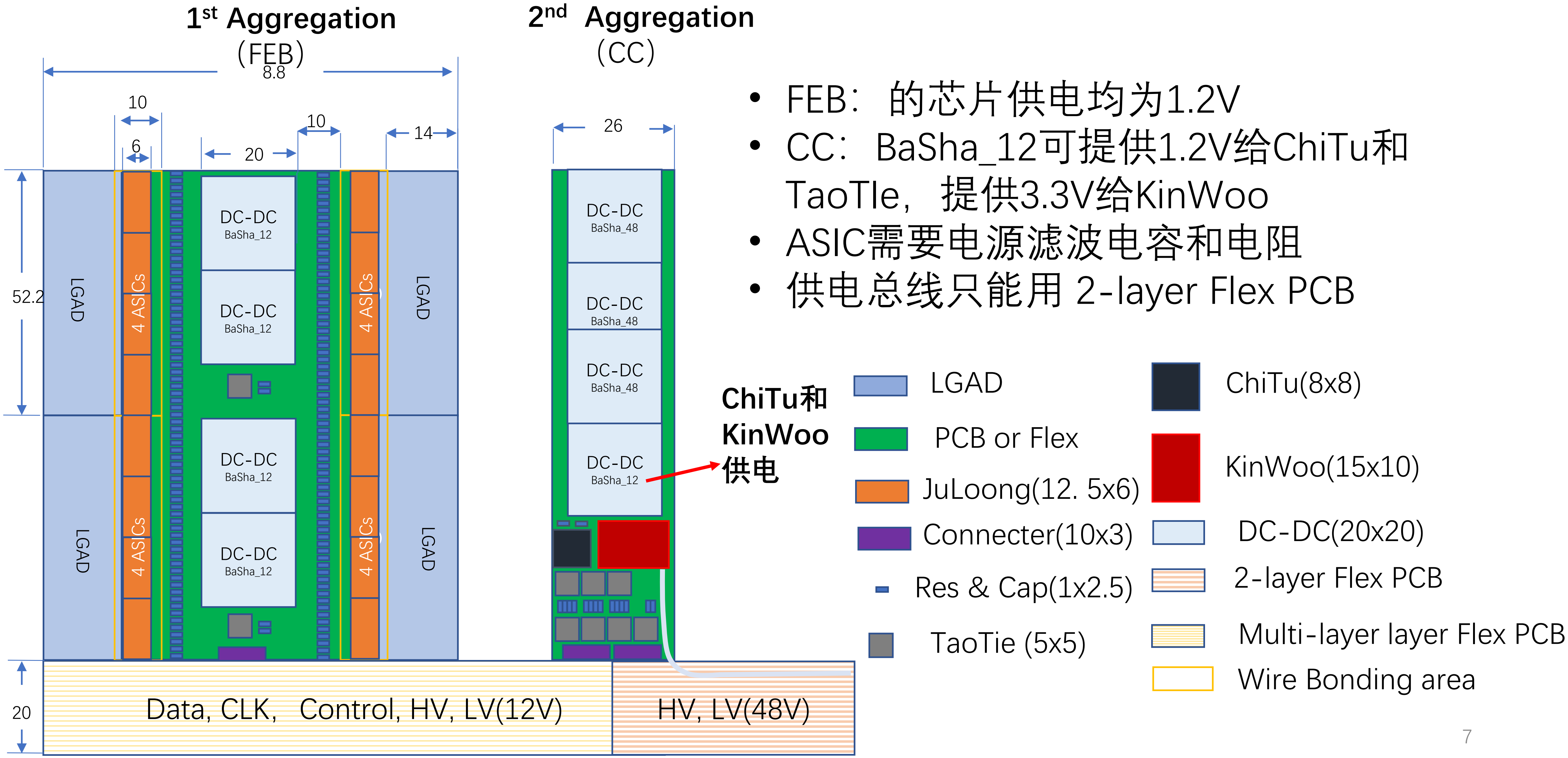


	输出功率
BaSha_12	12W
BaSha_48	120W

- LV供电
  - Flex线阻计算：
    R≈0.05Ω/m（h=35um, w=10mm copper）
  - 每个Module的供电电流2.5A（30W）
    2.5A电流的压约0.25V/m， 线损0.7W/m
  - 每个Ladder的供电电流5A，（240W）
    5A电流的压约0.5V/m， 线损2.5W/m，
    最长2.9m的线损7.5W

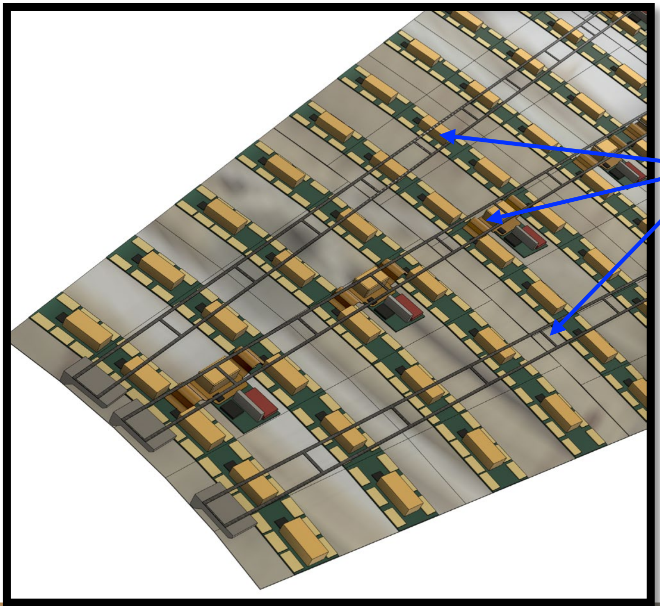
	按单位功率 20mW/ch	按单位功率 300mW/cm2
1 ASIC（128 chs）	2.56W	1.7W
1 Module（16 chips）	40.96W	27.4W
1 ladder (8 modules)	328W	219W

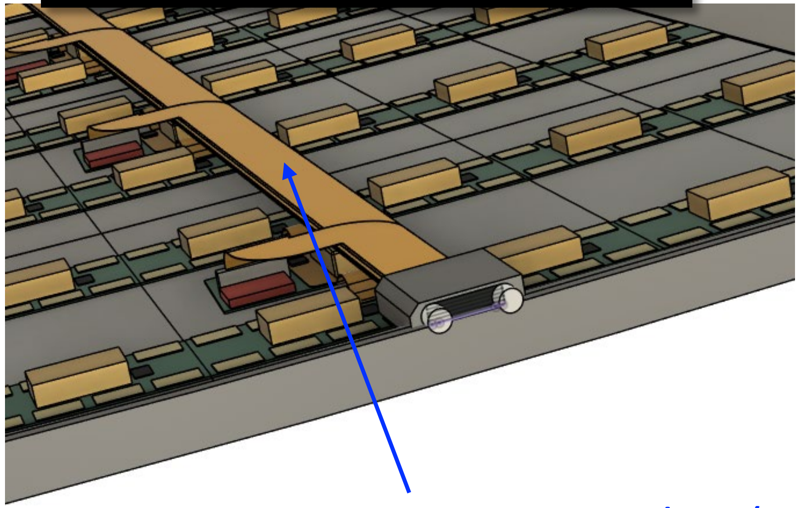
OTK Front End Board & Concentrator Card

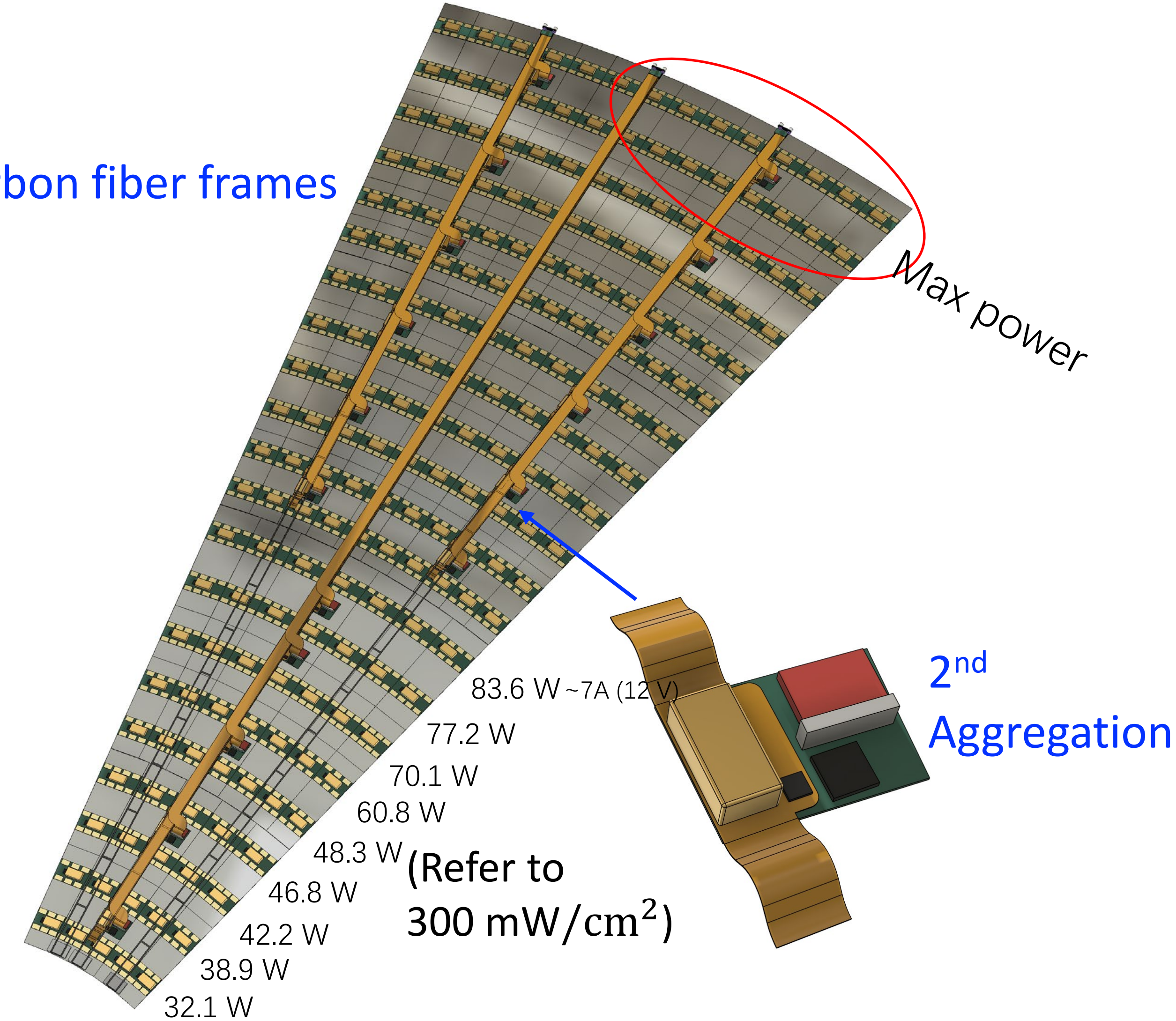


- FEB：的芯片供电均为1.2V
- CC：BaSha_12可提供1.2V给ChiTu和TaoTIe，提供3.3V给KinWoo
- ASIC需要电源滤波电容和电阻
- 供电总线只能用 2-layer Flex PCB

OTK Endcap layout -Power Buses on Frames







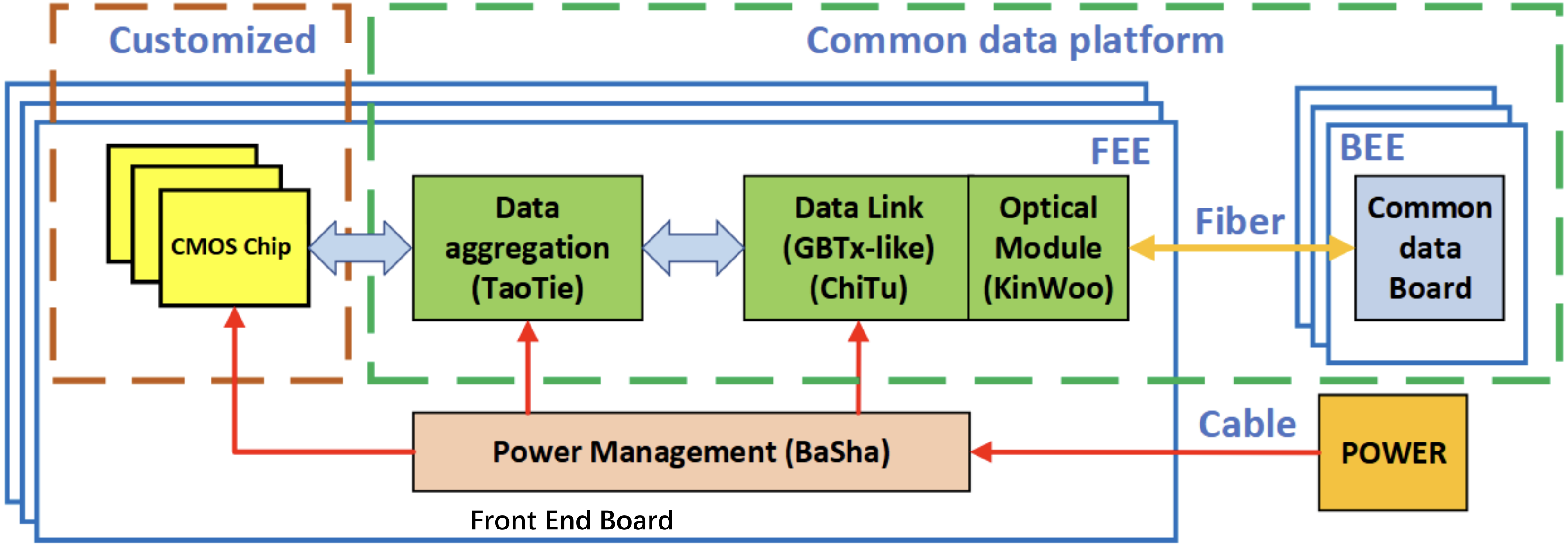
Power Bus transmits: HV and LV (48 V)

- 180 µm thick (with metal layer of 25 µm copper or aluminum) is more than sufficient
- Bus width is not limited

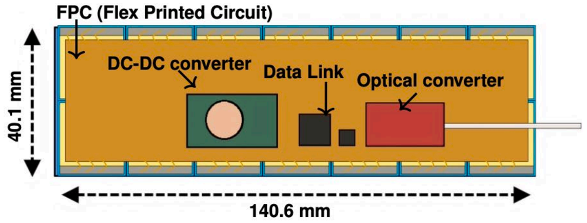
- Frame and Connector should be higher than bonding wire
- Max length: 1,330 mm
- Max power transmission: 4.8 A, 230 W

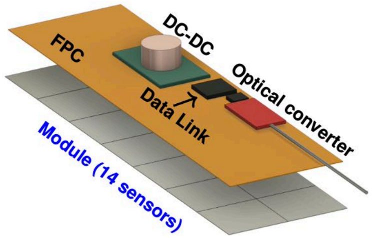
Section 5.3.3

ITK readout electronics



- 2级汇总架构集成在同一PCB上





Data transmission for ITK

- Data rate： 42 bit/ hit

  11 bit (6 TOT, 5 TOA)
  \+ adress(16 bit)
  +bunch ID(14bit)
  +polarity (1 bit)

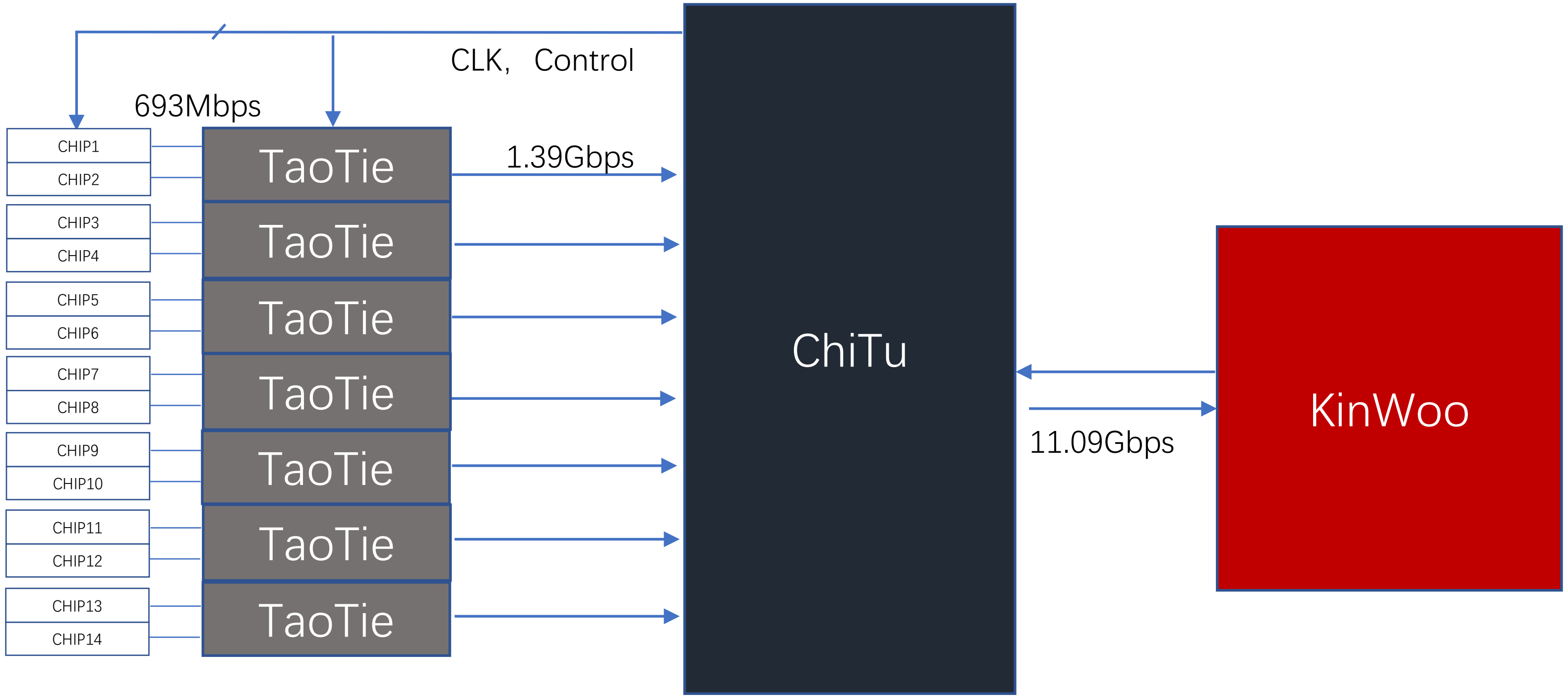
- Hit rate：
- Barrel: 370 KHz/chip
- Endcap: 2.35 MHz/chip

数据率远小于693Mbps

Estimated Silicon Tracker Hit Rates [10^4 Hz/cm^2]						
	Low Lumi Z		Higgs		High Lumi Z	
	Average	Max	Average	Max	Average	Max
ITKB1	3.93	9.41	0.012	0.108		
ITKB2	2.04	5.26	0.019	0.202		
ITKB3	0.72	2.37	0.021	0.154		
OTKB	0.18	1.56	0.014	0.148		
ITKE1	10.63	58.70	0.151	1.052		
ITKE2	6.19	41.07	0.193	1.429		
ITKE3	2.45	24.80	0.166	1.427		
ITKE4	1.70	8.25	0.140	0.657		
OTKE	0.38	4.41	0.026	0.353		

Table 5.18: Estimated Silicon Tracker Hit Rates

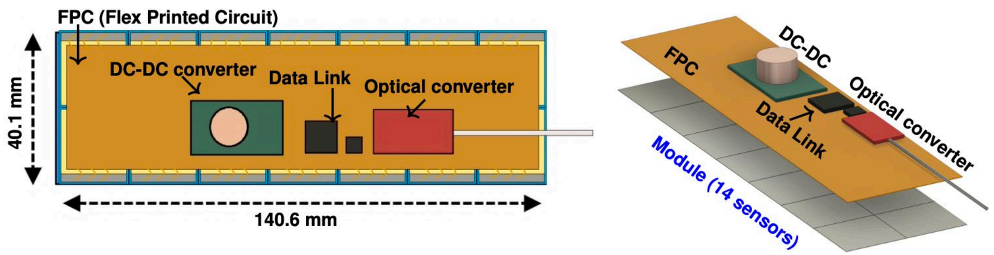
数据率按1.39Gbps根据Sensor 数量分配计算

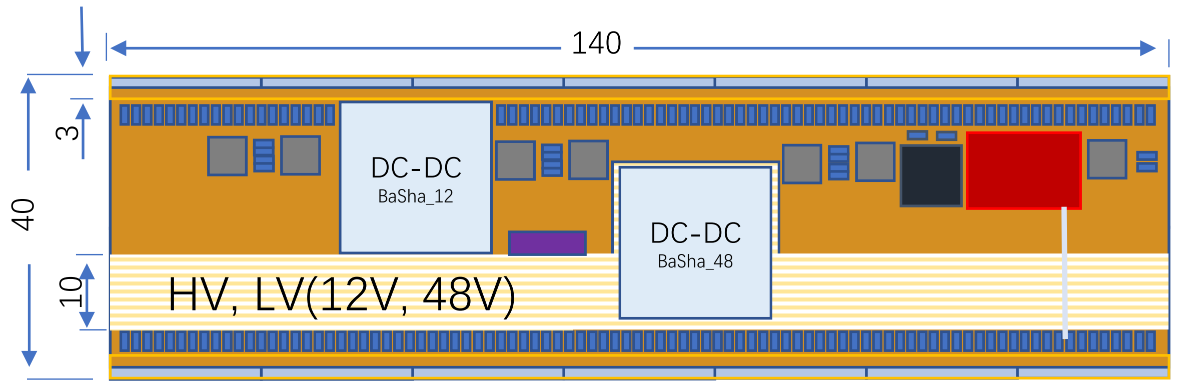


- TaoTie
  - Input: 8 uplinks, 1 clk
  - Output: 1 uplink

- ChiTu
  - input： 7 uplinks （1.39Gbps）
  - Output： 16 downlinks， 16 clks

ITK Front End Board layout





- LV供电：**总长度小于1m，可直接用多层Flex供电**
  - Flex线阻计算：

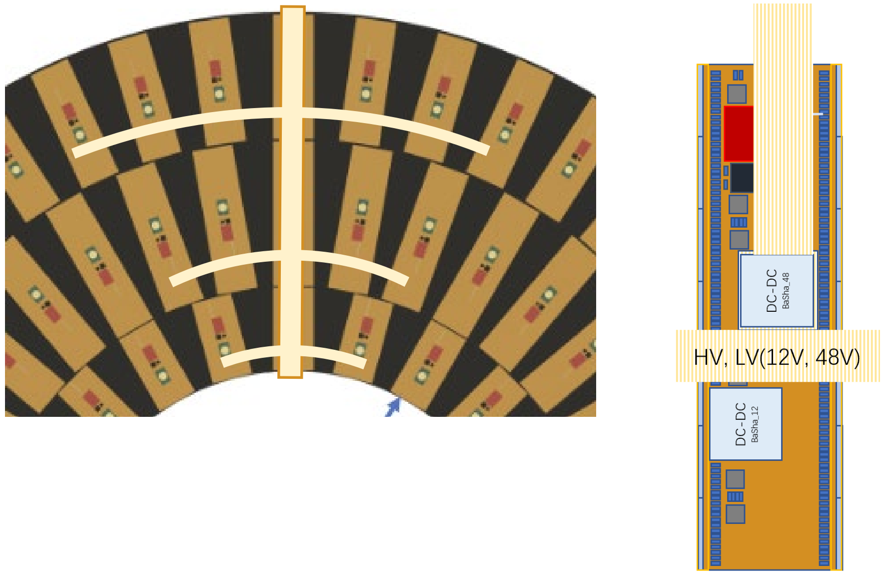
    R≈0.1Ω/m（h=35um, w=5mm,copper）
  - 每个Module的供电电流1A（12W）

    1A电流的压约0.2V/m，线损0.2W/m
  - 每个Ladder(7 modules)的供电电流2A，(96W)

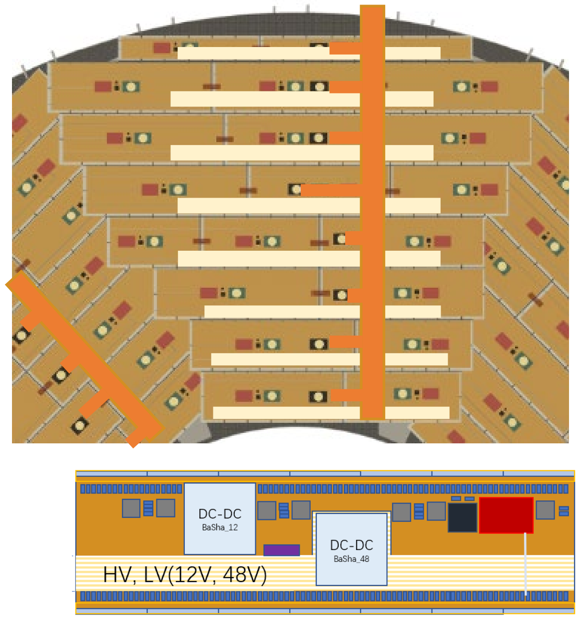
    2A电流的压约0.4V/m，线损0.8W/m，最长1m的线损0.8W

	功率
1 Sensor	0.8W
1 Module（14 chips）	11.2W
1 ladder (7 modules)	78.4W
1 ladder (5 modules)	56W

ITK Endcap layout



Pixel



Strip

- 支撑结构类似于OTK endcap
- 具体支撑结构有待进一步细化

5.4.1.2 AC-LGAD ASIC& R&D

5.4.1.2.1 General requirements

5.4.1.2.2 ASIC architecture

5.4.1.2.3 Single-channel readout electronics

- Preamplifier
- Discriminator
- TDC
- Calibration

5.4.1.2.4 Data process and digital blocks

- CLK
- Data process
- Slow control

5.4.1.2.5 Prototype

5.4.1.2.6 Power distribution and grounding

简单介绍芯片内电源设计考虑

5.4.1.2.7 Radiation tolerance

简单介绍抗TID，SEE的设计考虑

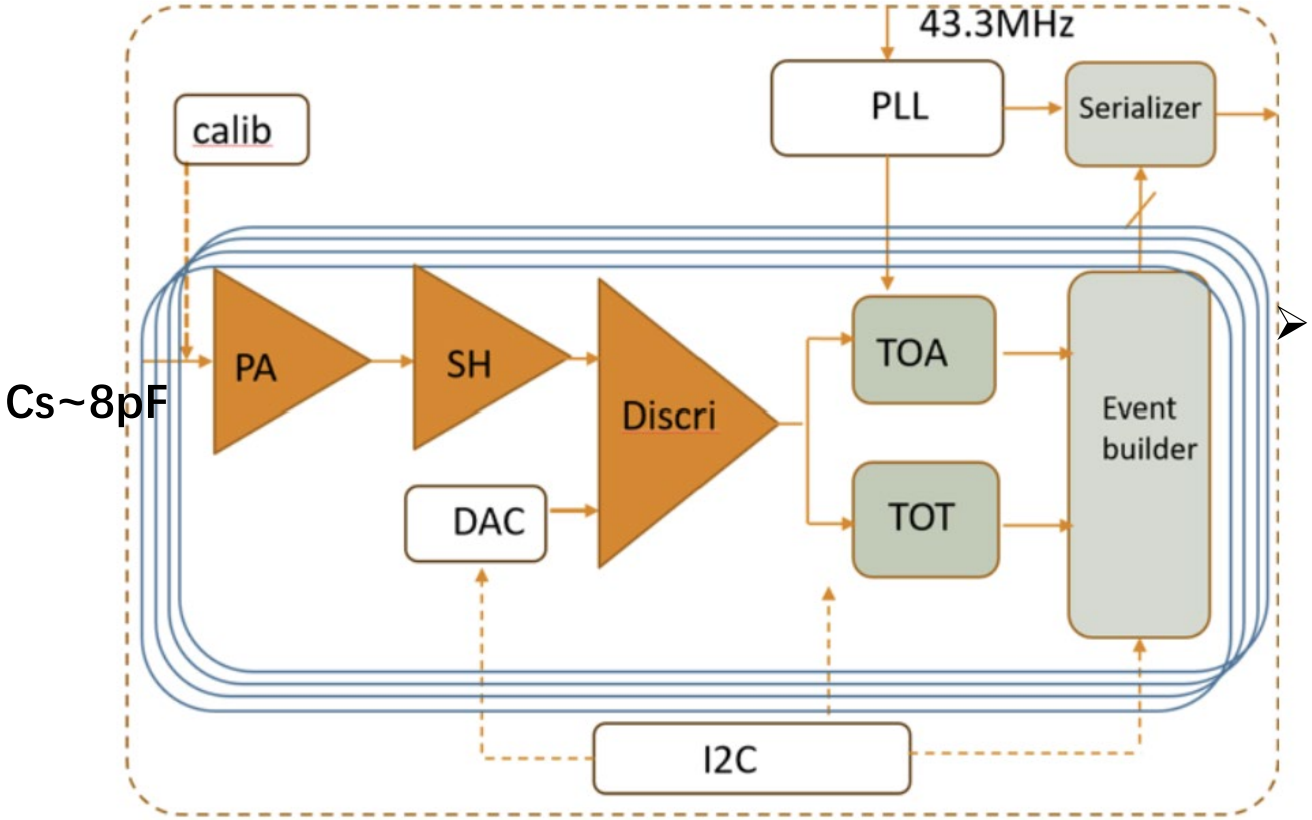
5.4.1.2.8 Monitoring

罗列一些常见参数，如温度、电压

5.4.1.2.9 Development plan and schedule

Section 5.4.1.2.1&2

OTK ASIC（JuLoong）scheme



- Details in TDR
  - Analog schematics：PA，SH，Dis，TOT
  - Digital data flow：CLK，Ctrl，data process

Specification

Voltage	1.2 V
Channel	128
Channel pitch	< 100 µm
Power dissipation per area (per ASIC)	300 mW/cm^2
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps
Temperature range	-40 °C to 40 °C
TID tolerance	1.0 MGy

Output bandwidth depends on data rate

➢ Performance Requirements:

- Single channel power consumption less than **20mW**;
- Time measurement resolution for TOA better than **30ps**.

5.4.1.2.2 **ASIC architecture** Building on the preliminary results of LGAD, an ASIC, the Out Tracker Read-Out Chip (OTKROC), is proposed to be developed in a CMOS technology. OTKROC includes 128 channels. The height of each channel should be less than 100 µm, which matches the pitch of the LGAD strip. Each channel in OTKROC has a preamplifier, a discriminator, and a time-to-digital converter (TDC) for the Time-Of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements. The preamplifier and discriminator are most critical parts for the contribution of jitter. The TOT is used to calculate the charge as well as to correct the time walk due to the charge Landau distribution in LGAD. The power consumption of OTKROC must stay below 2.5 W per chip, which means 20 mW per channel, constrained by the system cooling capacity. This value translates to a power budget of 15 mW for the front-end analog readout circuits in each channel. The time resolution of the Out Tracker is determined by the LGAD sensor and OTKROC together. The LGAD sensor has a jitter of about 40 ps due to non-uniform charge deposition. The OTKROC contribution should be below 30 ps to achieve 50 ps overall time resolution per hit. The Most Probable Value (MPV)

Section 5.4.1.2.3

Single Channel schematic details

前放电路　　　　甄别器电路　　　　TDC核心电路

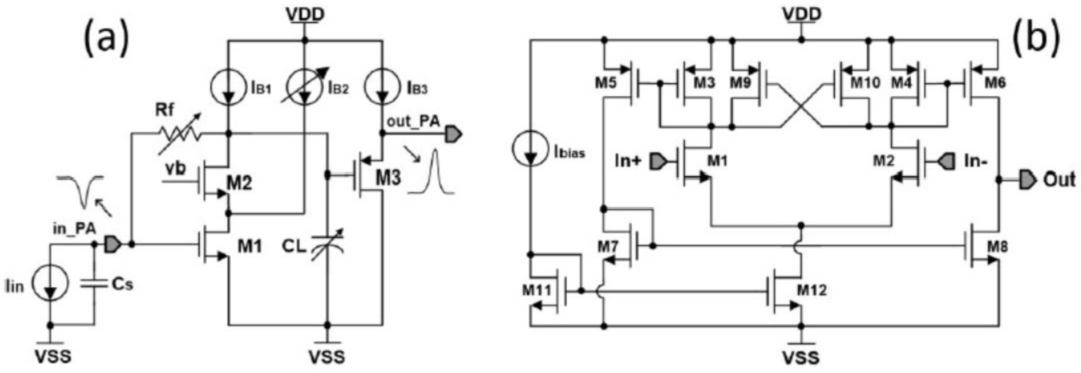


Figure 5.77: Schematic for the preamplifier (a) and Discriminator (b) in JuLoong.

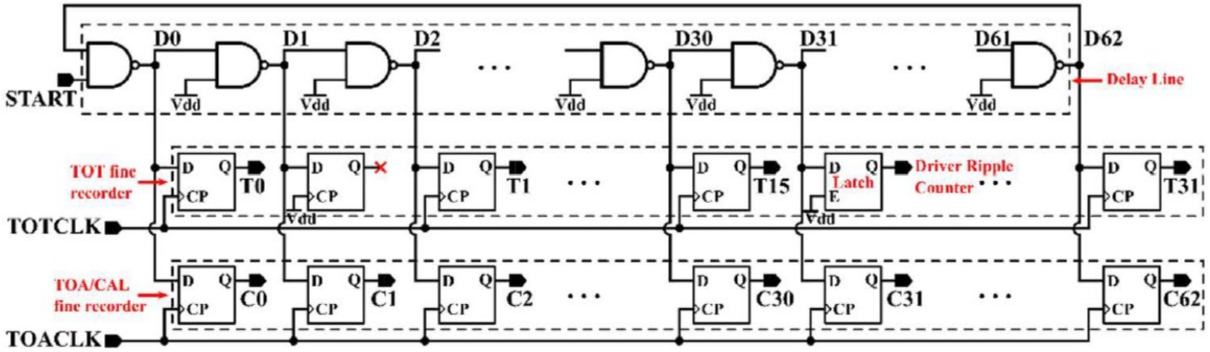


Figure 5.75: OTK ASIC3

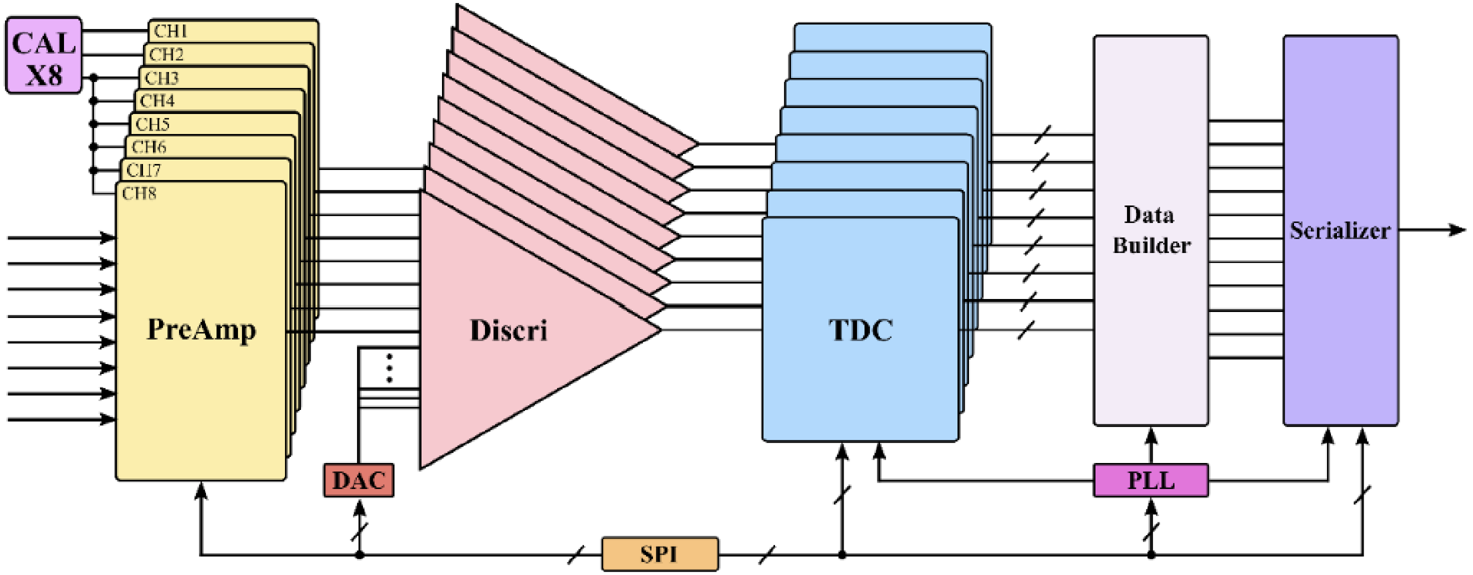
Preamplifier The preamplifier consists of two stages: a cascade amplifier (M1 and M2) as the first stage and a source follower (M3) as the second stage. The bias current of the input transistor (M1) has two components: the constant current The preamplifier consists of two stages: a cascade amplifier (M1 and M2) as the first stage and a source follower (M3) as the second stage. The bias current of the input transistor (M1) has two components: the constant current *IB1* is small due to that the VGS of M2 should not be too large. The transistor M2 and its gate voltage Vb set the DC operating point of M1. Vb is the replica bias voltage from *IB1*. The gain and bandwidth depend on the Gm of transistor M1.

Discriminator The discriminator consists of three stages of fully differential amplifiers, a comparator, and an internal buffer. The three stages of amplifiers receive the small input pulses, and

TDC The schematic of the TDC core is shown in the Figure 5.75. The OTKROC design faces two main challenges: the large area required for the OTK and the necessity of achieving both time and charge measurements while maintaining low power consumption. Additionally, the pitch of the LGAD strips is only 100 µm, which means that the height of the single-channel circuitry must also be less than 100 µm. To realize this on a smaller area, a single delay line is employed to simultaneously measure the time of arrival (TOA) and the time over threshold (TOT), with each delay cell providing a delay of 30 ps. The flip-flops record the times of the signal's rising edge, falling edge, and the reference clock's rising edge, storing these values sequentially in registers. The chip utilizes a single delay line without a delay-locked loop (DLL), and to reduce the number of delay cells, a cyclic structure is implemented. The delay of the delay line is influenced by process variations, power supply voltage, and temperature (PVT); thus, a pulse self-calibration scheme is necessary to compensate for the effects of PVT variations. This calibration is performed periodically using the system clock to measure and calibrate the delay chain. The data width of the TDC output includes 8 bits for TOT, 9 bits for TOA, 1

Section 5.4.1.2.5

Prototype design



Specification	
Power	1.2V
Channel	8
Cs	4pF
resolution	10ps
Data rate	10.24Gbps
Consumption	40mW/ch

- List design detail and simulation result in TDR
- 基本单元已验证
- 在此研究基础上，降低设计指标，优化尺寸和功耗

Design Figure 5.77 presents the block diagram of the FPMROC ASIC (application-specific integrated-circuits). Eight channels collectively utilize a data event builder for buffering, framing, scrambling and encoding parallel data from various channels. The ASIC includes a serializer for off-chip data transmission at a rate of 10.24 Gbps, and a low-jitter LC-based PLL for the generation of 5.12 GHz and 40 MHz clocks for the serializer and TDCs, respectively. Additionally, an SPI is integrated to provide configurations up to 200 bits.

Prototype Schematic and simulation

Schematic

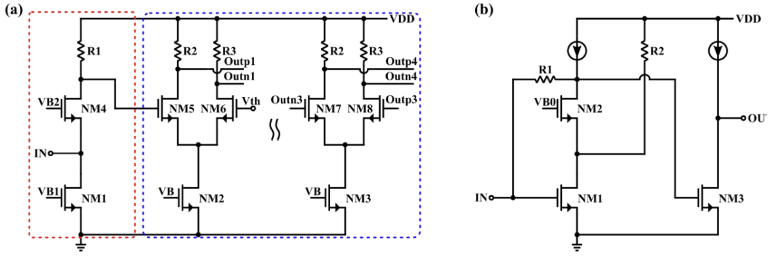


Figure 5.81: (a) Schematic of the saturated amplifier, (b) Schematic of the trans-impedance amplifier

放大甄别电路

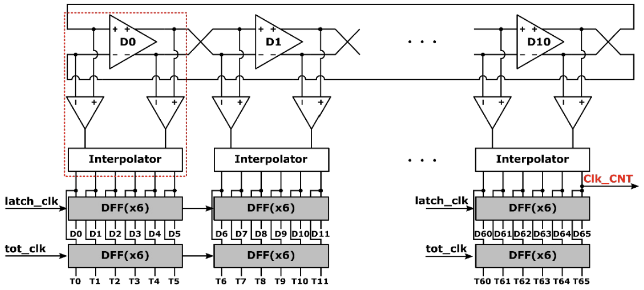


Figure 5.82: The architecture of the TDC delay line

TDC核心电路

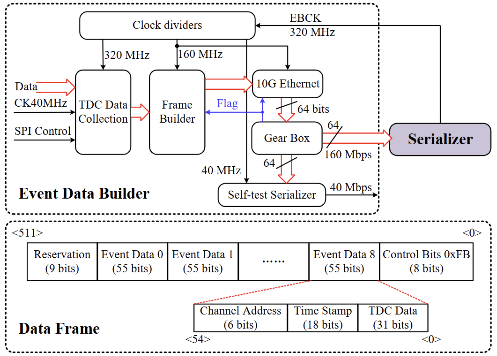


Figure 5.83: The scheme and data frame of the event data builder

数据处理框图

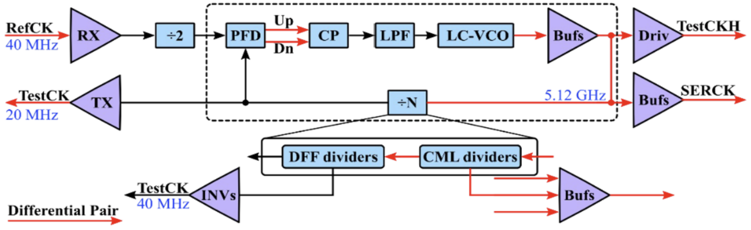
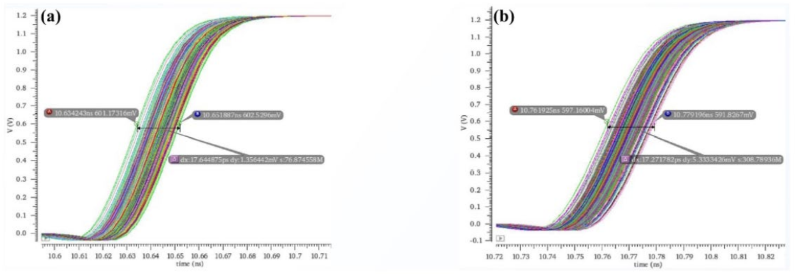


Figure 5.84: The block diagram of the PLL and serializer

时钟产生电路

Simulation result



(a) saturated amplifier (b) trans-impedance amplifier

Figure 5.85: Transient noise simulation for output of preamplifier

前放甄别jitter仿真结果

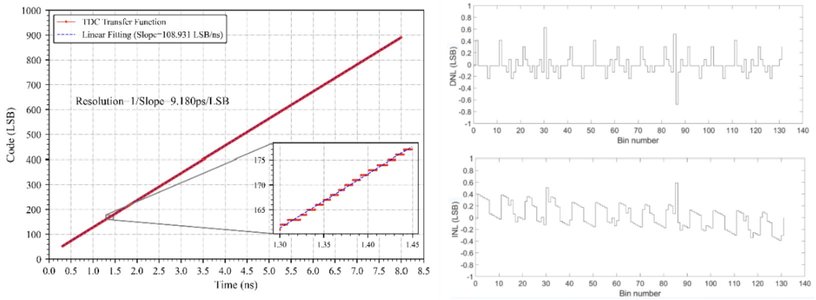
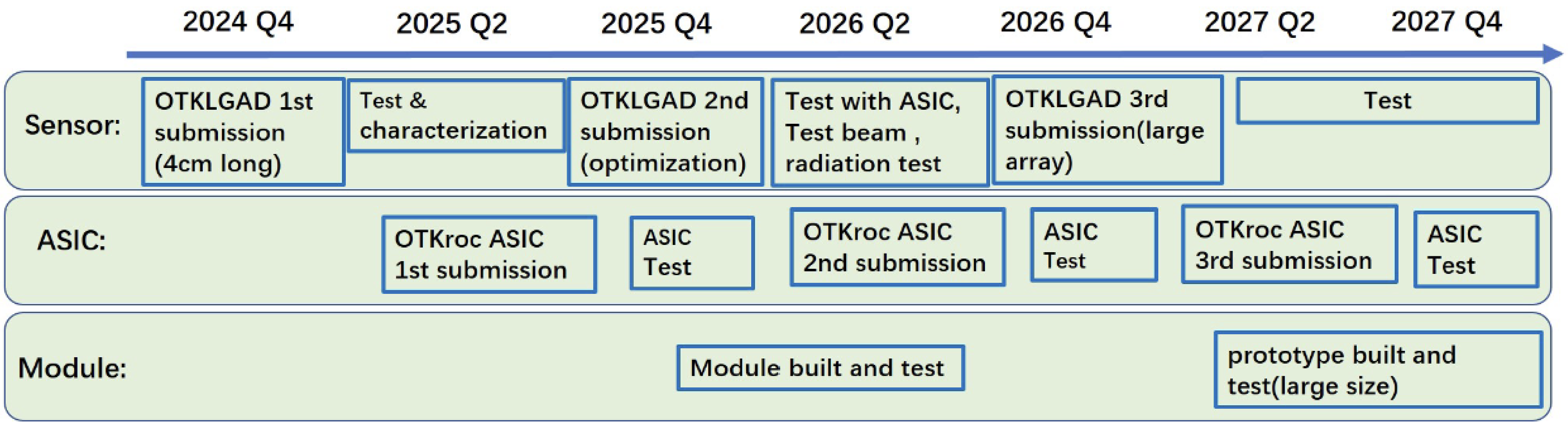


Figure 5.86: (a) TDC transfer function curve, (b) DNL and INL of the delay line

TDC转移曲线仿真结果

Section 5.4.1.2.9
Plan



5.4.1.2.9 Development plan and schedule In the second half of 2024, the design of the LGAD readout scheme and the verification of the corresponding ASIC will be conducted. In the Q1 of 2025, the ASIC will be submitted for wafer production to validate the performance of the preamplifier, discriminator, and TDC modules, along with the design of the ASIC test system. Performance testing of the ASIC will be carried out by the end of the year, and each module will undergo radiation hardness testing. In the Q4 of 2025, the ASIC design will be improved, incorporating a digital logic control section, and the first version of the multi-channel integrated design will be submitted for wafer production. In the first half of 2026, the design of the multi-channel ASIC test system will be completed, alongside performance testing of the ASIC and radiation hardness testing, culminating in the completion of the connection and debugging with the LGAD. In the end of 2026, the multi-channel ASIC design will be further refined, and the V1 version of the ASIC will be submitted for wafer production. Simultaneously, the prototype design of the LGAD readout frontend electronic system will be initiated. In the first half of 2027, performance testing of the V2 version of the ASIC will be conducted, along with testing of the LGAD readout electronic system prototype, ensuring coordination with the LGAD. In the second half of 2027, the prototype system will be finalized in preparation for the mass production of the chips.

谢谢！
请批评指正！