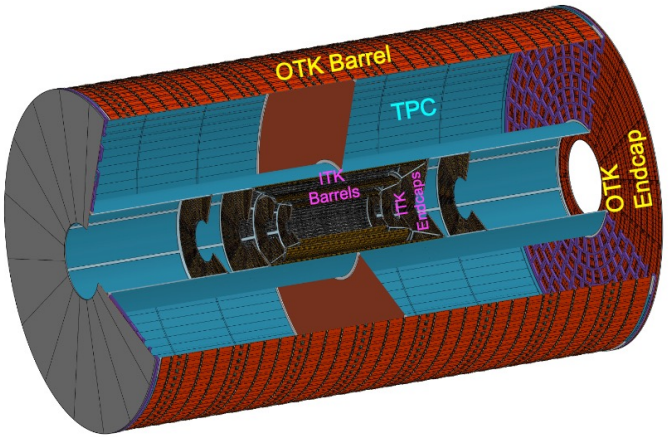
CEPC Silicon Tracker Ref-TDR Overview

Qi Yan *on behalf of the Silicon Tracker Group*

Feb 15, 2025, IHEP

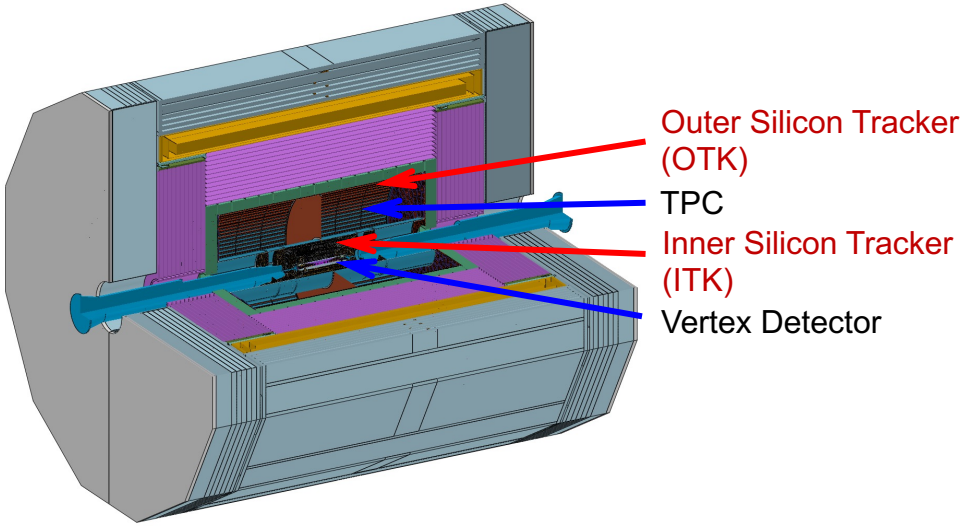


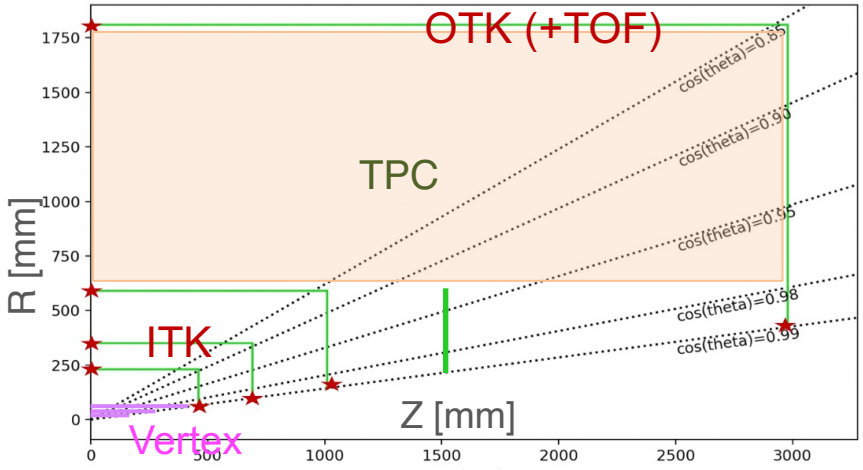
CEPC Ref-TDR Silicon Tracker章节概况

致力于完成一个合理自洽的 Silicon Tracker技术性设计报告（Ref-TDR）。Silicon Tracker章节的全部内容超过100页，是Ref-TDR中最大的一个章节。全部撰写工作需要在本月前完成，以应对4月份的国际评审。目前时间紧、任务重。

当前Ref-TDR填充完成的内容超过90%，剩下的少部分内容正在抓紧补充。希望能最终达到一定的技术水平，在能力范围内做到最好。虽然不能尽善尽美，也有许多不足的地方，请大家谅解。

特别感谢叶竞波近期在阅读后提供的宝贵反馈意见。我们也欢迎更多的人能花时间多读一读、提供建设性的意见，帮助一起更好地完成这部分的内容。





Outline of Silicon Tracker Ref-TRD

Chapter 5 Silicon Trackers 总负责人：严琪

>90% of the content has been implemented, with the full chapter nearing 100 pages.

Section 5.1: Requirements

The CEPC is designed to operate across a wide energy region, including Z-pole (91 GeV), W^+W^- threshold (160 GeV), the energy maximizing ZH production (240 GeV), and $t\bar{t}$ threshold after upgrade (360 GeV). In High Lumi Z mode, the luminosity reaches $\mathcal{L} = 115 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at 30 MW ($192 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at 50 MW), with a 23 ns interval between bunch crossings. The stringent requirements of both physics and operational conditions impose high demands on the CEPC tracking system.

5.1.1 Physics requirements

- Higgs and electroweak physics studies
- Flavor physics, the precise reconstruction of B and D hadrons
- Flavor physics studies and jet substructure analysis

Summarized physics requirements:

- Momentum resolution
- Impact parameter measurement
- Particle identification
- Solid angle coverage

5.1.2 Specific requirements on Silicon Tracker

- Layout
- Spatial resolution and material budget
- Timing resolution

Section 5.2: Overview of ITK and OTK

The layout of the tracker system is crucial for accurately identification and determination of particle trajectories. This section provides an overview of the CEPC tracker system, with a particular focus on the Silicon Trackers and their layout optimization to enhance performance.

5.2.1 Technology options and boundary conditions

- Spatial Measurements
- Materials
- Particle Identification (PID) Compatibility

5.2.2 Optimization tool

- Lic Toy (LDT): a MatLab software designed to model and optimize the layout of detector taking in to account physical constraints, material budget, and performance metrics.

5.2.3 Layout optimization

- Optimization of geometrical envelope of the tracking system
- Optimization of the Layout in barrel region
- Optimization of the Layout in endcap region
- Optimization summary

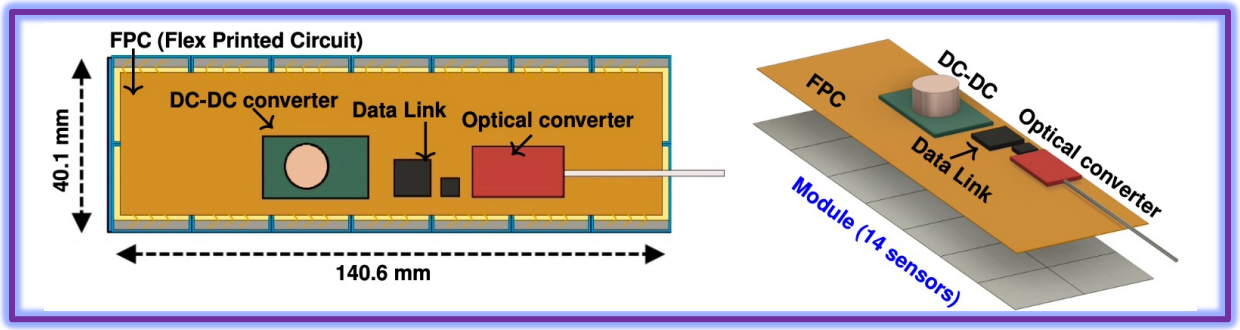
Section 5.3: Inner Silicon Tracker (ITK)

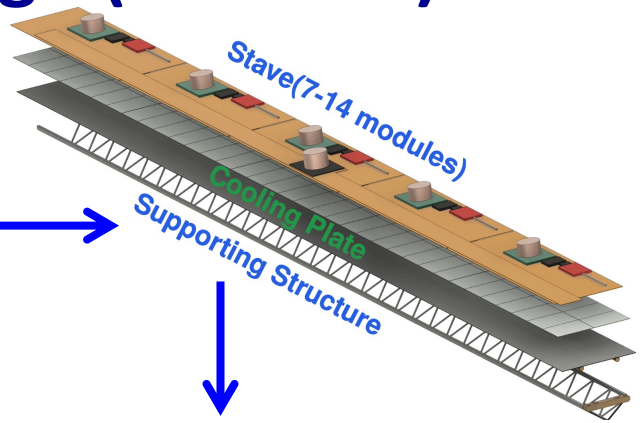
5.3.1 CMOS chip R&D

Yiming's will give a detailed presentation

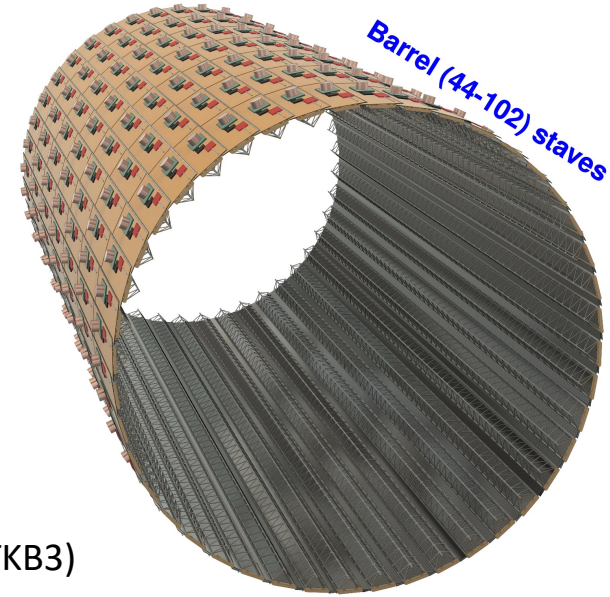
5.3.2 ITK design

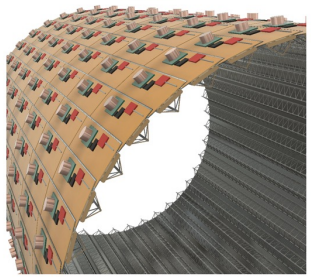
Section 5.3.2.1: ITK barrel design (Baseline)





- HVCMOS pixel sensor:
  - Sensor size: 20 mm × 20 mm (active area of 17.4 mm × 19.2 mm)
  - Array size: 512 rows × 128 columns
  - Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~200 mW/cm^2
- Module:
  - 14 sensors (2 rows × 7 columns)
  - Sensor gap: 100 μm
  - Module dimensions: 140.6 mm × 40.1 mm
- Stave:
  - Module gap: 300 μm
  - Length: 986.6 mm (ITKB1), 1,409.6 mm (ITKB2), and 1973.2 mm (ITKB3)
- Barrel radii: 235 mm (ITKB1), 345 mm (ITKB2), and 555.6 mm (ITKB3)

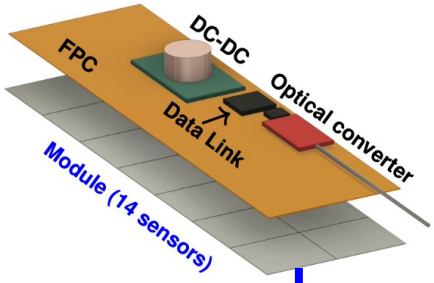




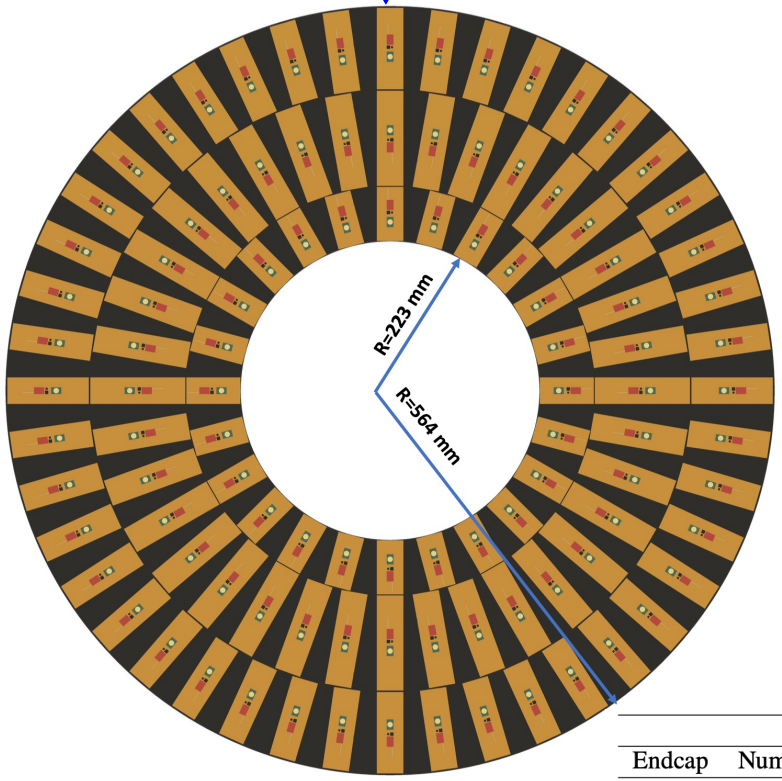
Information about staves, modules, and sensors used for 3 ITK barrels construction

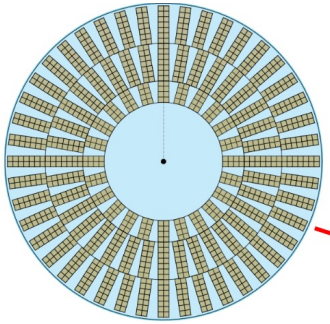
Barrel	Number of staves	Modules per stave	Sensors per module	Total number of sensors	Sensor area [m^2]
ITKB1	44	7	14	4312	1.72
ITKB2	64	10	14	8960	3.58
ITKB3	102	14	14	19992	8.00
Total	210			33264	13.31

Section 5.3.2.2: ITK endcap design (Baseline)

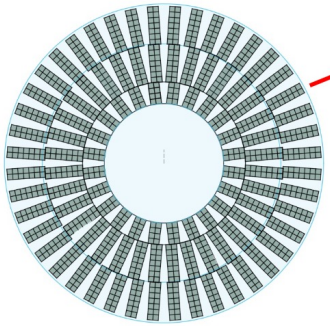


- Module:
  - 3 types of modules: 8, 12, and 14 sensors for all 4 ITK endcaps
- Endcap active area radii:
  - 81.5 mm<r<242.5 mm(ITKE1), 110.5 mm<r<352.3 mm (ITKE2), 163 mm <r<564 mm (ITKE3), and 223 mm<r<564 mm (ITKE4)

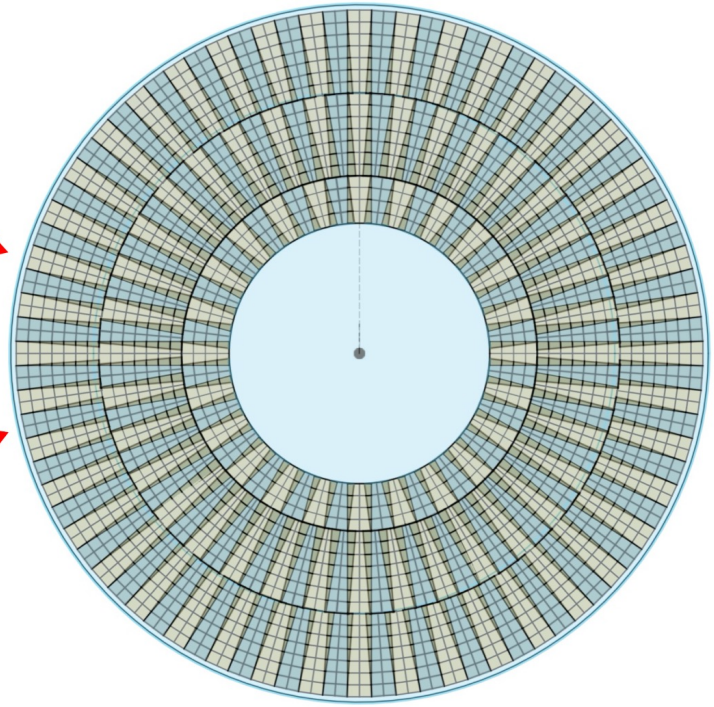




Front view of endcap



Back view of endcap

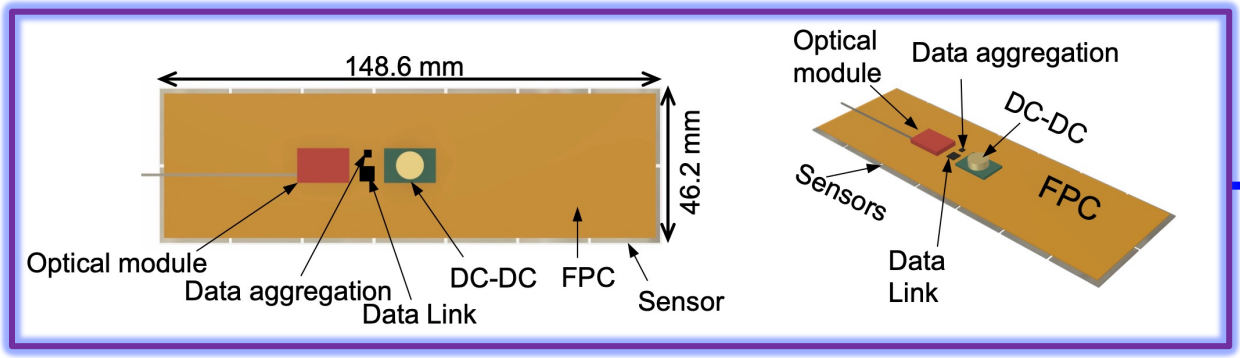


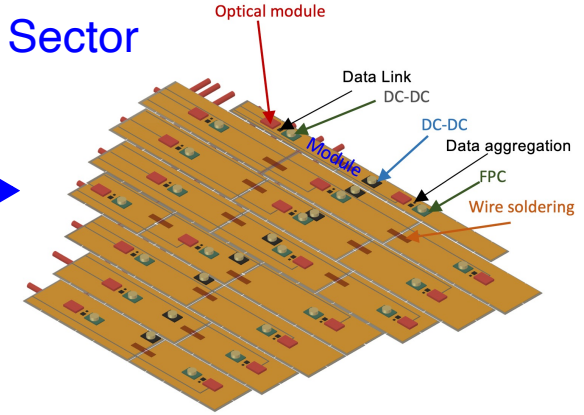
Perspective view of full endcap

The Module and Sensor Layout of a Single Face of Each ITK Endcap

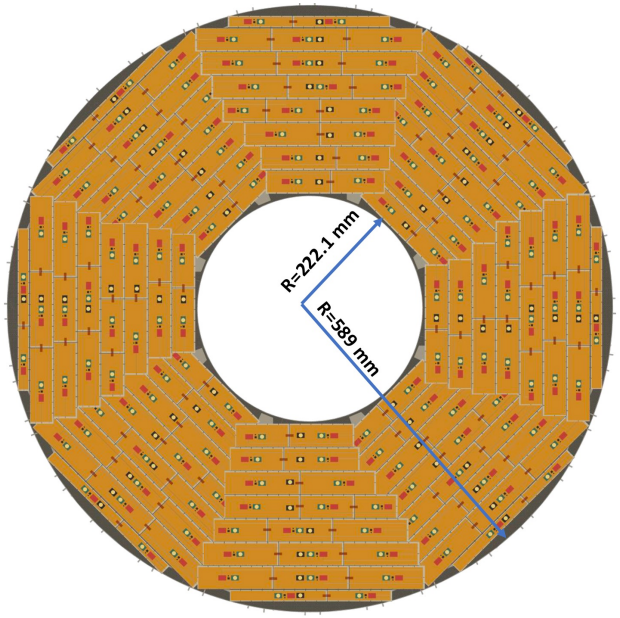
Endcap	Number of module rings	Number of modules per module ring	Number of sensors per module	Total sensors
ITKE1	2	13,20	8,8	264
ITKE2	2	16,24,28	8,8,8	544
ITKE3	3	24,36,44	12,14,14	1408
ITKE4	3	24,36,44	8,12,14	1312
Total				3528

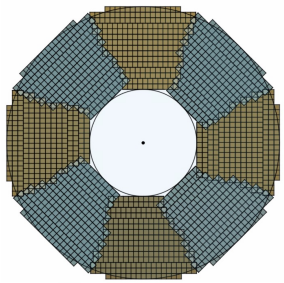
Section 5.3.2.3: Alternative design for the ITK



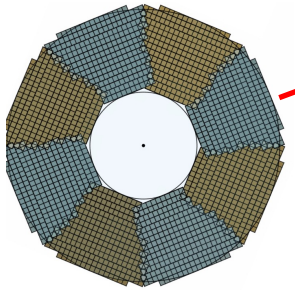


- CMOS Strip Chip/Sensor (CSC) for CEPC:
  - Chip size: 21 mm × 23 mm
  - Strip number per chip: 1024
  - Strip pitch size: 20 μm (spatial resolution 5 μm)
  - Time resolution: 3-5 ns
  - Power consumption: ~80 mW/cm

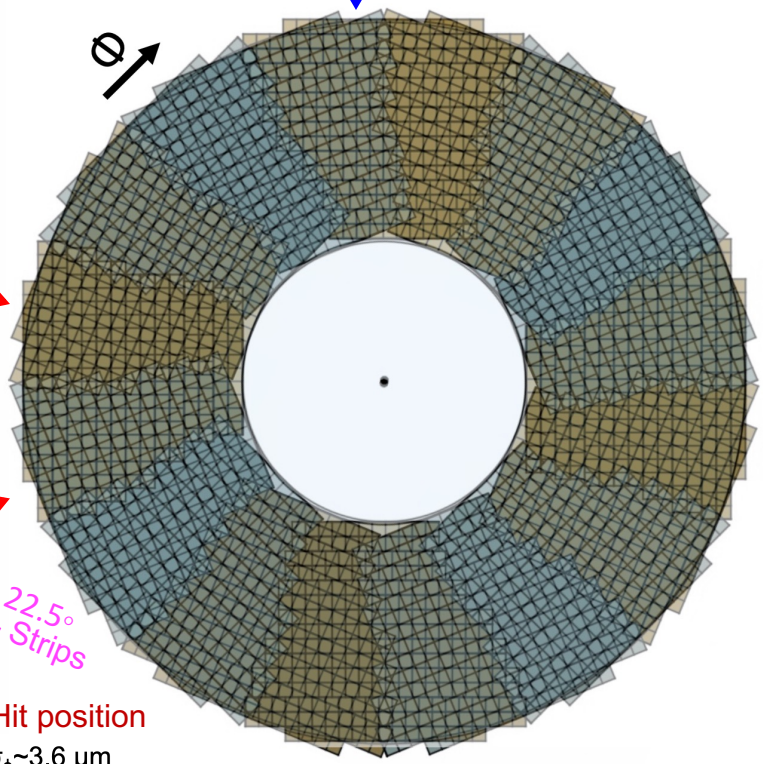


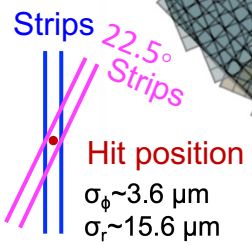


Normal half endcap



22.5◦ half endcap

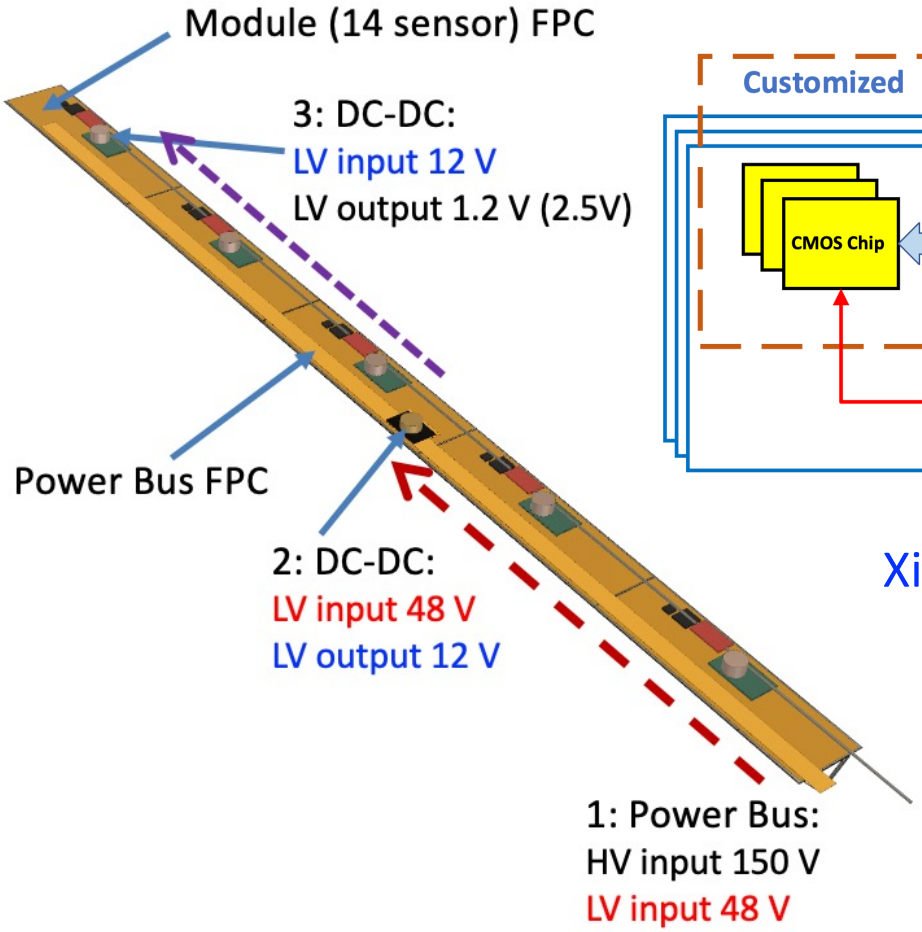


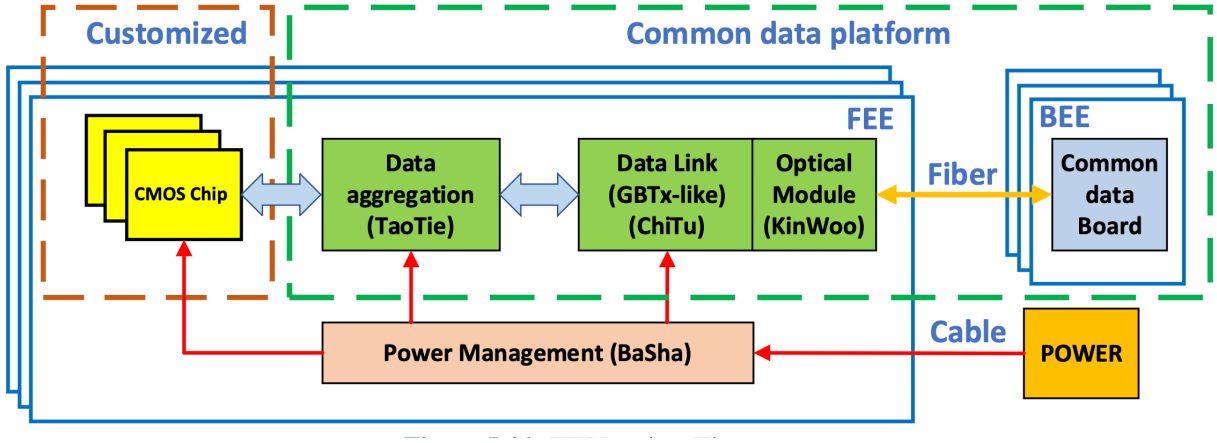


Section 5.3.3: Readout electronics

5.3.3 Readout electronics

In each ITK module, 14 monolithic HV-CMOS pixel sensors are bonded to a common flexible PCB (FPC), as shown in Fig. 5.34. The FPC transmits digital signals from the sensors to the data aggregation chips and subsequently to the optical fiber. To ensure error-free data transmission, the FPC integrates two ASICs for data aggregation: the TaoTie chip and the ChiTu chip.

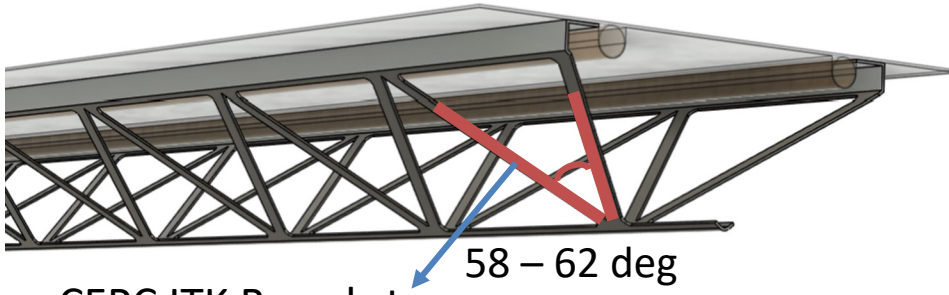




Xiongbo will give a detailed presentation

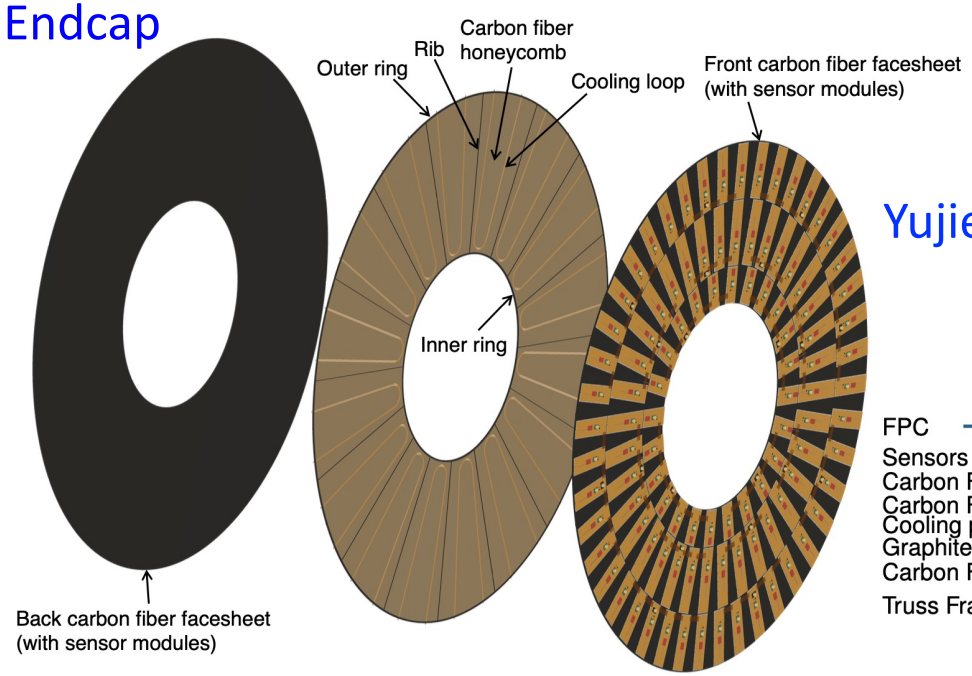
Section 5.3.4: Mechanical and cooling design

5.3.4 Mechanical and cooling design

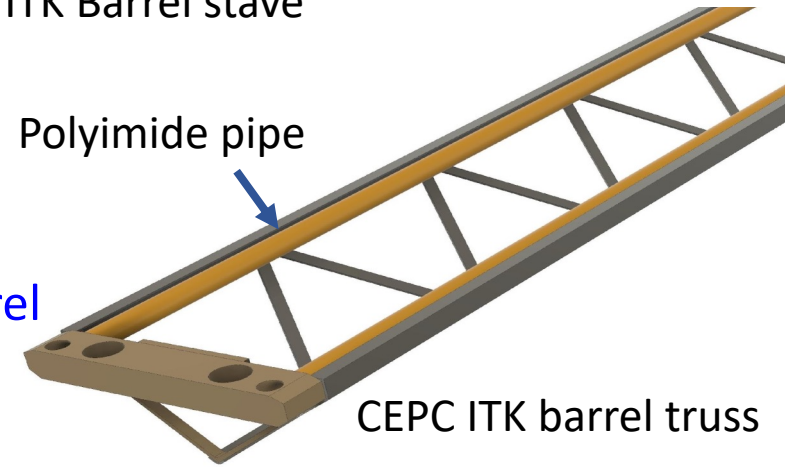


CEPC ITK Barrel stave

Endcap

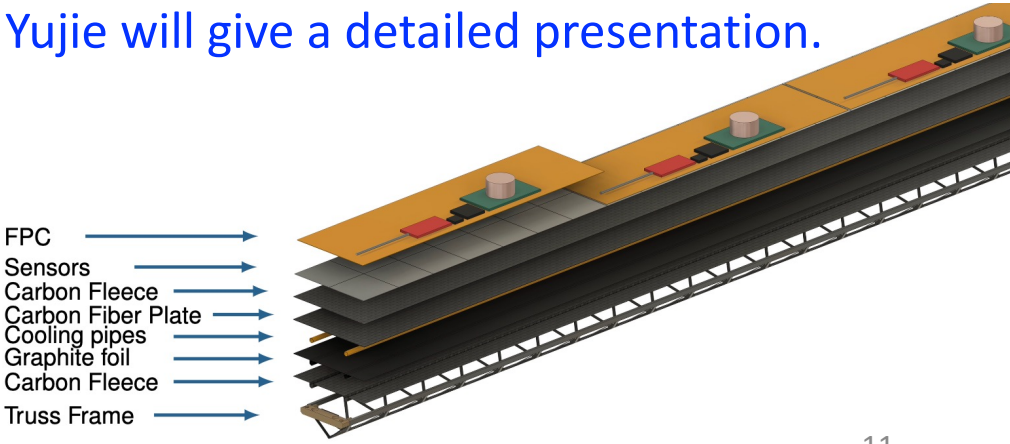


Barrel



CEPC ITK barrel truss

Yujie will give a detailed presentation.



Section 5.3.5: Prospects and plan

The CEPC team has successfully developed several fully functional Monolithic Active Pixel Sensors (MAPS), including JadePix, TaichuPix, and CPV, based on the CMOS Image Sensor (CIS) process. The HV-CMOS pixel sensor and the CMOS strip sensor, both new monolithic full-depletion sensors, are distinguished by their exceptional radiation tolerance, high spatial resolution, and particularly good timing for bunch tagging. These two sensor approaches are key detector technologies targeted for application in the CEPC ITK.

Notably, the HV-CMOS pixel sensor as the baseline for ITK, developed using the 55 nm process, has undergone two rounds of prototype tape-outs, achieving critical principle verification. Meanwhile, the CMOS strip sensor as an alternative approach, offers advantage in spatial resolution and has technological differentiation. Its first design has been completed, and fabrication is scheduled. Over the next few years of iterations, both CMOS sensors will move steadily toward fully functional, full-size sensors. In parallel, the development of module level and system level integration, including R&D on supporting electronics, mechanical structures, cooling systems, as well as detailed integration methodologies, is also in progress.

这部分的内容会根据这几月COFFEE3的最新流片情况做一定的补充。

Section 5.4: Outer Silicon Tracker (OTK)

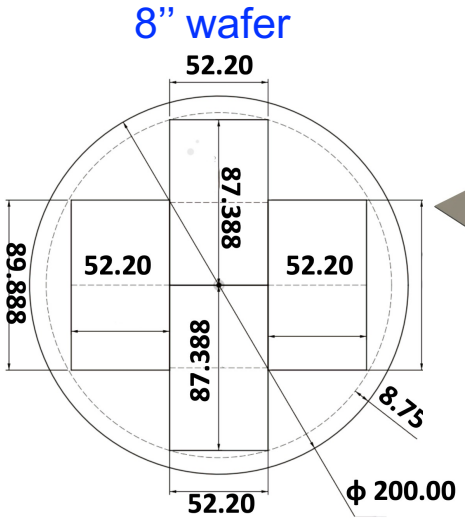
5.4.1 AC-LGAD sensor and ASIC R&D

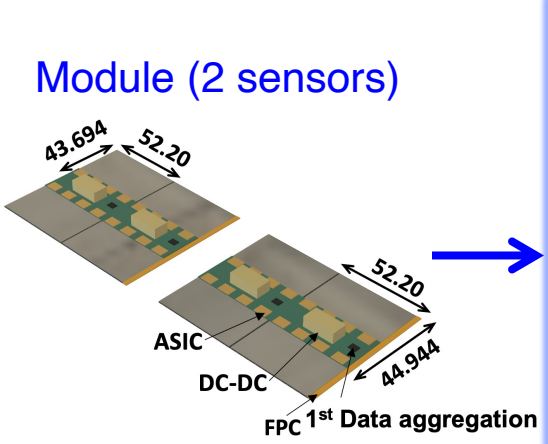
Zhaomei and Yunyun will give a detailed presentation.

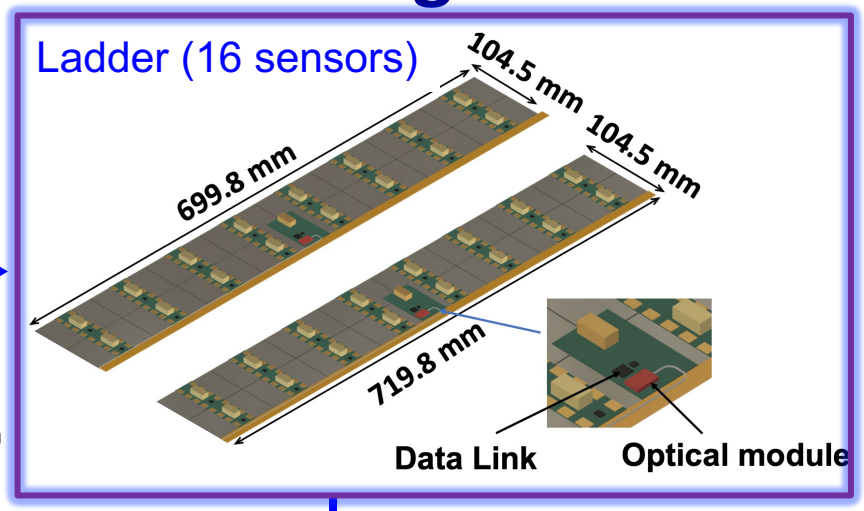
Xiongbo will give a detailed presentation.

5.4.2 OTK design

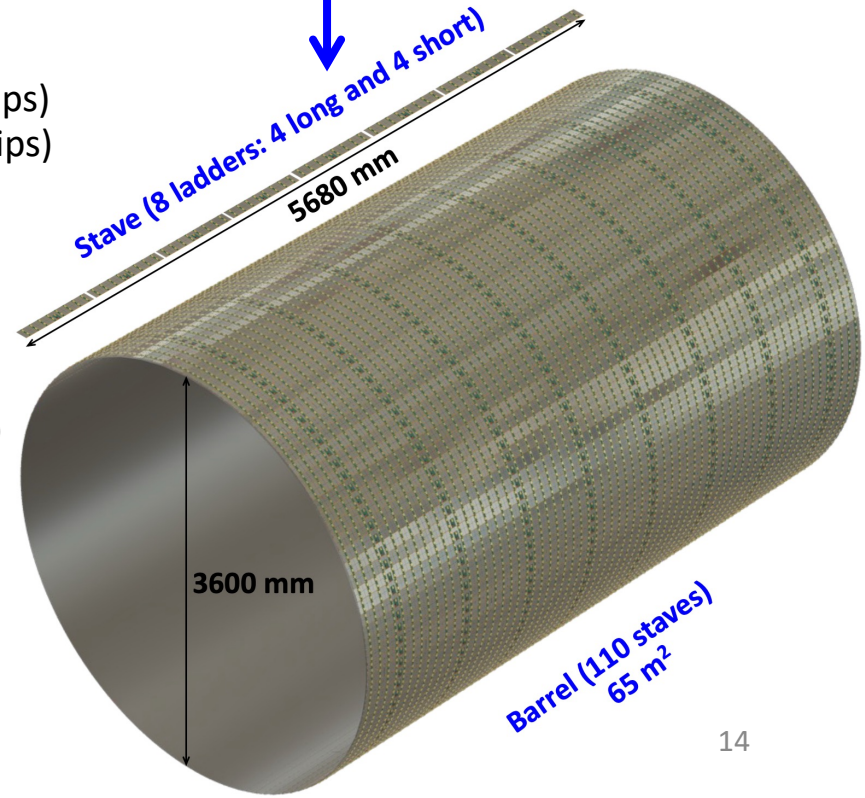
Section 5.4.2.1: OTK barrel design





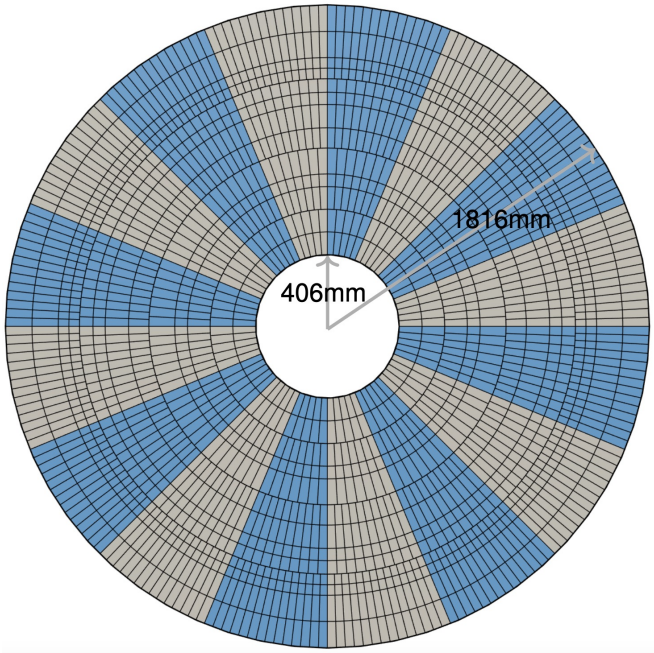


- AC-LGAD strip sensor:
  - Sensor size: 87.388 mm × 52.20 mm (2 sets of strips)
    89.888 mm × 52.20 mm (2 sets of strips)
  - Strip length: 43.644 mm or 44.894 mm
  - Strip number: 512 ×2
  - Strip pitch: 100 μm
  - Time resolution: 50 ps
  - Power consumption: 300 mW/cm^2
- Module: 2 sensors (16 readout ASICs with 128-channels)
- Ladder:
  - 8 modules (16 sensors)
  - Length: 699.8 mm or 719.8 mm
- Stave: 8 ladders (4 short+4 long)

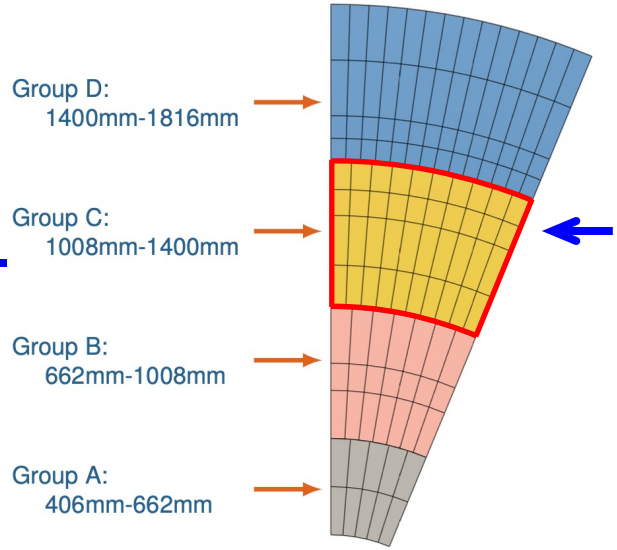


Section 5.4.2.2: OTK endcap design

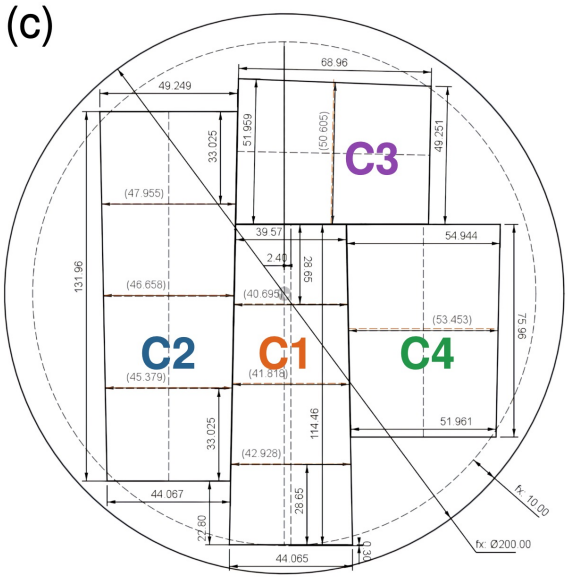
Endcap (16 sectors, 10 m^2)



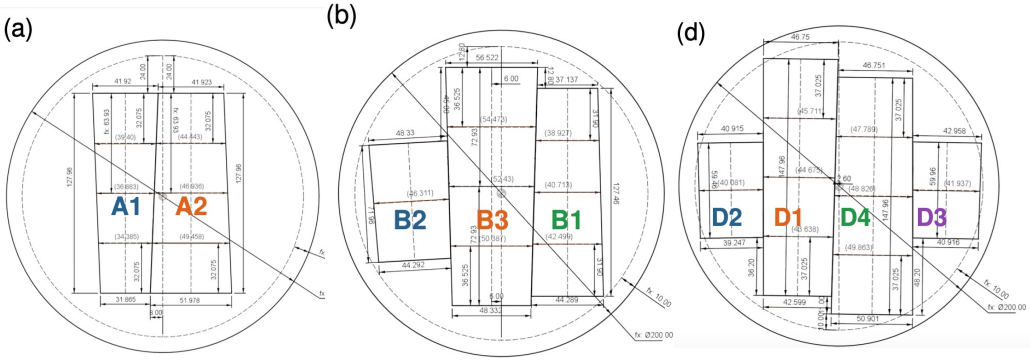
1/16 Sector



Sensor: 8'' wafer (group C sensors)



- OTK endcap consists of 13 rings, arranged into 4 groups.
- Each group contains 2-4 types of trapezoid sensors, dicing from one 8'' silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
- The long sensor contains 4 sets of short strips while short sensor contains 2 sets of short strips.
  - Strip pitch : 80.7-113.8 μm
  - Strip length : 28.38-37.61 mm

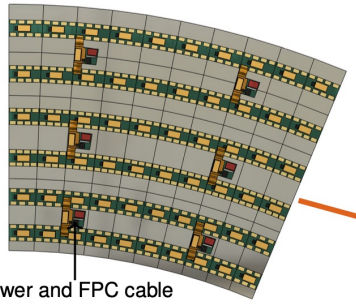


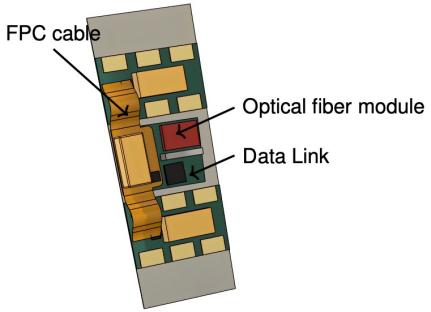
8'' wafer (group A, B, D sensors)

Maximize the use of silicon wafers and facilitate detector assembly.

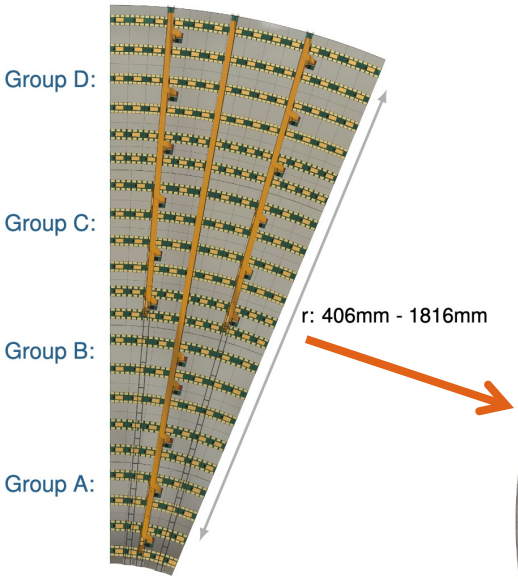
Section 5.4.3: Readout electronics

Group C sensors

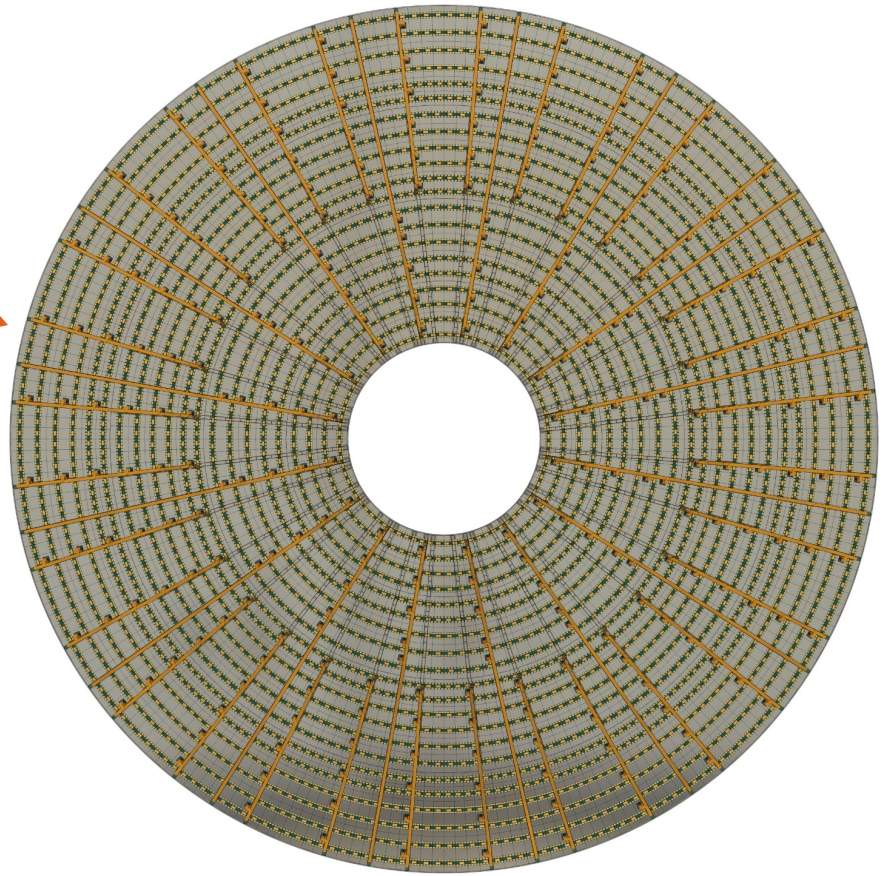




1/16 Sector



Endcap (16 sectors)



OTK Endcap Trapezoidal Sensor Strip Parameters

Sensor type	Number of strip sets	Number of strips per set	Strip pitch [μm]	Strip length [mm]
A1	4	384	81.5-107.6	31.755
A2	4	512	80.7-100.3	31.755
B1	4	384	95.1-113.8	31.630
B2	2	512	85.3-93.2	35.610
B3	4	512	93.2-109.2	36.255
C1	4	384	101.5-113.2	28.380
C2	4	512	84.9-95.0	32.755
C3	2	512	95.0-100.3	34.110
C4	2	512	100.3-106.1	37.610
D1	2	384	100.6-105.0	29.360
D2	2	384	105.0-109.4	29.610
D3	4	512	82.0-90.1	36.755
D4	4	512	90.1-98.2	36.755

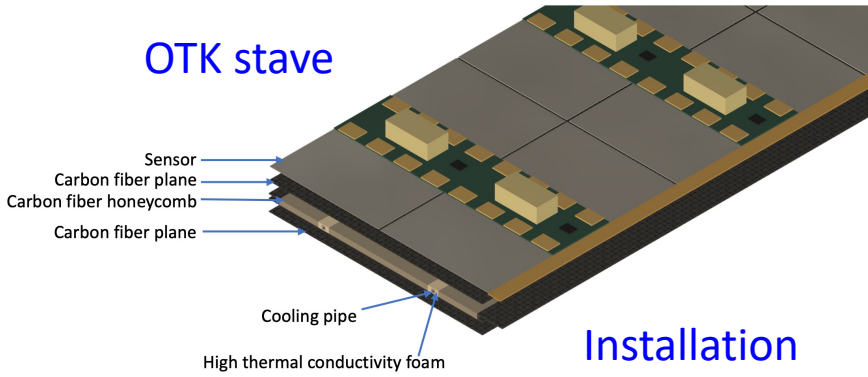
Xiongbo will give a detailed presentation.

Section 5.4.4: Mechanical and Cooling Design

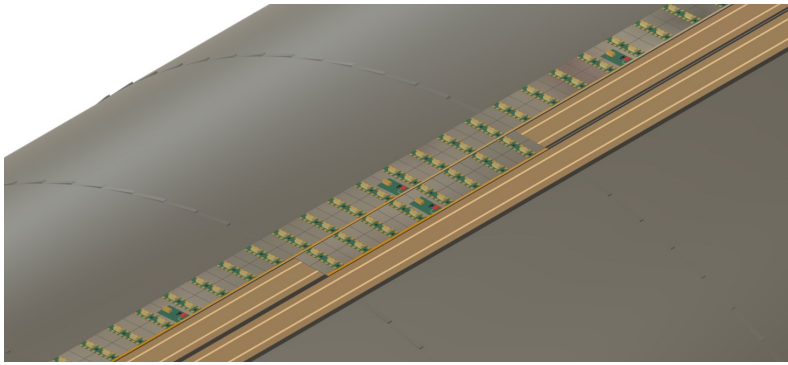
5.4.4 Mechanical and cooling design

Yujie will give a detailed presentation.

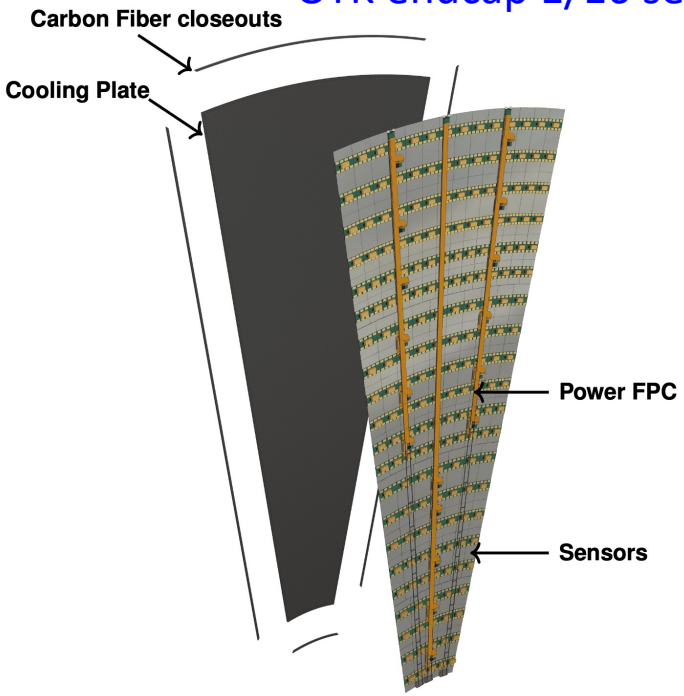
OTK stave

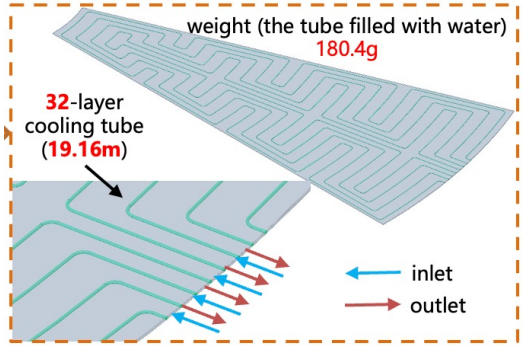


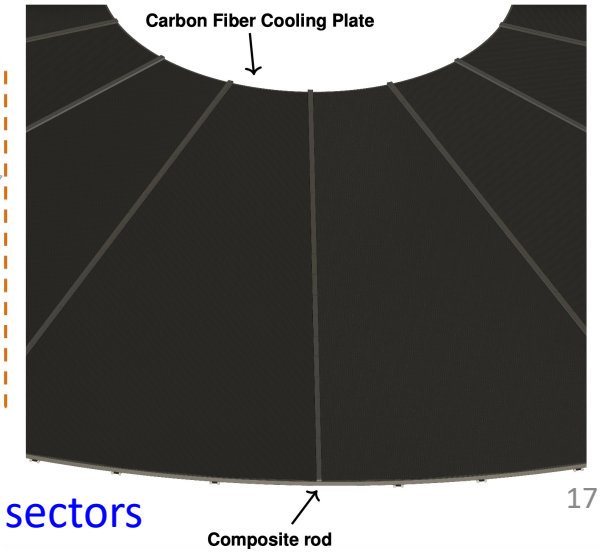
Installation



OTK endcap 1/16 sector







Mounting 1/16 sectors

Section 5.4.5: Prospects and plan

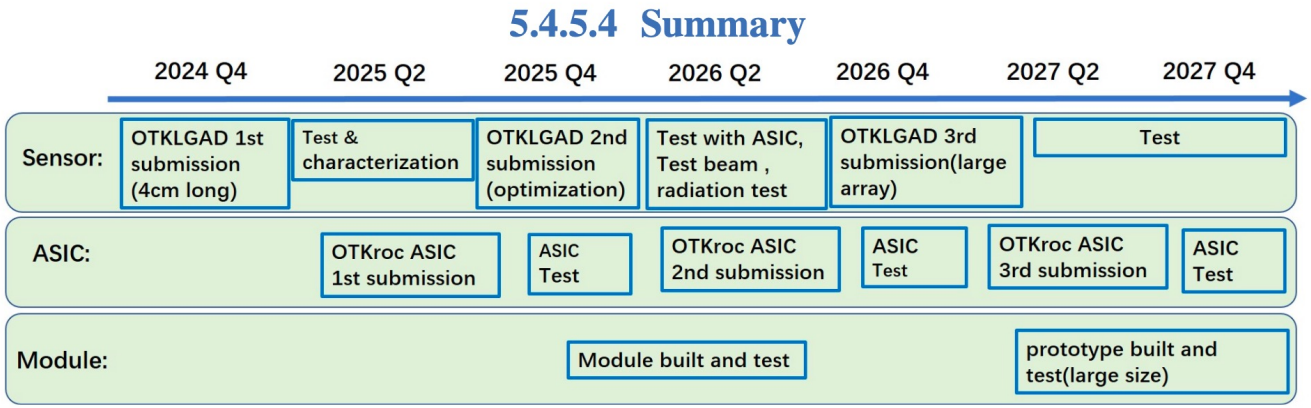


Figure 5.106: Timeline for OTK, including sensor, ASIC, mechanics and so on

All the R&D mentioned above is part of a 3-year plan, as detailed in Fig. 5.106. Considering the project timeline of more than 5 years from construction, the CEPC project is flexible enough to adjust its technical approach and has sufficient backup plans for the engineering phase. For example, if the performance of the AC-LGAD strip sensor degrades significantly for large-dimension strip sensor, we may consider using conventional large-dimension sensor, with or without an external time-of-flight detector, or opt for bump bonding or monolithic AC-LGAD technology if it becomes mature.

For the OTK system, including sensor, readout ASIC, and mechanical and cooling components, we are open to both domestic collaborations with research units and industry as well as international partnerships. In light of all these factors, we are confident in delivering a high performance OTK system that meets the physics requirements in a timely manner.

LGAD strip的流片会在本月提交。这部分的内容会根据最新流片情况做一定的补充。

Section 5.5: Background (Hit rate) Estimation

5.5 Beam background estimation

5.5.4 OTK tolerable hit rate

For the AC-LGAD strip sesnor used in the OTK, each fired strip generates 48 bits of data, with an average of ∼2 strips firing per hit. Data from 6 or 8 sensor readout ASICs (6 ASICs are used only in specific parts of the OTK endcap) is aggregated by a primary data aggregation chip. In the OTK barrel, 16 primary data aggregation chips (e-links) are connected to a common data link chip (ChiTu) on the second aggregation board, with each primary data aggregation chip connecting via a 346.67 Mbit/s e-link. In the OTK endcap, 10 to 14 primary data aggregation chips (e-links) are connected to a common data link chip on the second aggregation board, with each primary data aggregation chip connecting via a 693.33 Mbit/s or 346.67 Mbit/s e-link.

The supported data rate per sensor readout ASIC is up to 43.33 Mbit/s for the barrel and up to 86.67 Mbit/s for the endcap, corresponding to a maximum hit rate of 8.0×10^4 Hz/cm^2 for the barrel (detector active area ∼1.28 cm × 4.4 cm per ASIC) and 2.1×10^5 Hz/cm^2 for the endcap (detector active area ∼1.28 cm × 3.3 cm per ASIC). This detector's tolerable hit rate is ∼5 times larger than the estimated maximum background hit rate for the OTK barrel (OTKB, 1.56×10^4 Hz/cm^2) and ∼5 times larger than that for the OTK endcap at Low Lumi Z (OTKE, 4.41×10^4 Hz/cm^2), as summarized in Table 5.18.

Section 5.6 Performance

5.6 Performance

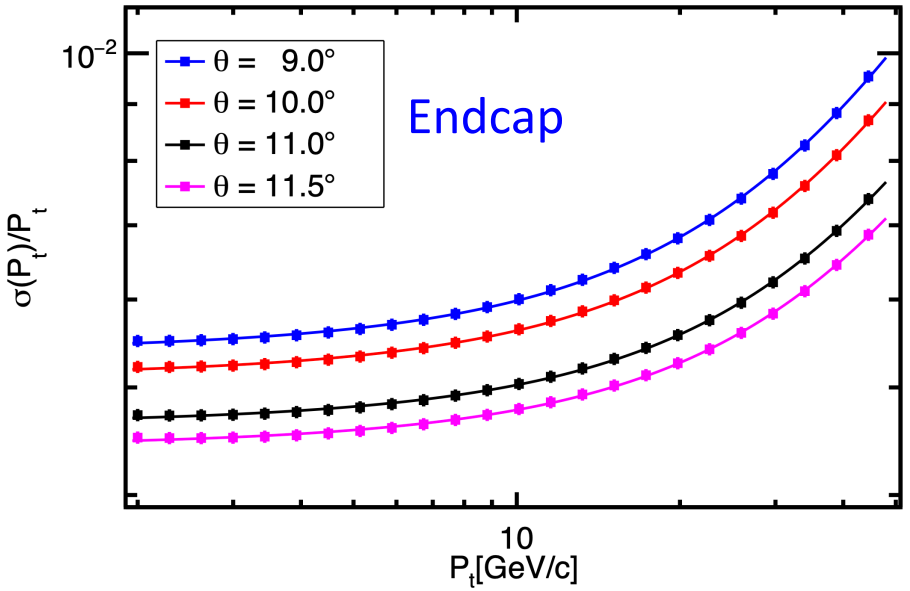
Momentum resolution in the barrel region:

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{Si}} = ap_t \oplus \frac{b}{\beta\sqrt{\sin\theta}}$$

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{TPC}} = as_1 p_t \oplus \frac{bs_2}{\beta\sqrt{\sin\theta}}$$

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{\text{Combined}} = \frac{1}{\sqrt{\left(\frac{\sigma_{p_t}}{p_t}\right)^{-2}_{\text{Si}} + \left(\frac{\sigma_{p_t}}{p_t}\right)^{-2}_{\text{TPC}}}}$$

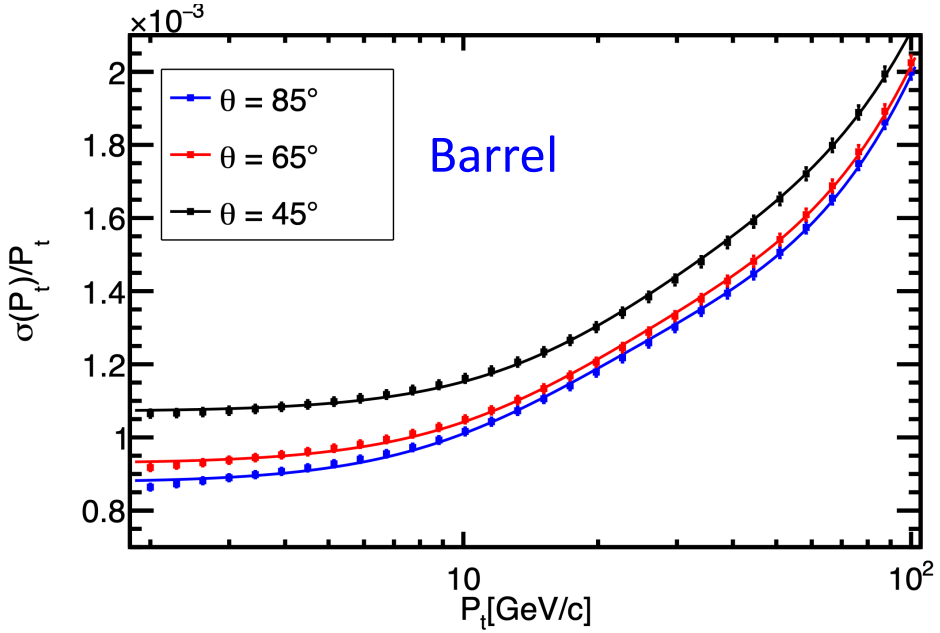
where $a = 1.5 \times 10^{-5}$, $b = 1.4 \times 10^{-3}$, $s_1 \approx 6$, and $s_2 \approx 0.8$.



Momentum resolution in the endcap region:

$$\frac{\sigma_{p_t}}{p_t} = \frac{a' p_t}{(tan\theta)^2} \oplus \frac{b'}{\beta tan\theta\sqrt{\cos\theta}} \oplus \frac{c'\sqrt{p_t}}{\sqrt{\beta}(\tan\theta)^{\frac{3}{2}}(\cos\theta)^{\frac{1}{4}}}$$

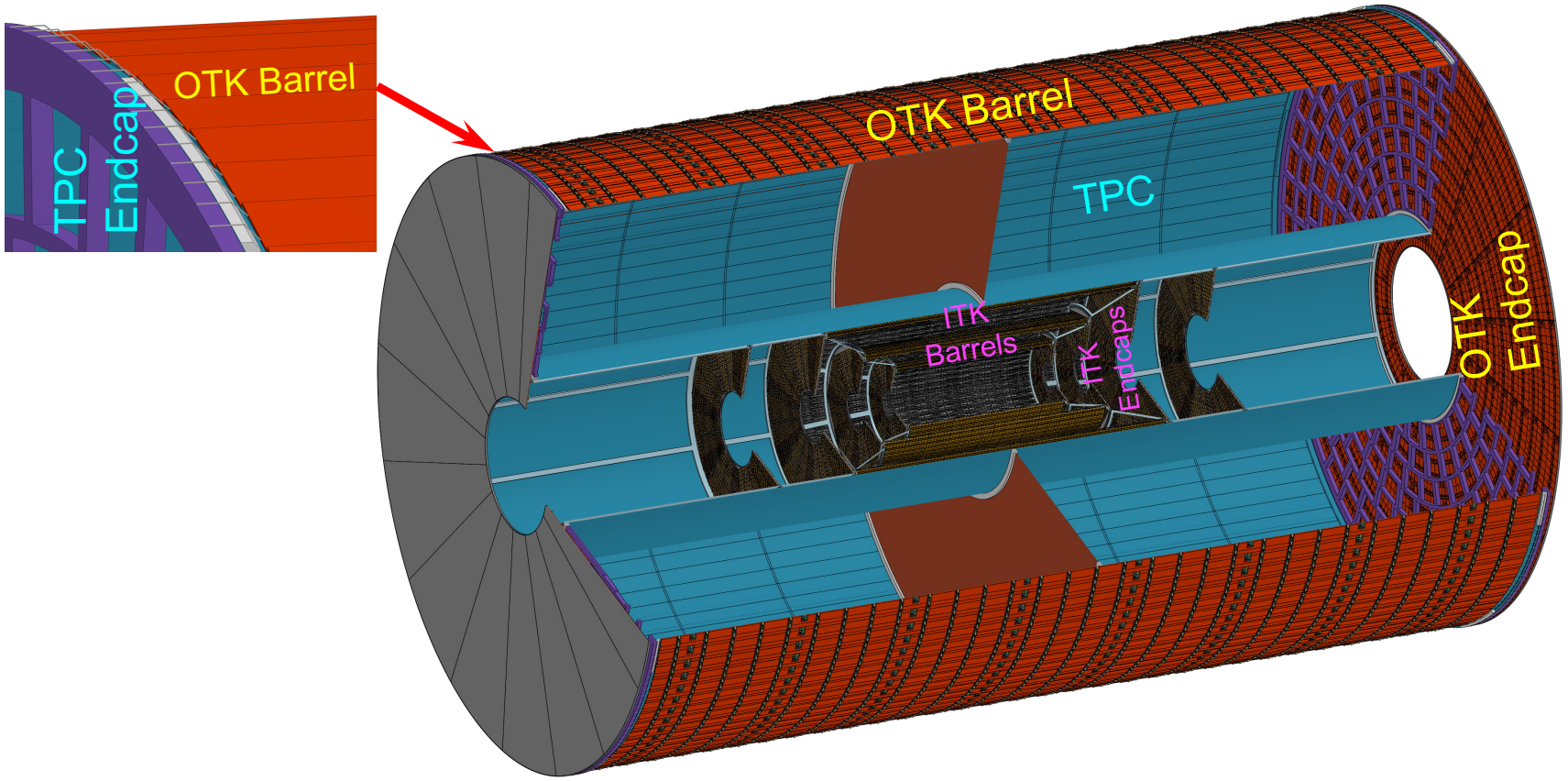
where $a' \approx 0.4 \times 10^{-5}$, $b' \approx 0.9 \times 10^{-3}$, and $c' = 4.5 \times 10^{-5}$.



对探测器分辨有系统性的了解。

Silicon Tracker Ref-TDR的下一步工作

- 进一步完成Silicon Tracker章节的内容填充、完善。
- 完成对references和figure captions的系统性整理。



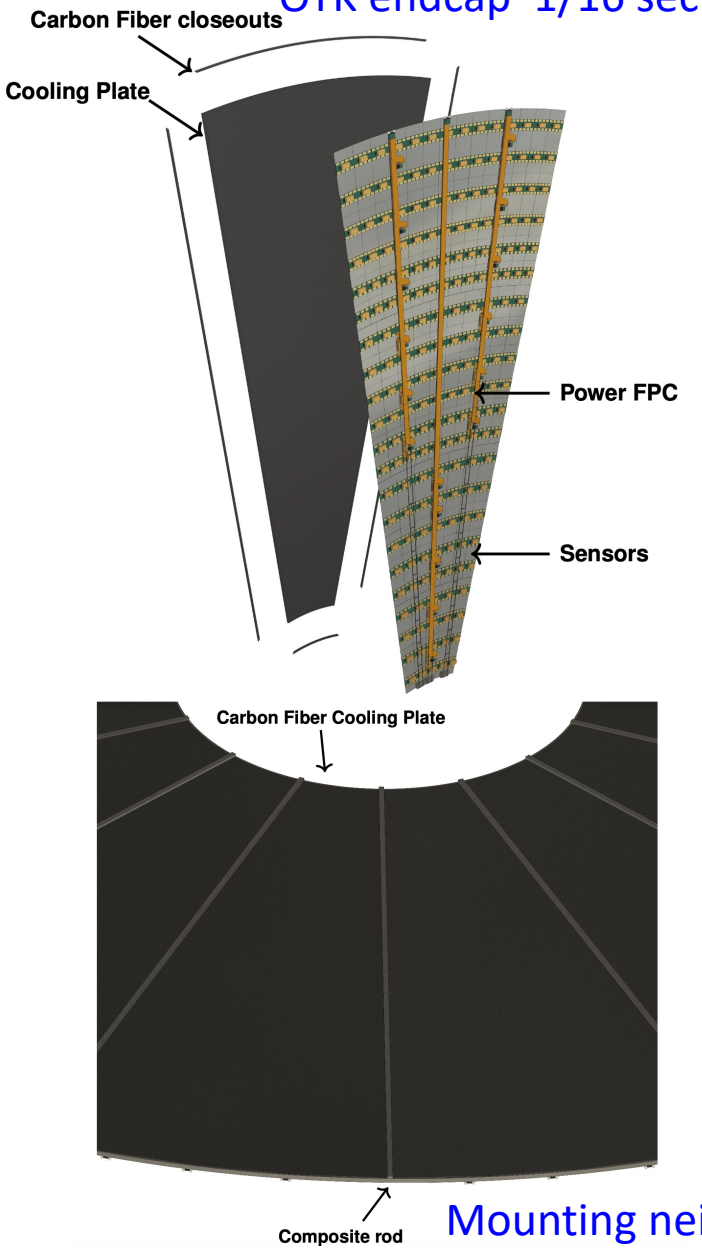
不足的地方，请大家批评指正！

Agenda

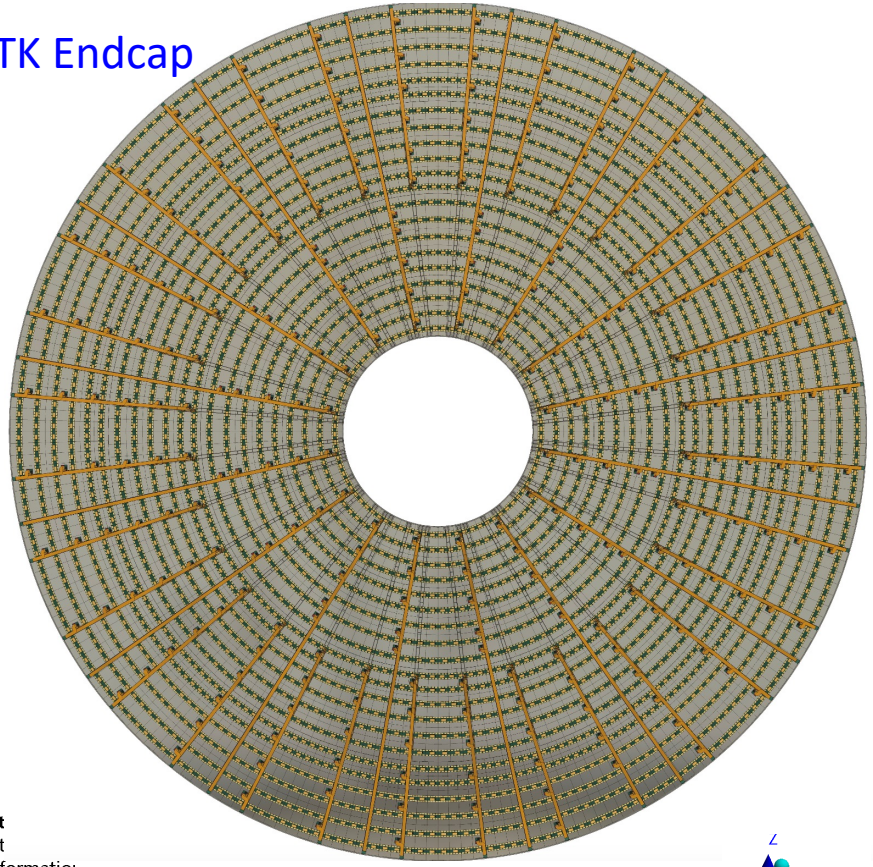
- TDR Overview (Yan Qi)
- Mechanical (Li Yujie)
- Sensor chip + Prototyping of ITK (Yiming)
- AC-LGAD chip design (Zhao Mei)
- AC-LGAD test (Yunyun)
- Electronics (Xiongbo)

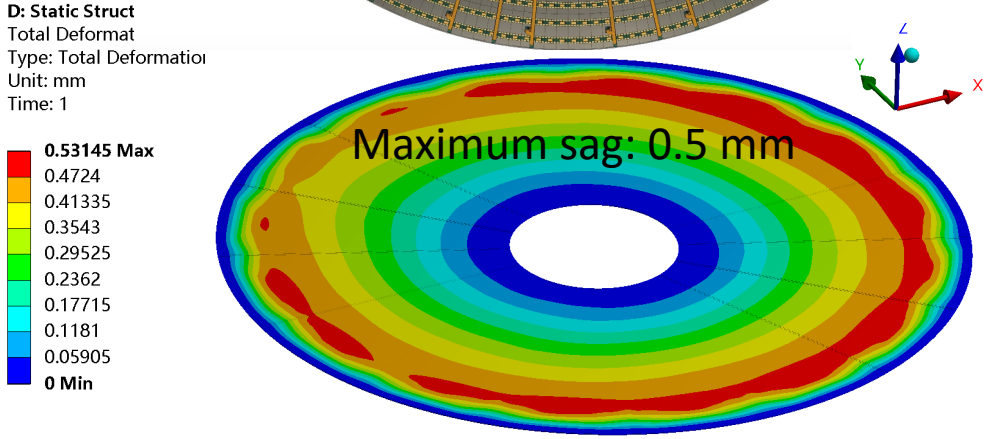
Mechanical and Cooling Design for the OTK Endcap

OTK endcap 1/16 sector



OTK Endcap





Mounting neighboring 1/16 sectors

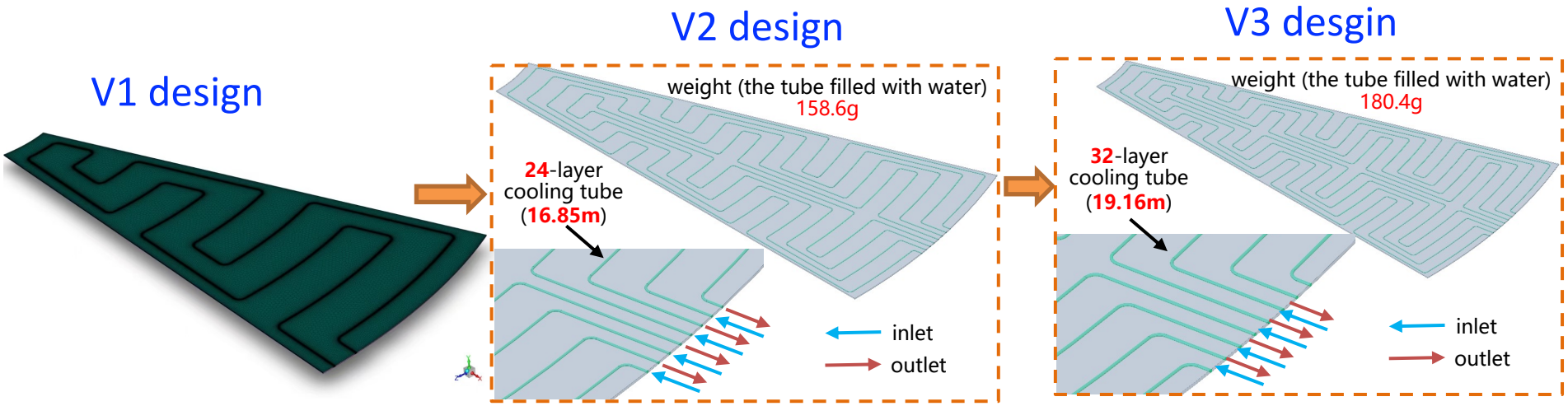
Yujie LI *and* Quan JI

Cooling Loop Design for the OTK Endcap

A few months ago, Quan Ji, Gang Li, and I visited Zhengzhou University of Light Industry, to explore ways to strengthen CEPC's R&D capabilities in mechanical and thermal systems.

The School of Energy and Power Engineering at Zhengzhou University of Light Industry has extensive experience and a strong focus on thermal system development, including CO_2 cooling. During our visit, we were highly impressed by their expertise in both thermal and mechanical engineering.

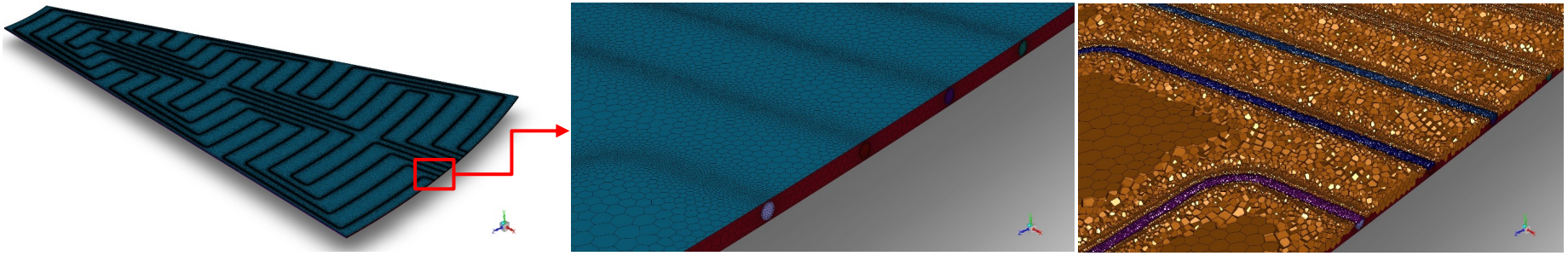
On Jan 10, the Dean of the School of Energy and Power Engineering, Professor Xuehong Wu, and his team, visited IHEP in return. They are now actively contributing to the design and analysis of the CEPC thermal system.



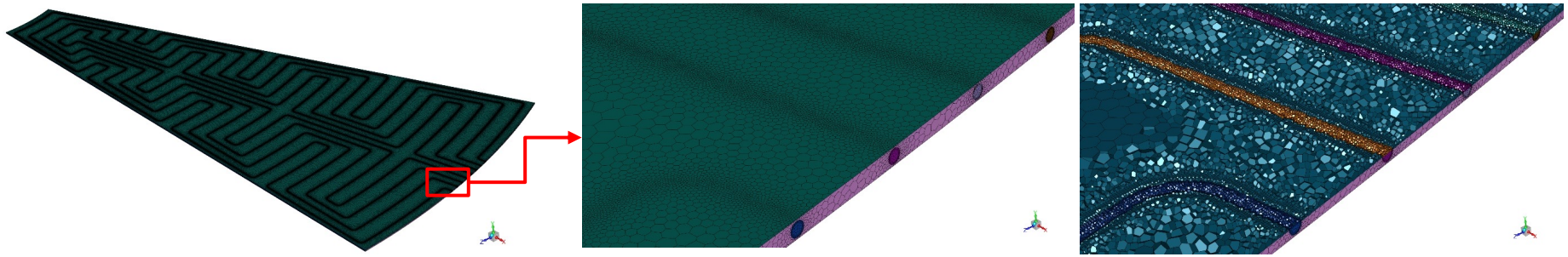
Cooling loops design and thermal analysis for the OTK endcap performed by Zhengzhou University of Light Industry（郑州轻工业大学）.

OTK Endcap Thermal Mesh Generation

ZHENGZHOU UNIVERSITY OF LIGHT INDUSTRY



24-layer cooling tube(16.85m, cell count 9356670，Orthogonal Quality≥0.5)



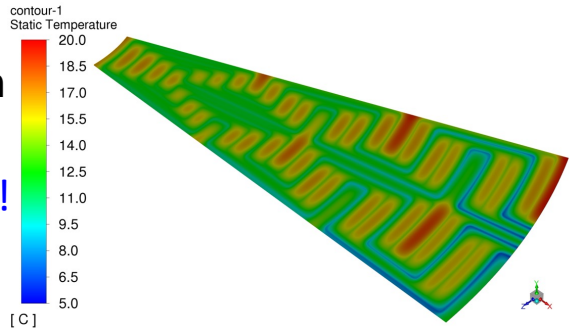
32-layer cooling tube(19.16m, cell count 10645946，Orthogonal Quality≥0.5)

- ✓ The mesh generation is performed for two different cooling tube arrangements, and numerical solutions are obtained using the finite volume method.
- ✓ The cooling performance of both arrangements is analyzed and compared.

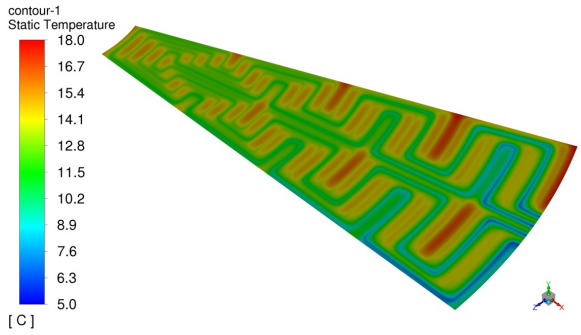
- Cooling tube diameter: 2.6 mm
- Water inlet velocity: 2.5m/s

Continuous optimization is ongoing!

Xuedong Wu, Yong Liu, ...
(郑州轻工业大学)



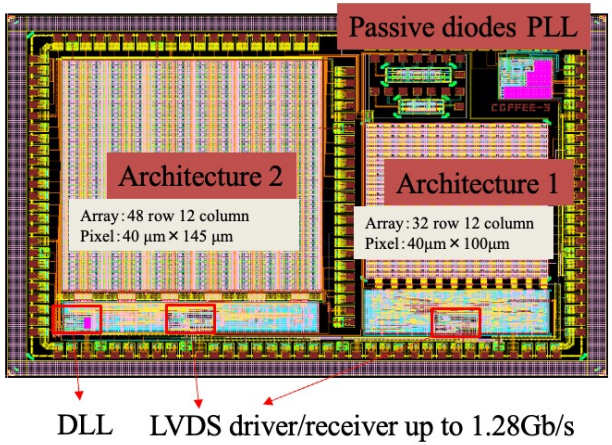
24-layer cooling tube



32-layer cooling tube

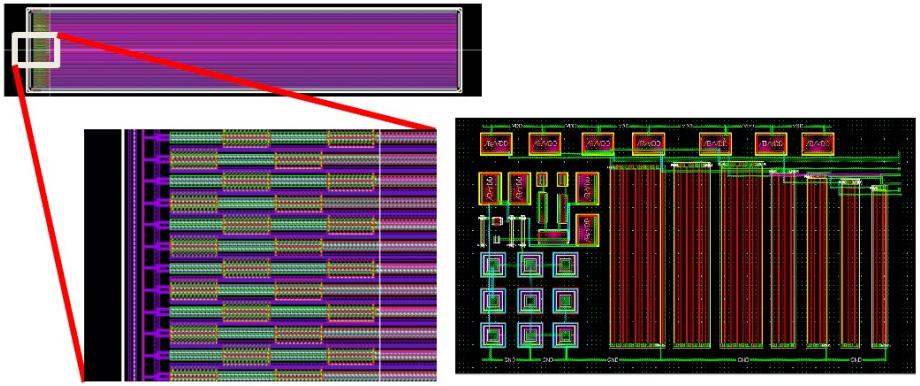
Sensor and ASIC R&D Plan

- HV-CMOS Pixels (COFFEE3):



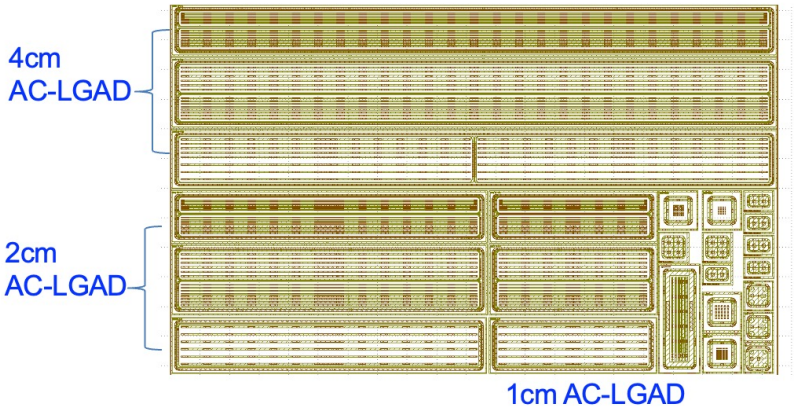
Submitted in 2025.1 and expected received in 2025.5

- CMOS Strips (CSC1):



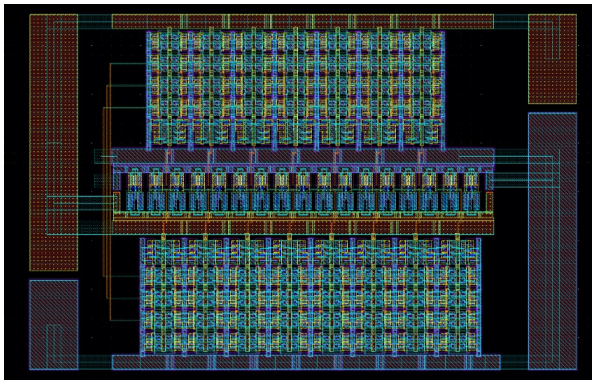
Scheduled for submission on March 5, 2025

- AC-LGAD Strips



Scheduled for submission in Feb 2025

- Pre-phototype for AC-LGAD ASIC (JuLoong, 烛龙)



Scheduled for submission in April 2025