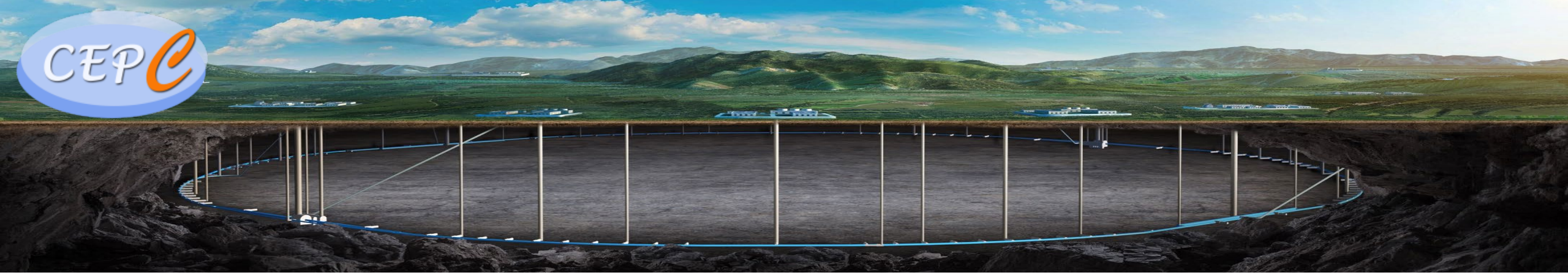


Brief Overview of the CEPC Electronics System

Wei Wei
On behalf of the CEPC Elec-TDAQ study team

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Content

- Introduction
- Global framework of the electronics system
- Schedule of the ASIC development
- Summary

Requirement from Sub Detectors (@Higgs)

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit	42bit	32bit	40~48bit		48bit	48bit				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg: 2.9Mbps/chip Max: 3.85Mbps/chip	Avg: 38.8Mbps/chip Max: 452.7Mbps/chip	~70Mbps/ module Inmost	Avg. 0.96Gbps/module Max:9.6Gbps/module		Max. 144Mbps/module-layer	Max. 350Mbps/module-layer	Avg: 15.36 Mbps/chip Max: 153.6 Mbps/chip
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)		< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	<=24:1 @ O (400 Mbps)
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	0.52M chn ~32500 chips 260 modules	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	43.2k ch 72 Aggregation board
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	460Gbps	250Gbps	811.2Gbps	537.6Gbps	~ 24.1 Gbps

Consideration on global framework of Elec-TDAQ

- Two main stream frameworks for the electronics-TDAQ can be simply categorized as FEE-triggerless readout & readout with conventional trigger
- Comparison on main aspects

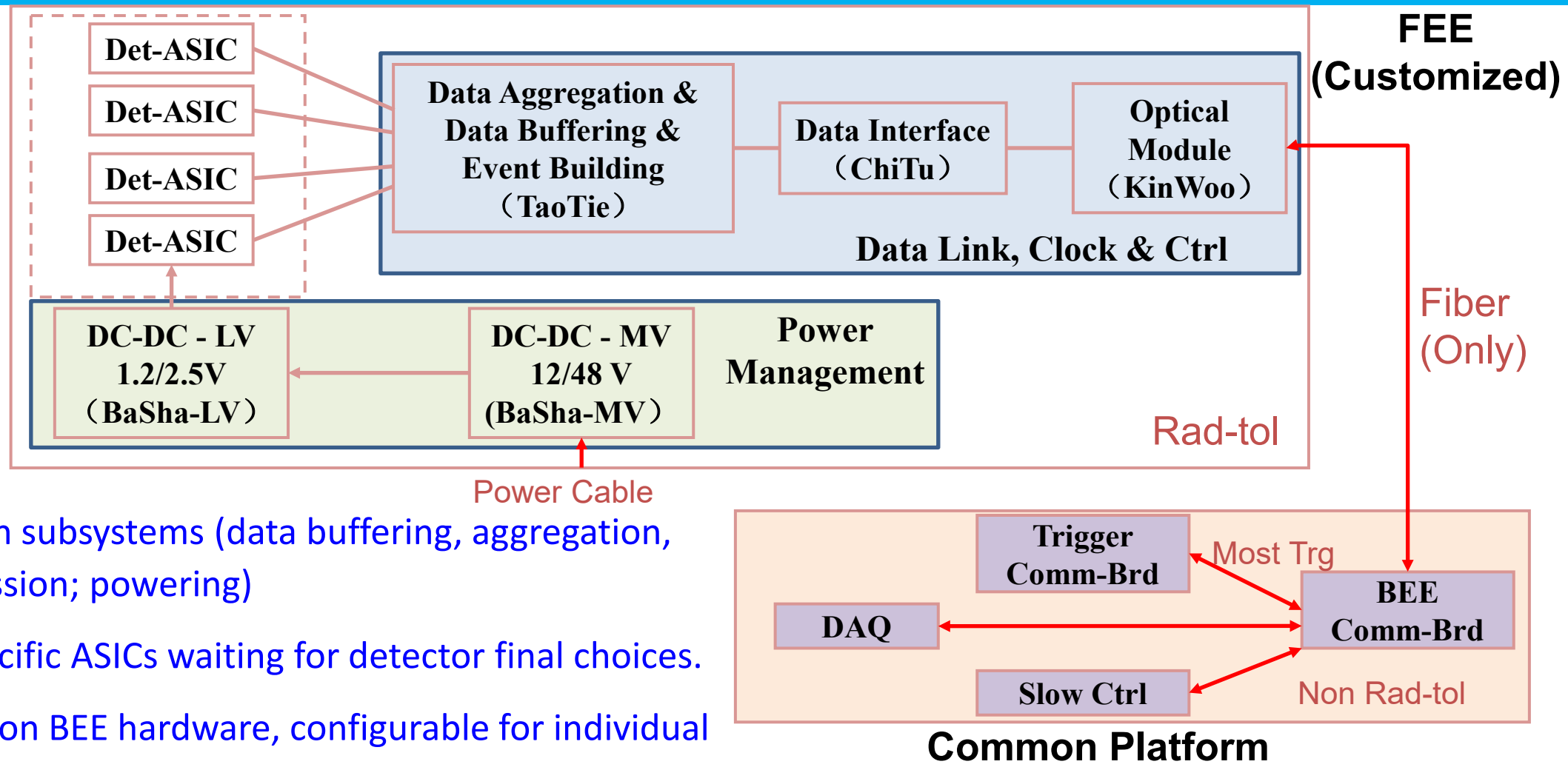
	FEE-Triggerless	Conventional Trigger	Superiority
Where to acquire trigger info	On BEE	On FEE	FEE-Triggerless
Trigger latency tolerance	Medium-to-long	Short	
Compatibility on Trigger Strategy	Hardware / software	Hardware only	
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm	
Upgrade possibility on new trigger	High	Limited	
FEE data throughput	Large	Small	Conventional Trigger
Maturity	Mature but relatively new	Very mature	
Resources needed for calculation	High	Low	
Representative experiments	CMS, LHCb, …	ATLAS, BELLE2, BESIII, …	

Our choice on global framework

- We choose **FEE-triggerless readout (Backend Trigger) as our baseline global framework, while keep conventional trigger readout as the backup**, for the Elec-TDAQ system:

1. Maintain the maximum possibility for new physics and future upgrades.
   - Readout all the information w/o pre-assumed trigger conditions.
2. Speed-up the FEE-ASIC iteration & finalization process
   - W/o the need to consider the undefined trigger algorithm, esp. regarding the potential tight schedule.
3. Enable a common platform design for all Sub-Detectors
   - Common BEE Brd, common Trg Brd, common data interface…
   - Scalable based on the detector volume
4. Sufficient headroom for FEE data transmission based on the current MDI background rate
   - 10Gbps per link on FEE (max by ×4 links)

Global framework of the CEPC Elec system



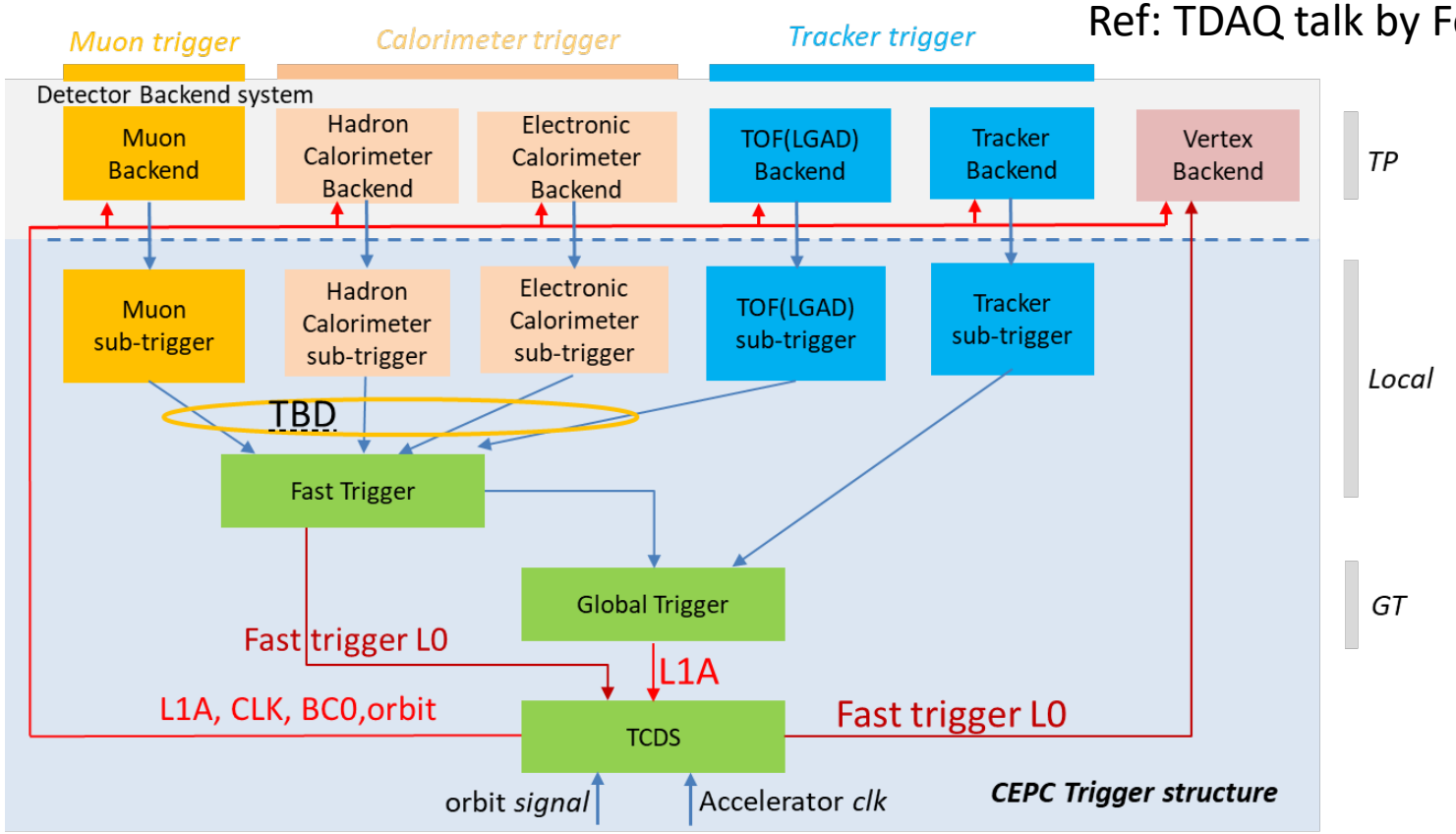
- Common subsystems (data buffering, aggregation, transmission; powering)
- Det. specific ASICs waiting for detector final choices.
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

Backup scheme of the framework

- The proposed framework was based on the estimated background rate of all sub-det.
- In case of under-estimation or unexpected condition:

1. Additional optical links can be allocated to the hottest module.
2. In case the background rate is too high for FEE-ASIC to process, Intelligent Data Compression algorithm can be integrated on-chip, for the initial data rate reduction.

Ref: TDAQ talk by Fei Li



The conventional trigger scheme can always serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

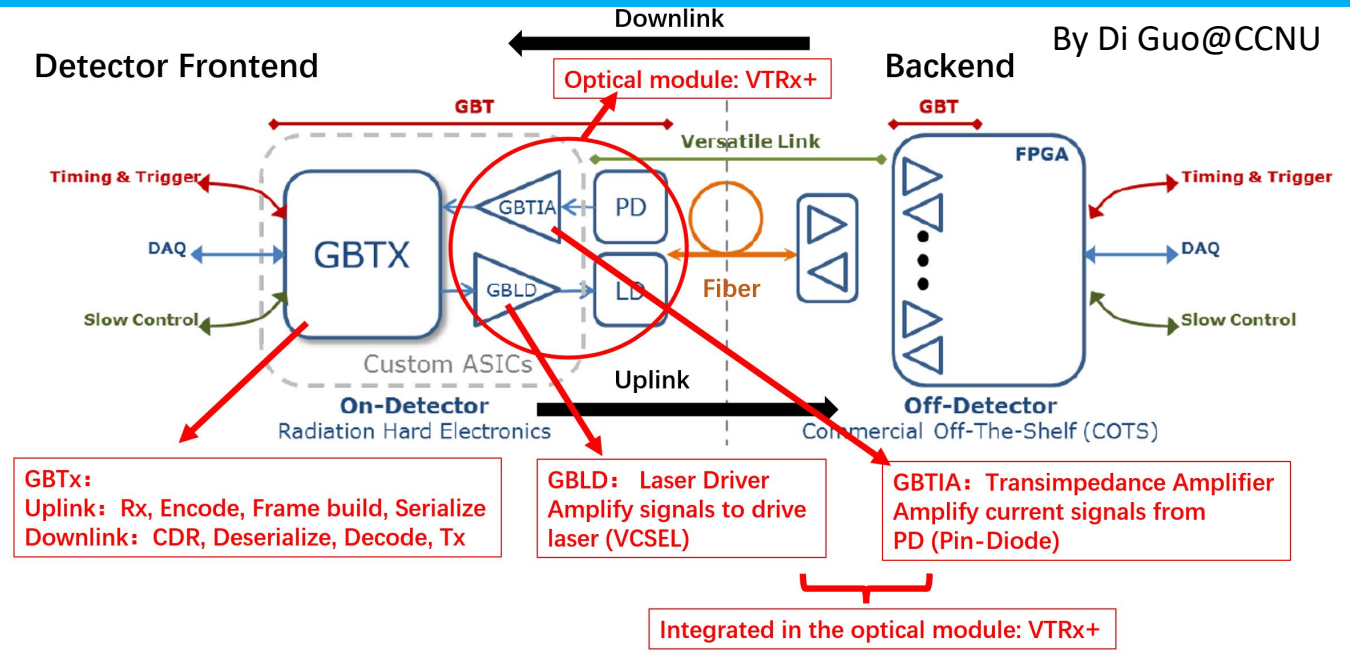
Key Electronics Components

- Key components of the Full CEPC Electronics System
  - Customized FEE, mostly ASIC based
    - ASICs for each sub-detector
    - Common Data Link
    - Common Powering
    - FEE PCB & interconnection
  - Common Backend Electronics
- SiPM will be shared by ECAL/HCAL/Muon, also becomes a common device
  - So as the SiPM ASIC ChoMin

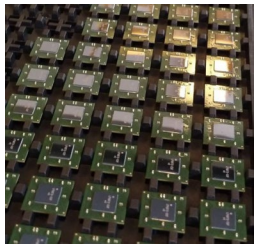
Technical Survey on Data Transmission System

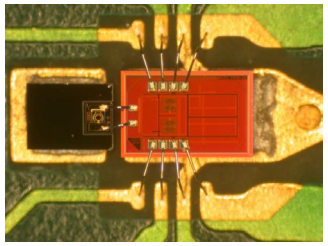
- GBT Project:
  - The lpGBT & VTRx chip series, developed by CERN, are widely used by LHC experiments, as a common project
  - Core components:
    - GBTx: Bidirectional Serdes ASIC
    - GBLD: Laser driver
    - GBTIA: Transimpedance amplifier
    - Customized Optical Module
- Our choice:
  - Build a GBT-like universal bidirectional data transmission system
  - Take the lpGBT as a reference, the protocol can be a minimum & necessary set for the readout, clocking & control

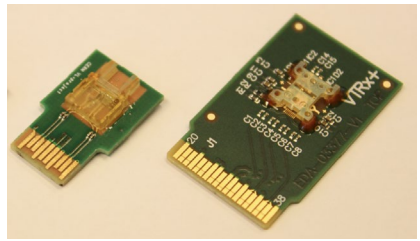
By Di Guo@CCNU



GBT Architecture Developed by CERN







lpGBTx
Uplink: 10.24Gbps
Downlink: 2.56 Gbps

GBLD (LDQ10)
10.24 Gbps x 4ch

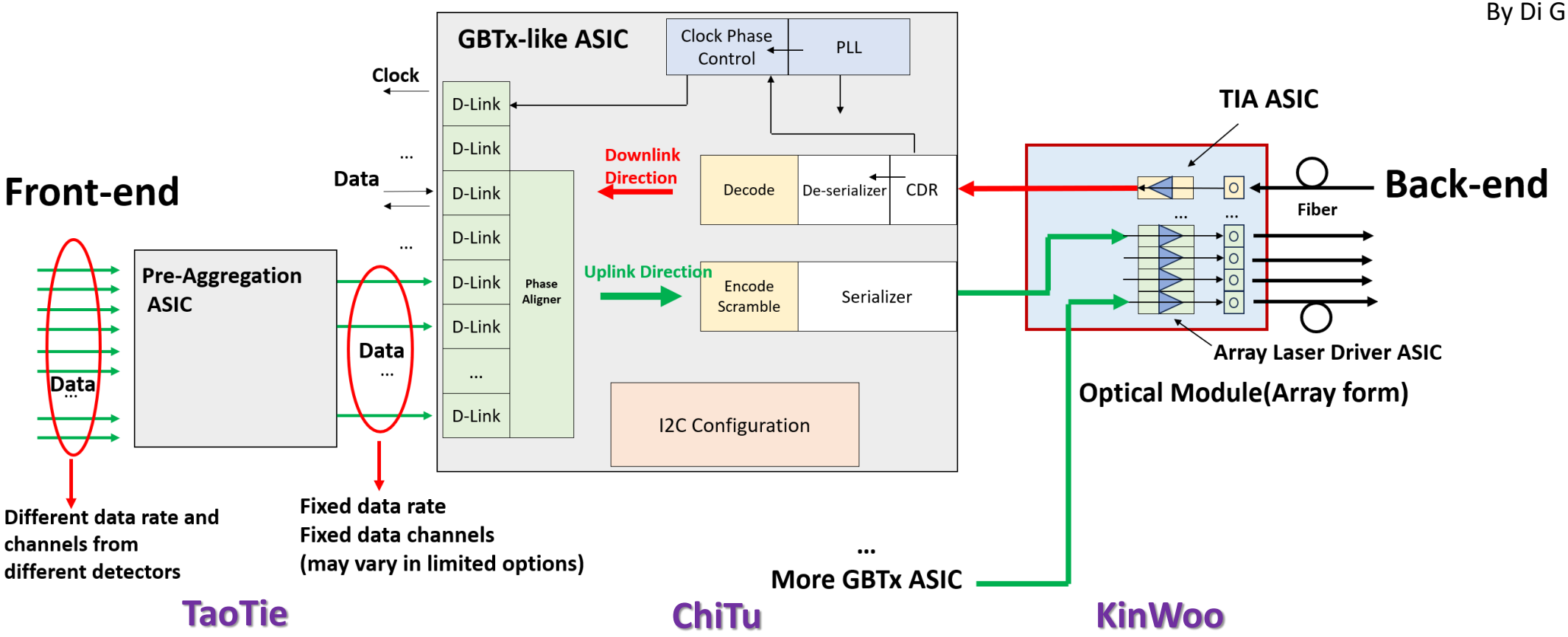
GBTIA
2.56 Gbps

VTRx+
4Tx + 1Rx
Array Optical Module

GBT Series ASICs and optical module

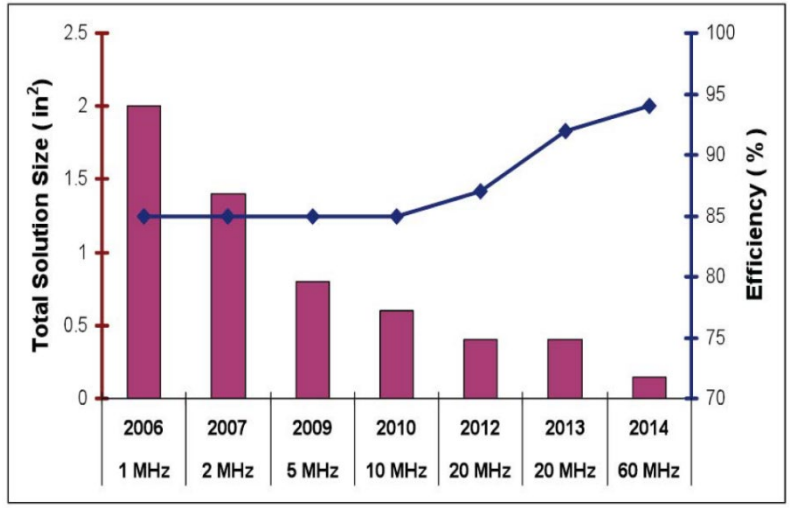
Detailed design on Data Transmission Structure

By Di Guo@CCNU

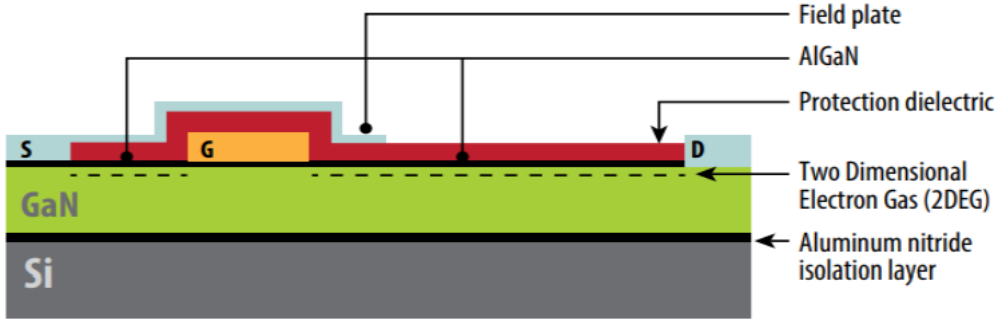


- Pre-Aggregation ASIC (TaoTie): Intend to fit with different front-end detector (different data rates/channels)
- GBTx-like ASIC (ChiTu): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …
- Array Laser Driver ASIC + TIA ASIC + Customized Optical module (KinWoo)

Technology survey and our choice on Powering

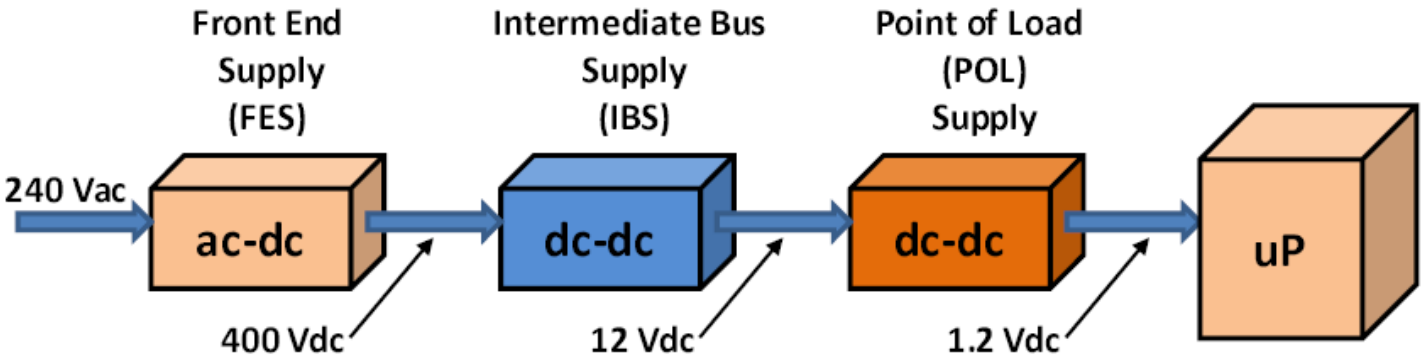


Higher switching Freq, smaller size,
higher efficiency, lower on-resistance



Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel)

Ref. Satish K Dhawan, 2010
Ref. S. Michelis, Prospects on the Power and readout efficiency



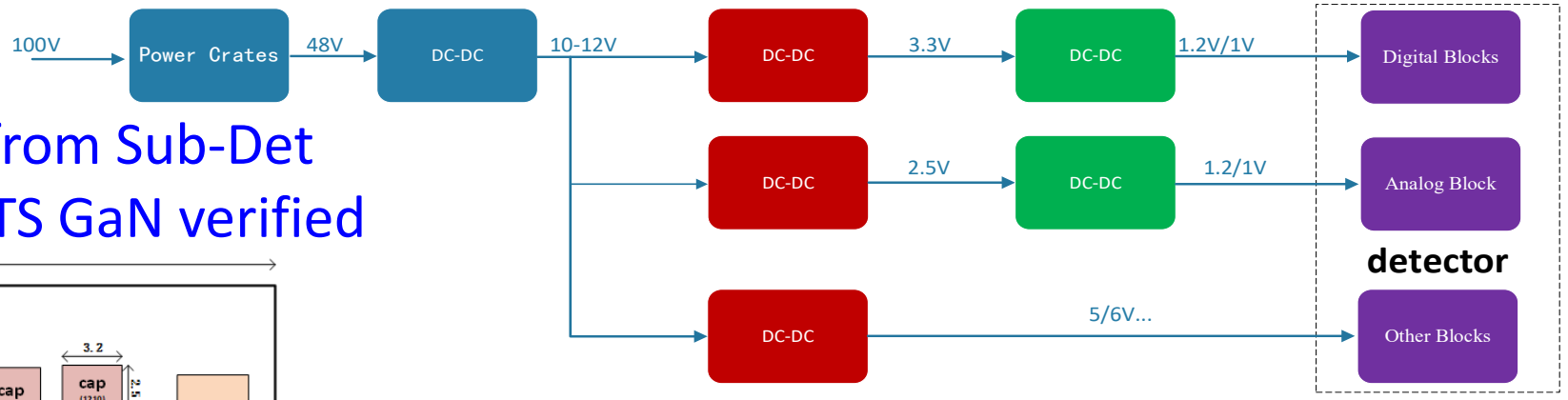
A 400V to 1.2V chain, lower power loss on cable

- Investigation was also conducted to compare the key component schemes of the power module, esp on LDO & DC-DC convertor.
- The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.
- We choose a GaN-based DC-DC as the baseline power module scheme. This also enables high voltage power distribution, for low cable material and low power loss.

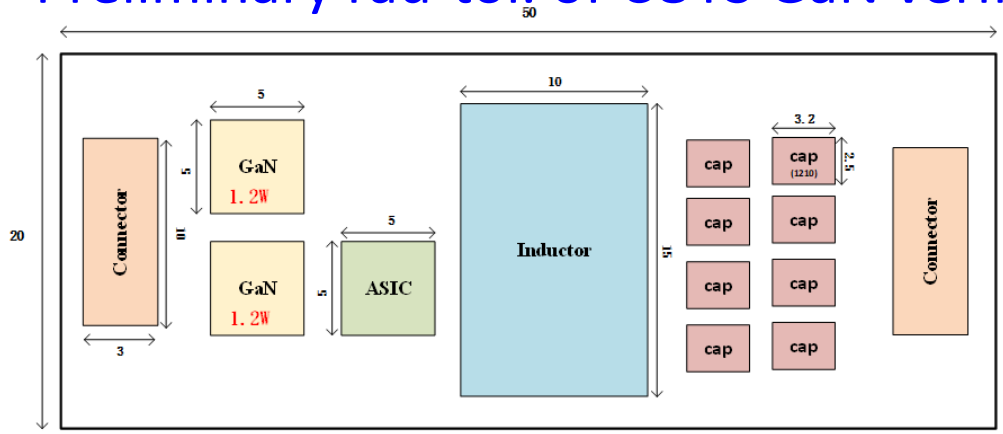
R&D efforts preliminary design on powering

- Structure of the power distribution system

By Jia Wang@NPU



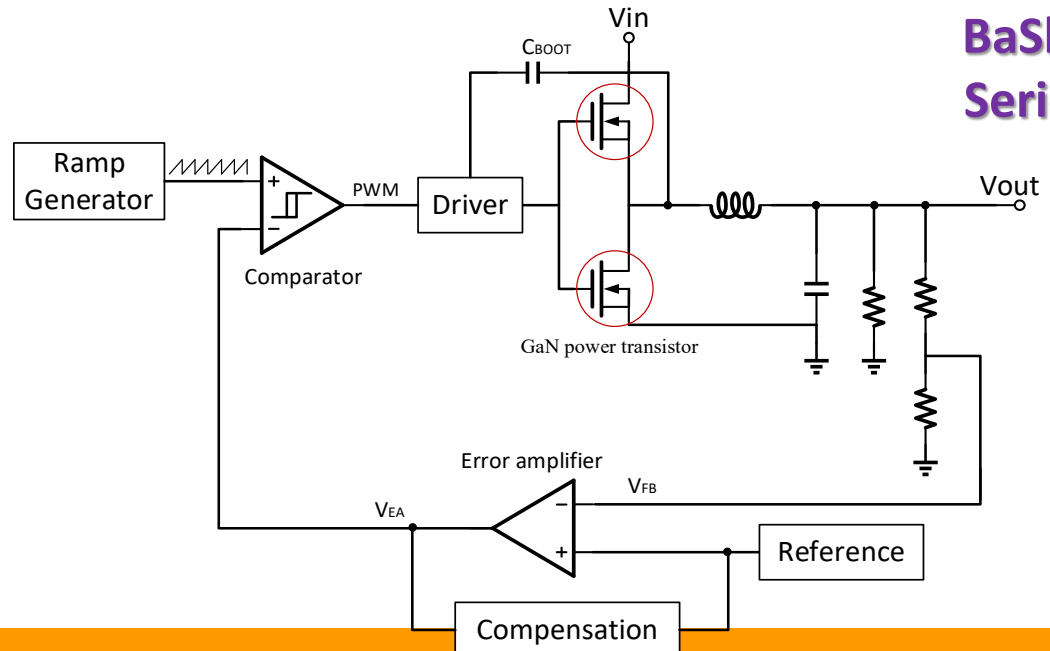
- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified



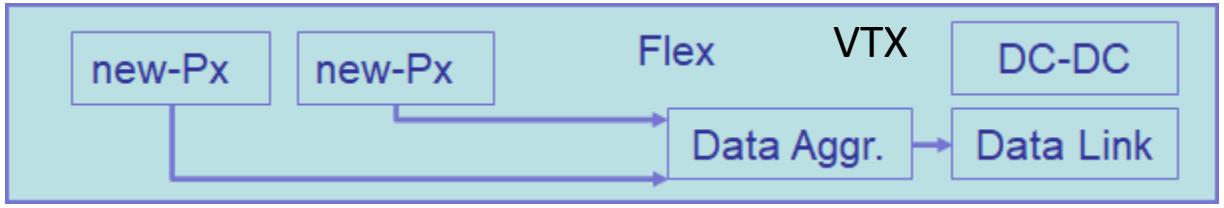
	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、2.5V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

- Proposed design of BUCK DC-DC convertor

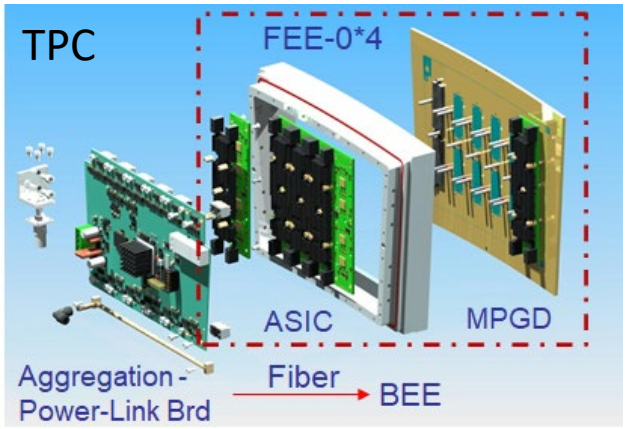
BaSha Series

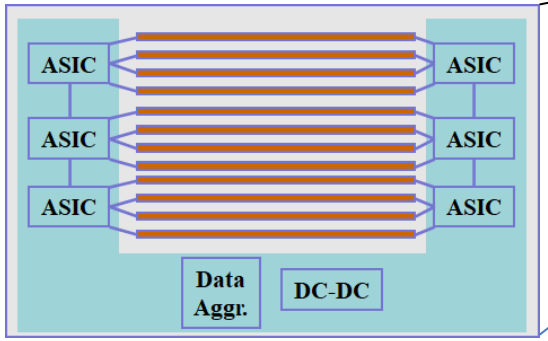


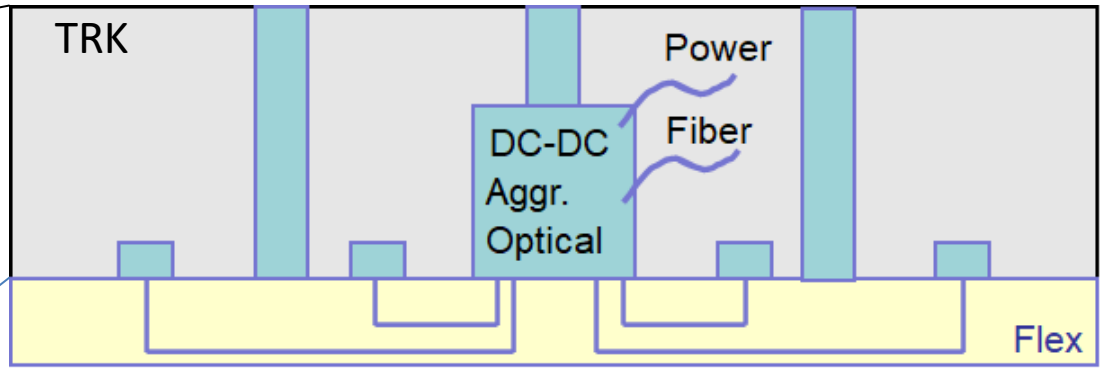
An overview of the Sub-Det readout Elec.

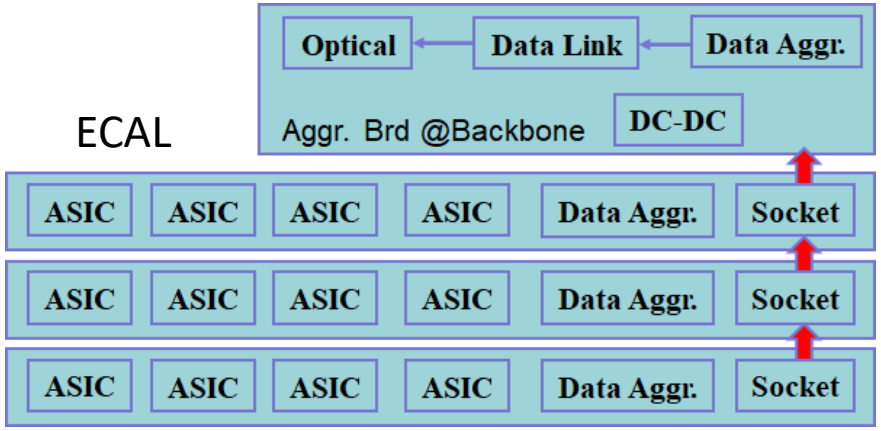


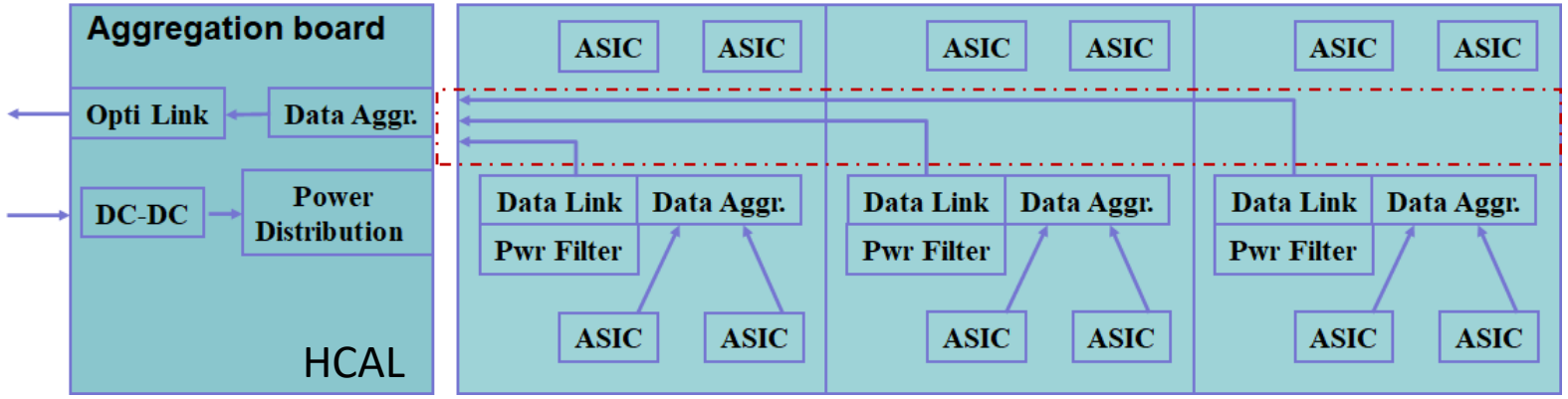
- All sub-det readout electronics were proposed based on this unified framework, maximizing the possibility of common design usage.



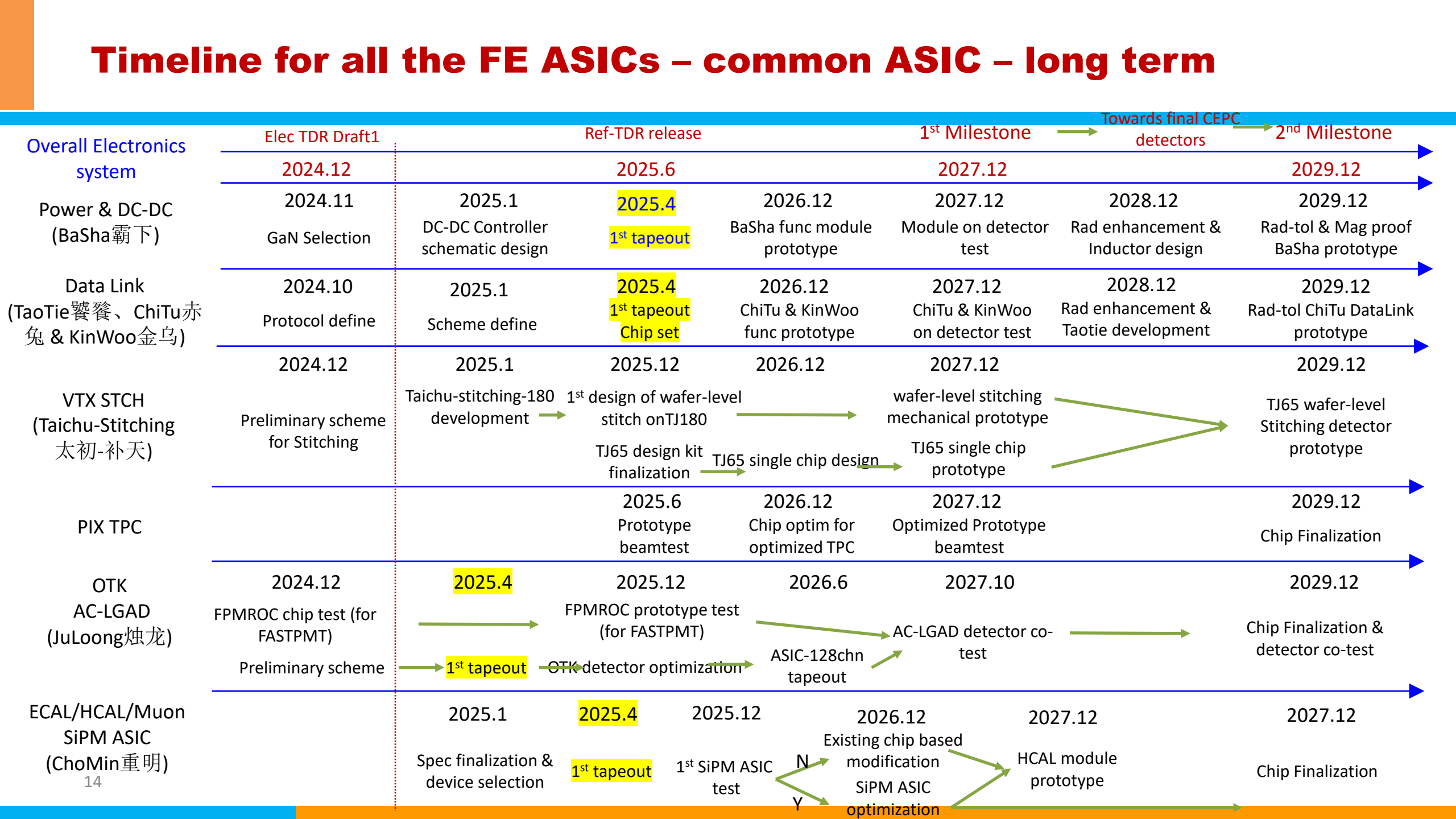






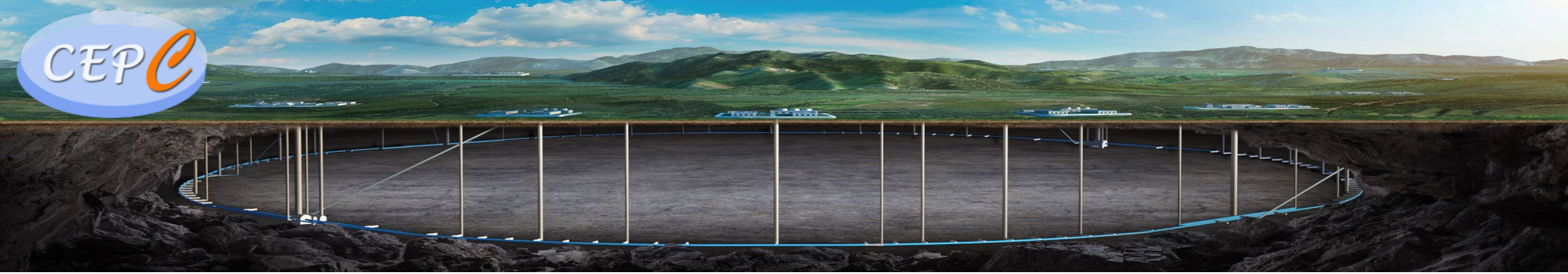


Timeline for all the FE ASICs – common ASIC – long term



Arrangement of this review

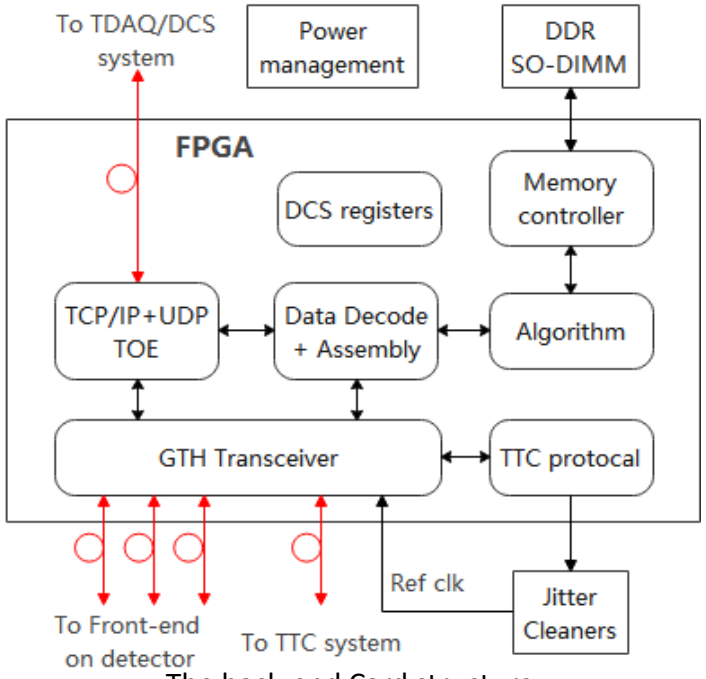
- 在所有前端ASIC中，共4种/组ASIC待研发，其他芯片均已有初步原型设计及测试结果
- 计划将在2025年集中进行第一版芯片设计，本次芯片评审主要考察总体方案、系统接口考虑
- 数据传输芯片组：数据汇总+数据接口+光电模组
- 前端电源模块
- SiPM读出芯片—重明
- OTK读出芯片—烛龙



Thank you for your attention!

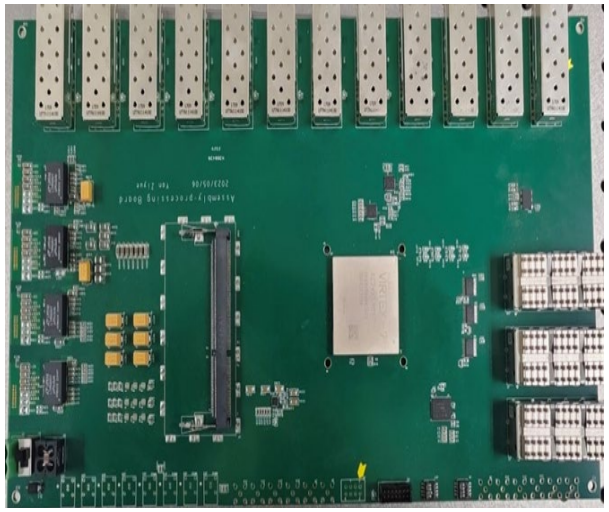
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Detailed design on common BEE



The back-end Card structure

By Jun Hu@IHEP



Data aggregation and processing board Prototype for Vertex detector

	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data between the optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

- A cost-driven device selection: FPGA XC7VX690T
- Interface： SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

Naming of the common ASICs

ChiTu & Guan Yu

KinWoo in the sun

TaoTie

BaSha carrying a monument

- GBTx-like: ChiTu (赤兔）， the most famous horse in Chinese tales, ridden by the Chinese God of War Guan Yu. It is in charge of transportation with ultra fast speed, just as GBTx-like chip is doing.
- VTRx: KinWoo (金乌）， the bird who lives in the sun in Chinese tales, an avatar of the sun and in charge of the light, just as the VTRx chip does, to convert electronic signal to/from optical.
- Data aggregation: TaoTie (饕餮）， a mythical animal in Chinese tales, who can swallow anything, just as the chip does, to collect all the input data streams.
- DC-DC module: BaSha (霸下）， one of the nine sons of the Chinese Loong, who is famous for its strongness and always to bear a monument. Just like the powering system which is the basement and support of all electronics.

Naming of the new FEE ASICs

Nuwa Mends the Sky (Taichu-Stitching)

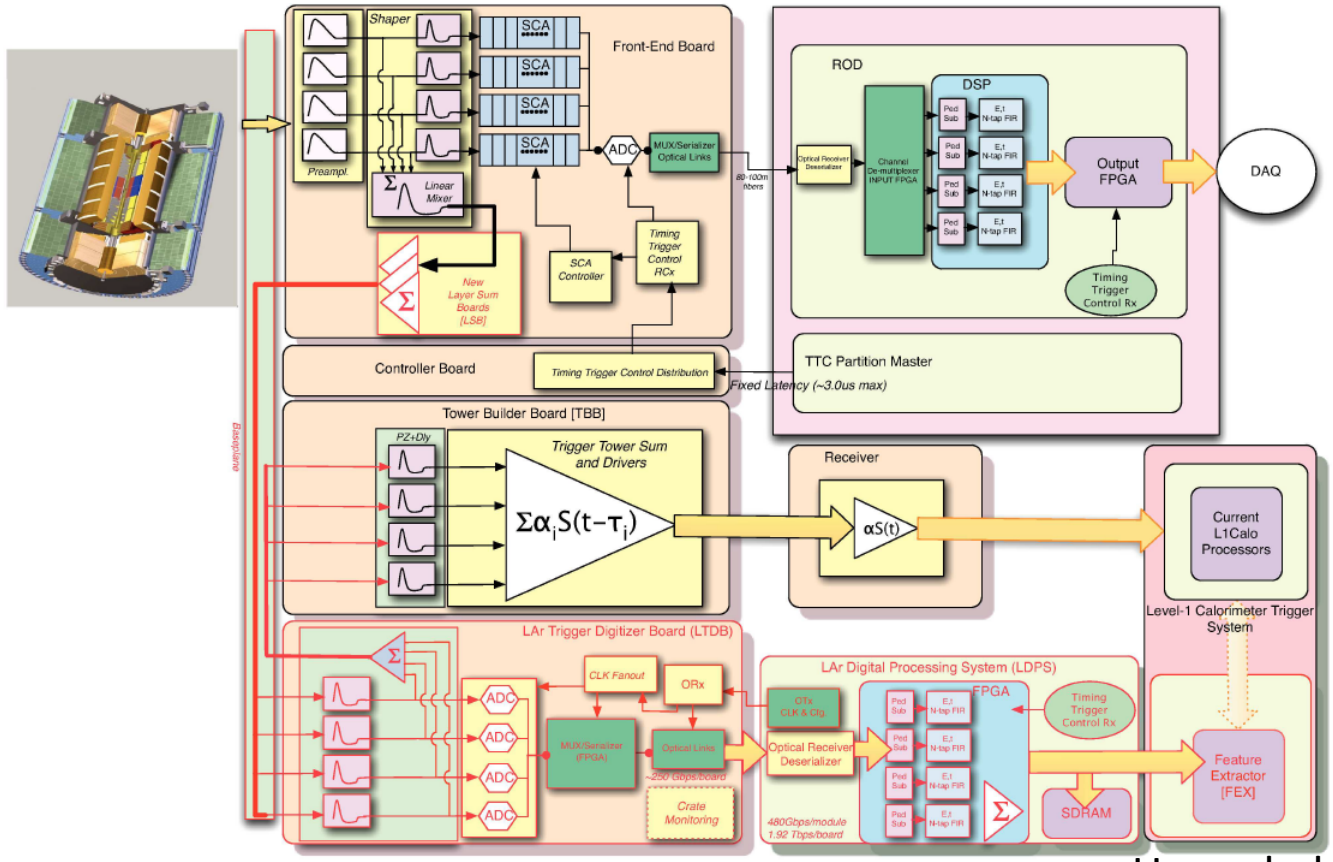
JuLoong in Classic of Mountains and Seas

A statue of the bird of ChoMin

- Taichu-Stitching(太初-补天) @ VTX:
  - One of the most events happened in the very beginning of the ancient world (Taichu's Period 太初时期) is "Nuwa Mends the Sky（女娲补天）", well known in Chinese story. The action mending equals to stitching, both make a surface seamless.
- JuLoong(烛龙) @ OTK:
  - A divine beast in Chinese mythology that governs time. As the front-end ASIC of the OTK detector, its primary design goal is to achieve the highest time resolution performance of the entire detector, corresponding to the function governed by JuLoong
- ChoMin (重明) @ SiPM for ECAL/HCAL/Muon:
  - An ancient Chinese legend tells of a mythical bird called "Double Vision" with two eyeballs in each eye. This bird will serve as a versatile ASIC in ECAL, HCAL, and Muon detectors, symbolizing the concept of ChoMin, which is to detect signals from multiple detectors. The main design challenge is to accommodate the wide dynamic range of ECAL, so the chip will feature dual-range amplification in the front-end, aligning with the idea of multiple visions.

Technology survey on global framework

ATL-CAL-PROC-2017-001

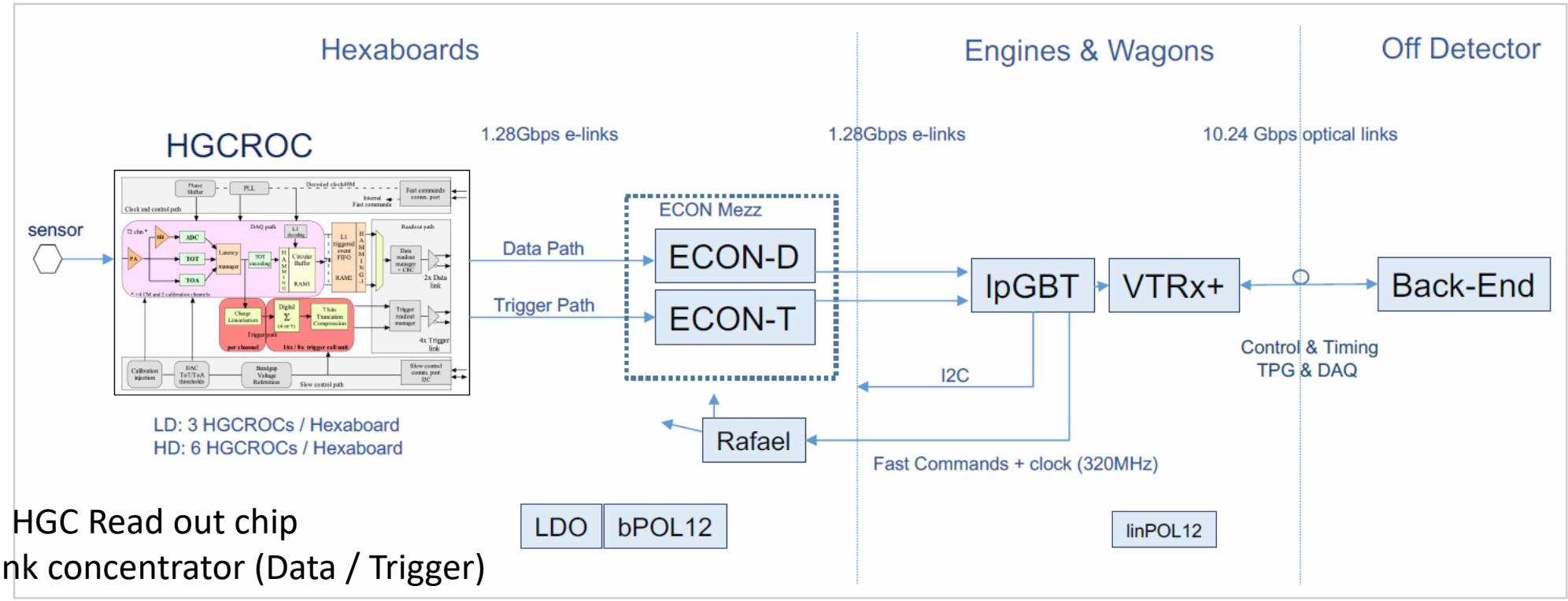


Upgraded LAr readout schemes for Phase-I

- A typical readout framework can be referred to ATLAS detector system(e.g. LAr CAL)
- It can be noted the FEE not only has to generate and send out trigger info.(e.g. SUM), but also store data for trigger latency and accept the trigger decision.

Technology survey on global framework

From Paul Aspell, CMS HGCAL An Electronics Perspective



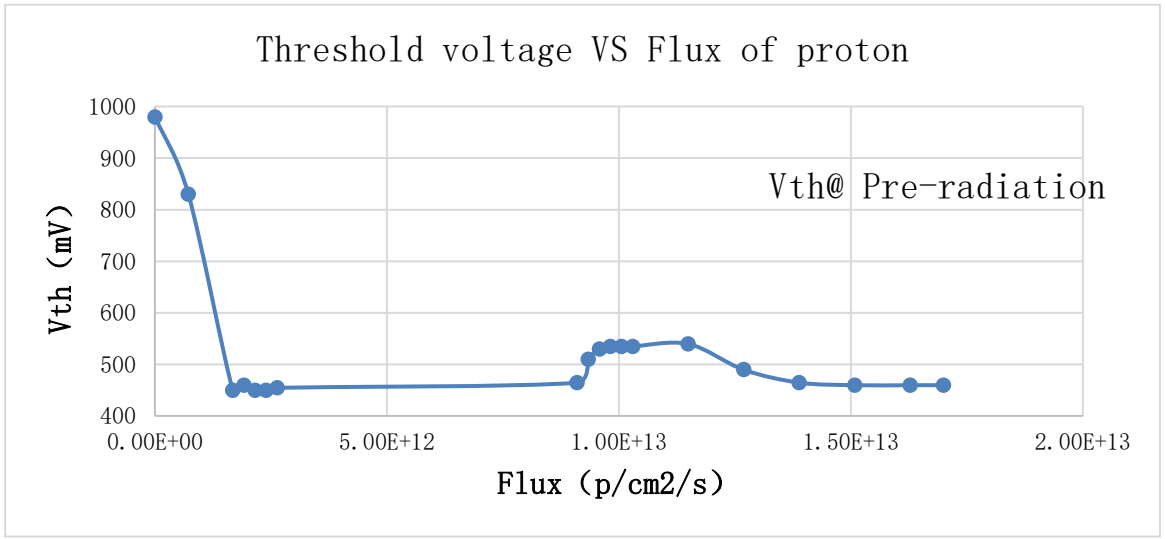
HGCROC: HGC Read out chip
ECON: elink concentrator (Data / Trigger)

- The electronics readout framework can also be inspired by CMS detector system(e.g. HGCAL).
- It can be observed that the data stream is mostly in a single direction to the BEE, and the electronics system architecture is relatively compact.

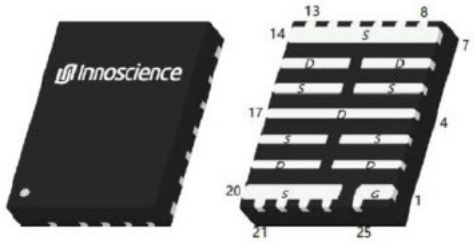
Requirement of the powering system

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Technology	65nm CIS	55nm HVCMOS	55nm HVCMOS	55nm CMOS		65 CMOS	55nm CMOS (or 180 CMOS?)				
Power Supply Voltage (for DC-DC) (V)	1.2	1.2	1.2	1.2		1.2	1.2 (or 1.8?)				
Power@chip	40mW/cm^2 200mW/chip	200mW/cm^2 800mW/chip	200mW/cm^2 336mW/chip	20mW/chn 2.56W/chip		280μW/chn 35mW/chip	15mW/chn 240mW/chip				
Max chips@module	29	14	22	22	3	1115	64	Needs detector finalization	8~30	92~365	Needs detector finalization
Power@module (W)	5.8	11.2	7.39	56.3	58.9	39.7	30	Needs detector finalization	9~36	21.9~87.5	Needs detector finalization

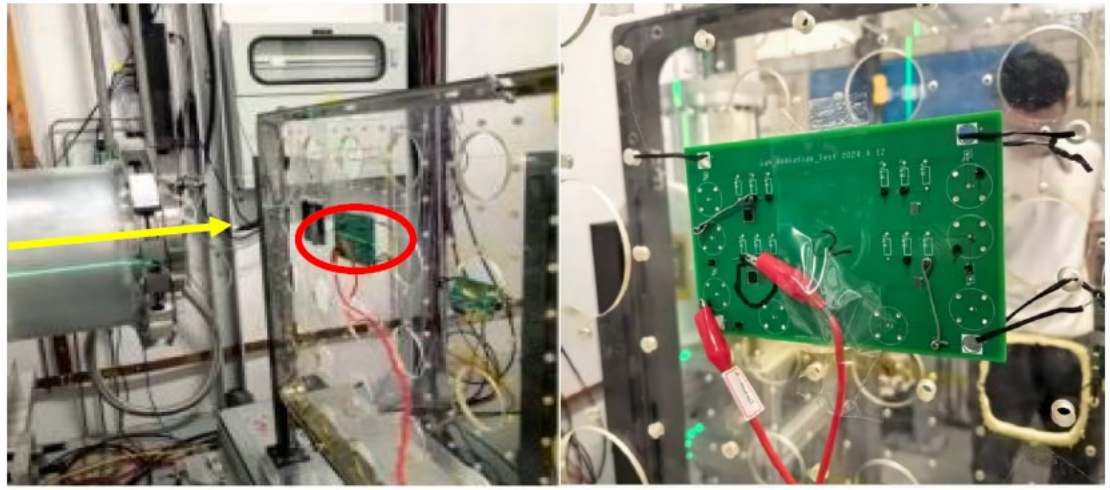
Update on common Power module



- Power requirements summarized according to the current readout schemes of each SubD
- Rad-test of COTS samples initiated, preliminary proved the GaN transistor can survive in the CEPC rad environment
- Recent plan:
  - Key component evaluation



测试仪器：源表、电源、万用表

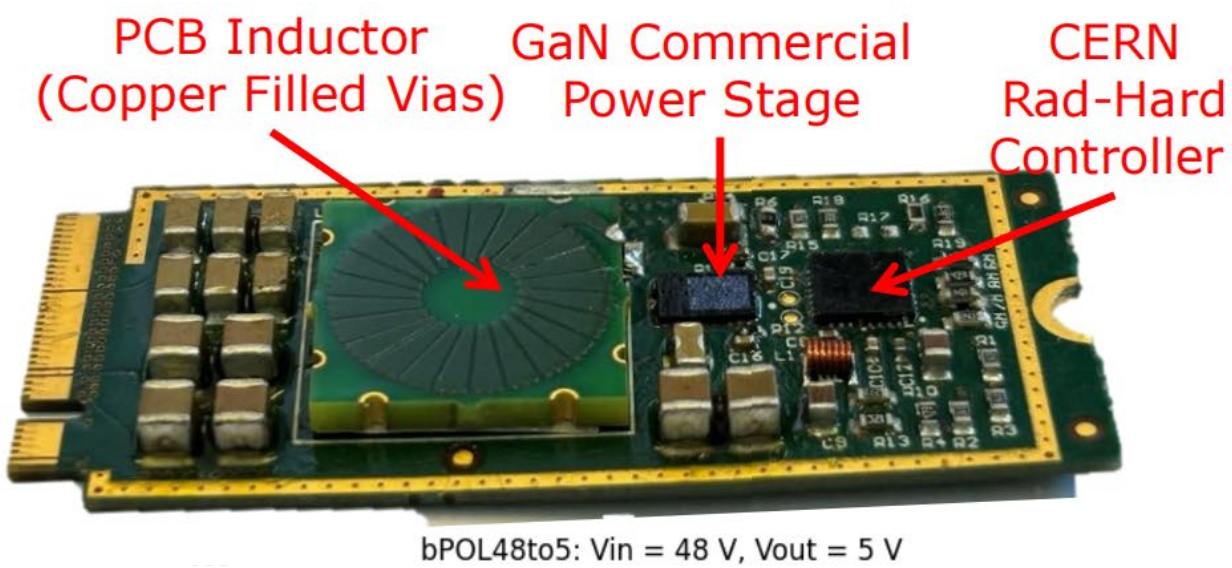


测试PCB固定到样品台上的实物照片(左图中黄色箭头为束流方向)

Using available stock of bPOL48V (~70K dies)

Volume optimized bPOL48 modules:

- bPOL48to12 (EPC2152): 48V to 12V with 6A out
- Dimensions: 24 x 55 x 4 mm



bPOL48to5: Vin = 48 V, Vout = 5 V

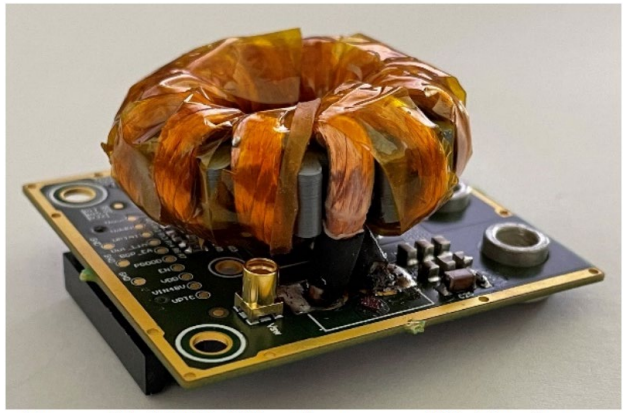


Figure 14: bPOL48V with air-core 220nH inductor.

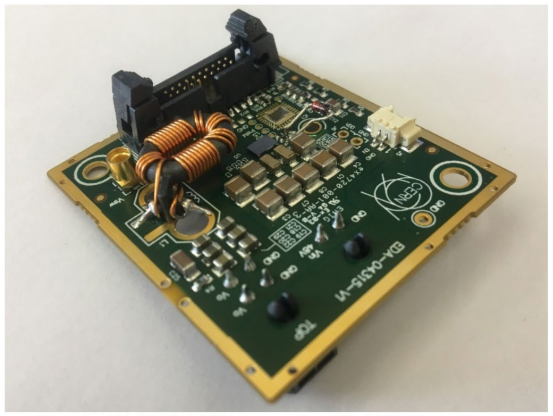
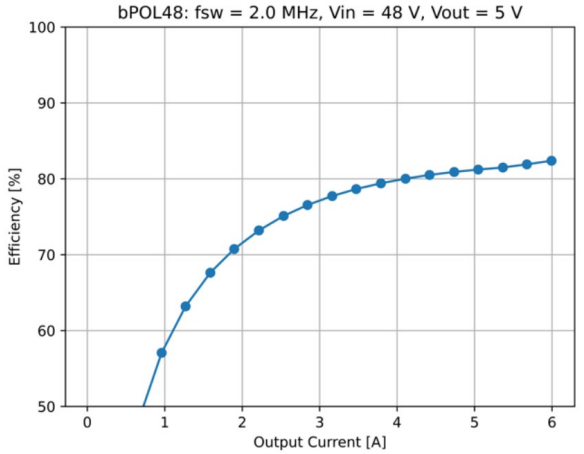
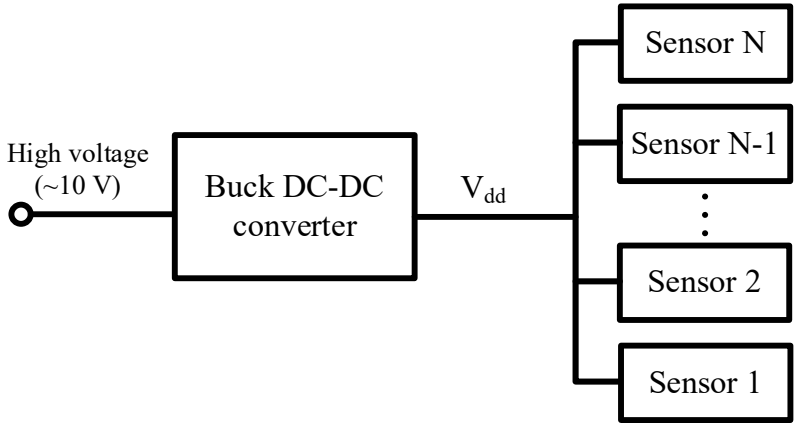


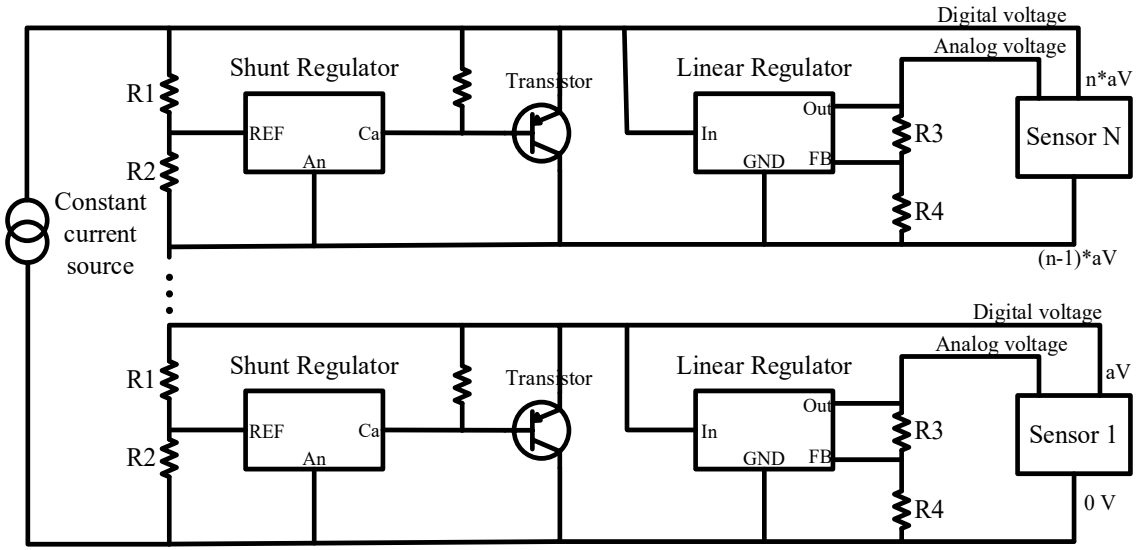
Figure 17. bPOL48V using the FEASTMP inductor.



Technology survey and our choices

- Parallel powering with DC-DC converter VS Serial powering





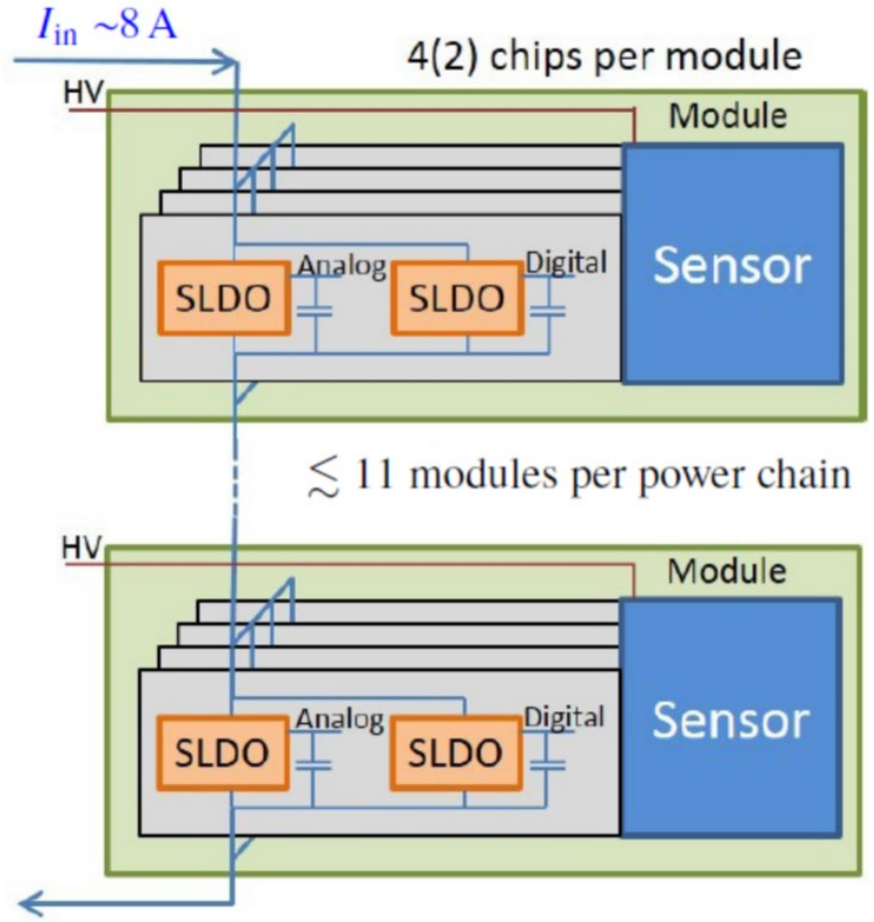
Parallel powering

- ✓ Compatible with the conventional power system
- ✓ Few changes of readout circuit or sensor required
- ✓ High reliability
- ✓ Unecessary on-chip regulator-> less die area
- ✗ Noisy ripple voltage
- ✗ Large-area air-core inductor
- ✗ EMI

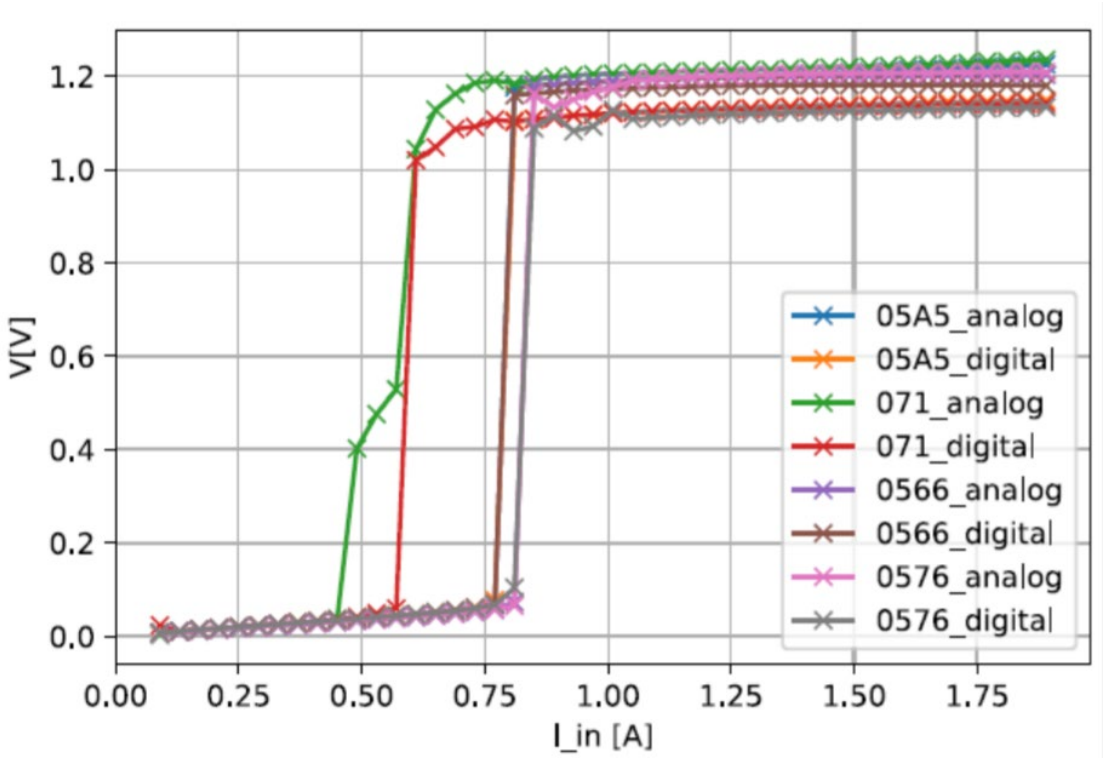
Serial powering

- ✓ Less cable mass
- ✓ Higher power efficiency, more suitable for large current load
- ✓ Low noise
- ✓ Unrequired Magnetic components
- ✗ Many changes with the old power system
- ✗ Lower reliablity
- ✗ Different groud potential -> AC-coupled output, no suitable for stiching chips, very high bias voltage of sensors
- ✗ “Larger” threshold current required to switch on shunt regulator
- ✗ Consistency of shunt regulator and LDO

Backup------Serial powering



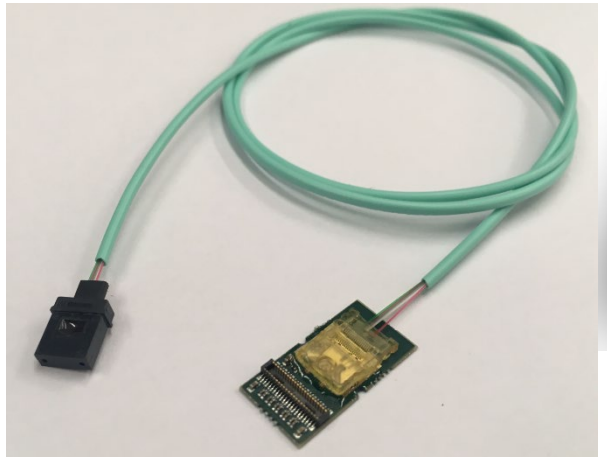
Structure of serial powering for CMS pixel detector

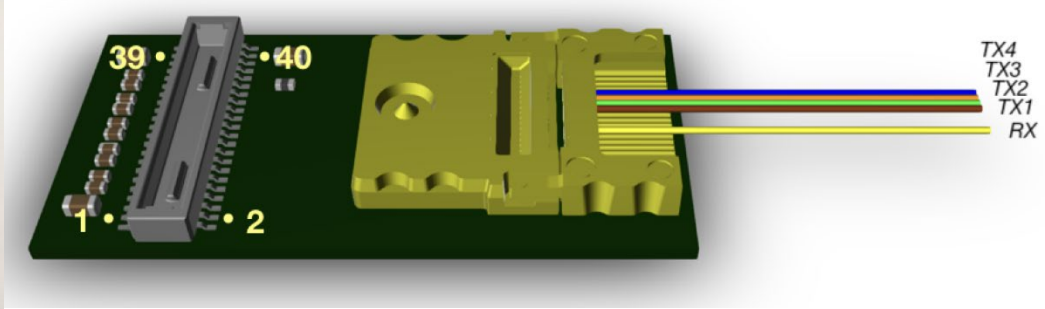


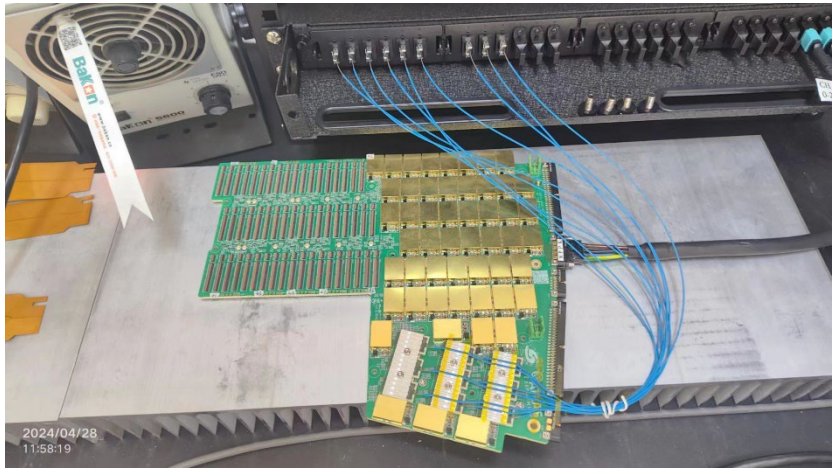
Regulated voltage for four single chips with different switching on current

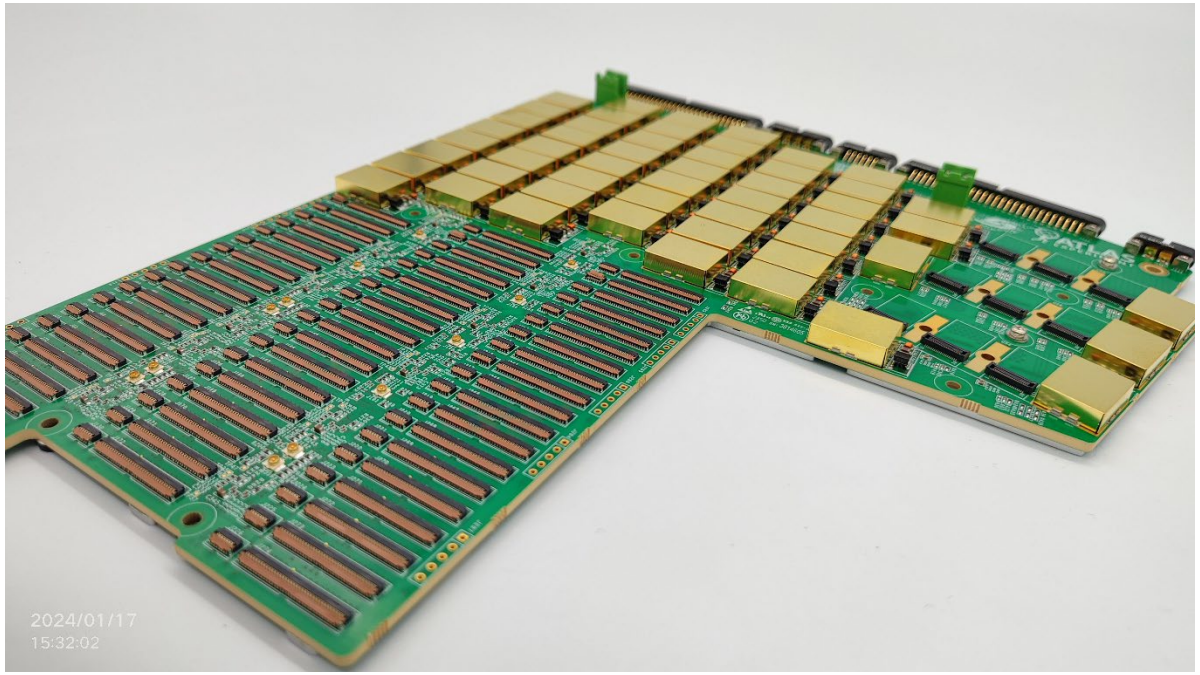
[Vasilije Perovic, Serial powering in four-chip prototype RD53A modules for Phase 2 upgrade of the CMS pixel detector, NIMA, Volume 978,2020,164436,]

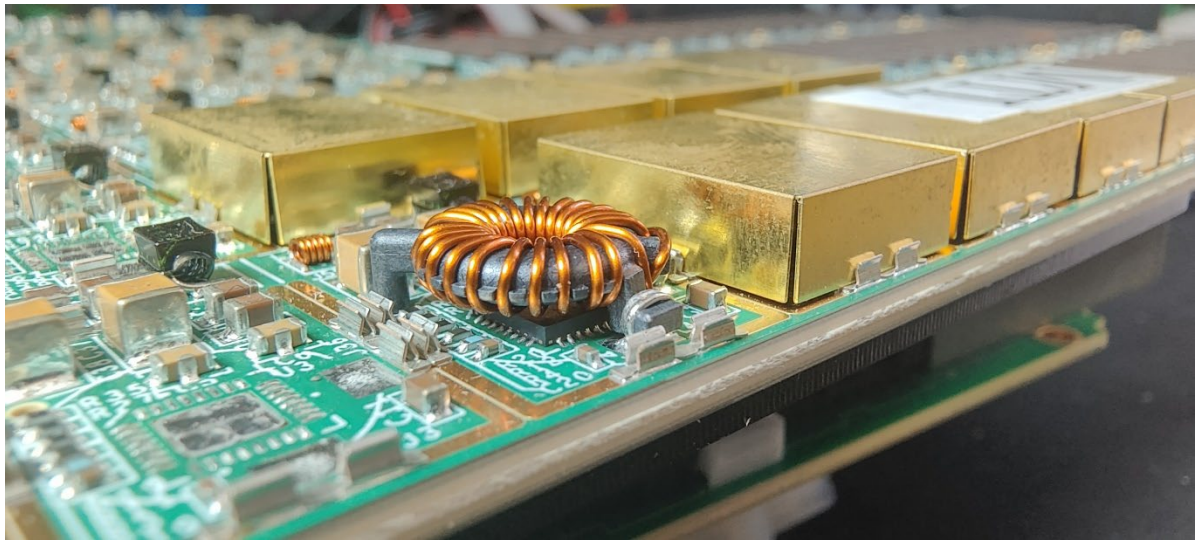
Size of bPol & GBT



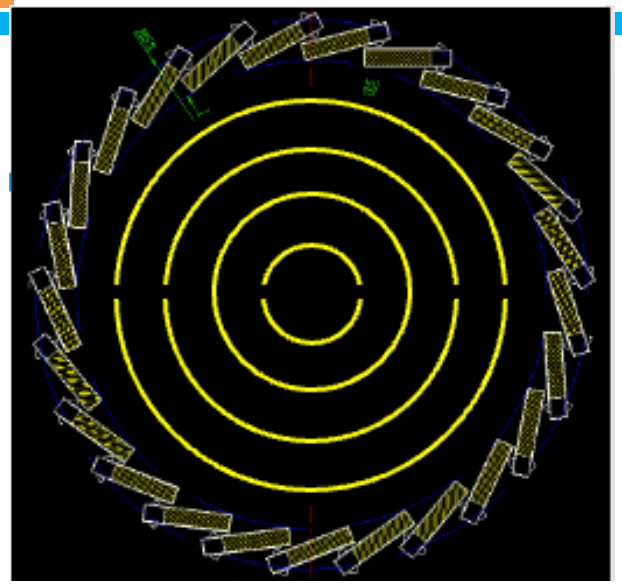


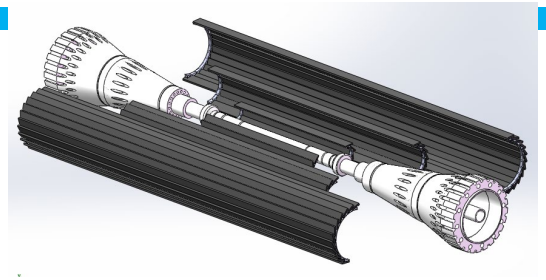


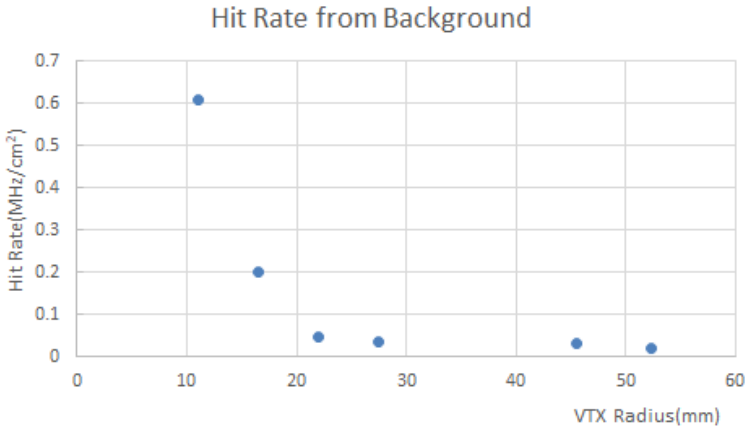




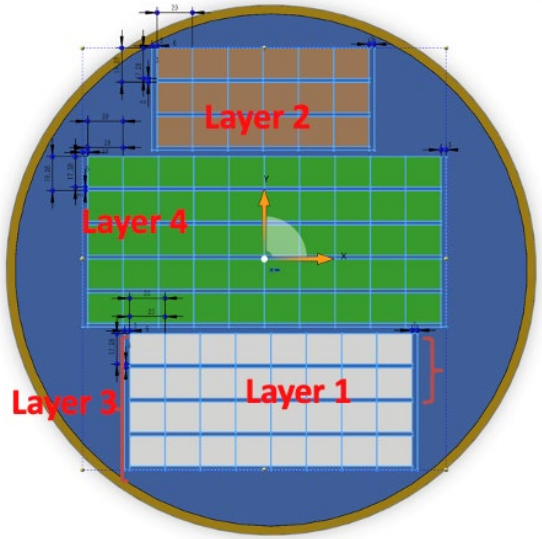
VTX-Data Link







- VTX scheme: Inner 4 layers stitching, with 1 typical double-sided ladder (layer 5&6)
- Bkgrd rate @50MW @Higgs with safety factor 1.5
- Assume RSU@stitching = ladder chip = 1024*512 matrix, then data rate for the innermost layer for a "chip" is 2Gbps, other layers according the bkgrd ratio
- Inner 2 layers needs 2 fiber chns for each row, due to the high data rate
  - possible to merge into less optical MTX interfaces
- In total 88 fibers = 6 BEE Brd = 1 Data Crate



From Zhijun

Layer	Comment	Data Rate/chip	Chips/Row	Data rate/row	Rows	Links@10Gbps
1	Stitching	2Gbps	8	16G	2*2=4	2*4=8（2 fiber chns）
2	Stitching	1.3Gbps	12	15.6G	3*2=6	2*6=12（2 fiber chns）
3	Stitching	0.27Gbps	16	4.3G	4*2=8	1*8=8
4	Stitching	0.25Gbps	20	5G	5*2=10	1*10=10
5	Ladder-side0	0.16Gbps	29	4.64G	25	1*25=25
6	Ladder-side1	0.16Gbps	29	4.64G	25	1*25=25

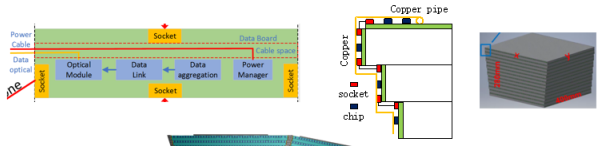
VTX-Power

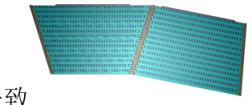
Layer	Comment	Power/chip	Chips/Row	Power /row	Rows	Chip Power of Layers	Total Power/Layer (Chip+Link) *1.18
1	Stitching	200mW	8	1.6W	2*2=4	6.4W	(6.4+4) *1.18=12.2
2	Stitching	200mW	12	2.4W	3*2=6	14.4W	(14.4+6) *1.18=24
3	Stitching	200mW	16	3.2W	4*2=8	25.6W	(25.6+8) *1.18=39.5
4	Stitching	200mW	20	4W	5*2=10	40W	(40+10) *1.18=58.8
5	Ladder-side0	200mW	29	5.8W	25	145W	(145+25) *1.18=200
6	Ladder-side1	200mW	29	5.8W	25	145W	(145+25) *1.18=200

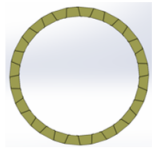
- For simplicity, assume the power of Unit(RSU/Chip) is the same 200mW(40mW/cm2 * 2.6cm*1.6cm)
  - Main contribution of power: analog static power + data link, not varying with bkgrd rate
- Extra cost by using optical: fixed 1W each set
  - 0.75W for Data Interface & 0.25W for 1 Rx+4Tx VTRx
- Efficiency of BaSha DC-DC is 85% = extra efficiency cost of DC-DC 18% (1÷85%=118%)
- Total power: 449.8W
  - 16 power channels each layer for 1~4, each chn for a semi-; 2 chn for each ladder in 5/6 layer, 50 chn in all
  - Power will be provided from both ends for long barrel
  - 66 power channels = 2 power crate
    - Very likely to be merged due to the limited room for VTX

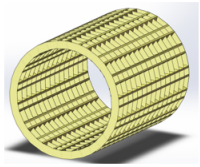
ECAL – Data Link(skip)

ECAL电缆估算



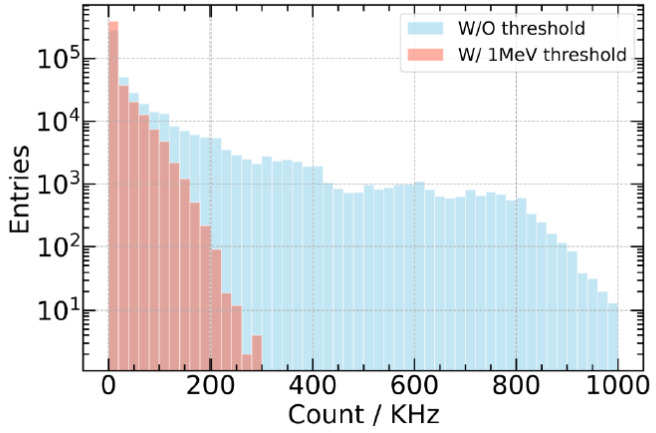






层数	反梯形	正梯形
2	27	39
4	29	37
6	29	37
8	31	37
10	31	37
12	33	37
14	35	35
16	35	35
18	37	35
20	37	35
22	39	33
24	41	33
26	41	33
28	43	33

- ECAL桶部，正反梯形排布
  - 模块数量：Phi：32，Z：15，共480个模块
- 每个模块：
  - 1层到28层，奇数层每层36根，偶数层晶体数目不一致
  - 正梯形晶体数量1000，反梯形晶体数量992
- 电缆估算：1根/模块
  - AWG15（线径1.45mm，电流：6.5A/7.4A）
  - AWG18（线径1.08mm，电流：3.2A/3.7A）
  - 模块功耗估计：1000*2*20mW = 40W
- 光纤估算：1根/模块
  - 模块数据量估算：待定
- 桶部电缆总计
  - 类型：高压，低压（正负？），光纤
  - 电缆双向走向，每端240根（平均方案）
  - 电缆双向走向，一端224根，一端256根
- 未确定电缆：刻度方案

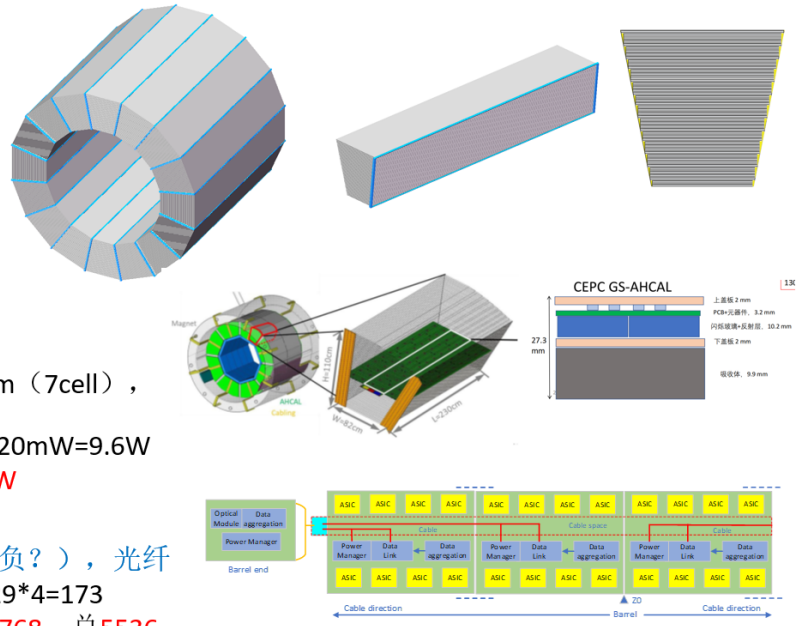


- The overall detector design: ~480 Module (Dual-trapezium scheme), ~1000 bar/module
- Current bkgrd estimation: avg. event rate 100kHz / crystal bar w/ threshold; Data width 48bit/event (current ASIC scheme)
- @Dual readout each crystal bar, total data rate: 1000*100kHz*48bit*2ends=9.6Gbps, not possible for 1 fiber for each module, at least 2 fibers for each module
  - For max. bkgrd rate@300kHz@Higgs, also needs enough room
  - For Z pole, bkgrd will be much higher, also needs extra room

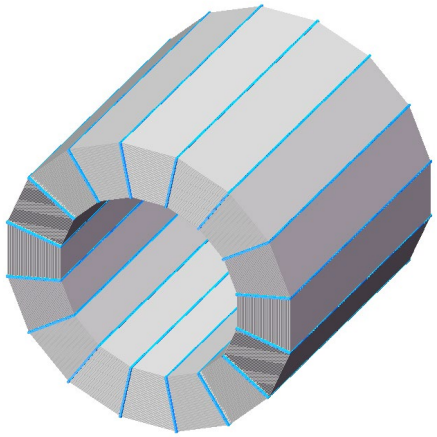
HCAL-Data Link(barrel)

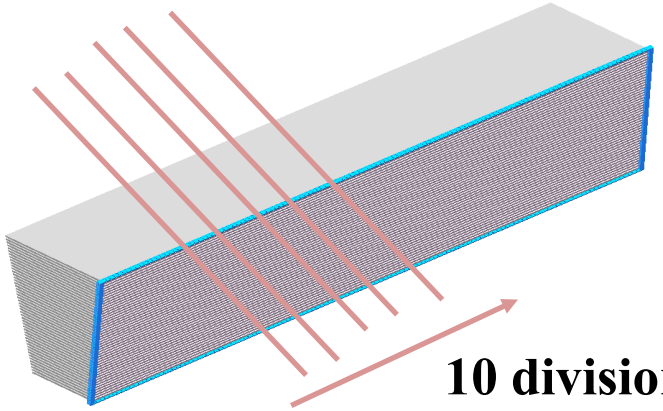
HCAL电缆估算

- HCAL桶部排布
  - 总通道数：338万
  - 分区：16
  - 层数：48
  - Cell尺寸：4*4cm
- 电子学板尺寸
  - Z向：60cm（15cell）
  - Phi向：24cm（6cell），28cm（7cell），32cm（8cell）
  - FEE单板最大功耗：15*8*4*20mW=9.6W
  - 汇总板最大功耗：9.6*5=48W
- 桶部电缆数量
  - 电缆类型：高压，低压（正负？），光纤
  - 1/16 分区电缆数量：19*3+29*4=173
  - 总电缆数量：一端173*16=2768，总5536
  - AWG12（线径2.05mm，电流：13.1A/14.9A）

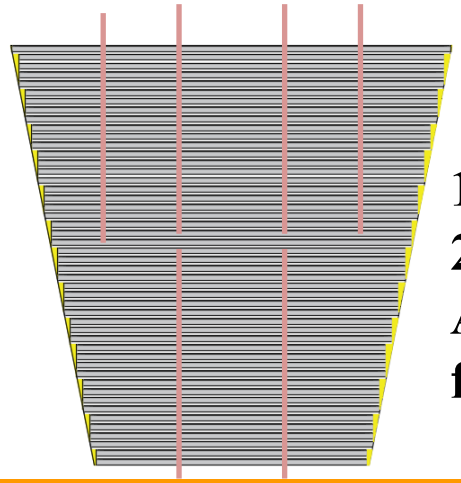


- Currently, HCAL is not finalized, especially for the module design, e.g. cell size and channel number
- Data have to be aggregated at the end of barrel for each layer, also the DC-DC
- By rough estimation, the bkgrd will be low（5kHz/GS），the aggregated data rate for each layer board should not exceed 8Gbps (10Gbps for the fiber)
  - Then 1 fiber for each aggregation board is reasonable
- Fibers：
  - Aggr. board number every 1/16 sector：19*3+29*4=173
  - 1 fiber per aggregation board: 173*16*2=5536 fibers
  - =346 BEE = 36 Data Crates





10 divisions



1~19layer 3PCBs width
20~48layer 4PCBs width
Aggr Brd for 5 PCBs along z from both ends, with 1 fiber