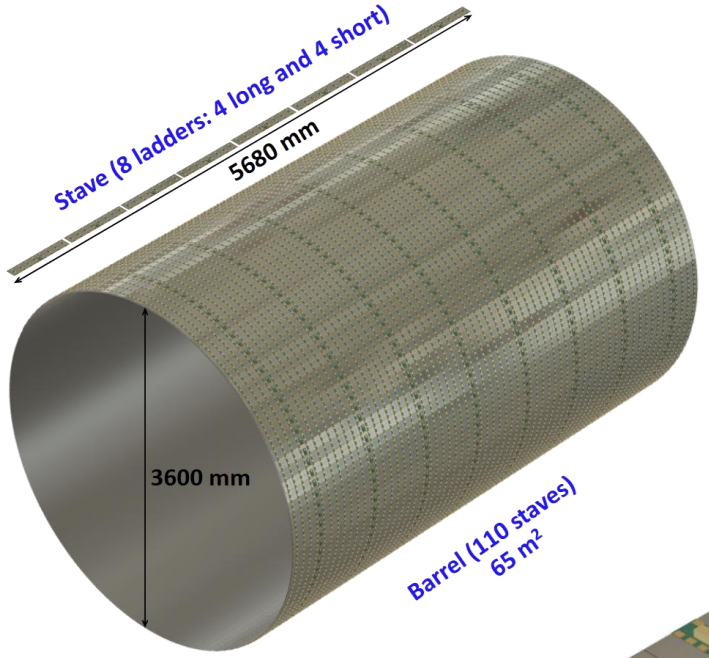
OTK front-end electronic & Readout Chip

Outline

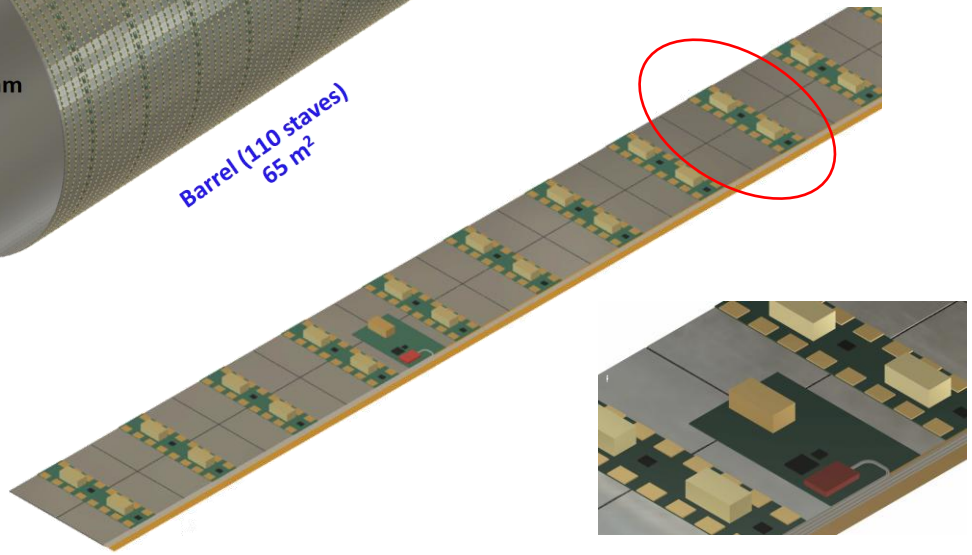
1.OTK前端电子学系统方案

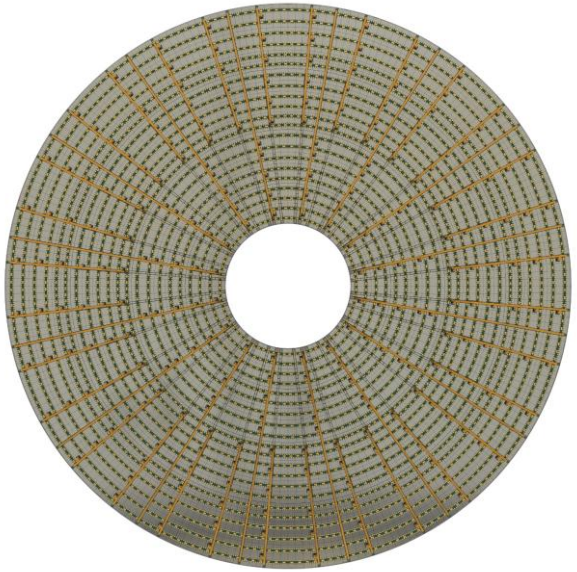
2.OTK前端读出芯片方案

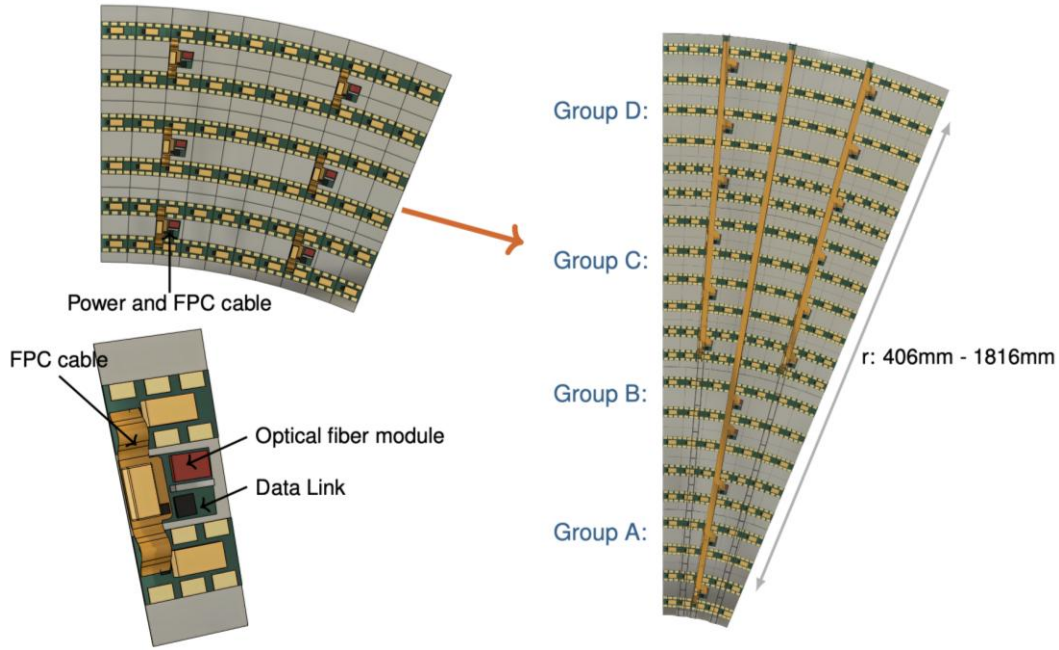
CEPC OutTracker



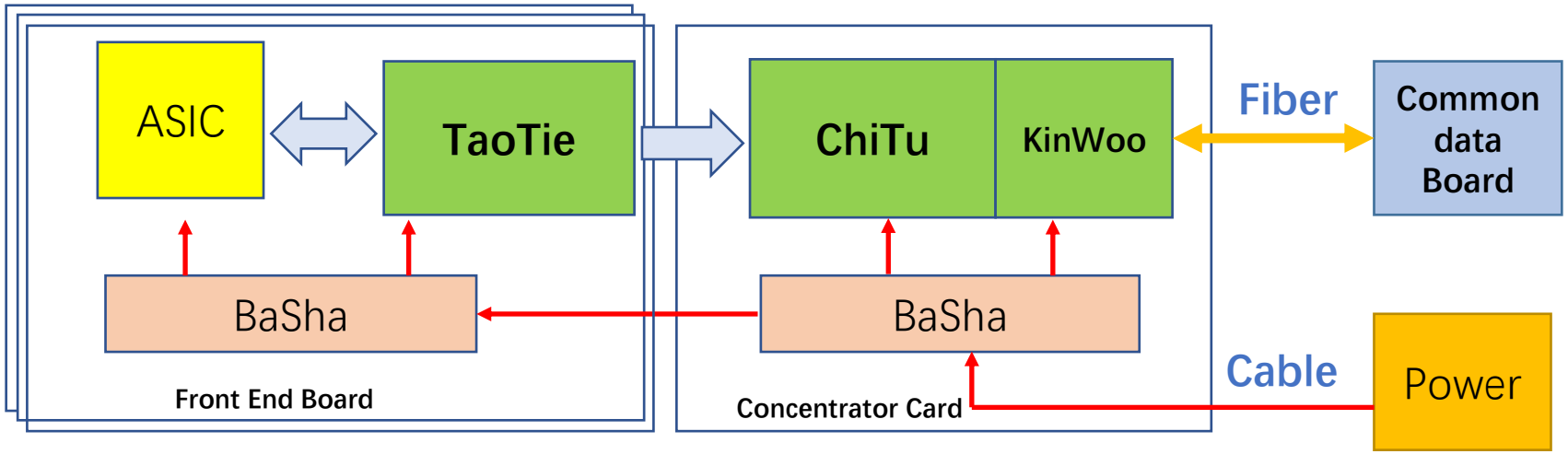
- 16ASIC/module
- 128ch /ASIC
- LGAD pitch 100um





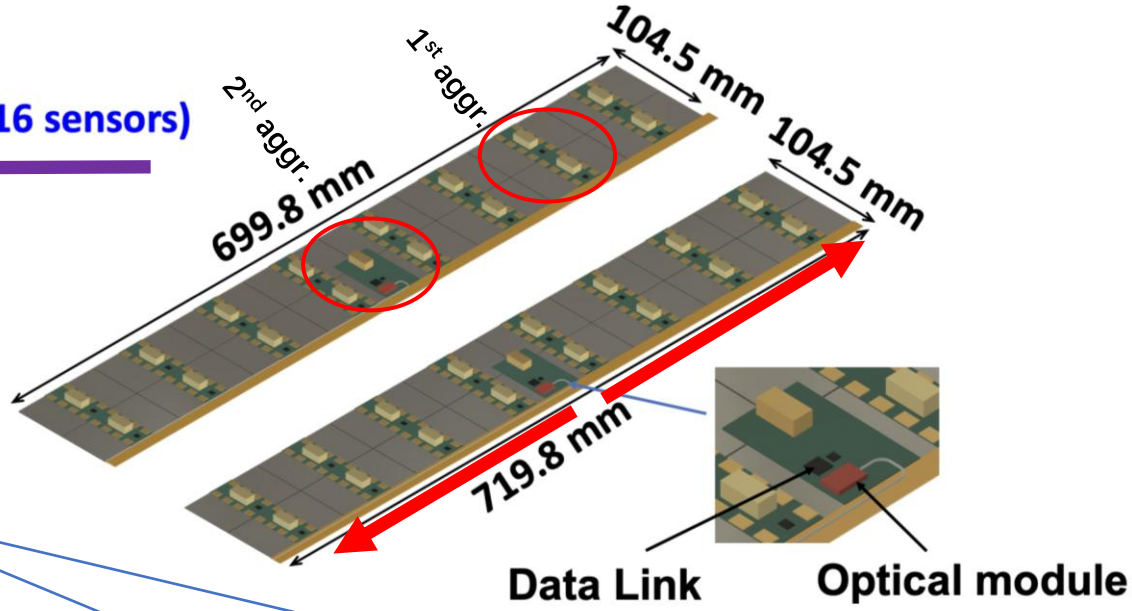


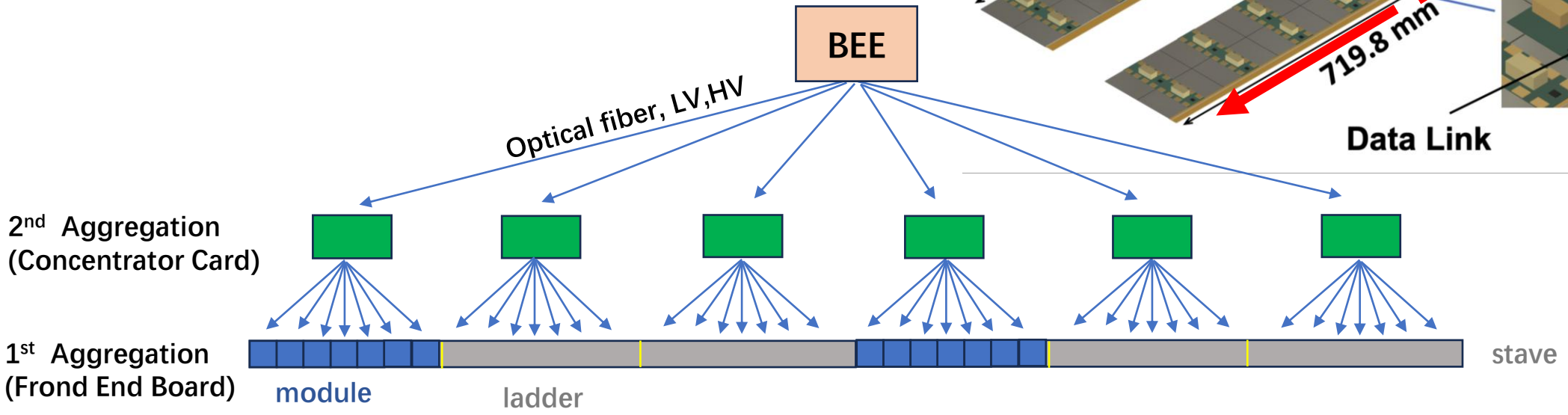
OTK readout electronics



- 主要考虑探测器近端ASIC的供电方案和数据汇总方案
  - 电源采用层级降压，减少器件数量
  - 为提高传输效率，数据采用分级汇总，光纤输出
  - 光纤以后的电子学属于通用系统电子学

前端电子学整体层级架构 16 sensors)





- 电源和数据均采用二级架构
  - 第一级：产生1.2V电压，针对module前端芯片数据初步汇总、传输
  - 第二级：产生12V电压，为module提供时钟和慢控，针对Ladder数据汇总、传输

Data transmission for OTK

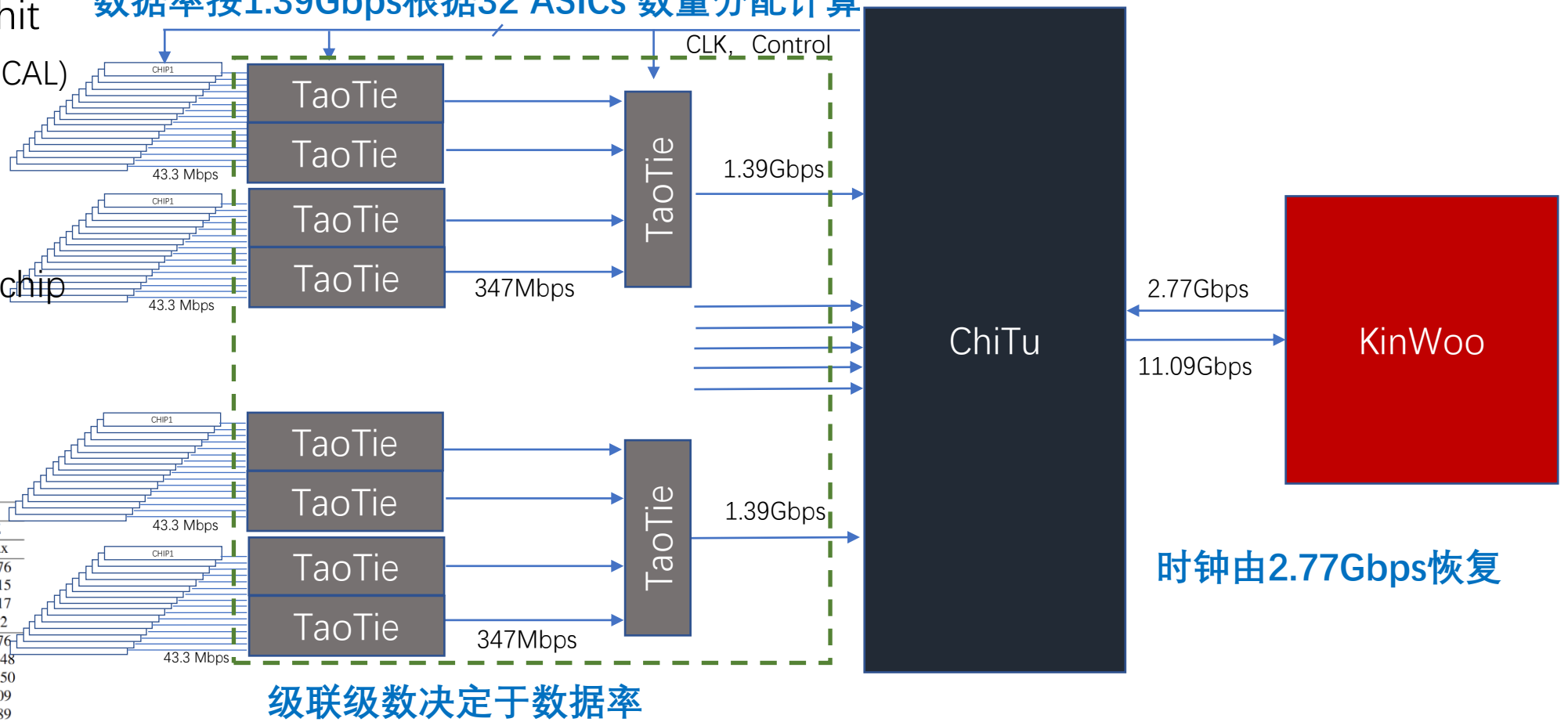
- Data rate： 48 bit/ hit

28 bit (10TOA, 8 TOT， 10CAL)
+ channel(7bit, 128)
+bunch ID(8bit)
+ chip ID (5 bit)

- Max Hit rate：
  - Endcap: 1.34 KHz/chip

最大数据率6.5 Mbps

数据率按1.39Gbps根据32 ASICs 数量分配计算



时钟由2.77Gbps恢复

级联级数决定于数据率

Estimated Silicon Tracker Hit Rates [10^3 Hz/cm^2]

	Low Lumi Z		Higgs		High Lumi Z	
	Average	Max	Average	Max	Average	Max
ITKB1	3.11	4.70	0.60	0.91	24.16	34.76
ITKB2	1.85	4.21	0.44	1.11	13.04	21.15
ITKB3	0.95	1.94	0.27	0.50	5.98	10.17
OTKB	0.62	0.92	0.23	0.35	3.30	4.82
ITKE1	11.20	50.96	2.72	12.08	98.64	34.76
ITKE2	7.01	41.59	1.89	9.65	50.30	326.48
ITKE3	3.13	28.93	0.92	7.53	17.57	130.50
ITKE4	2.23	10.03	0.69	2.52	13.03	59.09
OTKE	0.98	4.00	0.37	1.45	5.45	23.89

Table 5.19: Estimated Silicon Tracker Hit Rates (data:250118)

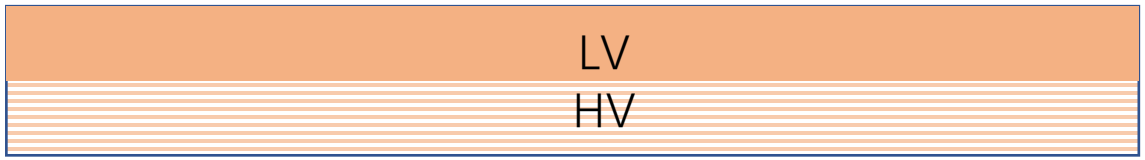
- TaoTie （可降频）
  - Input: 8 uplinks, 1 clk
  - Output: 1 uplink

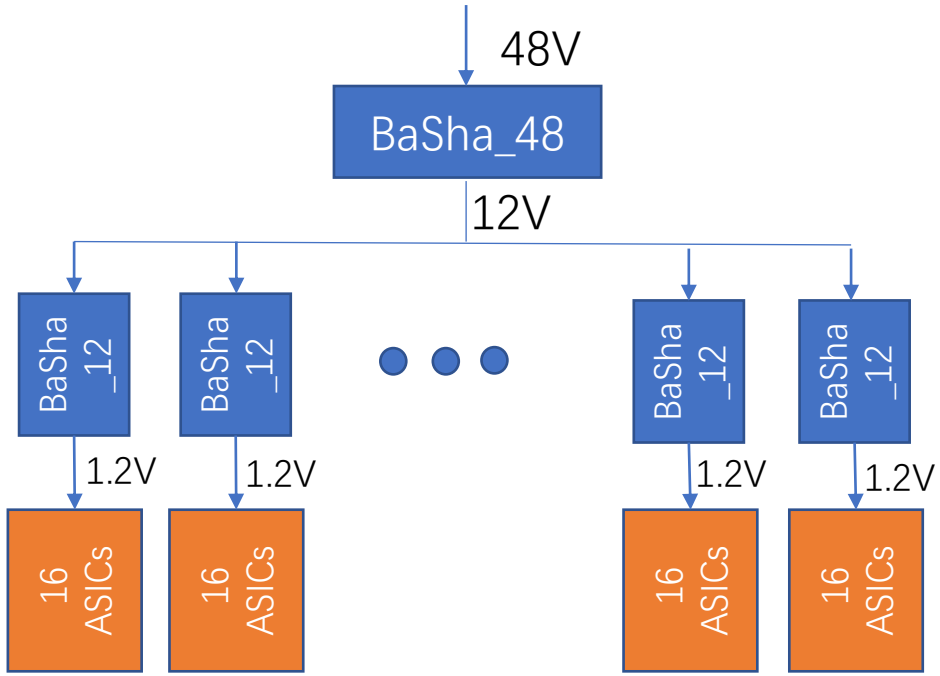
- ChiTu
  - input： 7 uplinks （1.39Gbps）
  - Output： 16 downlinks， 16 clks

OTK Power Supply

- HV：直接由机箱供电
- LV：机箱供电48V
  - Basha_48: 48V->12V（10A）
  - Basha_12: 12V-1.2V（10A）/3.3V

- LV供电
  - Flex线阻计算：
    $R \approx 0.05\Omega/m$（h=35um, w=10mm copper）
  - 每个Module的供电电流2.5A（30W）
    2.5A电流的压约0.25V/m，线损0.7W/m
  - 每个Ladder的供电电流5A,（240W）
    5A电流的压约0.5V/m，线损2.5W/m,
    最长2.9m的线损7.5W(3%)

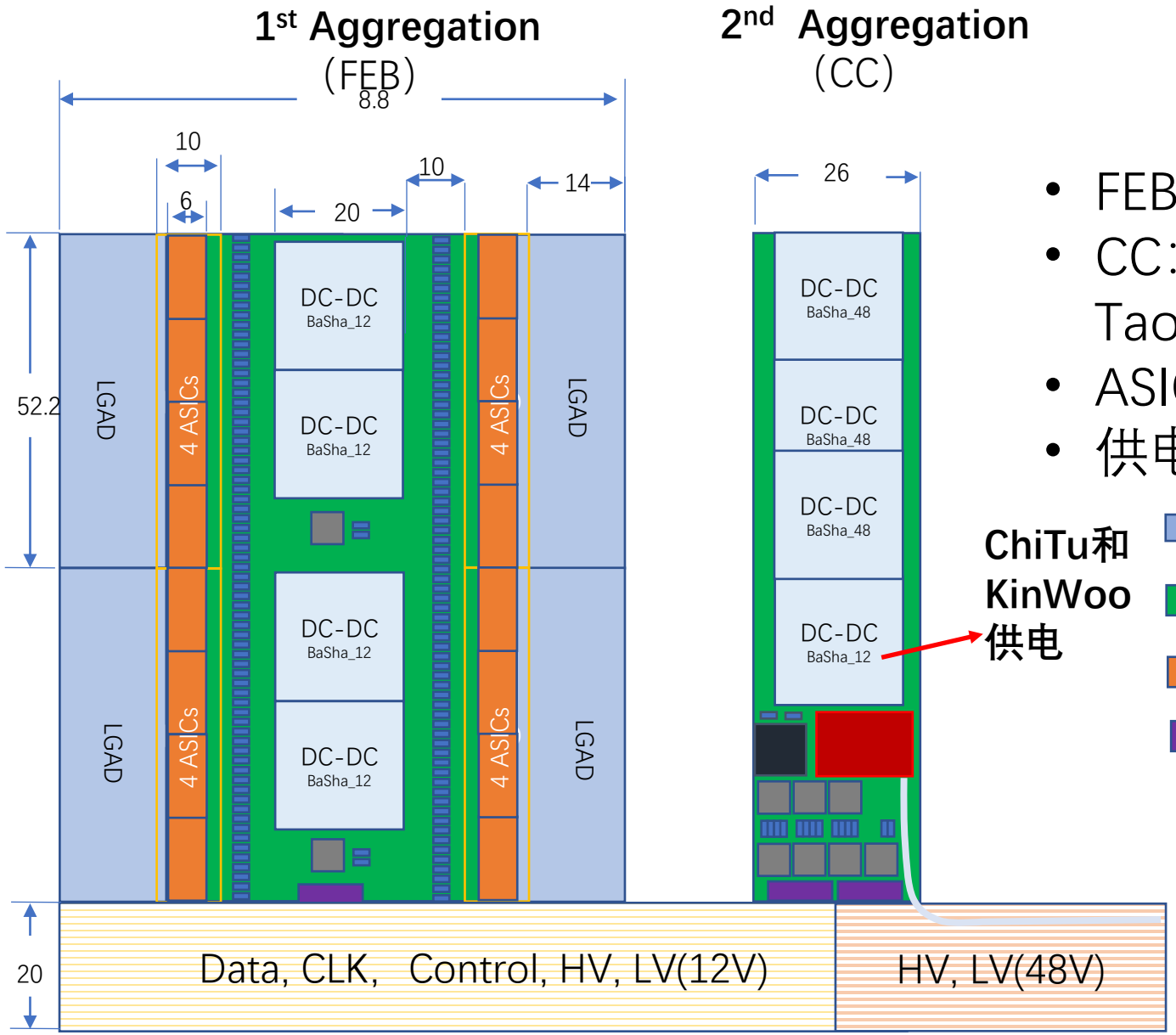




	输出功率
BaSha_12	12W
BaSha_48	120W

	按单位功率 20mW/ch	按单位功率 300mW/cm2
1 ASIC（128 chs）	2.56W	1.7W
1 Module（16 chips）	40.96W	27.4W
1 ladder (8 modules)	328W	219W

OTK Front End Board



- FEB：的芯片供电均为1.2V
- CC：BaSha_12可提供1.2V给ChiTu和TaoTie，提供3.3V给KinWoo
- ASIC需要电源滤波电容和电阻
- 供电总线只能用 2-layer Flex PCB

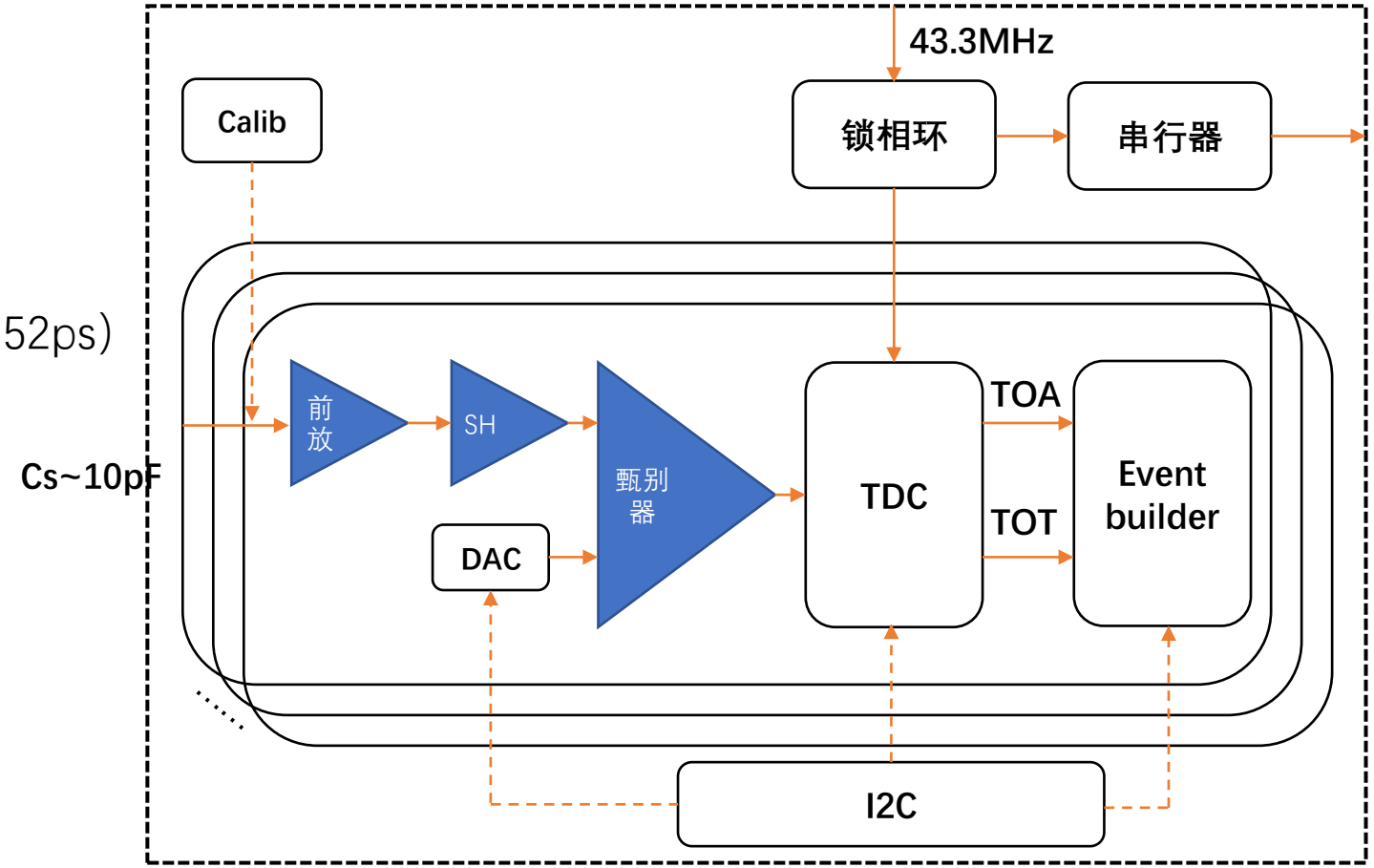
ChiTu和KinWoo供电

LGAD
PCB or Flex
JuLoong(12. 5x6)
Connecter(10x3)
Res & Cap(1x2.5)
TaoTie (5x5)
ChiTu(8x8)
KinWoo(15x10)
DC-DC(20x20)
2-layer Flex PCB
Multi-layer layer Flex PCB
Wire Bonding area

前端读出芯片（JuLoong）设计指标及架构

OTK系统：时间分辨<50ps, 位置分辨<10um
LGAD：时间分辨40ps，pitch 100um

- 工艺：SMIC55
- 通道数：128
- 时间测量精度：30ps
  - TDC TOA测量——15ps（LSB=$15*\sqrt{12}$=52ps）
  - 前放——25ps
  - 时钟——5ps
- 时间测量范围：0.5ns~23.3ns
- 功耗：<20 mW/channel
- 单通道高度：<100u
- LGAD电容：10pF



是否还需要锁相环？jitter cleaner是否就足够？

前端放大甄别

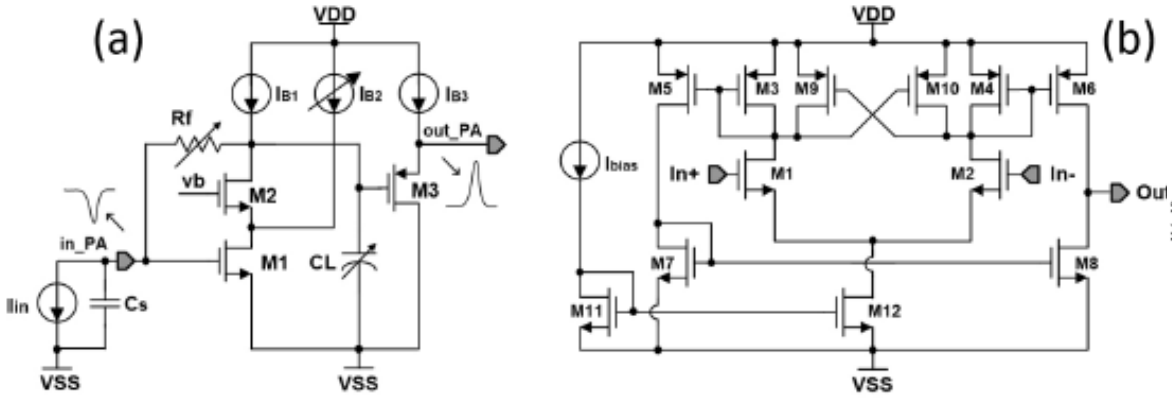
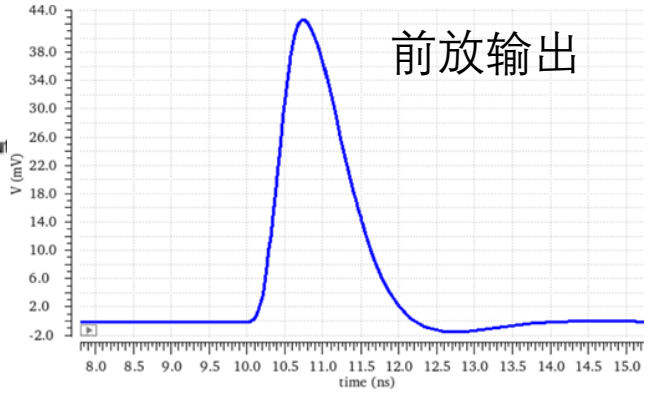
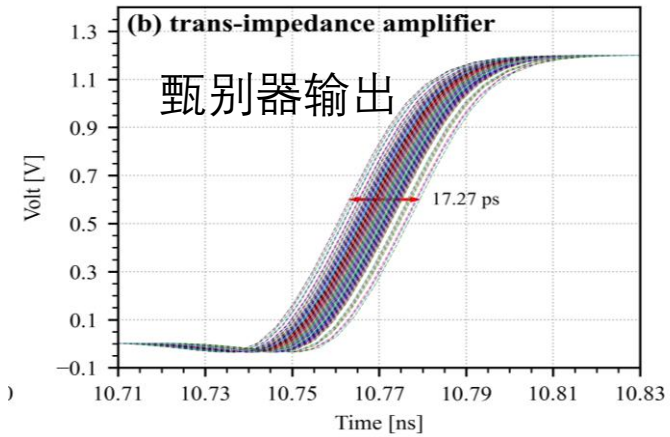


Figure 2. Schematic of the preamplifier (a) and the comparator (b).

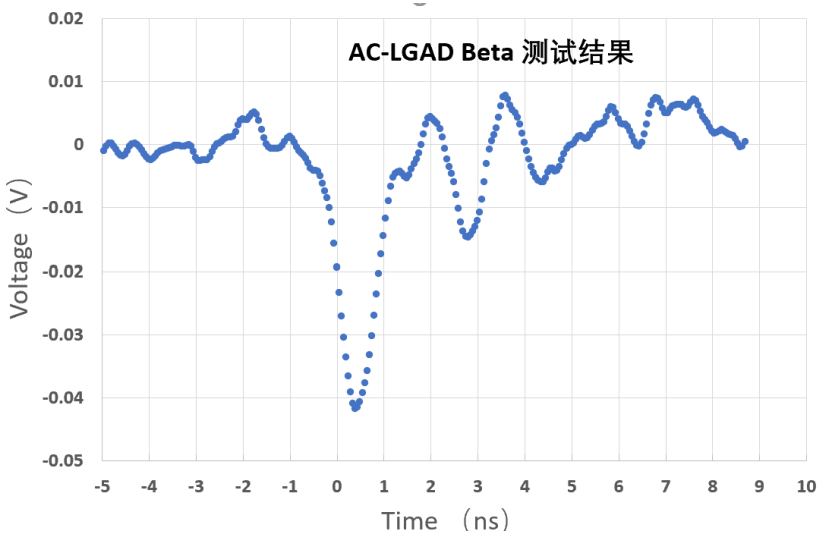




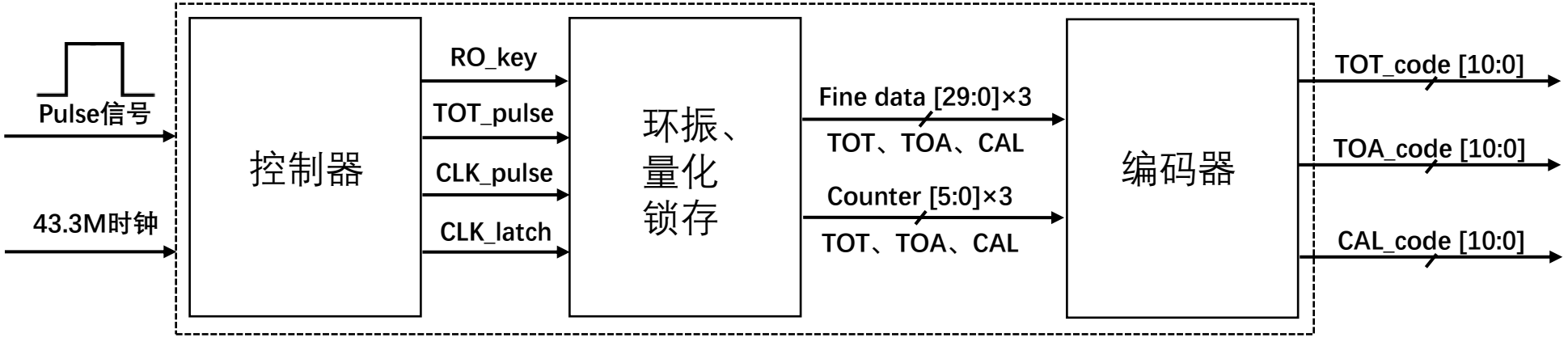
Transient noise simulation for output of preamplifier@8pF 16fC

LGAD 信号前沿~300ps

-jitter <15ps
-BW~1.2GHz
-Gain： 67.5dBΩ
- Input impedance： ~50Ω （LGAD实际传输线阻抗待测）
- Power Consumption：8mW

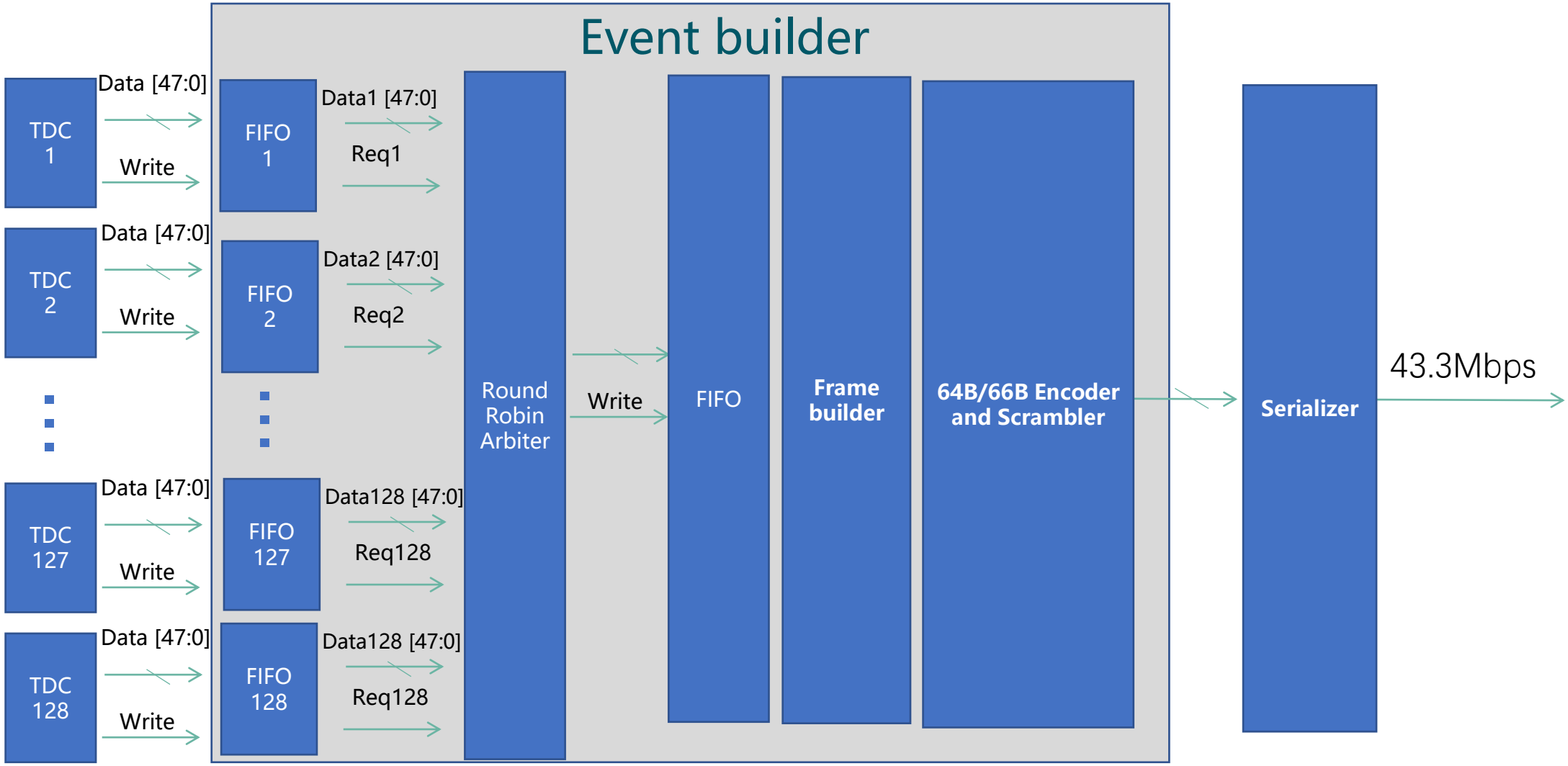


单通道TDC

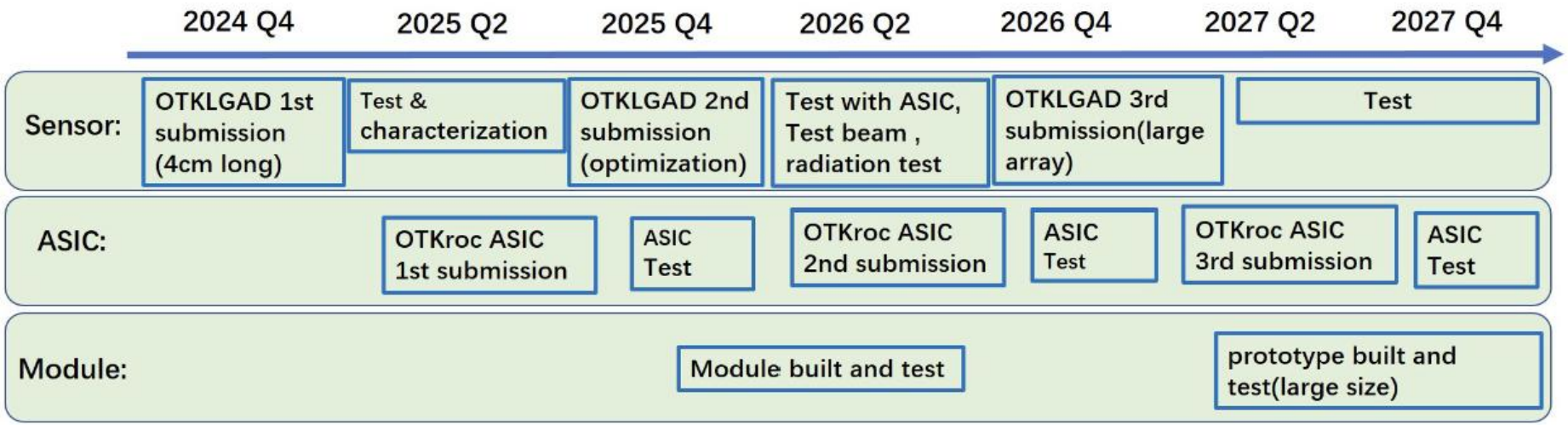


- TDC部分由数字控制模块、环振及量化锁存模块、编码器三部分组成，实现TOA测量、TOT测量；每个事例TOT，TOA测量完成后，额外测量一次参考时钟的周期（CAL测量），实现标定功能；
- 数字控制模块接收信号及43.3M参考时钟，产生环振启停信号、TOT和TOA量化锁存信号、CAL锁存信号；
- 环振量化锁存模块中，TOT、TOA、CAL均被量化为30位细计数温度码+6位粗计数二进制码；
- 编码器将温度码转为二进制码。

Event Builder



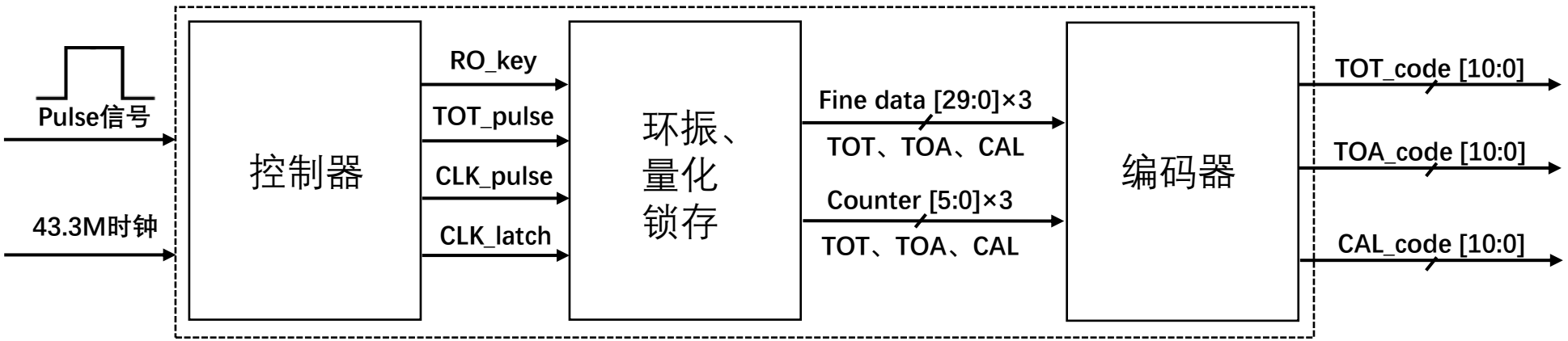
后续计划



2025 Q1， preamplifier, discriminator, and TDC modules模块验证
2025 Q2，Q3，测试系统设计和芯片功能测试，数字部分FPGA验证
2026 Q1, 模块改进，增加数字部分电路，多通道集成
2026 Q2，Q3,多通道芯片测试系统设计和芯片测试.
2026 Q4 , 多通道芯片改进, LGAD读出系统设计
2027 Q2, 芯片测试及LGAD联调测试.
2027 Q4, 工程批预生产准备

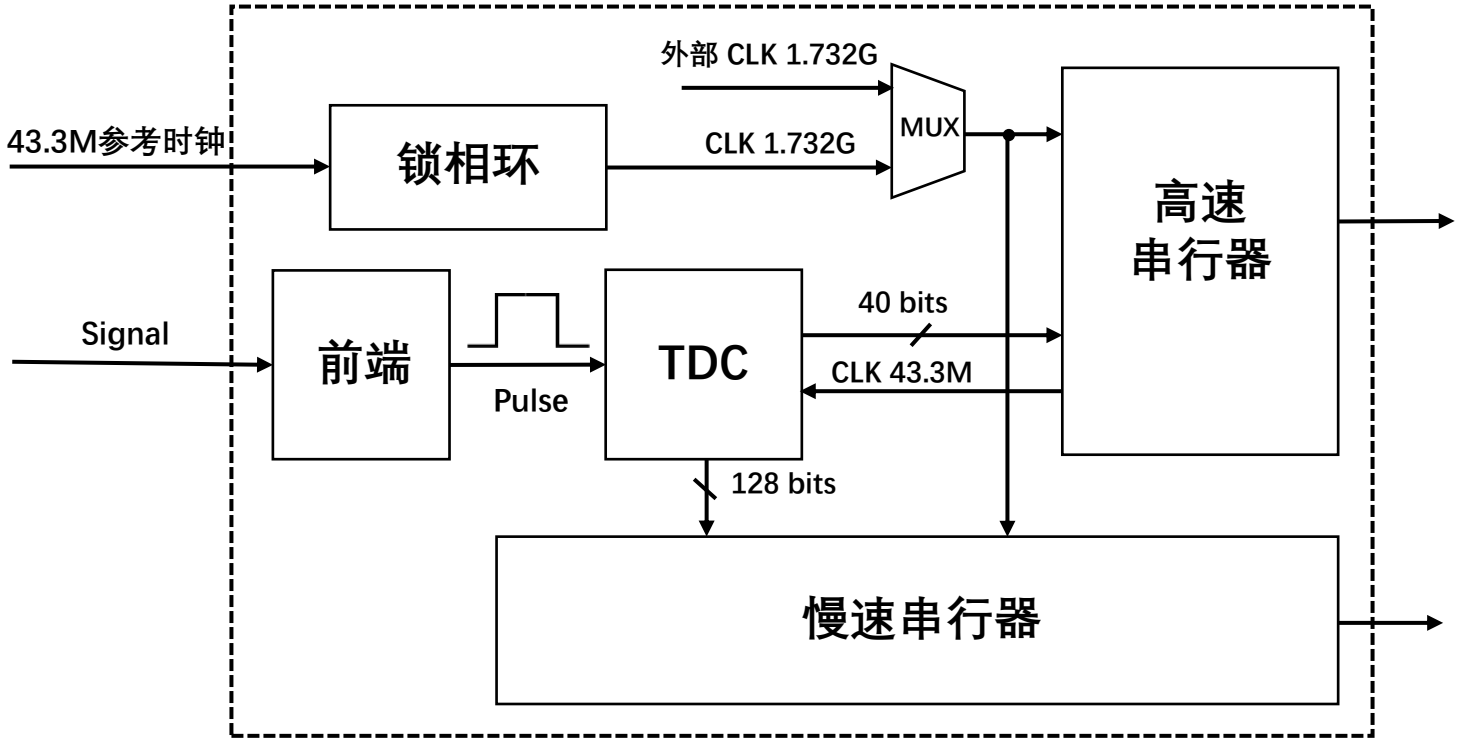
4月份流片模块
TDC核心功能验证芯片

王传烨



核心功能验证芯片架构

- 用于四月流片，验证核心结构功能；
- 包括前端、锁相环、TDC、高速串行器、低速串行器五个主要部分；
- 外部提供43.3M参考时钟，锁相环产生1.732G时钟，与外部1.732G时钟选通后给串行器；
- TDC模块输出40位编码后的数据和128位未编码的原始数据（包括若干位header），参考时钟由高速串行器提供；
- 两组串行器，分辨用于串行输出编码后的40-bit数据和编码前的128-bit数据。



■ 环振及量化锁存模块

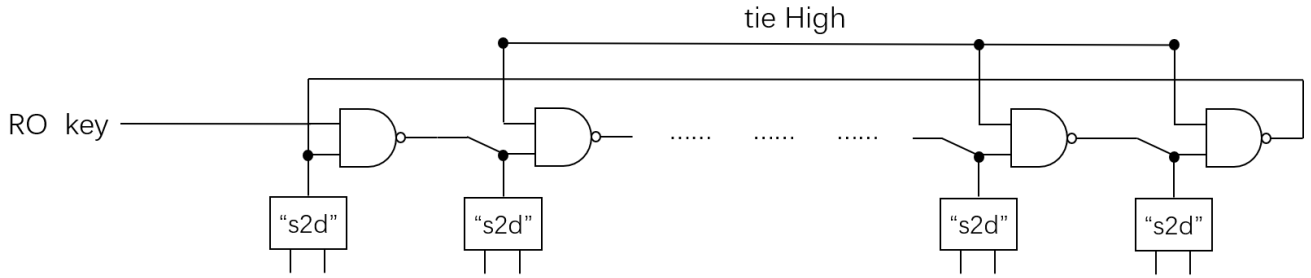
➢ 事例驱动型环振

- 使能信号RO_key为0时，延迟链各与非门输出端状态为：

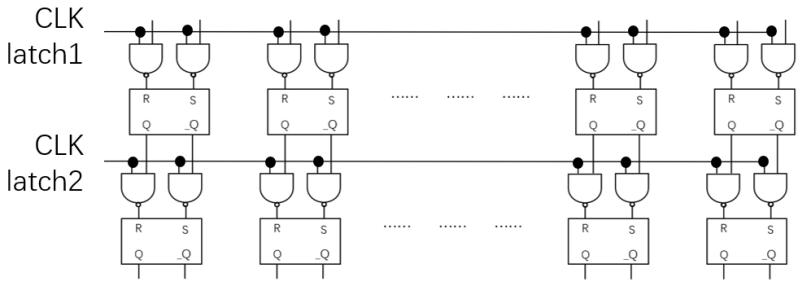
  101010101010101

- 使能信号RO_key置1时，环振按以下规律开始震荡：

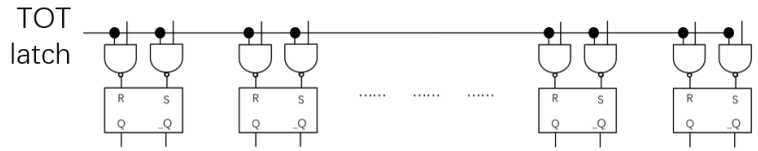
  101010101010101
  001010101010101
  011010101010101
  ……
  010101010101010
  110101010101010
  ……
  101010101010101



15-stage NAND delay chain + s2d block, 30 bit fine phase output



TOA and CAL fine count latch

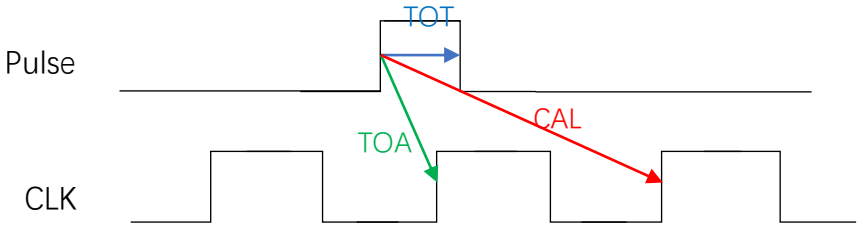


TOT fine count latch

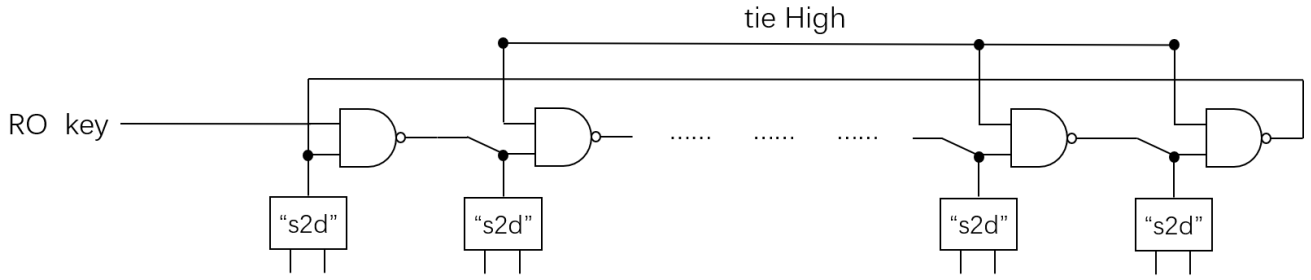
单通道延迟链及量化模块框图

■ 环振及量化锁存模块

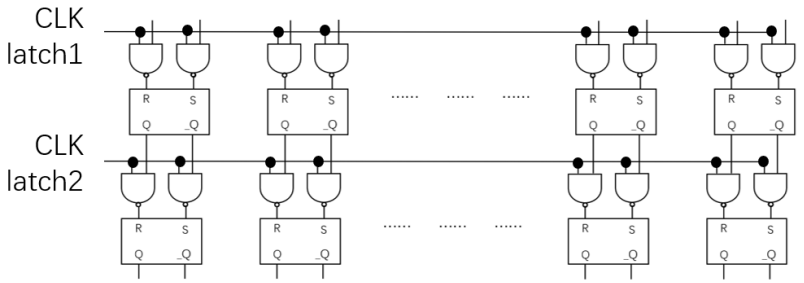
- SR锁存结构
- 15*3组SR锁存器，实现TOA、TOT、CAL量化和锁存功能
- SR锁存器为电平锁存，高电平时输出随输入变化，低电平时输出锁定，因此CLK_latch1, CLK_latch2, TOT_latch信号均为有一定宽度（>300ps）的pulse型信号。



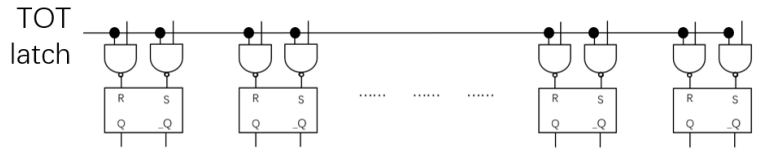
TOA、TOT、CAL示意图



15-stage NAND delay chain + s2d block, 30 bit fine phase output



TOA and CAL fine count latch



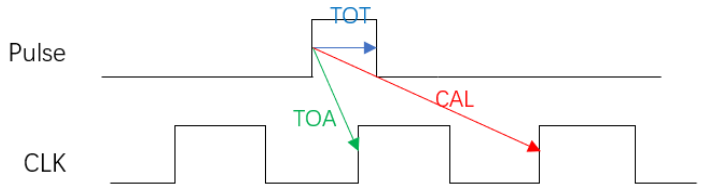
TOT fine count latch

单通道延迟链及量化模块框图

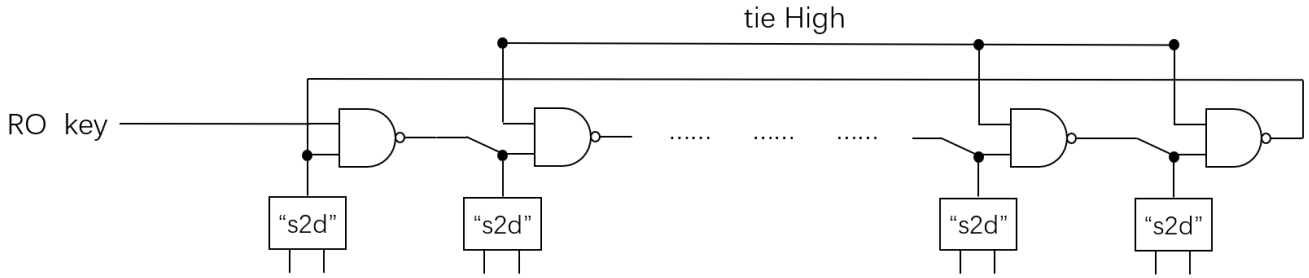
■ 环振及量化锁存模块

➢ 量化锁存逻辑

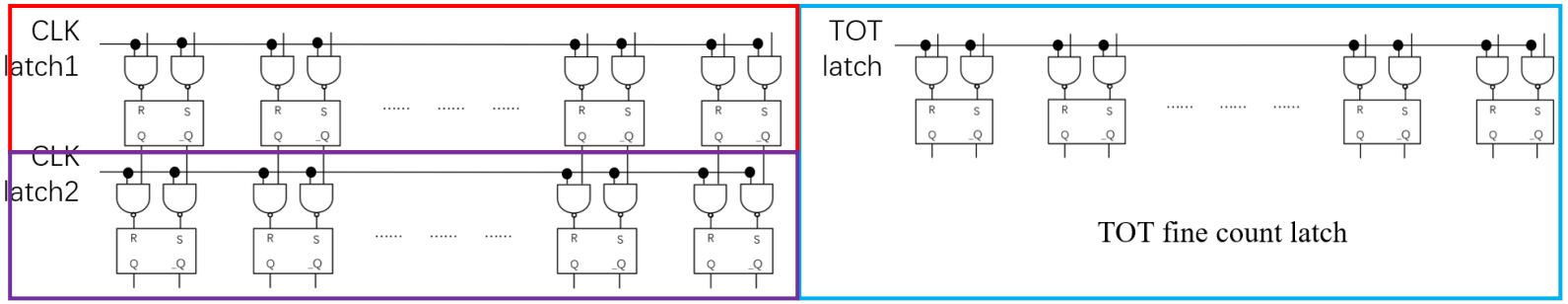
1. 待测Pulse信号上升沿到来时，RO_key置1，环振从101……101状态开始起振，内部门控参考时钟开启。
2. 待测Pulse信号下降沿到来时，生成TOT_latch信号（宽度300ps的pulse型信号），使TOT锁存单元（蓝框内）跟随读取环振状态，300ps后锁存，实现TOT量化锁存。
3. 参考时钟第一个上升沿到来时，生成CLK _latch1信号的第一个pulse（宽300ps），使红框中的锁存单元跟随读取环振状态，300ps后锁存，量化锁存TOA。如未能生成有效pulse（宽度≥300ps）则顺延至下一次参考时钟上升沿。
4. CLK _latch1有效pulse后的第一个参考时钟下降沿到来时，生成CLK_latch2的pulse信号（宽度约300ps），读取红框内锁存单元的输出值后锁存，此时TOA被复制到紫框锁存单元。



TOA、TOT、CAL示意图



15-stage NAND delay chain + s2d block, 30 bit fine phase output



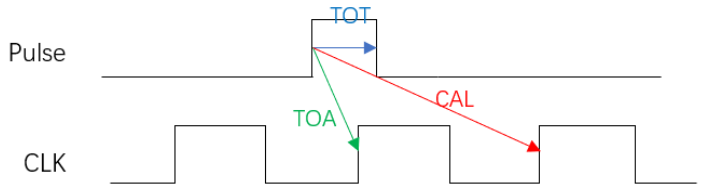
TOA and CAL fine count latch

单通道延迟链及量化模块框图

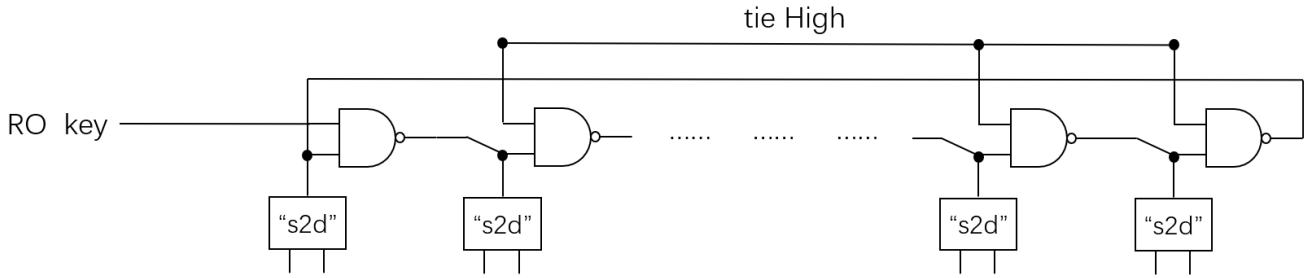
■ 环振及量化锁存模块

➢ 量化锁存逻辑

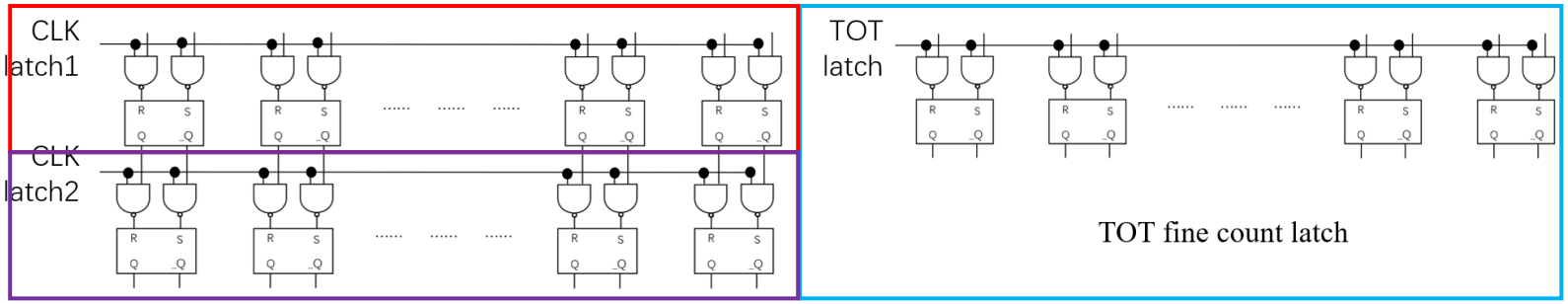
5. 参考时钟第二个上升沿到来时，生成CLK_latch1信号的第二个pulse（宽300ps），使红框中的锁存单元跟随读取环振状态，300ps后锁存，此次锁存为TOA+一个时钟周期后的环振状态，覆盖掉原来的TOA，记为CAL，CAL量化完成后内部参考时钟关闭。
6. TOT_latch出现一次有效pulse（宽度≥300ps），且CLK_latch1出现两次有效pulse （宽度≥300ps），则认为完成TOT、TOA、CAL测量，将RO_key置0，环振复位回101……101状态。
7. 此时蓝框内锁存TOT、紫框内锁存TOA、红框内锁存CAL。



TOA、TOT、CAL示意图



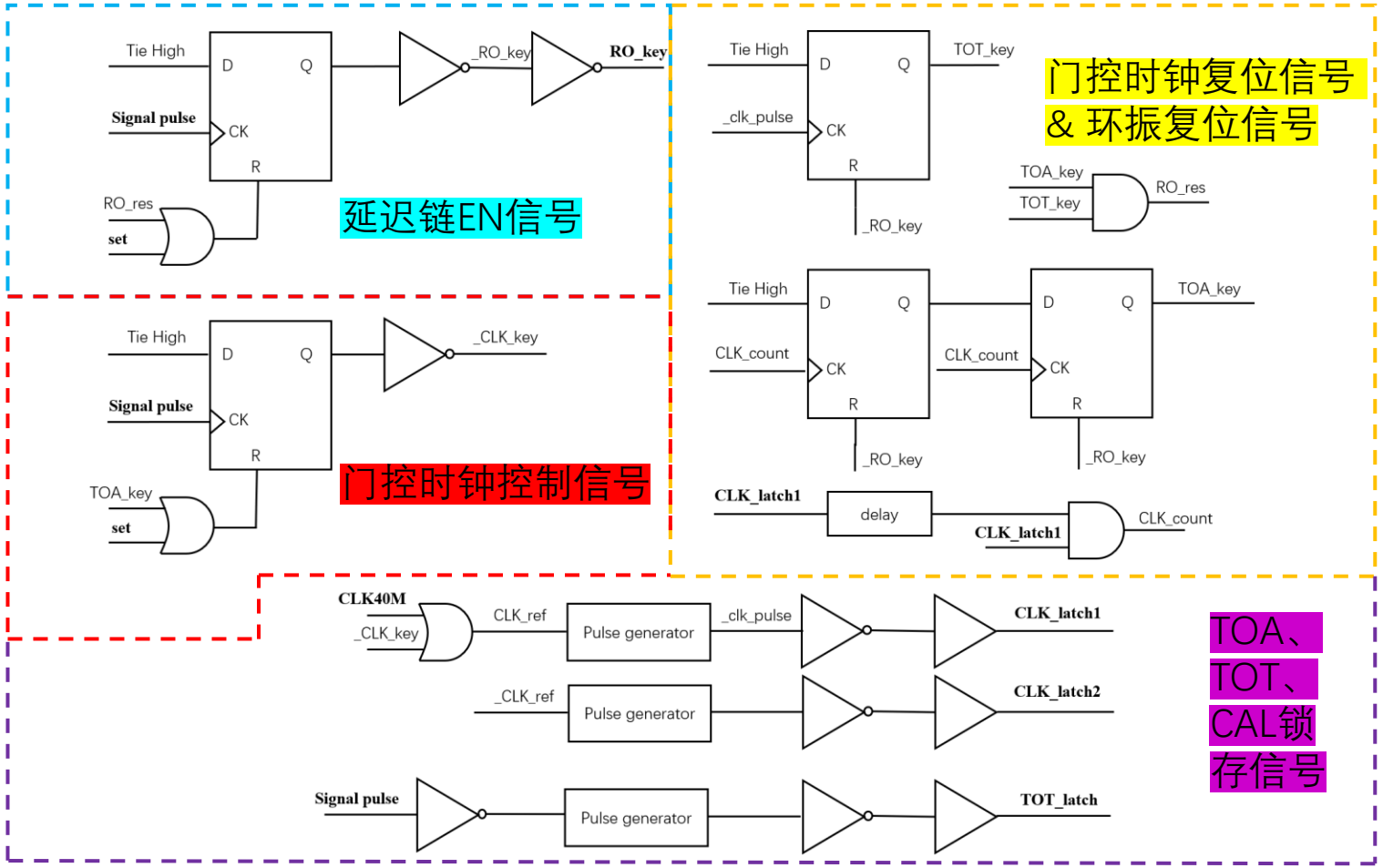
15-stage NAND delay chain + s2d block, 30 bit fine phase output



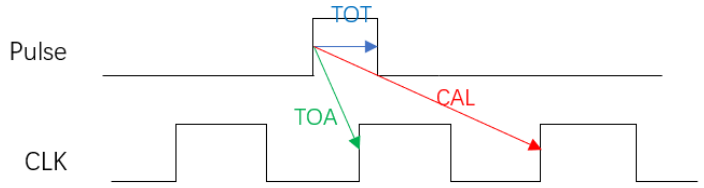
TOA and CAL fine count latch

单通道延迟链及量化模块框图

■ 控制器电路——核心控制电路产生信号

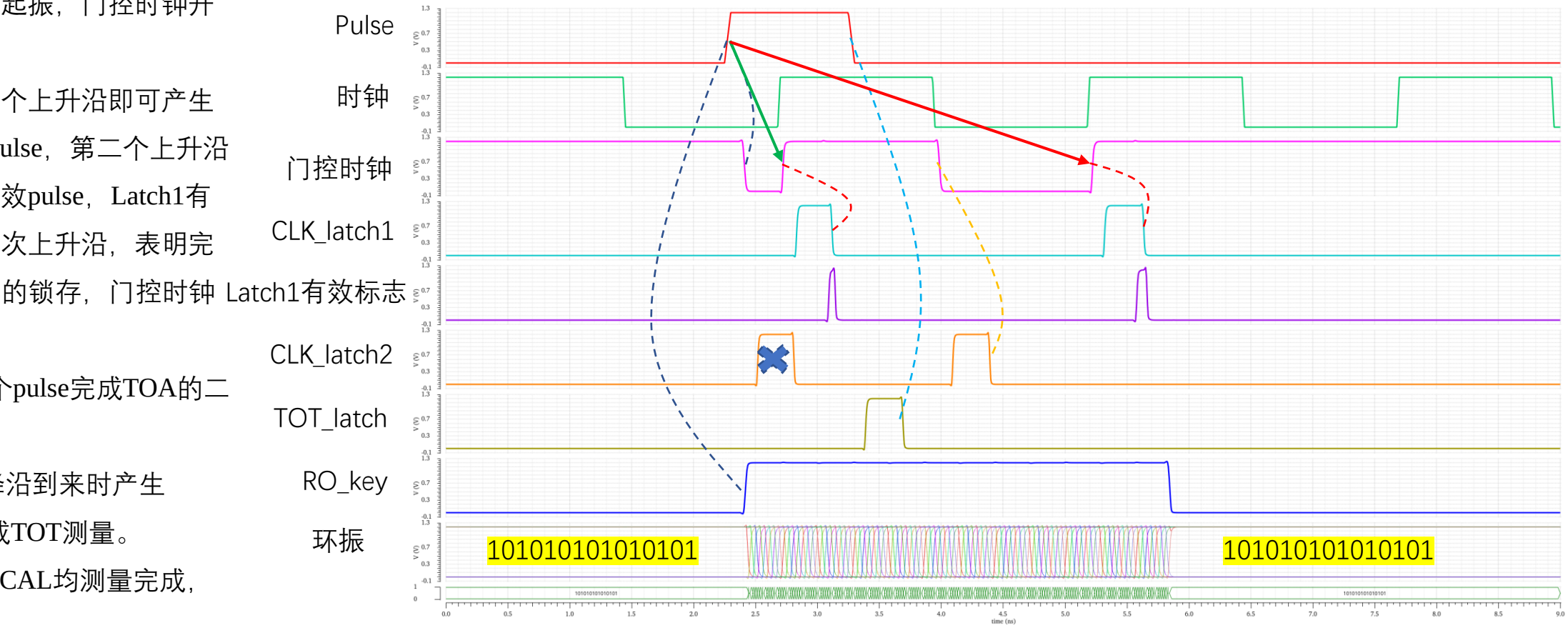


■ 控制器模块时序图（常规模式）

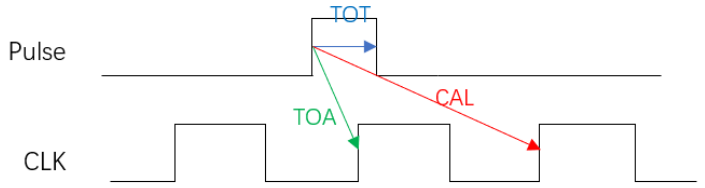


TOA、TOT、CAL示意图

- **非边界状态下**，pulse信号上升沿到来时，环振起振，门控时钟开启。
- 门控时钟第一个上升沿即可产生latch1的有效pulse，第二个上升沿产生第二个有效pulse，Latch1有效标志出现两次上升沿，表明完成TOA、CAL的锁存，门控时钟关闭。
- latch2的第二个pulse完成TOA的二级锁存。
- Pulse信号下降沿到来时产生TOT_latch完成TOT测量。
- TOT、TOA、CAL均测量完成，环振复位

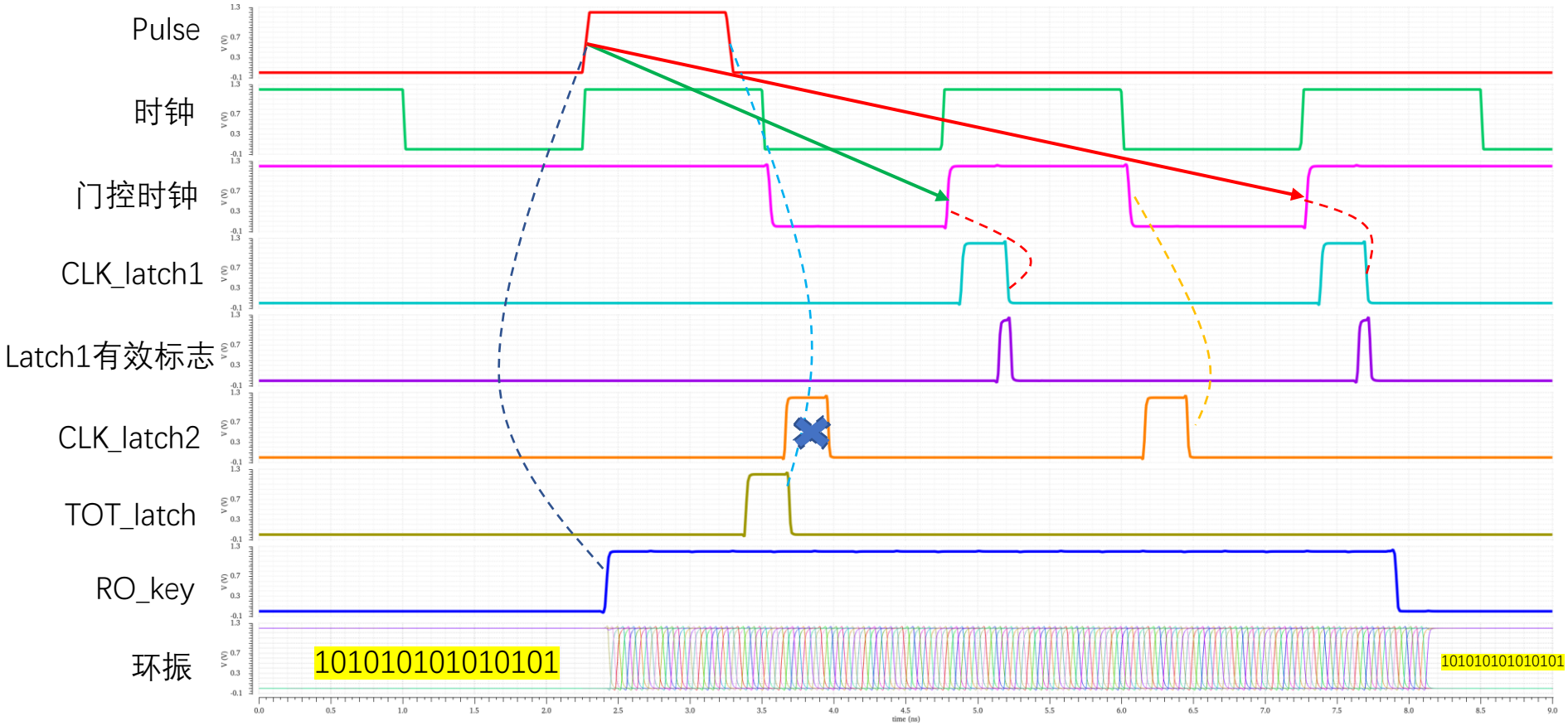


■ 控制器模块时序图（TOA边界情况1）

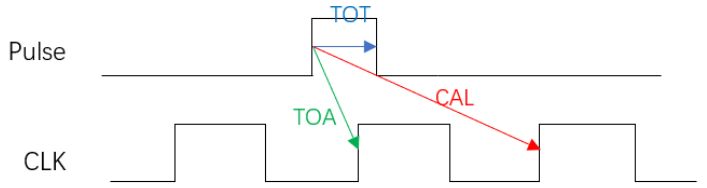


TOA、TOT、CAL示意图

- Pulse信号上升沿与时钟上升沿对齐时，距离pulse信号上升沿最近的时钟上升沿没有产生latch1的有效pulse，TOA的量化锁存顺沿至下次时钟上升沿，CAL同理。
- 相对常规情况，TOA、CAL测量向后顺延一个时钟周期，其余没有区别。

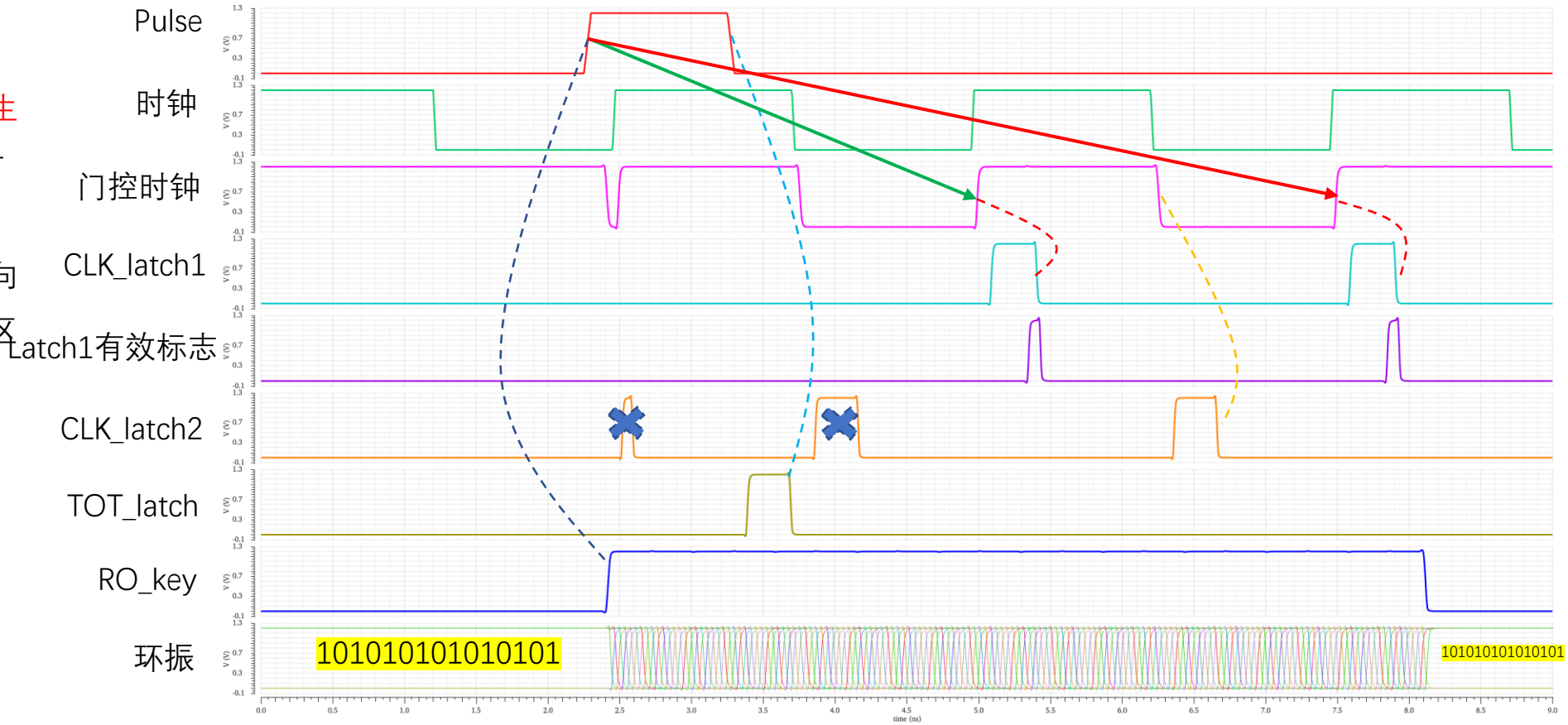


■ 控制器模块时序图（TOA边界情况2）

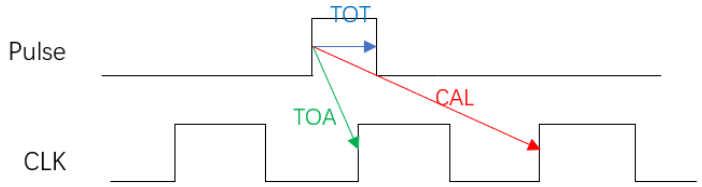


TOA、TOT、CAL示意图

- Pulse信号上升沿相对时钟上升沿对齐稍有提前时，距离pulse信号上升沿最近的时钟上升沿没有产生latch1的有效pulse，顺沿至下次时钟上升沿。
- 相对常规情况，TOA、CAL测量向后顺延一个时钟周期，其余没有区别。

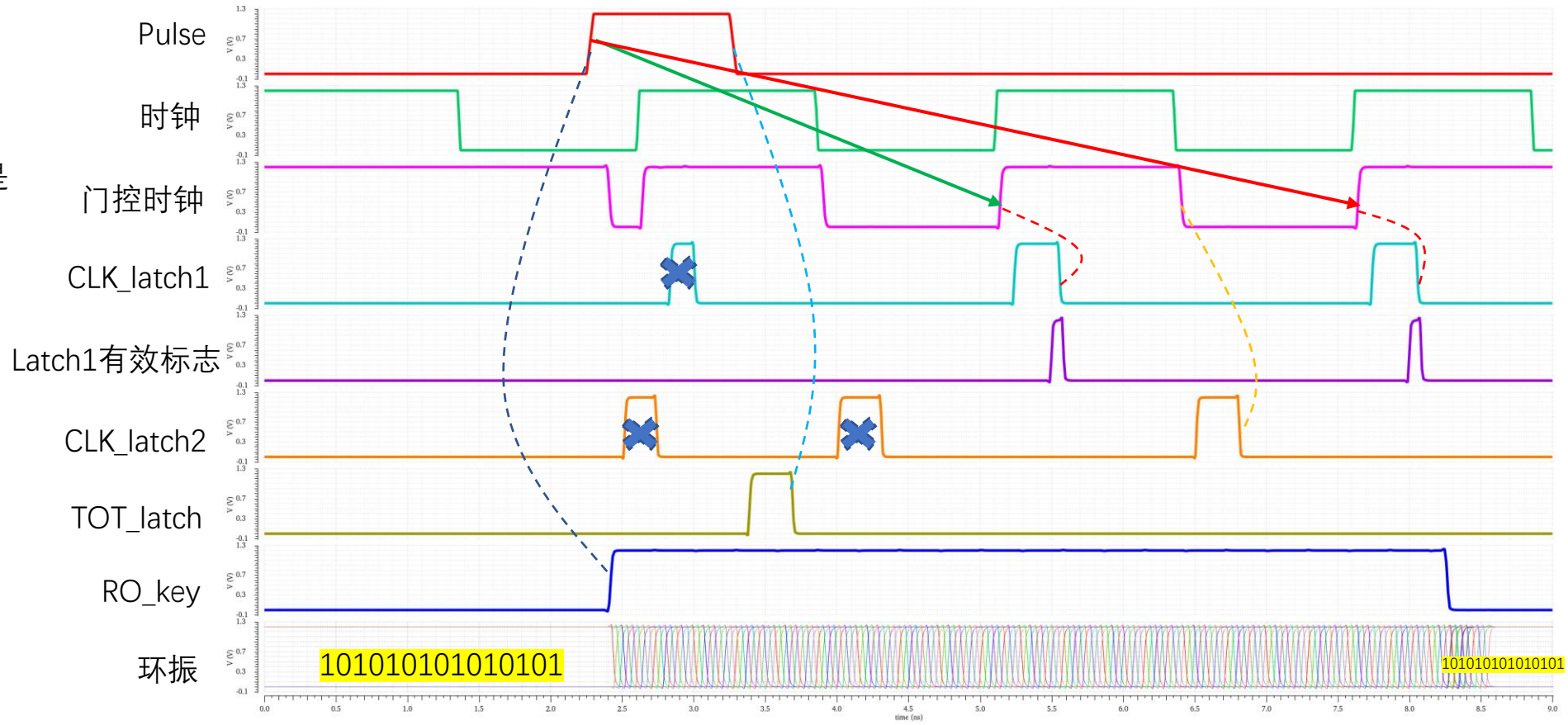


■ 控制器模块时序图（TOA边界情况3）



TOA、TOT、CAL示意图

- Pulse信号上升沿相对时钟上升沿对齐较明显提前，但<450ps时，距离pulse信号上升沿最近的时钟上升沿产生了latch1的pulse，但是pulse宽度小于300，latch1有效标志没有对应产生上升沿，此次锁存不计入，顺延至下一个时钟上升沿。
- 相对常规情况，TOA、CAL测量向后顺延一个时钟周期，其余没有区别。



- Pulse信号上升沿相对时钟上升沿对齐较提前超过450p时，为常规情况。

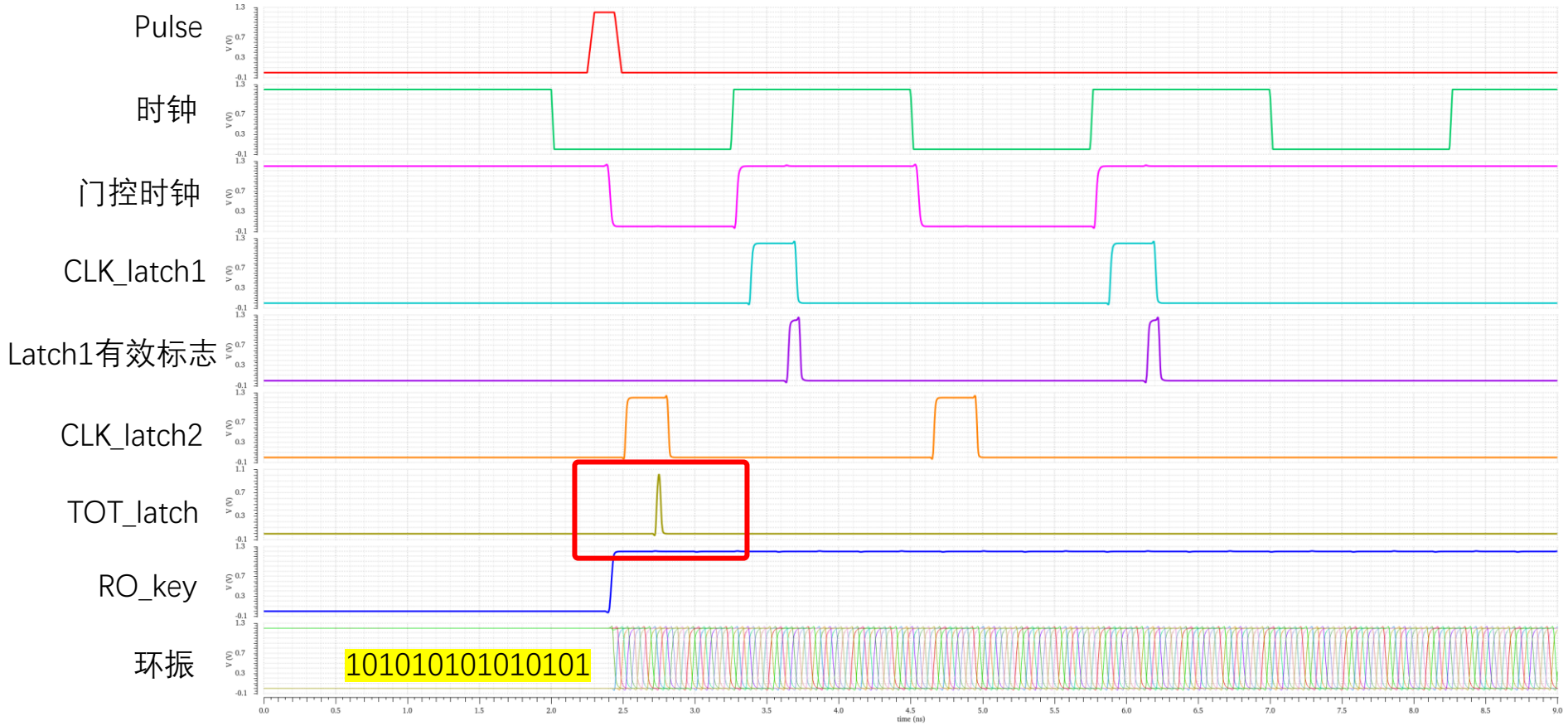
■ 控制器模块时序图（TOT边界情况）

- Pulse信号宽度小于400ps时，生成的TOT_latch信号宽度小于300p，量化锁存结果不可靠。

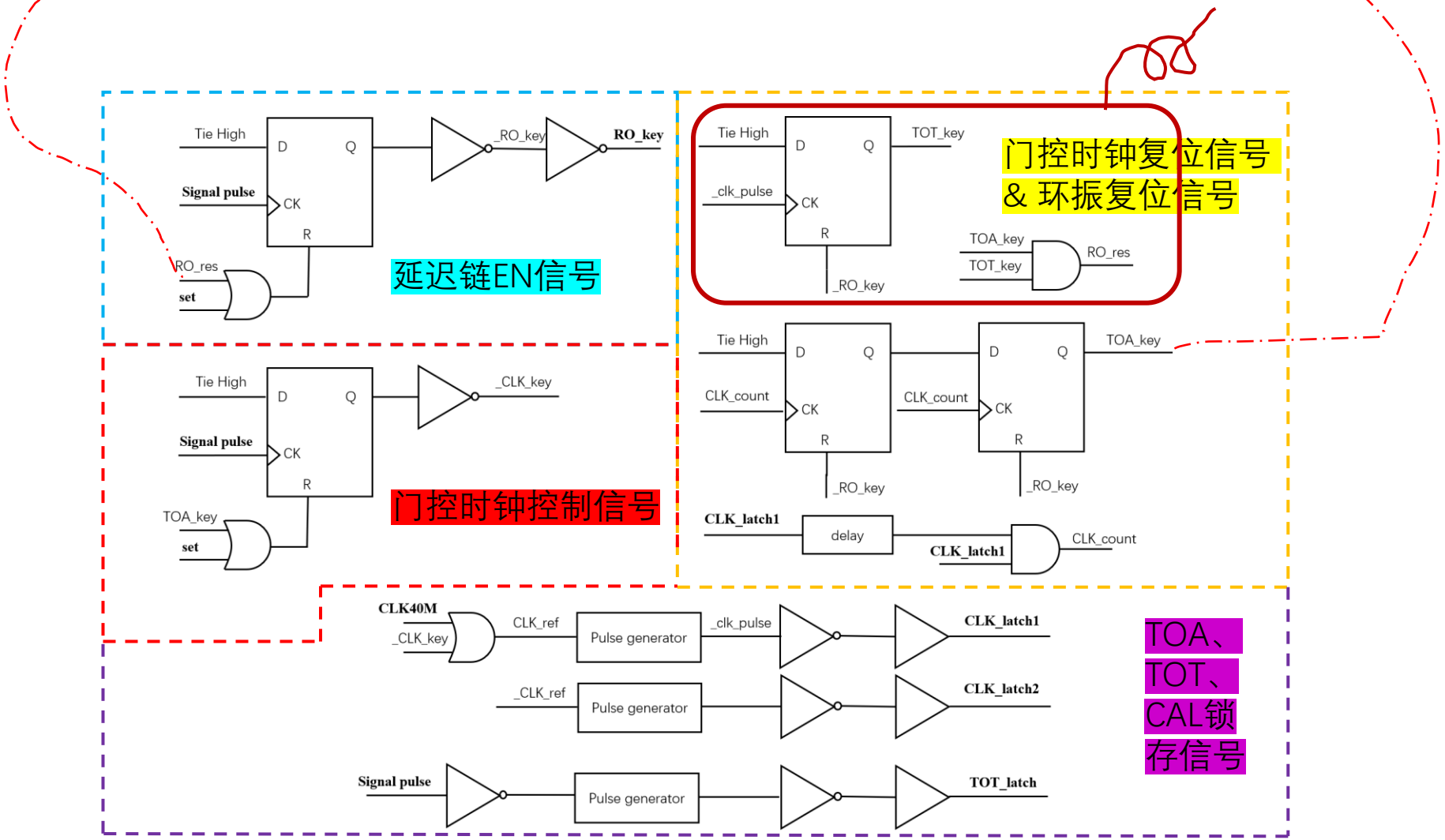
- 图示为Pulse信号宽度小于200p时的情况，Pulse信号过窄无法产生TOT_latch，TOT测量始终处于未完成状态，环振无法停止。

- 解决方案

- 如果TOT < 一个时钟周期，可CAL测完后直接关掉门控时钟和环振。
- 如果TOT不能保证小于一个时钟周期，可以计数参考时钟上升沿个数，至4关掉环振。

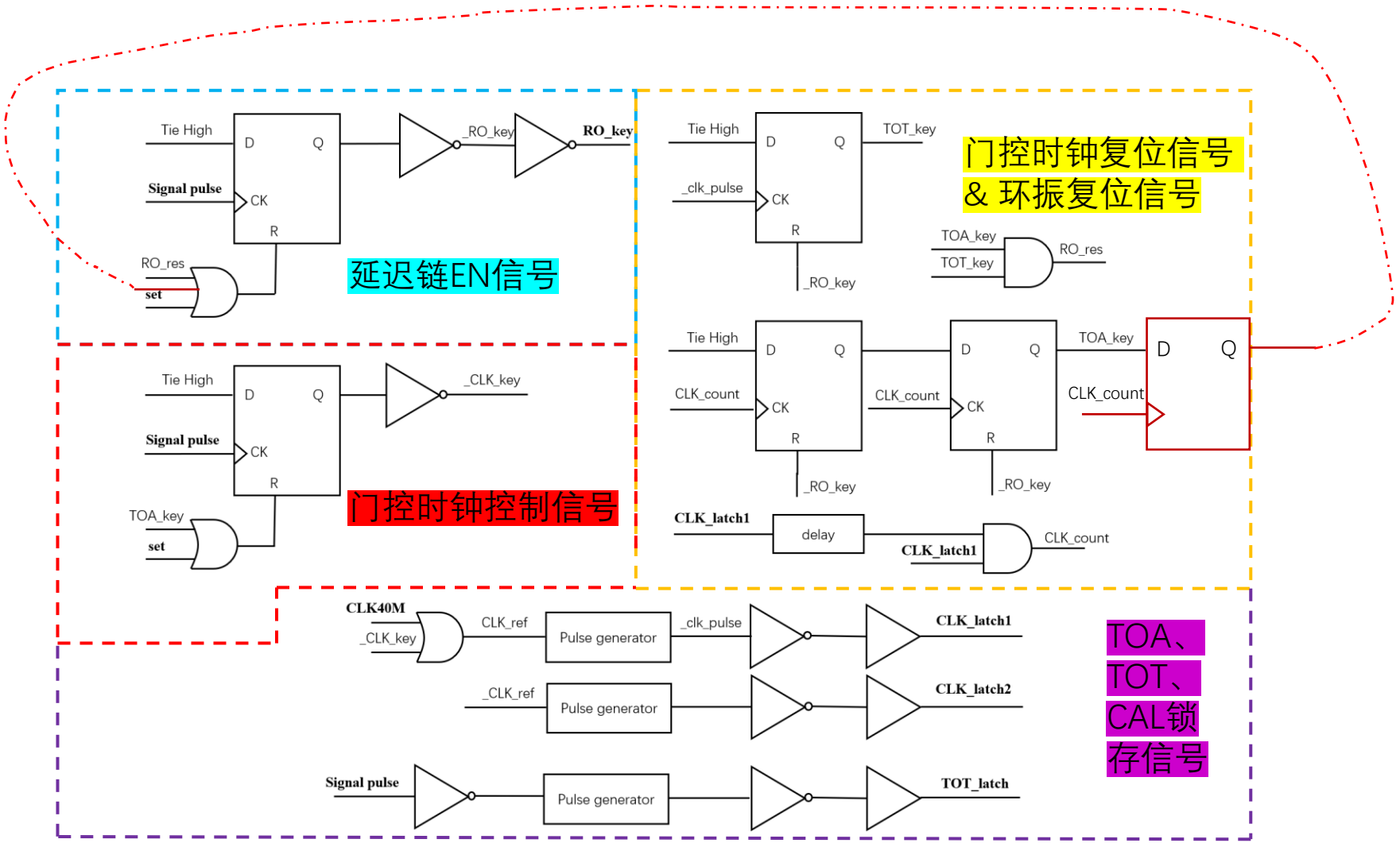


■ 解决方案1


Tie High
D
Q
_RO_key
RO_key
Signal pulse
CK
R
RO_res
set
延迟链EN信号
Tie High
D
Q
TOT_key
_clk_pulse
CK
R
_RO_key
TOA_key
TOT_key
RO_res
门控时钟复位信号
& 环振复位信号
Tie High
D
Q
_CLK_key
Signal pulse
CK
R
TOA_key
set
门控时钟控制信号
Tie High
D
Q
TOA_key
CLK_count
CK
R
CLK_count
D
Q
CK
R
_RO_key
_RO_key
CLK_latch1
delay
CLK_latch1
CLK_count
CLK40M
_CLK_key
CLK_ref
Pulse generator
_clk_pulse
CLK_latch1
_CLK_ref
Pulse generator
CLK_latch2
Signal pulse
Pulse generator
TOT_latch
TOA、
TOT、
CAL锁
存信号

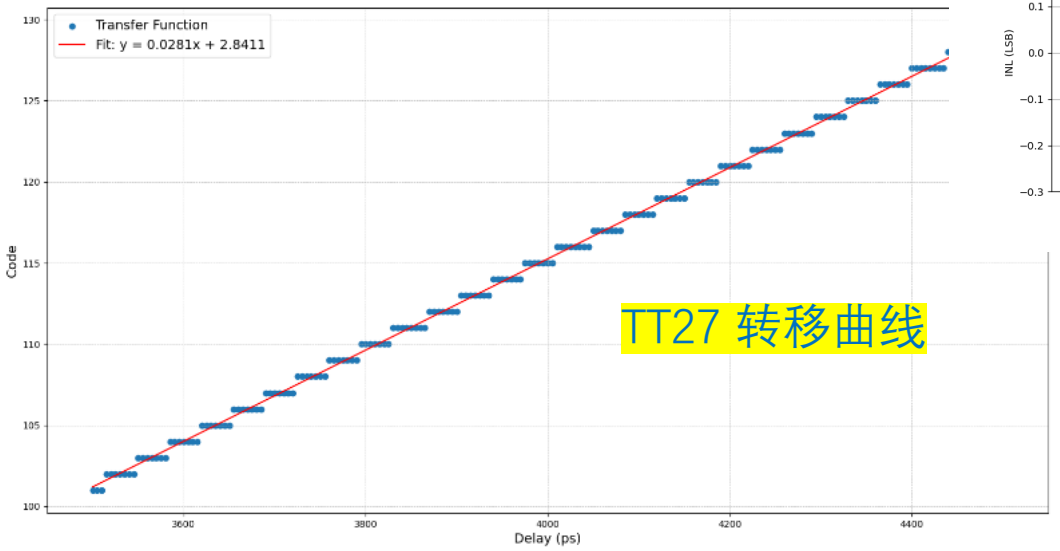
■ 解决方案2

- 图示为记四个时钟周期后重置。
- 如果想记三个时钟就停，可对二位计数器的输出取与作为reset信号。

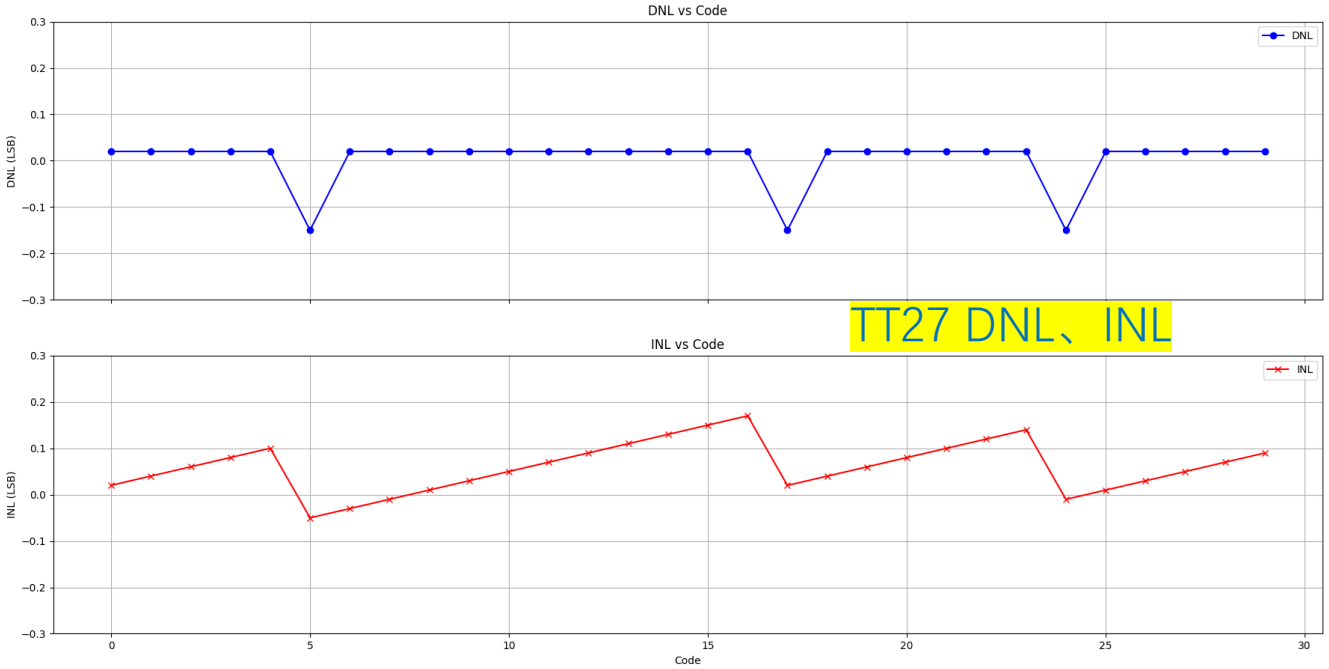


■ 后仿真

- TT27 LSB—— 35.59ps;（lvt环振LSB=28.99ps）
- FF85 LSB—— 29.41ps;
- SS-40 LSB—— 42.02ps;



TT27 转移曲线



TT27 DNL、INL

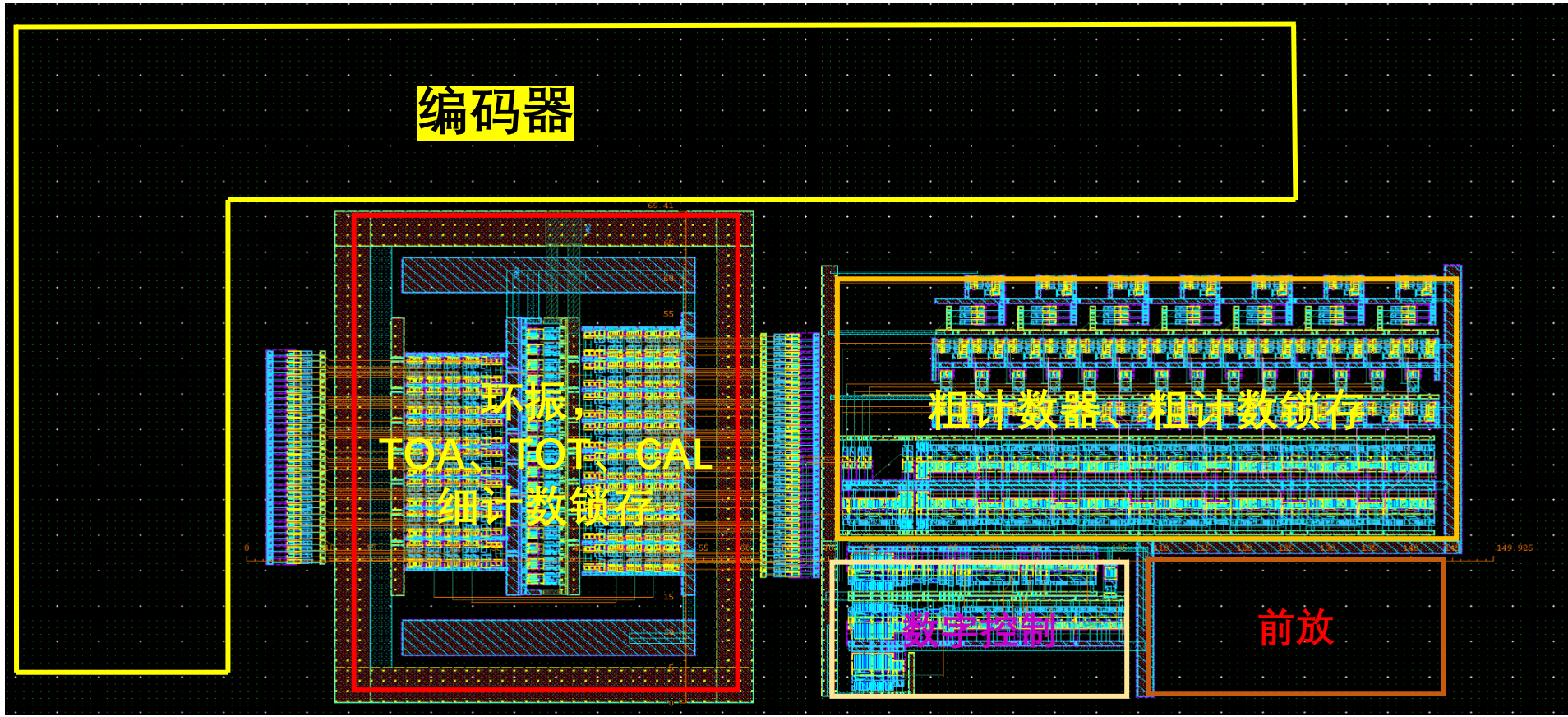
- 转移曲线仿真step为5ps，每个“台阶”只有7~8个点，待更精细的仿真；
- DNL好于± 0.15 LSB，INL好于±0.18 LSB

■ TDC后仿真

参数	需求	后仿（tt27）
工艺	SMIC55	
LSB	40ps	<36ps
精度	15ps	10.4ps
测量范围	0.5ns-25ns	0.45ns~69ns(考虑标定，范围需>50n)
INL/DNL	±0.5LSB	好于 ± 0.18LSB
功耗		单次测量平均电流<850uA (TOT 1ns, TOA 1ns)

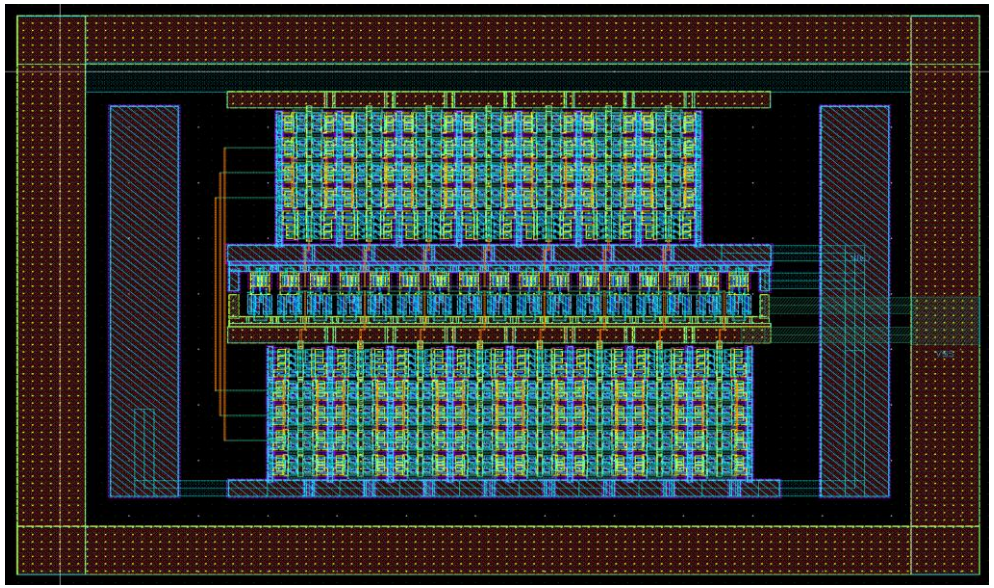
■ 整体layout进展(进行中)

- 编码器设计进行中
- 前放及串行器已有设计

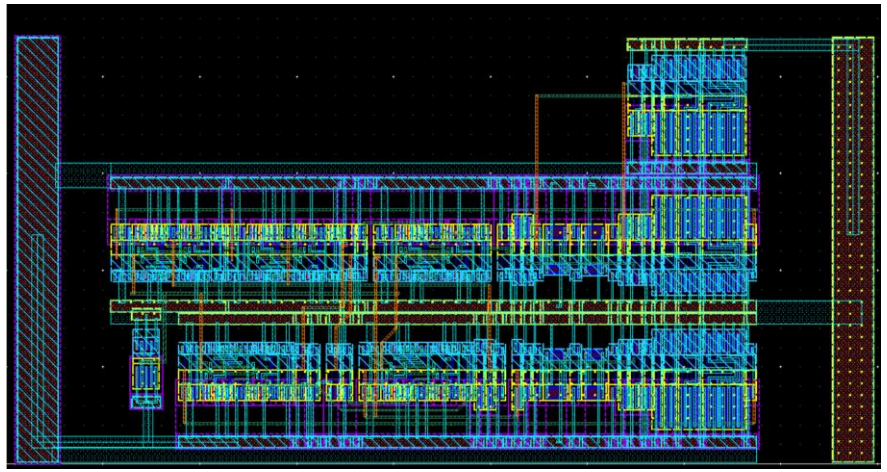


BACKUP

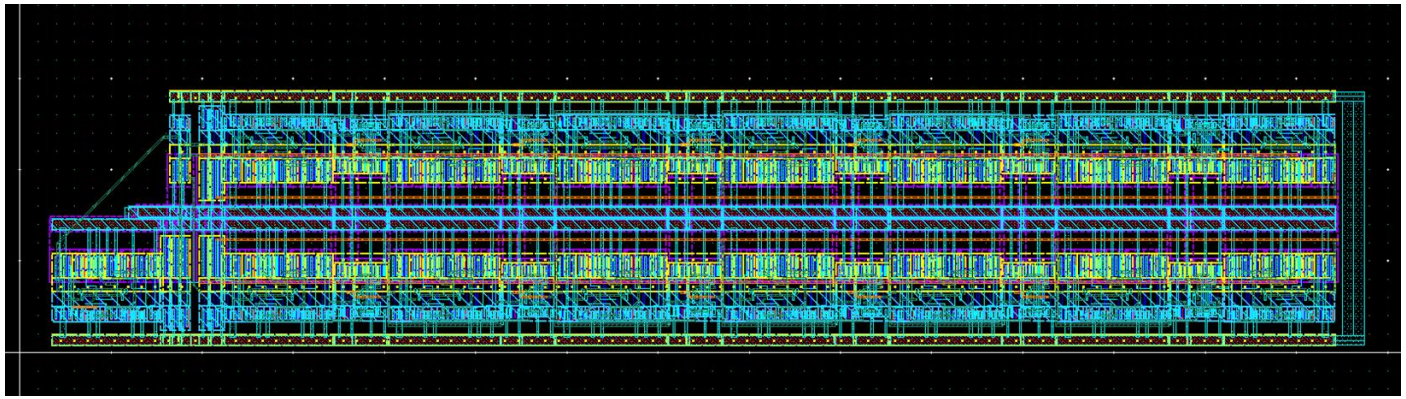
■ Layout



环振量化锁存模块



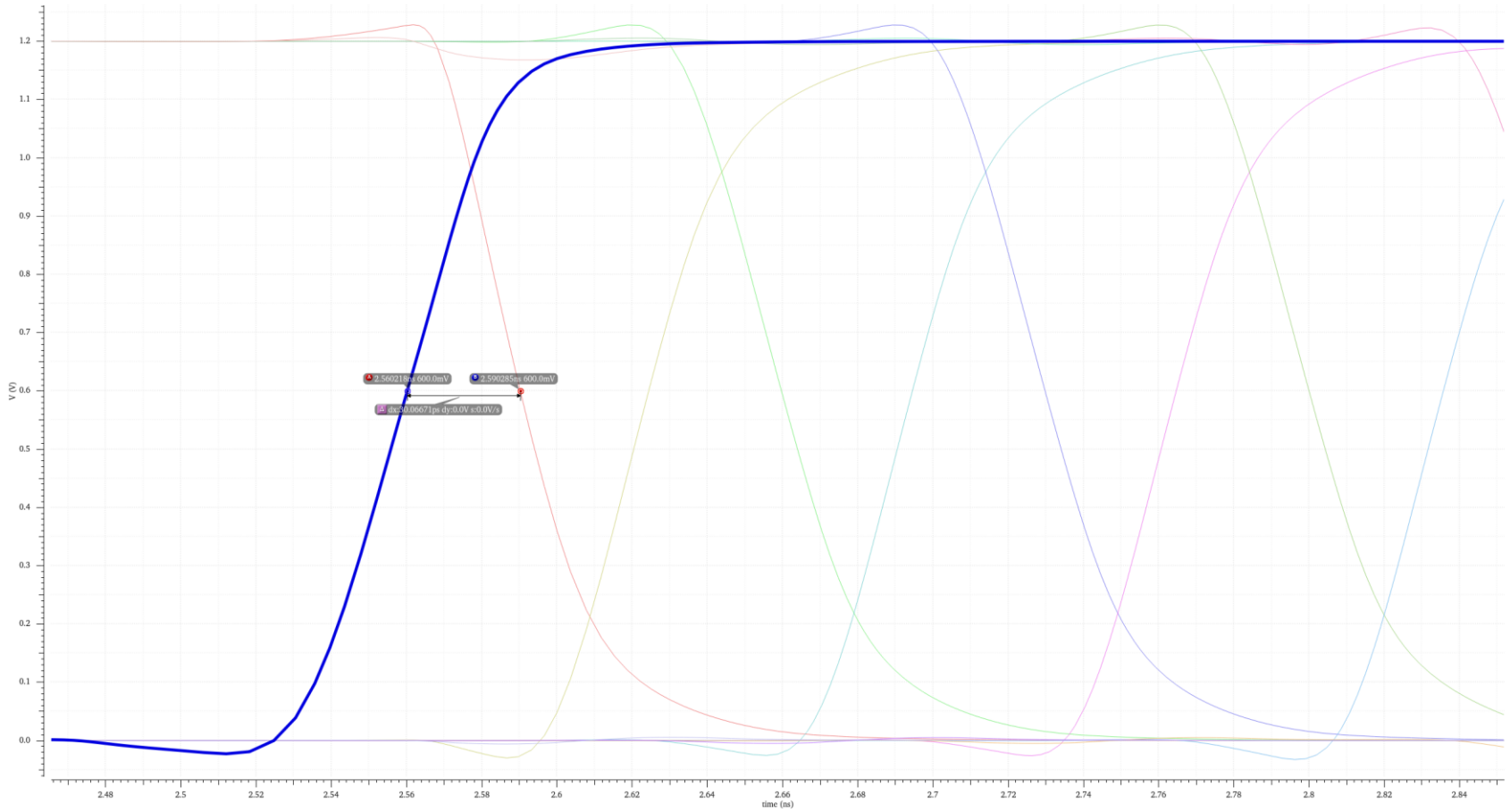
控制器模块



粗计数器

■ 环振开启

蓝色线为RO_key信号，起振是第一个延迟单元delay为30ps，延迟单元平均delay为~35ps



■ 环振状态对应温度码

101010101010101 s2d+SR——> (10)(01) (10)(01)(10)(01)(10)(01)(10)(01)(10)(01)(10)

排序——>（11111111111111000000000000000）

001010101010101 s2d+SR——> (01)(01) (10)(01)(10)(01)(10)(01)(10)(01)(10)(01)(10)

排序——>（01111111111111100000000000000）

011010101010101 s2d+SR——> (01)(10) (10)(01)(10)(01)(10)(01)(10)(01)(10)(01)(10)

排序——>（00111111111111110000000000000）

……

010101010101010 s2d+SR——> (01)(10) (01)(10)(01)(10)(01)(10)(01)(10)(01)(10) (01)

排序——>（00000000000000111111111111111）

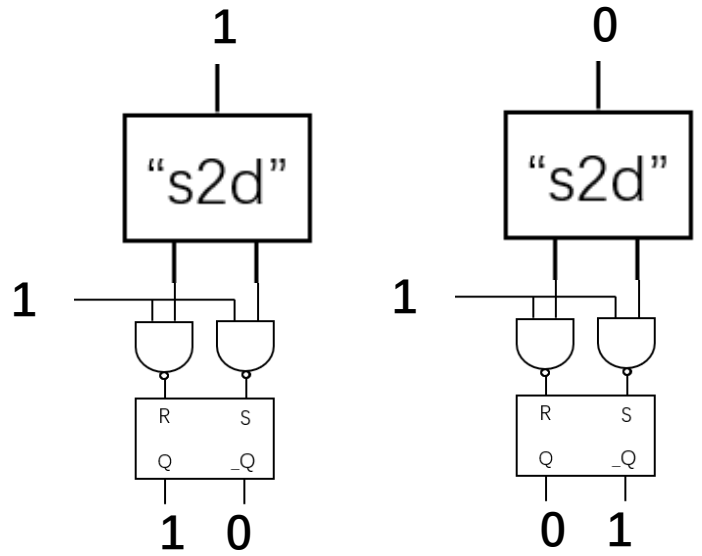
110101010101010 s2d+SR——> (10)(10) (01)(10)(01)(10)(01)(10)(01)(10)(01)(10) (01)

排序——>（10000000000000011111111111111）

……

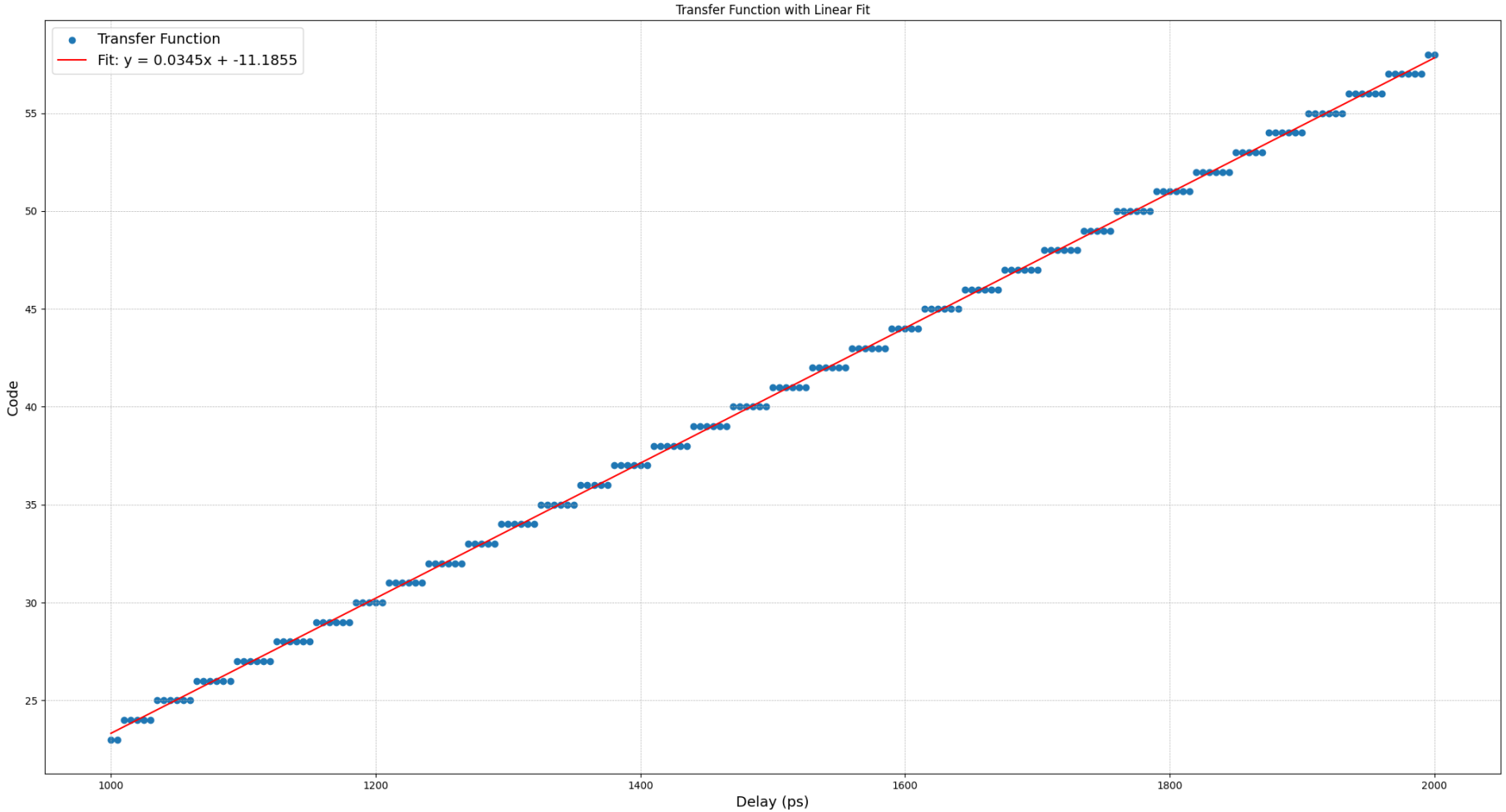
101010101010101 s2d+SR——> (10)(01) (10)(01)(10)(01)(10)(01)(10)(01)(10)(01)(10)

排序——>（11111111111111000000000000000）

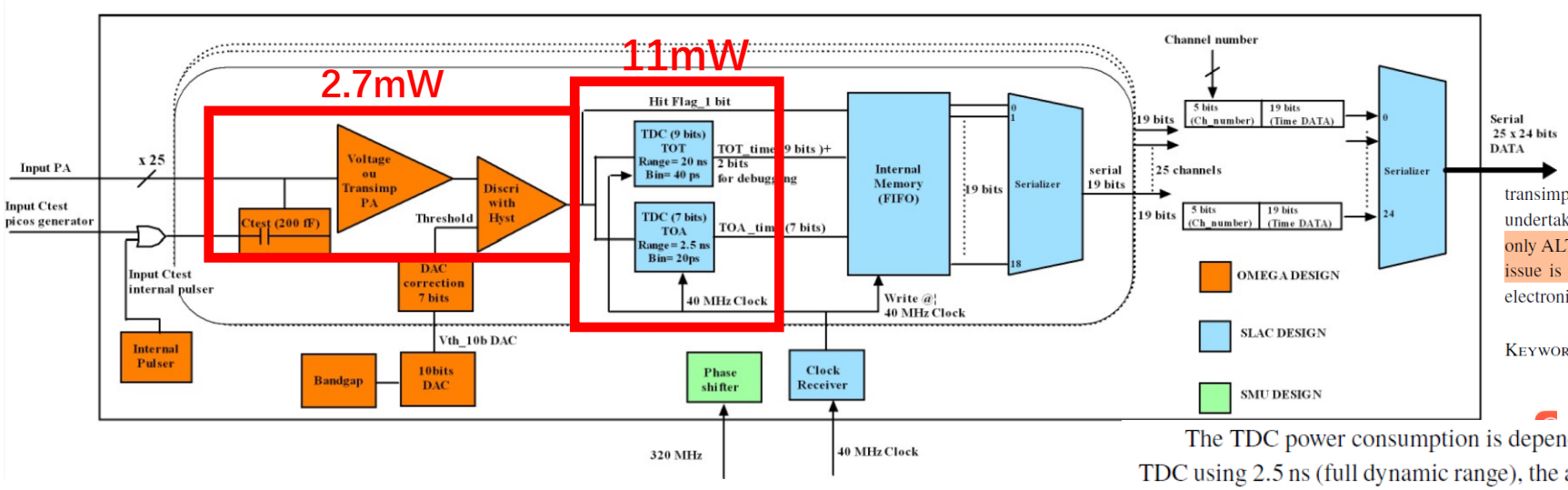


■ LVT环振TDC转移曲线

➢ LSB = 28.986ps



ALTIROC 功耗



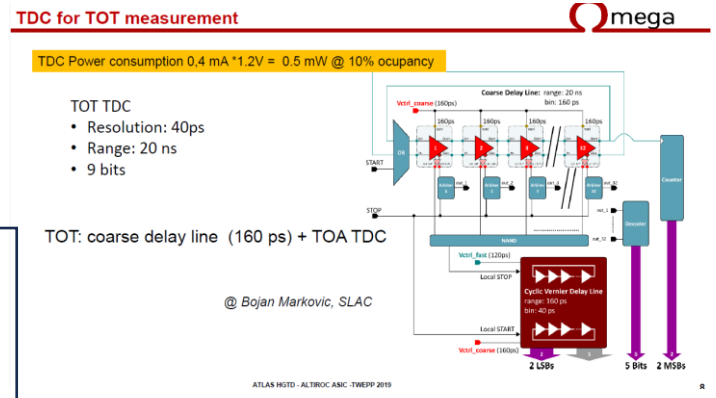
Both preamplifiers are built around a cascoded common source NMOS amplifier to ensure high bandwidth (see figure 2). The drain current (I_d) of the input transistor is adjustable between 200 µA and 1 mA. The transistor size is optimized to operate close to weak inversion while keeping its capacitance small compared to that of the sensor. The operating current is chosen to minimize the series noise while not dissipating too much power (< 2.25 mW/ch for the analog part). A PMOS follower is added to isolate the load from the discriminator. The total preamplifier power consumption is 0.85 mW using a nominal current I_d = 600 µA in the input transistor. A bank of seven capacitors (from 0 to 3.5 pF) can be connected by slow control to the preamplifier input to emulate the sensor capacitance when measuring the ASIC alone. They are not used when the ASIC is connected to the LGAD sensor array.

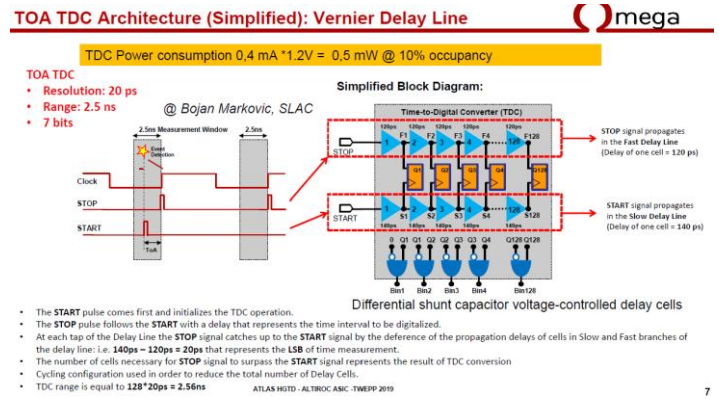
TOA measurement. Each discriminator output is sent to a sampling cell to generate a "Hit Flag" bit, that is equal to 1 in case of a hit or to 0 in case of no hit. The discriminator's power consumption is slightly less than 0.4 mW.

transimpedance preamplifiers. Beam test measurements with a pion beam at CERN were also undertaken to evaluate the performance of the module. The best time resolution obtained using only ALTIROC TDC data was 46.3 ± 0.7 ps for a restricted time of arrival range where the coupling issue is minimized. The residual time-walk contribution is equal to 23 ps and is the dominant electronic noise contribution to the time resolution at 15 fC.

KEYWORDS: Front-end electronics for detector readout; Timing detectors

The TDC power consumption is dependent on the time-interval being measured. For the TOA TDC using 2.5 ns (full dynamic range), the average power consumption over the 25 ns measurement period is about 5.2 mW. It is only 3.5 mW for a time-interval equal to half the dynamic range. Thanks to the reverse START-STOP operation, the power consumption of the TDC is much lower in the absence of a hit over threshold. This results in an average power consumption per channel of 1.1 mW for both TDCs, assuming a time interval uniformly distributed (1.25 ns average) and a maximal channel occupancy of 10%.





$$\sigma_{jitter} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}.$$

$$e_n = \sqrt{2kT/g_{m1}}.$$

$$g_{m1} = q \times I_d / 2kT$$

ALTIROC Cd：4pF

OTK Cd：10pF

FEE功耗至少15mW/ch

时钟系统和数字电路电路预计250mW/128通道

保守估计：occupancy 100%情况下，功耗至少20mW/ch

PLL& Serializer