SiPM需求及读出芯片方案

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目录

ECAL/HCAL/Muon设计需求

项目	指标	
	ECAL	HCAL
电荷测量动态范围[*1]	0.1MIPs(128fC) - 3000MIPs(3.84nC)	0.1MIPs(10pe) - 100MIPs(10000pe)
时间测量动态范围		
电荷分辨率[*2]	30% @ 0.1MIPs; 10% @ 1MIPs; 1% @ 100MIPs	同ECAL
时间分辨率[*3]	200ps @ 1MIPs; 100ps @ 12MIPs	不要求
积分非线性（INL）	<SiPM	
SiPM电容	45.9pF（待定）	50pF
SiPM增益		5.00E+05
单通道平均事例率[*4]	13kHz/ch	BR:0.24kHz, EC:1.45kHz
单通道最高事例率	230kHz	BR:6.2kHz, EC:46.3kHz
典型信号特征（不同幅度）		2,3ns
其他需要电子学实现的功能（例如刻度方式，随机触发，SiPM偏压调节，慢控等）	1，Random trigger 2，SiPM bias voltage fine tuning:1V（？）	

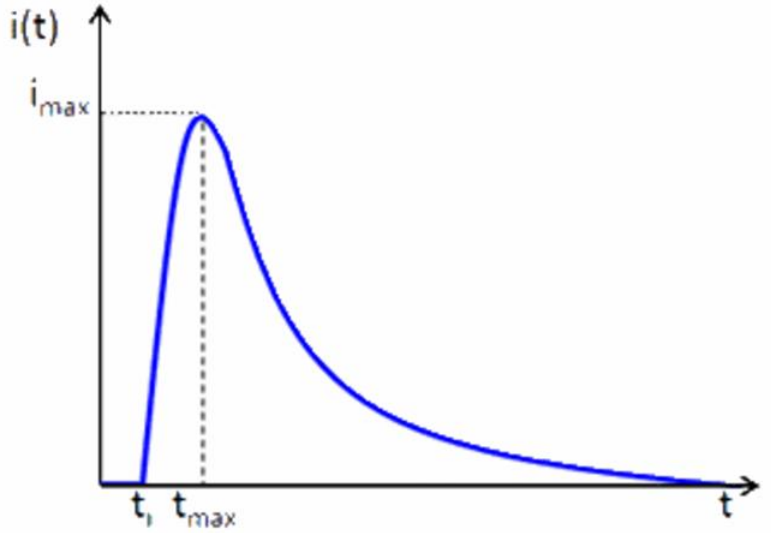
1,按晶体沉积能量计算，1MIPs - 200pe - 2.56pC，ECAL晶体双端读出，每端电荷量为1/2
2,物理上不需要单光电子分辨，刻度可能需要单光电子分辨
3，探测器总体时间分辨500ps，电子学时间分辨小于总体时间分辨
4，事例率已经考虑本底的影响

MUON requirement

- Readout design for ECAL and HCAL covers the requirements of Muon detector $N_{pe} < 100, \sigma_T < 0.5ns$
- Use the ASIC scheme from ECAL or HCAL, and customize the FEE based on ASIC.
- Revise according to the constraints from cooling and mechanical structure of the detector

Ref: page21, https://indico.ihep.ac.cn/event/23854/contributions/169297/attachments/82821/104811/Muon_Detector_IDRC_review_v2.pdf

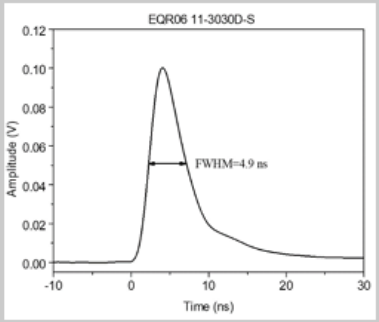
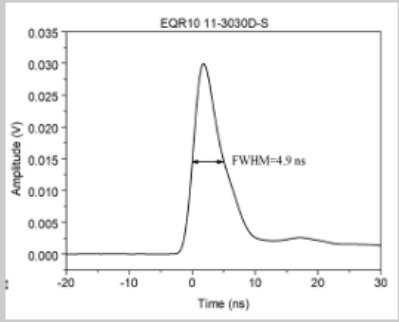
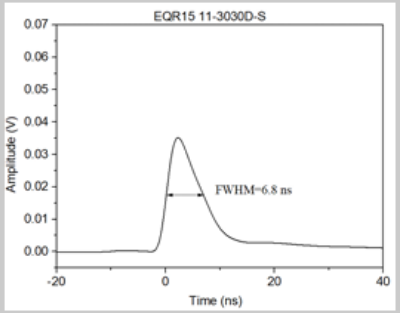
设计需求---SiPM电流波形计算（以ECAL为例）



- $Q = \int_0^\infty i * dt = I_0 * \frac{T_p}{2} + I_0 * \tau = I_0 * (\tau + \frac{T_p}{2})$
- 0.1MIP=**128fC**, 3000MIPs=**3.84nC**
- Assume $T_p = 40ns$, $\tau = 300\text{ns}$, for 0.1~3000MIPs (128fC~3.84nC)
  - I_0=**0.4uA~12mA**
  - Set SNR to 5, then I_{noise} =80nA
- For calibration channel, 1 p.e equals to 12.8fC, we use CSA
  - Set SNR to 10, then ENC=1.28fC
  - $C_d = 45.9pF$,

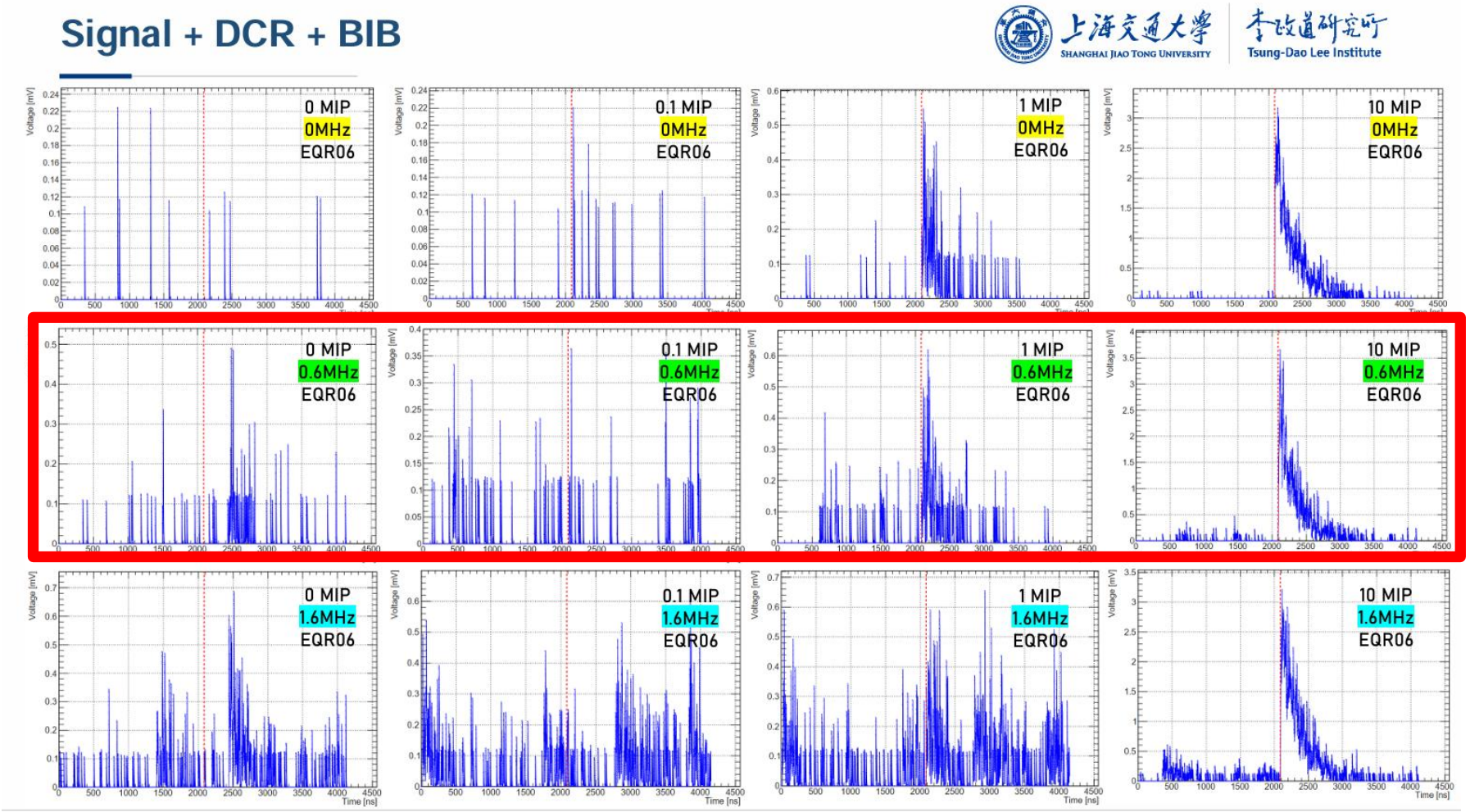
SiPM参数---以NDL SiPMs为例

NDL SiPMs: 6 μm, 10 μm, 15 μm pixel, 3×3 mm^2 active area

	EQR06 11-3030D-S	EQR10 11-3030D-S	EQR15 11-3030D-S
Micro-cell Number	27191 / mm^2	10000 / mm^2	4444 / mm^2
Operation Voltage	V_B + 8 V	V_B + 12 V	V_B +8 V
Peak PDE @420nm	30%	36%	45%
Gain	8×10^4	1.7×10^5	4×10^5
DCR	276 kHz / mm^2	400 kHz / mm^2	250 kHz / mm^2
Capacitance	5.1 pF / mm^2	3.5 pF / mm^2	5.6 pF / mm^2
Single Photoelectron Waveform			

SiPM参数---模拟数据（不同本底下）

Ref: https://indico.ihep.ac.cn/event/25007/contributions/180119/attachments/87762/113072/20250214_ThresholdEffect.pdf



SiPM DCR: 276KHz/mm2

在**0.6MHz BIB**条件下，**1MIP**及以下的信号离散

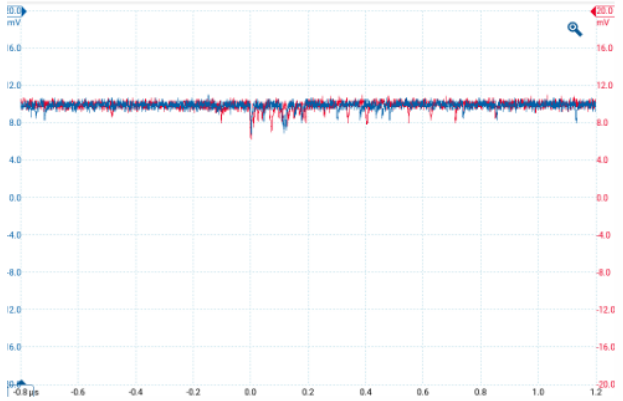
NDL SiPM测试数据

BGO-SiPM tests with Cs-137

Reference: talk in Jan 2, 2025

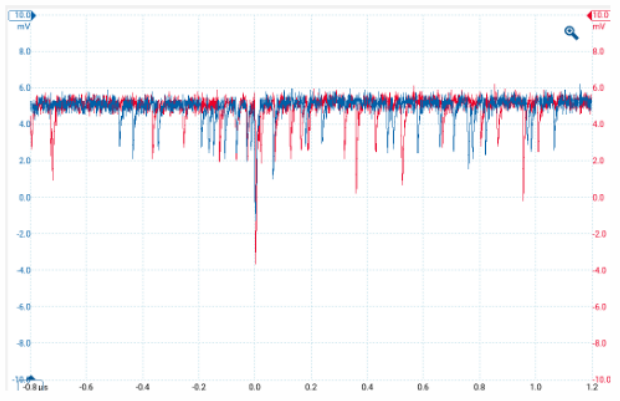
- Several NDL-SiPMs tested with 2cm BGO using Cs-137 (662 keV gamma)
- BGO-SiPM waveforms: discrete spikes due to narrow NDL-SiPM pulses and long BGO scintillation time
  - Extremely difficult for SiPM readout ASIC: *trigger* and *shape* smooth waveforms

EQR06



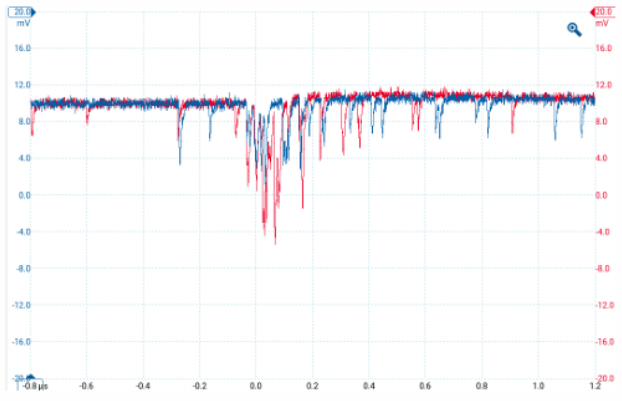
- Small amplitude due to its lower SiPM gain (8×10^4)

EQR10 (V_B + 8 V)



- Here with Over-Voltage=8V
- Can not work properly at OV=12 V

EQR15



- Relatively larger amplitude due to its higher SiPM gain (4×10^5)
- But waveforms still not smooth

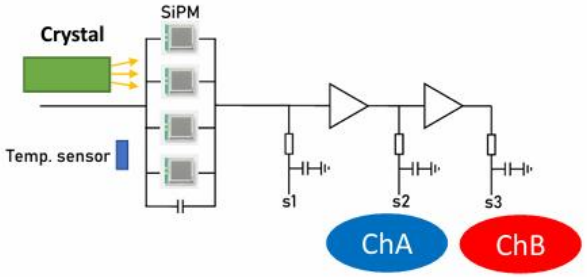
None of these NDL SiPMs can provide continuous/smooth waveforms

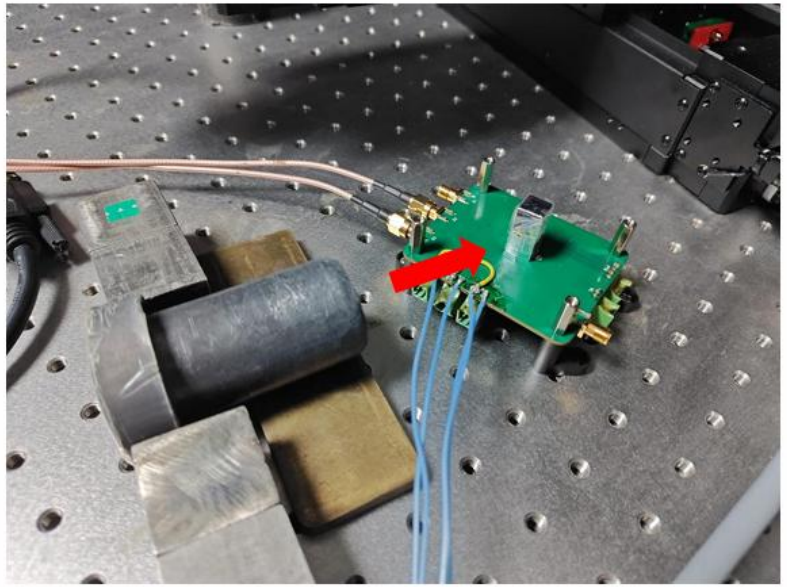
Ref: https://indico.ihep.ac.cn/event/25036/contributions/180358/attachments/87644/112887/2025_0207_NDL_SiPM_Discussions.pdf

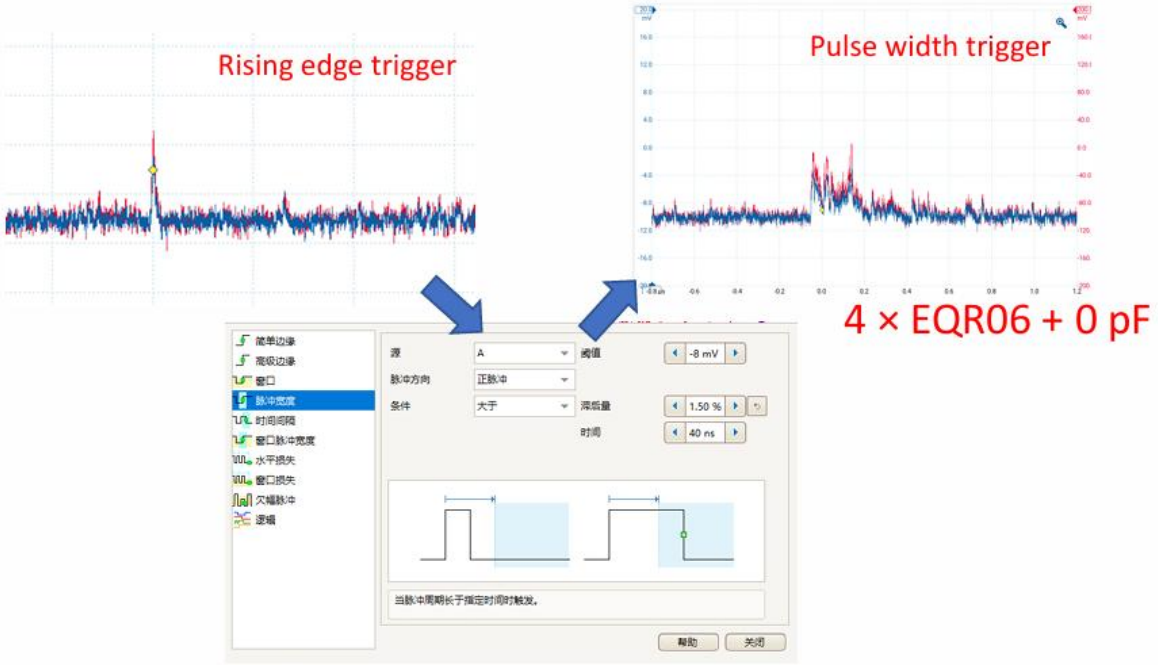
NDL SiPM测试数据

Radioactive source tests

- Cs-137 source (662 keV)
- 1×1×2 cm^3 BGO crystal, 4 EQR06 SiPM gives higher light output
- Advanced trigger method: only trigger events with large pulse width
  - Change capacitor: 100 pF, 200 pF, 330pF, 470pF



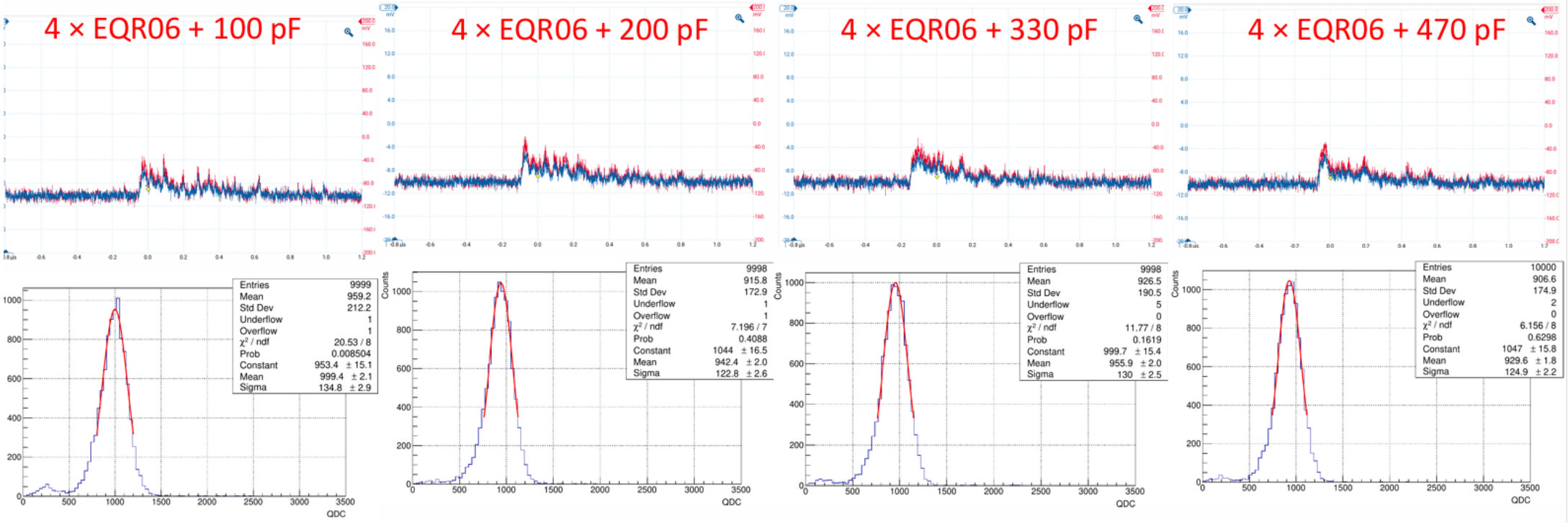




https://indico.ihep.ac.cn/event/25007/contributions/180120/attachments/87763/113077/20250214_NDL%20SiPM%20Parallel%20Connection%20Tests.pdf

NDL SiPM测试数据

Energy spectrum of Cs-137



- As the capacitance increases, the waveform becomes smoother
- Similar energy resolution for these setups

ECAL/HCAL/Muon设计需求、ASIC指标

项目	指标		ASIC指标	备注
	ECAL	HCAL		
电荷测量动态范围[*1]	1MIPs(1.28pC) - 3000MIPs(3.84nC)	1MIPs(1.6pC) - 100MIPs(160pC)	1.28pC-3.84nC	ECAL按增益8*10e4，HCAL按10e5算
时间测量动态范围				
电荷分辨率[*2]	10% @ 1MIPs； 1% @ 100MIPs	同ECAL	10%@1MIP	信号不离散的条件下，ASIC自身的分辨
时间分辨率[*3]	200ps @ 1MIPs； 100ps @ 12MIPs	不要求	200ps@1MIP	信号不离散的条件下，ASIC自身的分辨
积分非线性（INL）	<SiPM			
SiPM电容	45.9pF	100pF	100pF	ASIC按100pF设计
SiPM增益	8.00E+04	1.00E+05	1.00E+05	
单通道平均事例率[*4]	13kHz/ch	小于ECAL	13KHz/ch	
单通道最高事例率	230kHz	小于ECAL	500KHz/ch	
典型信号特征（不同幅度）		2,3ns		
典型脉冲宽度	BGO decay time=300ns	Glass decay time=500ns	1us	HCAL按decay time乘以2.36计算
其他需要电子学实现的功能（例如刻度方式，随机触发，SiPM偏压调节，慢控等）	1，Random trigger 2，SiPM bias voltage fine tuning:1V（？）		0.2V	
1,按晶体沉积能量计算，1MIPs - 200pe - 2.56pC，ECAL晶体双端读出，每端电荷量为1/2				
2,物理上不需要单光电子分辨，刻度可能需要单光电子分辨				
3，探测器总体时间分辨500ps，电子学时间分辨小于总体时间分辨				
4，事例率已经考虑本底的影响				

2025.021.4、2025.02.17分别与ECAL组、HCAL组讨论后，鉴于小于1MIP SiPM信号的离散性，
本次流片暂不考虑0.1~1MIP的信号，待ECAL/HCAL确定相应的SiPM型号、小信号波形后，再研究相应的读出电路

参考芯片： DIET

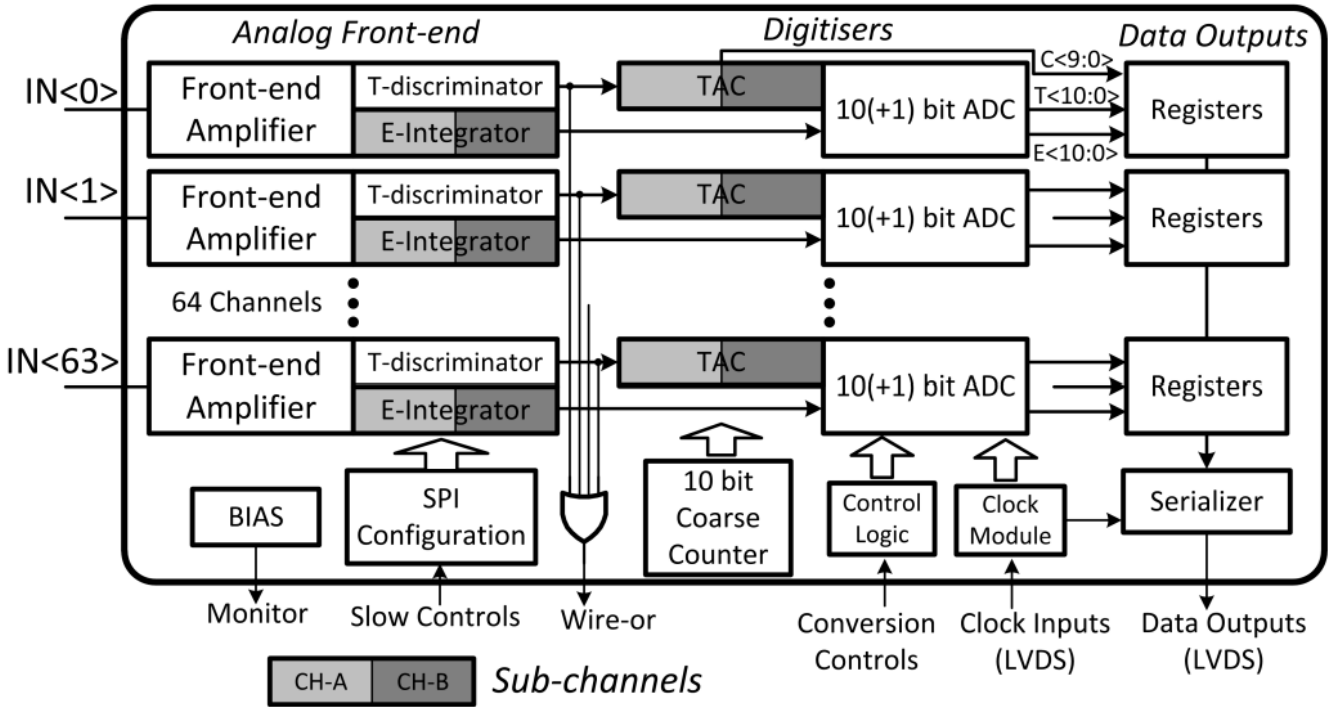


Figure 1. The block diagram of the DIET ASIC.

Table 1. The specification of the DIET ASIC.

Parameters	Specifications
Maximum Input Current	5 mA
Input Dynamic Range	0 ~ 46 pC (Low Range) 0 ~ 96 pC (High Range)
Integral Non-Linearity for Energy	Better than 1%
ADC Resolution	10 bit (1 extra bit for calibraion)
Timing Jitter	~ 25 ps rms @ C_{in} = 12 pF and threshold is 20 photoelectrons (80 μA)
(Fine) TDC Resolution	10 bit (1 extra bit for calibration)
(Fine) TDC Bin Width	25 ps
Power Consumption	5 mW / channel
Conversion Dead Time	12.5 μs
Readout Bandwidth	200 Mbps
Number of Channels	64

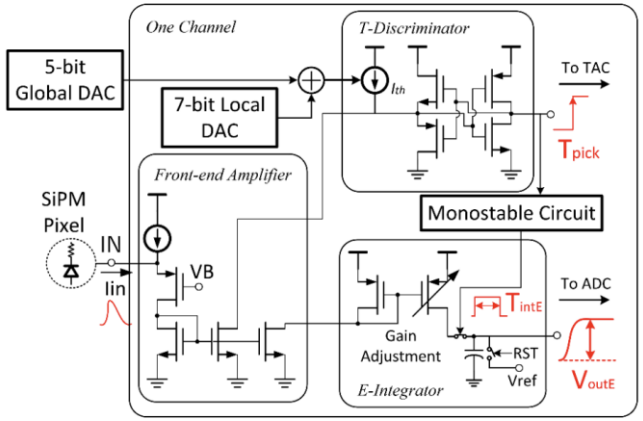
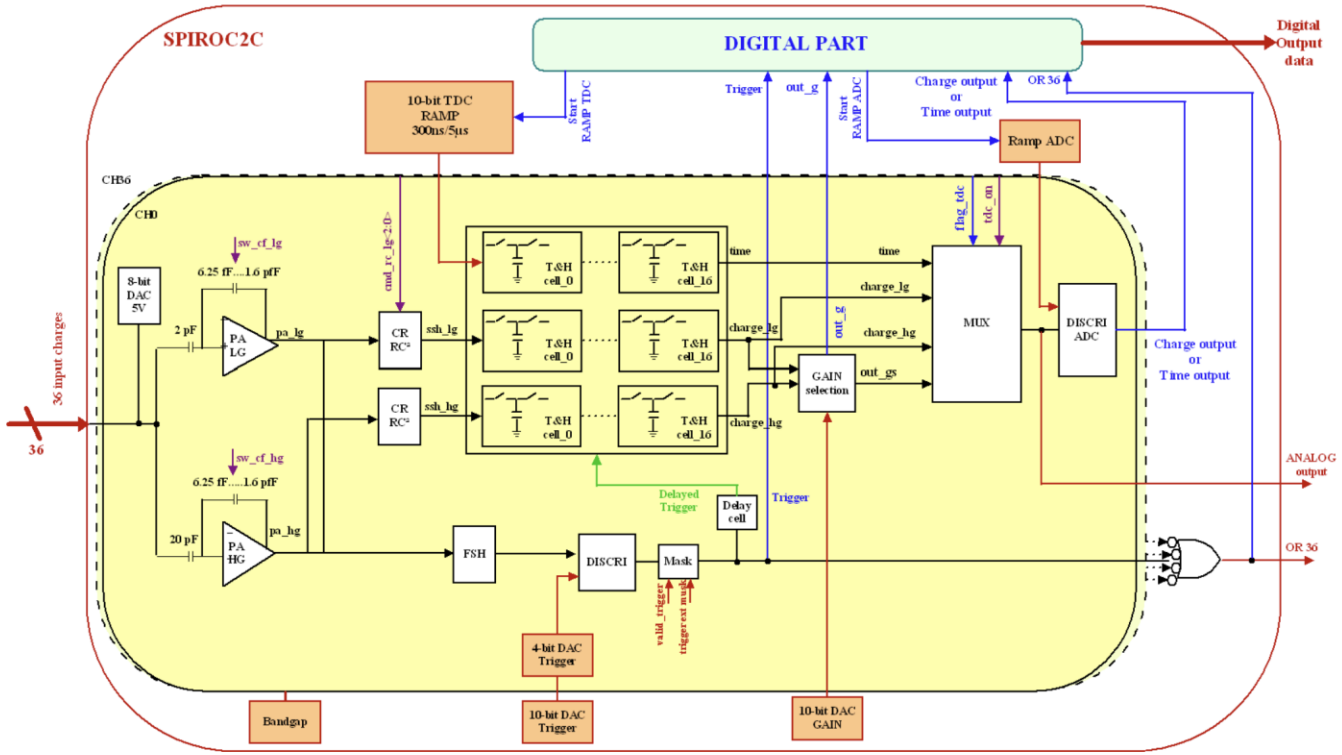


Figure 2. The block diagram of the analog front-end circuit.

Ref : DIET: a multi-channel SiPM readout ASIC for TOF-PET with individual energy and timing digitizer

参考芯片：SPIROC2C



SPIROC is a 36 channels readout ASIC for SiPM @HCAL for CALICE collaboration
It is designed to auto-trigger on 1/3 p.e. (50 fC) and stores up to 15 samples in an analog memory before the events are digitized and readout.

TABLE I SPIROC MAIN SPECIFICATIONS

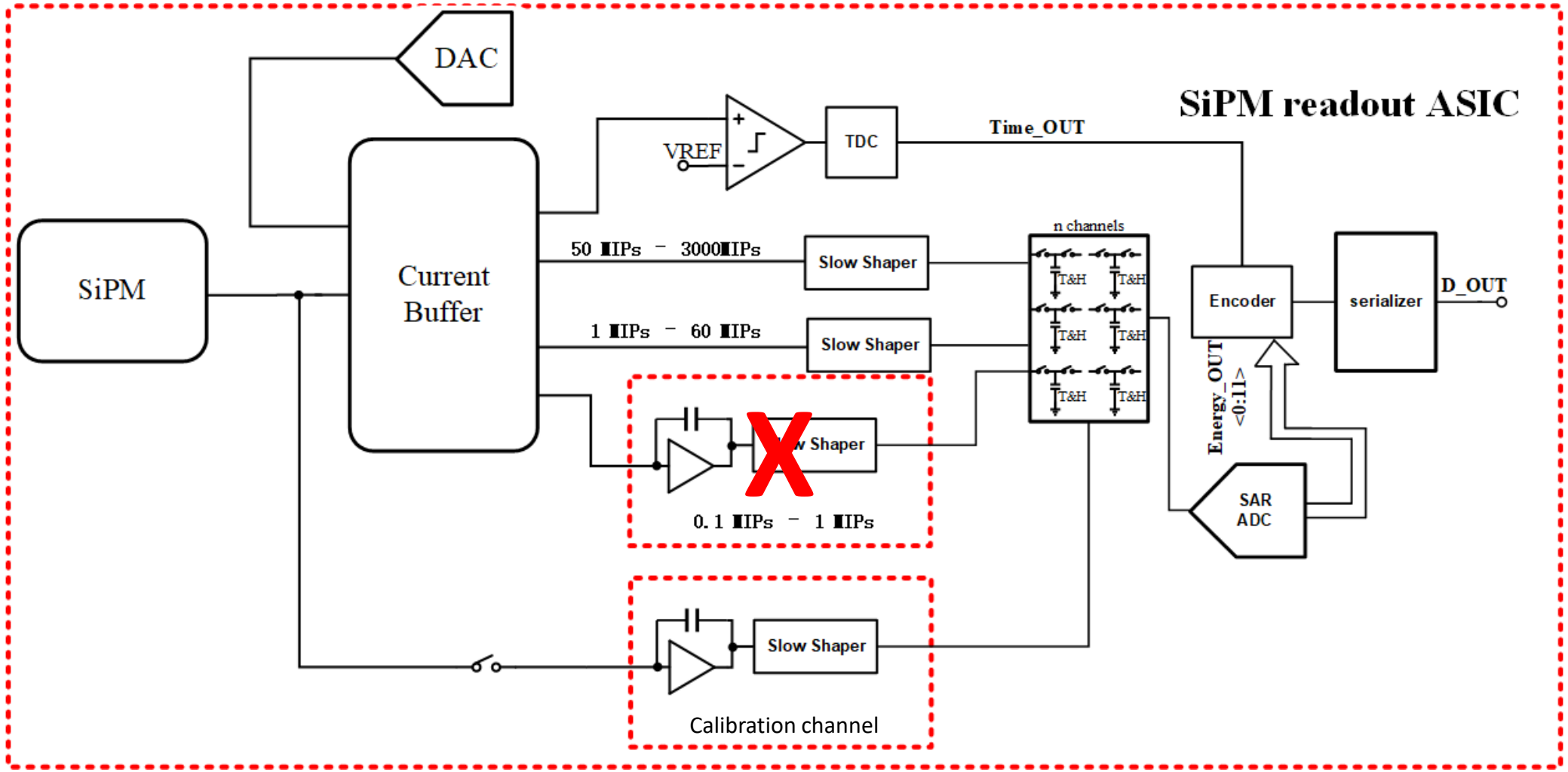
dynamic range	80 fC – 200 pC
signal to noise ratio	~7 (SiPM gain = 10^6)
analog output INL	$< \pm 1\%$
pedestal uniformity	$\sigma = 2$ mV
crosstalk	$< \pm 0.3\%$
effective noise charge	1.5×10^5 electrons @ 50pF (50ns shaping)
ADC resolution	0.6 mV (LSB)
timing resolution	100 ps
time walk @ 1/2 MIP	3ns
time jitter @ *1/2* MIP	$< \pm 2$ ns
trigger efficiency	100%@1/3 photon electron
trigger noise	8 mV
input DAC INL	$< \pm 2\%$
input DAC range	0.5 – 4.5 V
threshold DAC range	2 V
threshold DAC INL	$\leq \pm 1\%$
power consumption	25μW per channel[1]

Ref: SPIROC: design and performances of a dedicated very front-end electronics for an ILC Analog Hadronic CALorimeter (AHCAL) prototype with SiPM read-out

ASIC指标---ECAL/HCAL/Muon

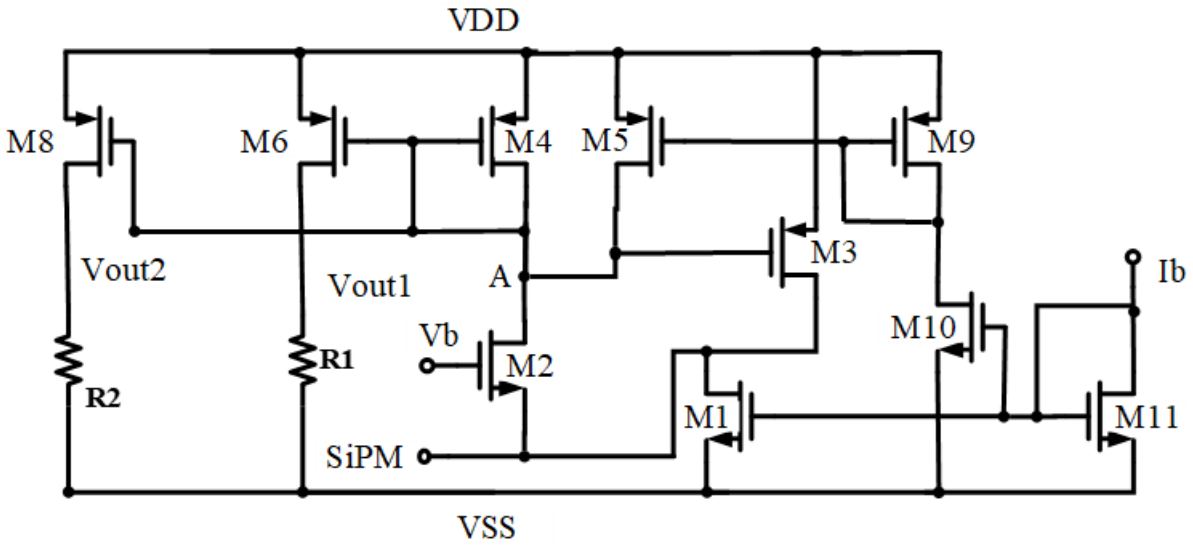
Parameters	Specifications
Input Dynamic Range	1.28pC~3.84nC
Energy Resolution	10%@1MIP=1.28pC, C_{det}=100pF
Time Resolution	200ps@1MIP=1.28pC, C_{det}=100pF
Max rate/ch	500KHz
ADC	40MHz, 10-bit
TDC Resolution	8bit
TDC Bin Width	100ps
Power consumption	<15mV/channel
Readout Bandwidth	346Mb/s
Voltage supply	1.2V
Number of channels	4

ChoMin ASIC单通道系统框图

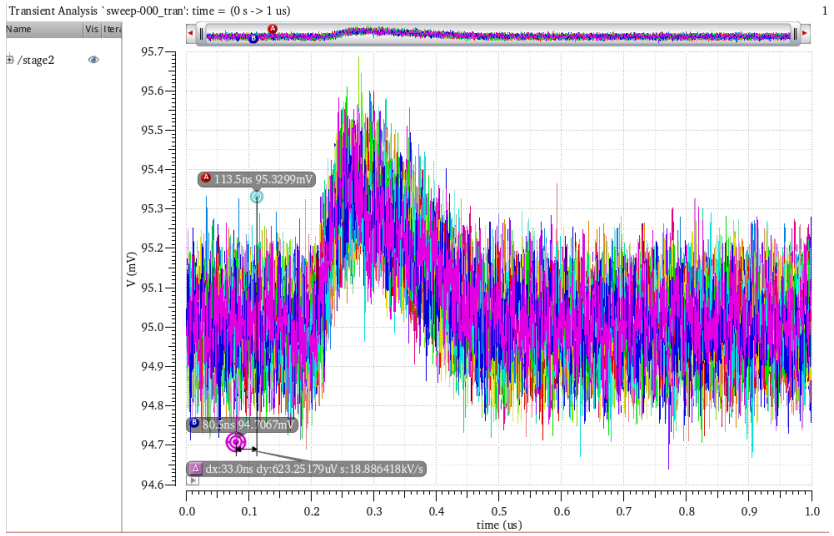


2025.02.18更新，本次流片先不考虑0.1~1MIP的信号

模块电路设计---Current Buffer



Current Buffer原理图



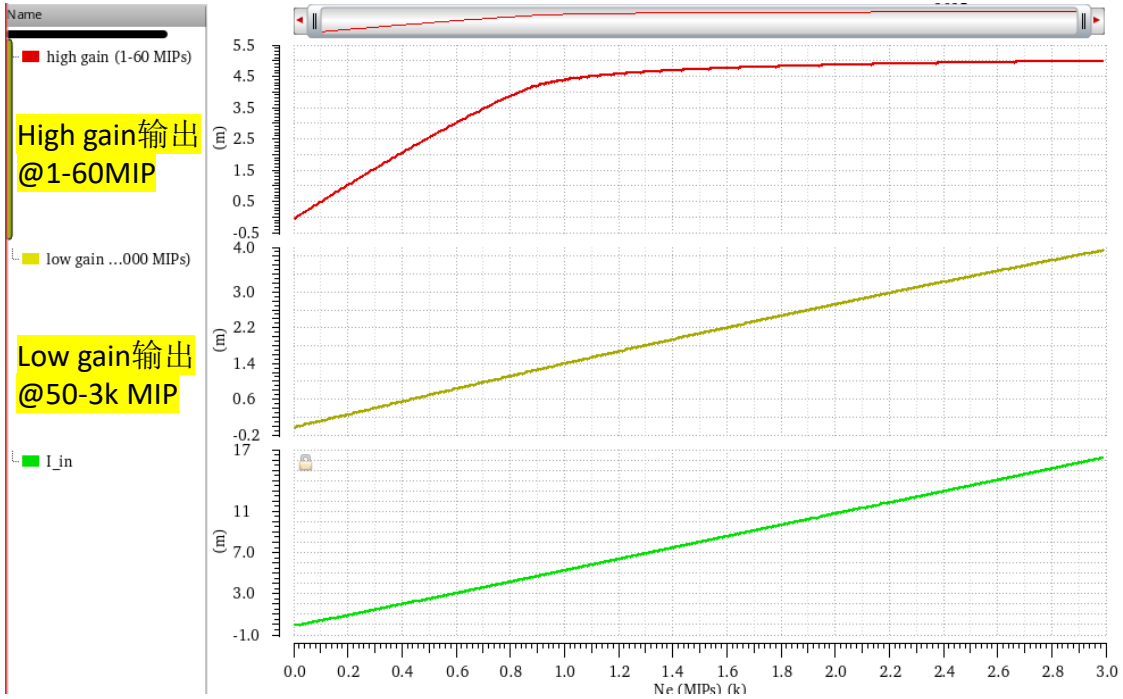
Current Buffer的噪声瞬态仿真（1MIP)

Current Buffer档#1的rms噪声为95 μV，等效为0.25MIP的输入，1MIP对应的信噪比为4，待进一步优化

两档设计，覆盖1-3000MIPs的动态范围

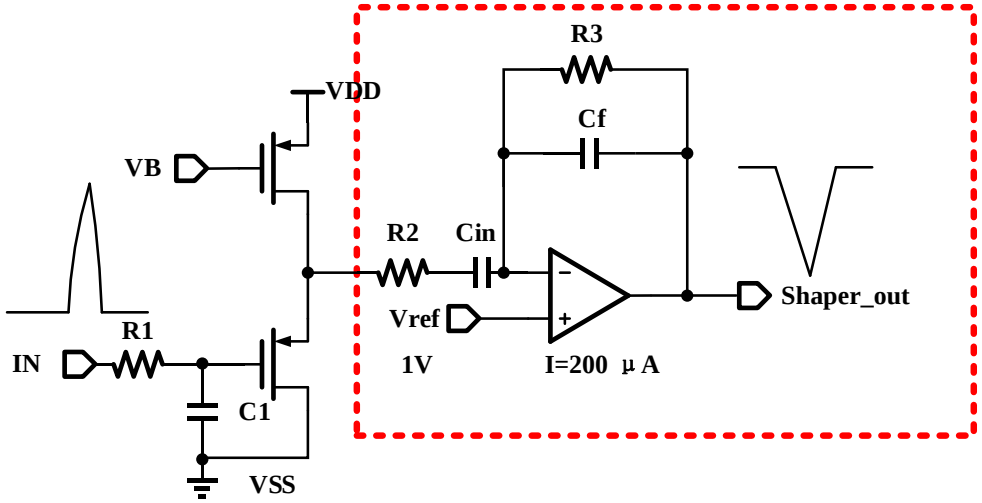
#1：1-60MIPs （60倍）

#2：50-3000MIPs （60倍）



Current Buffer的电流跟随能力仿真

模块电路设计---Slow Shaper

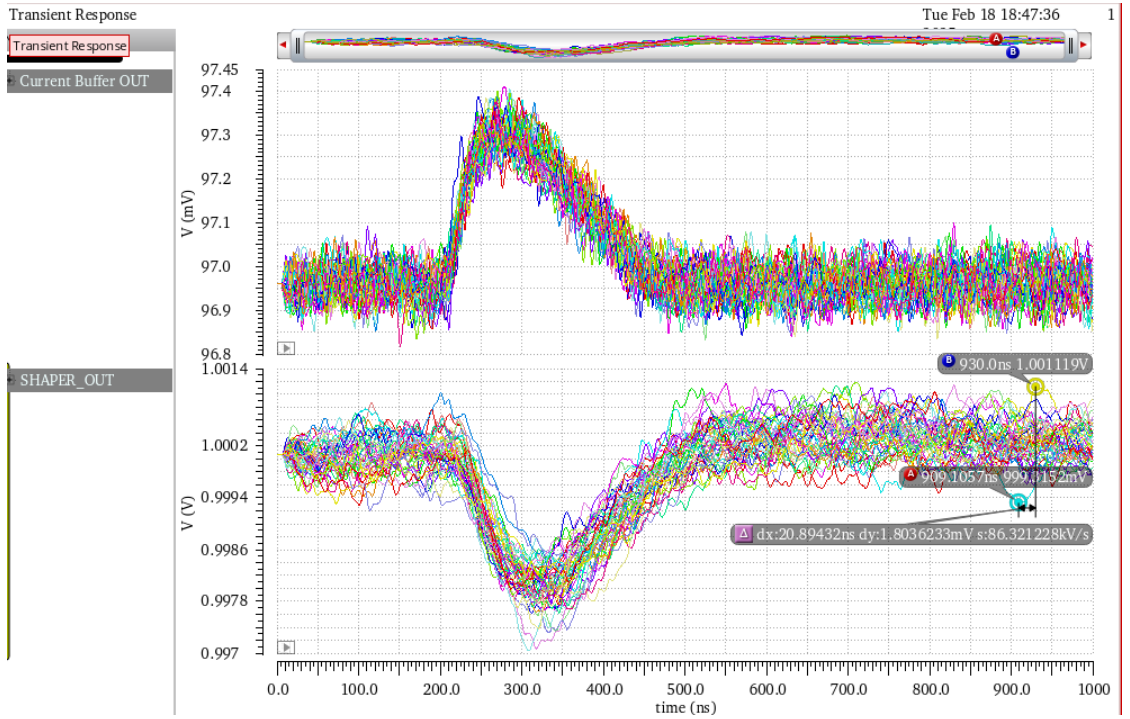


CR-RC² Shaper电路

$$H(s) = \frac{sR_3C_{in} * 0.8}{(1+sR_1C_1)(1+sR_2C_{in})(1+sR_3C_f)}$$

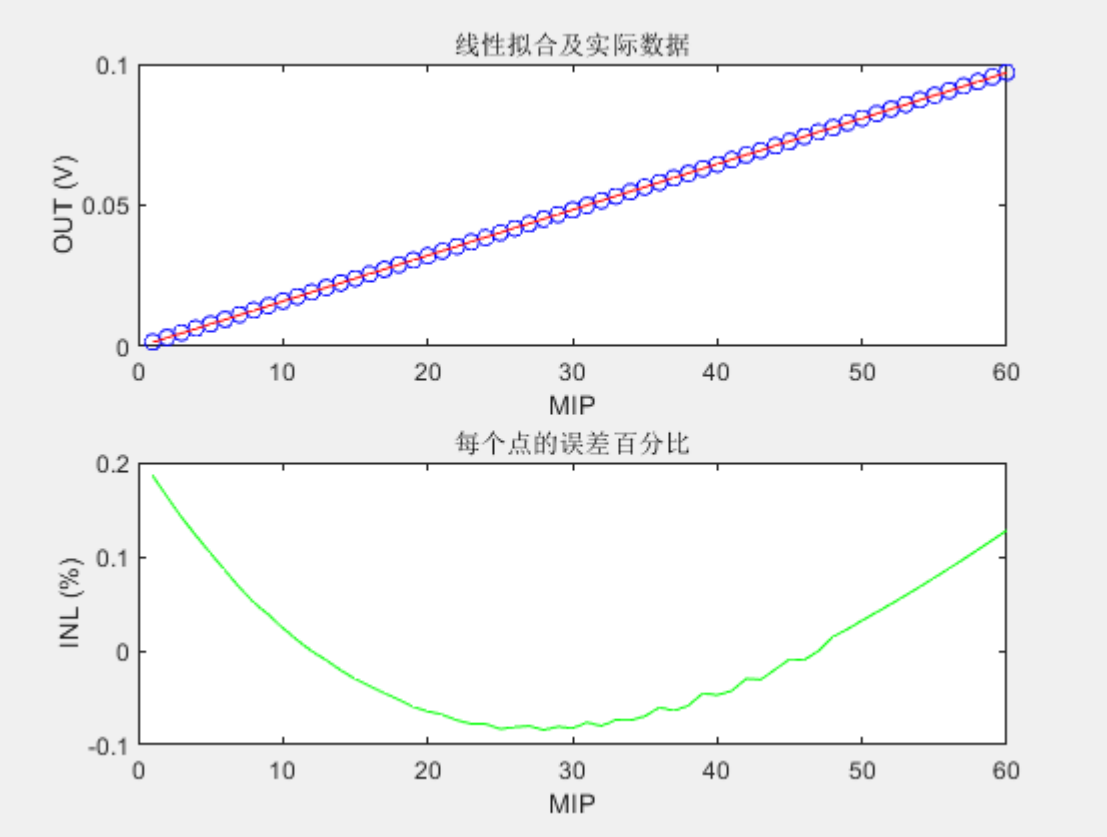
1-60 MIPs增益： 1.5mV/pC
50-3000 MIPs增益： 0.026mV/pC
shaper输出信号: Tp=120ns

下图为shaper的瞬态噪声仿真波形
shaper输出端的rms值为0.255 mV
等效到输入端为0.13 MIPs，信噪比约为7.4



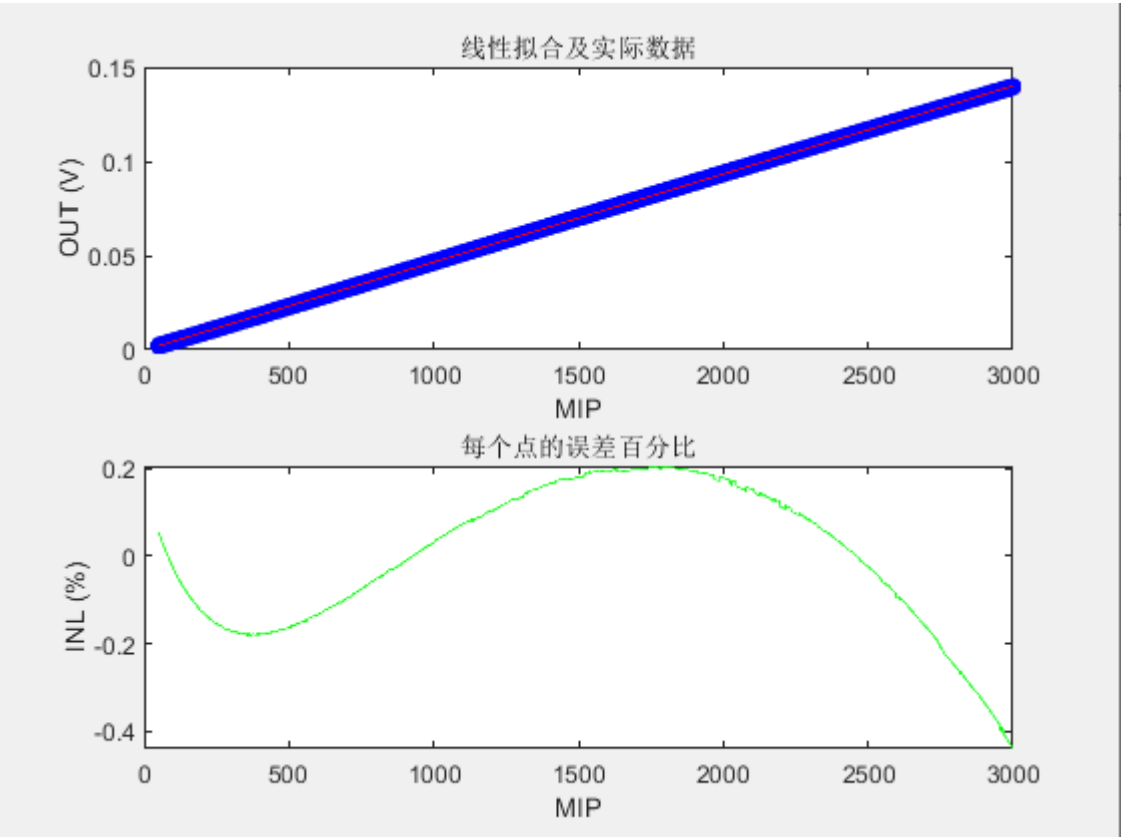
Shaper瞬态噪声@1MIP

模块电路设计---Slow Shaper



Shaper输出的INL（1-60 MIPs）

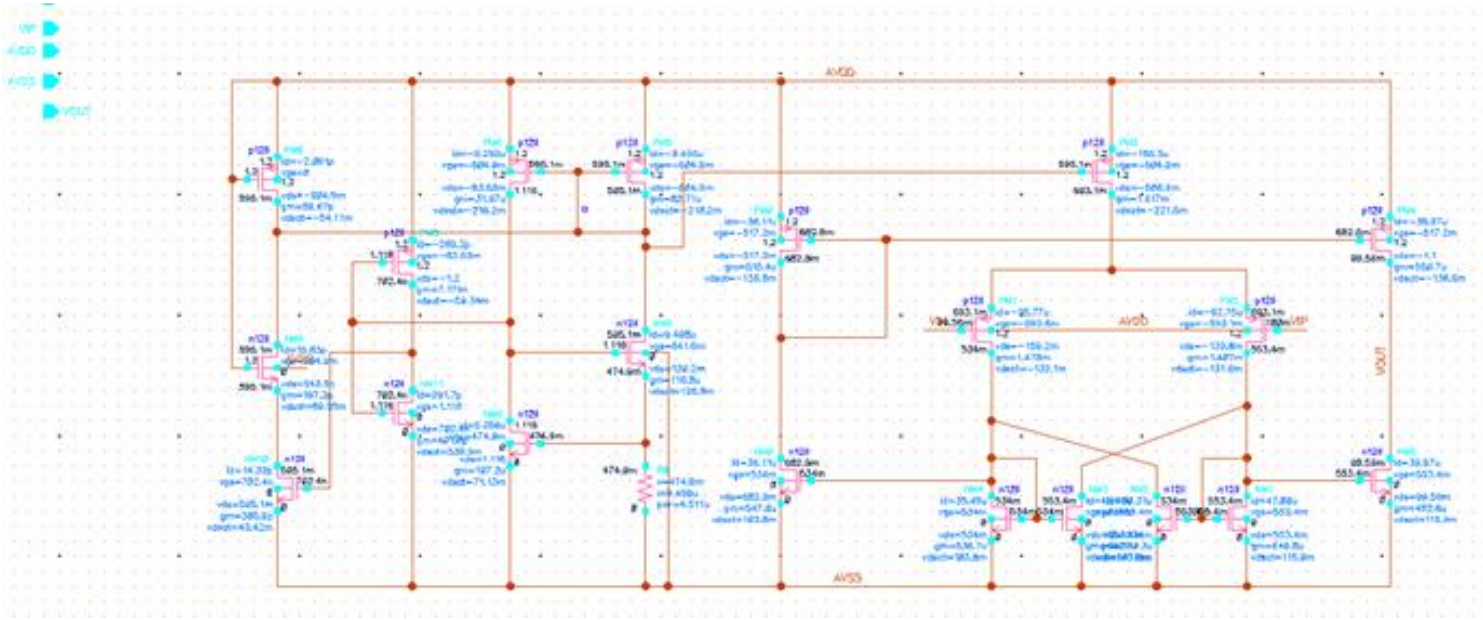
INL好于0.2%



Shaper输出的INL线性度（50-3000 MIPs）

INL好于0.4%

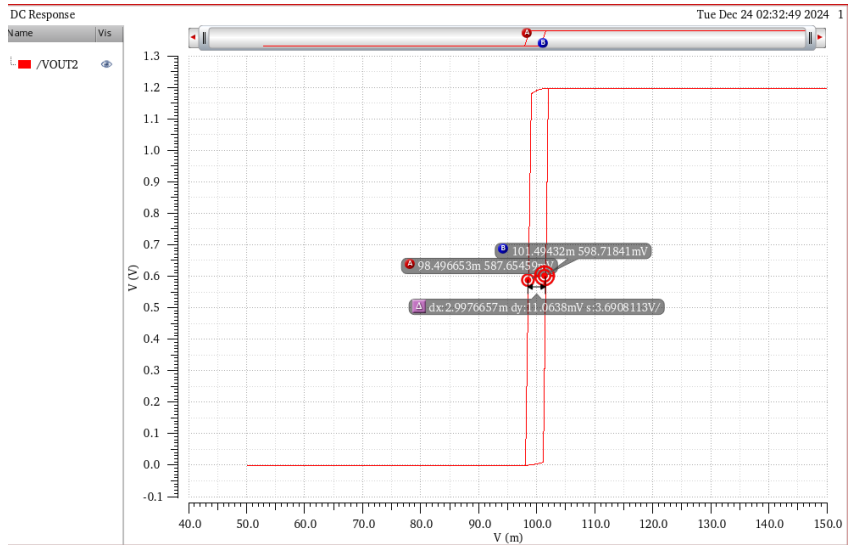
模块电路设计--discriminator



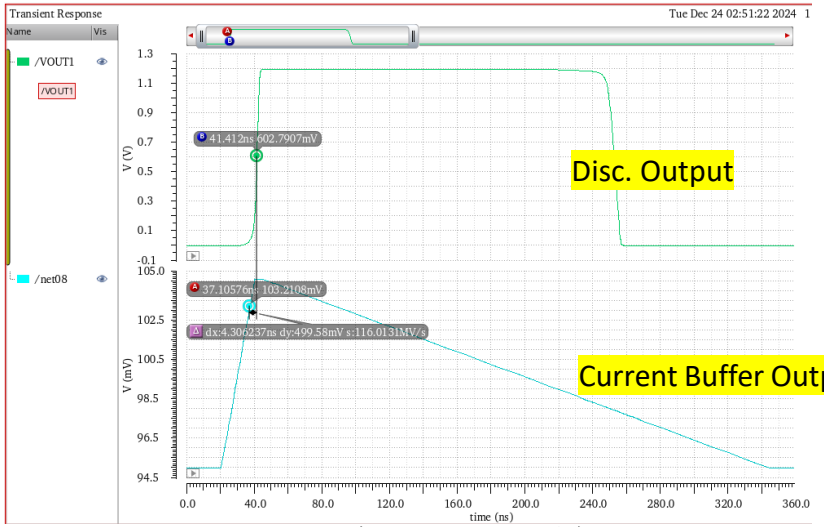
迟滞比较器（ 200 μA静态电流）

迟滞窗口： 3mV 即0.6 MIPs

Delay time： 4.3ns@2 MIPs

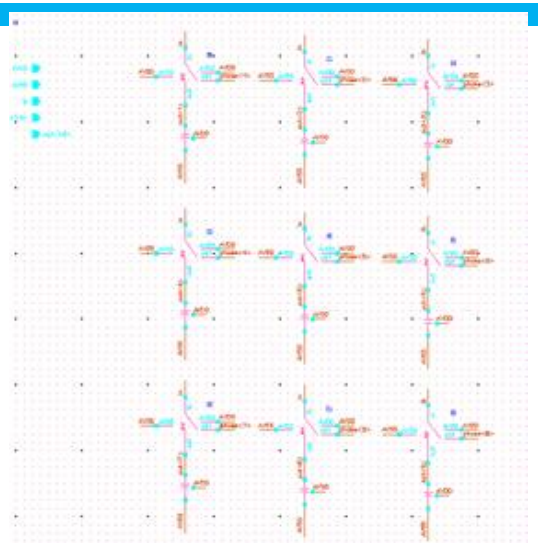


迟滞窗口仿真

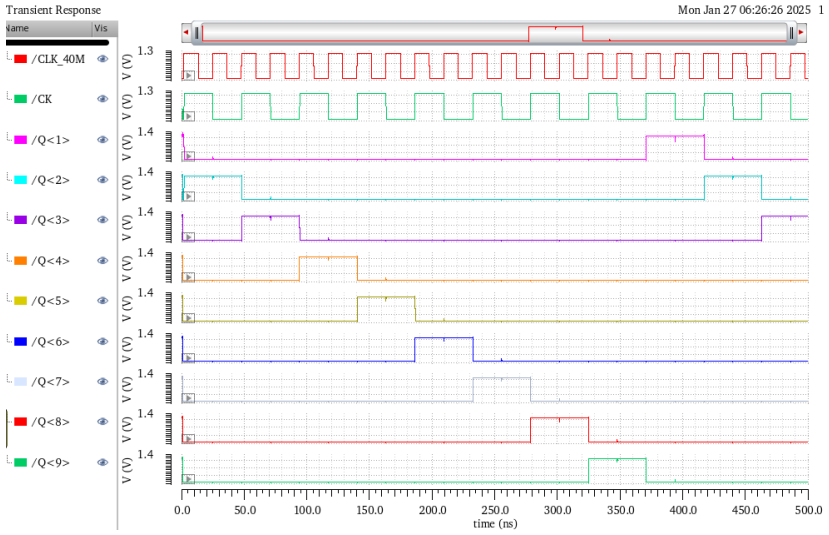


瞬态仿真@2MIPs输入

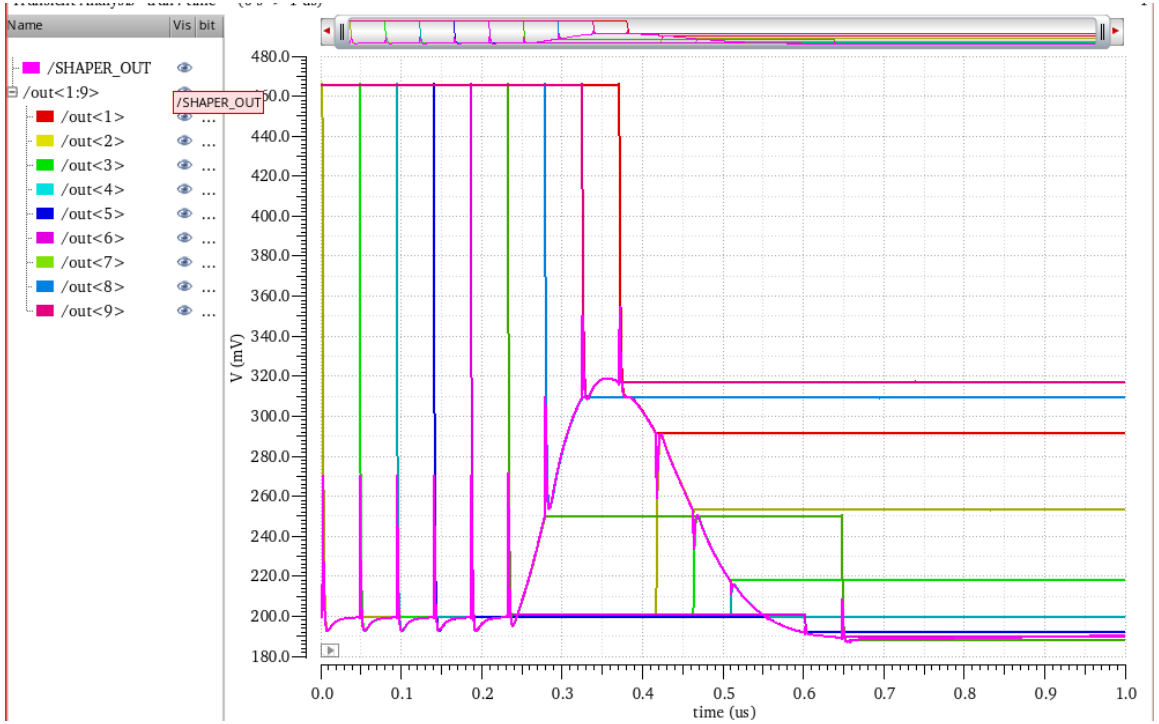
模块电路设计---开关电容采样



开关电容



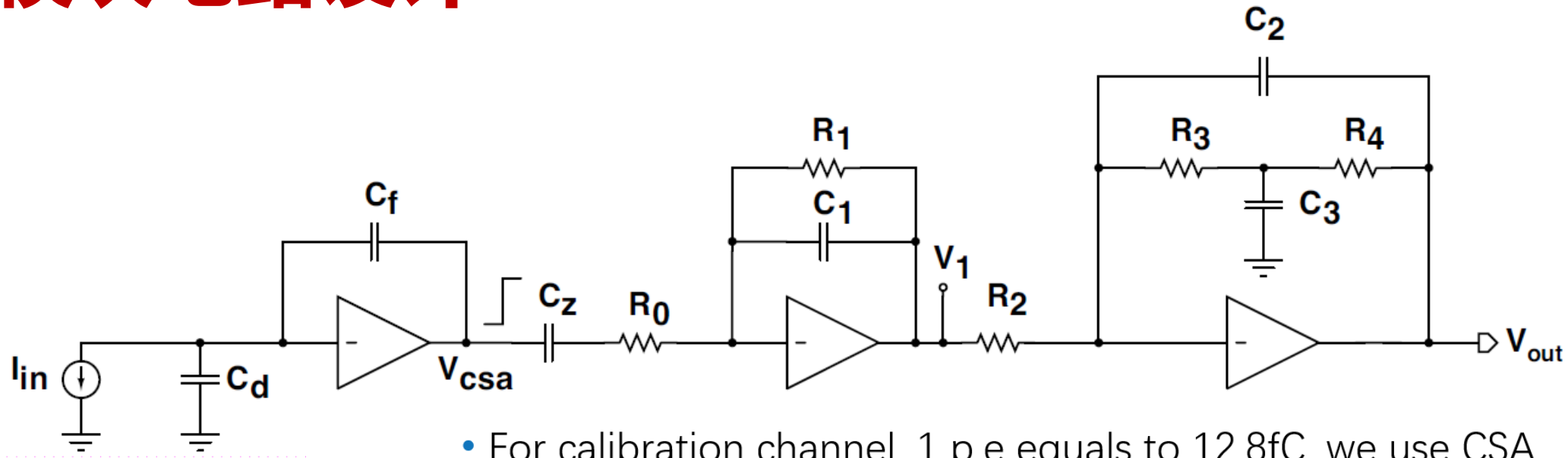
采样开关时序仿真



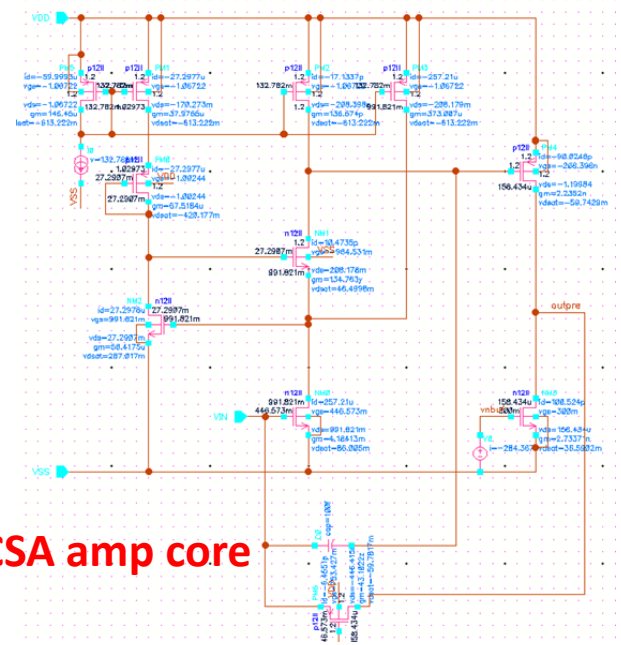
开关电容采样仿真

采样深度为9，采样频率约为20MHz；
前沿3个采样点，后延6个采样点
当检测到比较器输出的stop信号时停止采样，信号被保存在电容中由ADC量化

模块电路设计---calibration channel

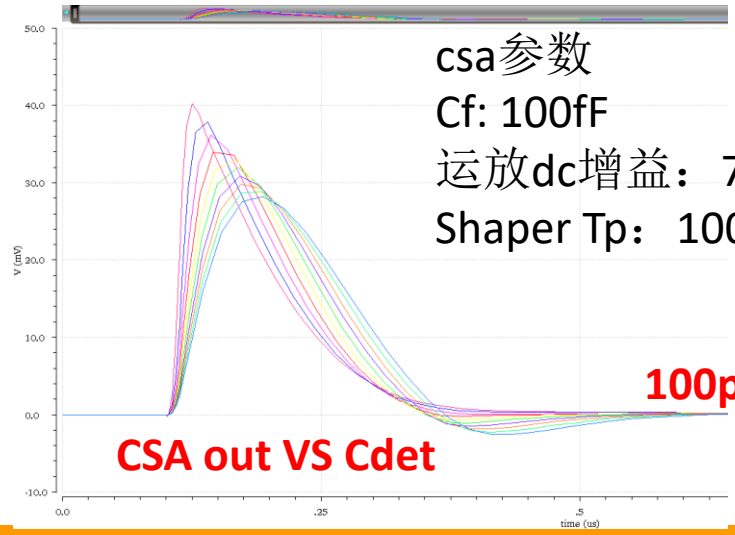


- For calibration channel, 1 p.e equals to 12.8fC, we use CSA
  - Set SNR to 10, then ENC=1.28fC
  - $C_d = 45.9pF$,



CSA amp core

探测器参数
sipm增益：10e5
1pe等效：16fC
单光子波形宽度：5~20ns
探测器电容：**100pF**



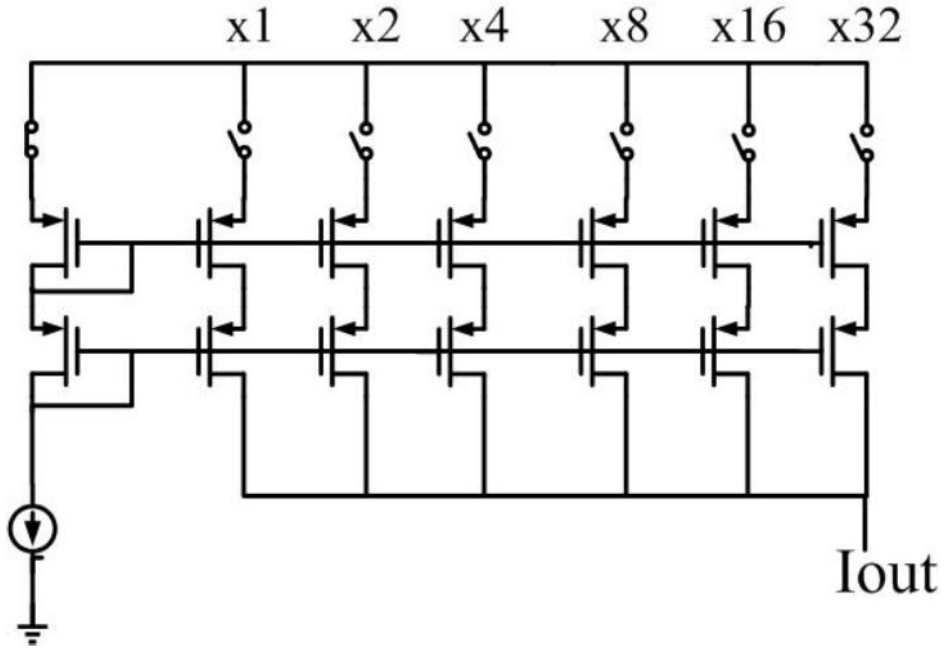
csa参数
Cf: 100fF
运放dc增益：70dB
Shaper Tp：100ns

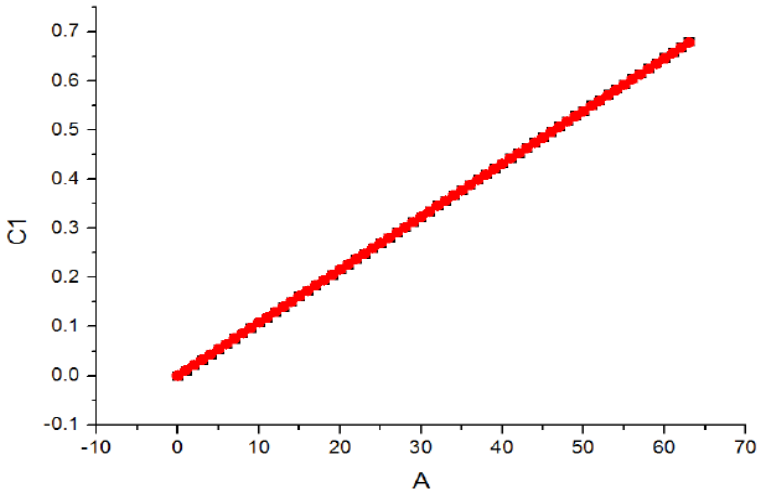
100pF信噪比10

CSA out VS Cdet

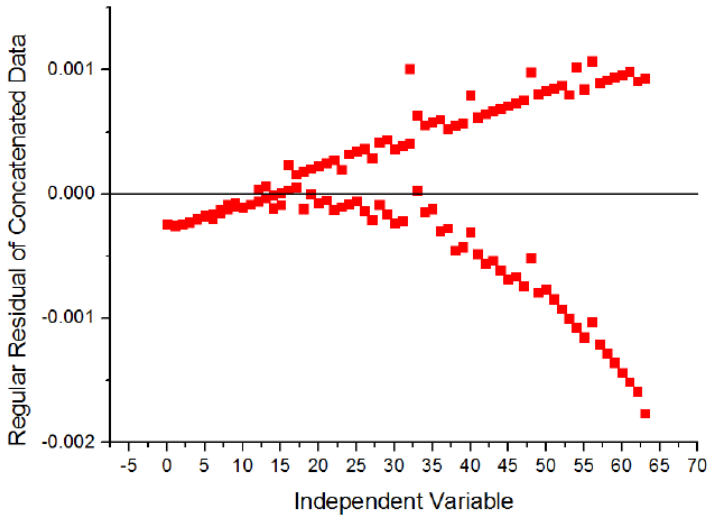
Tuning DAC for SiPM bias

- 6-bit Current DAC for SiPM bias
- Only for the bias of Current Buffer, no demand of speed
- LSB=4uA



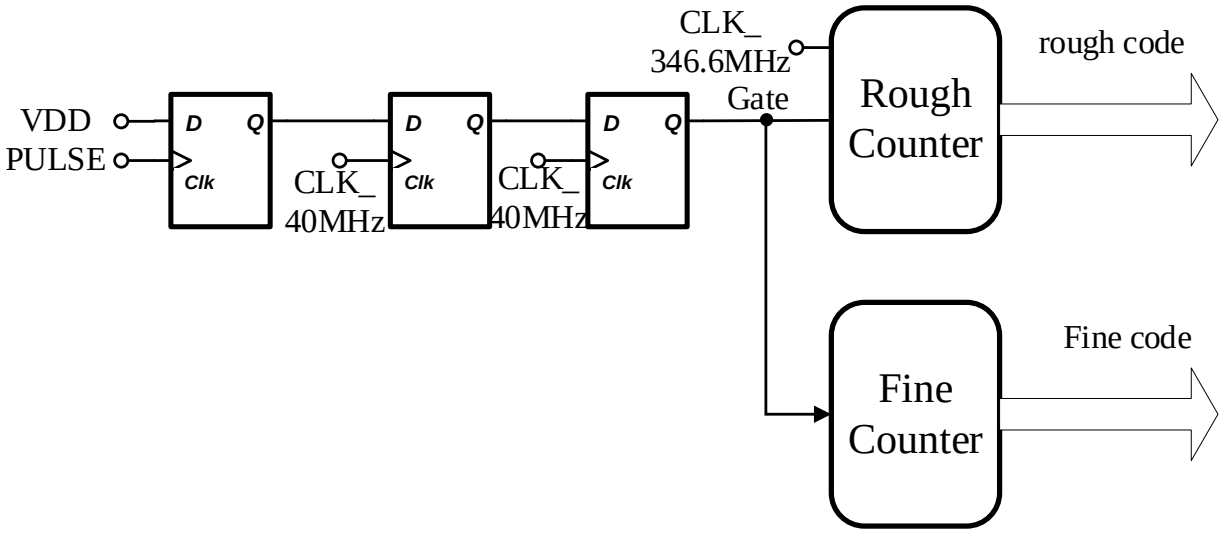


Voltage output @3KΩ

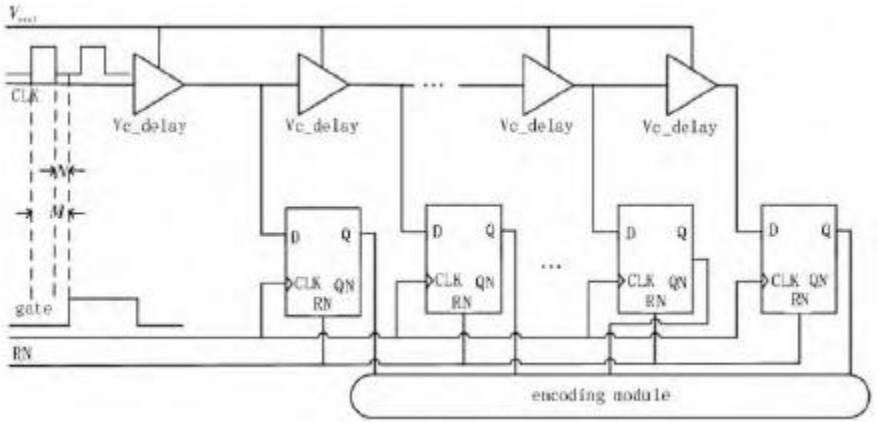


INL@3KΩ

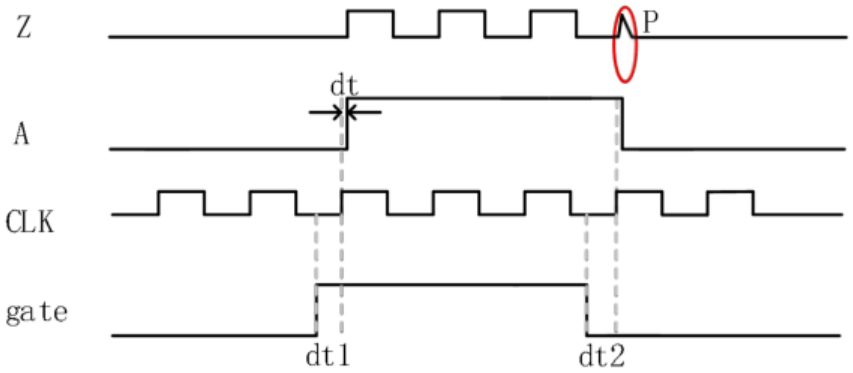
模块电路设计---TDC



TDC电路框图结构



延迟链结构



测量时序图

TDC按100ps的精度设计

采用两步式TDC结构

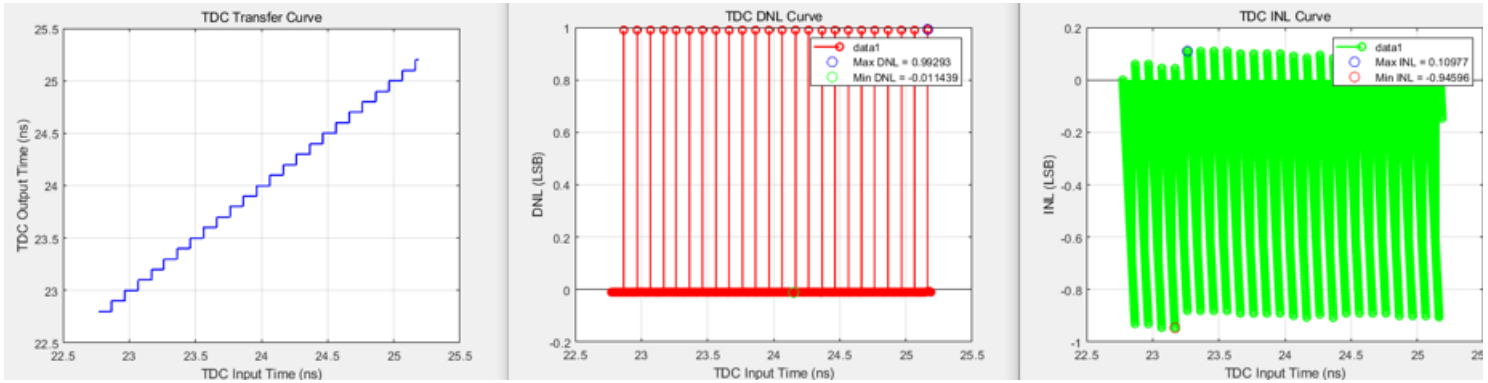
---粗计数由计数器进行测量

---细计数由延迟链进行测量

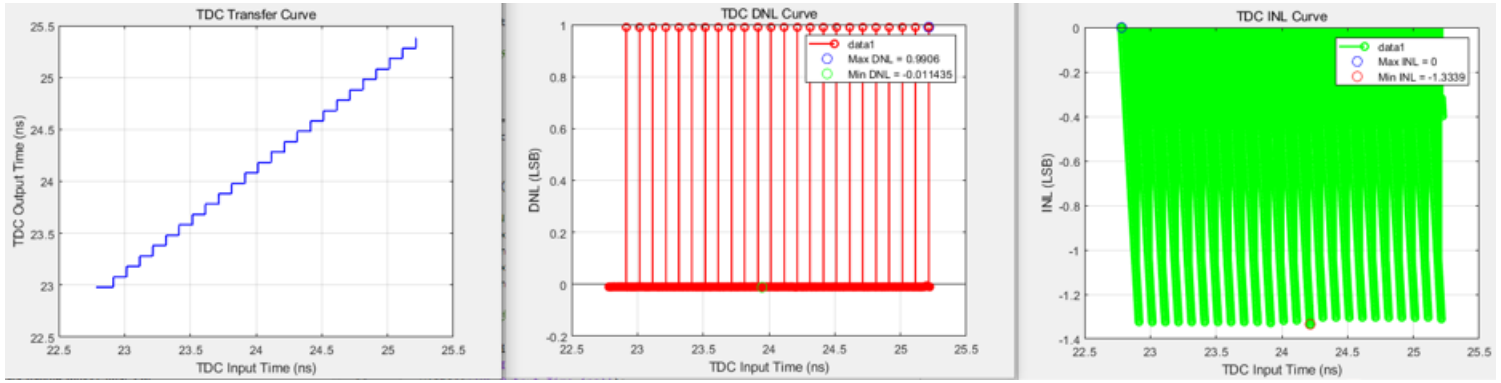
由细计数测量出少测量的时间和多测量的时间，最终得到总的输出

---总的时间T为粗计数时间+dt1-dt2

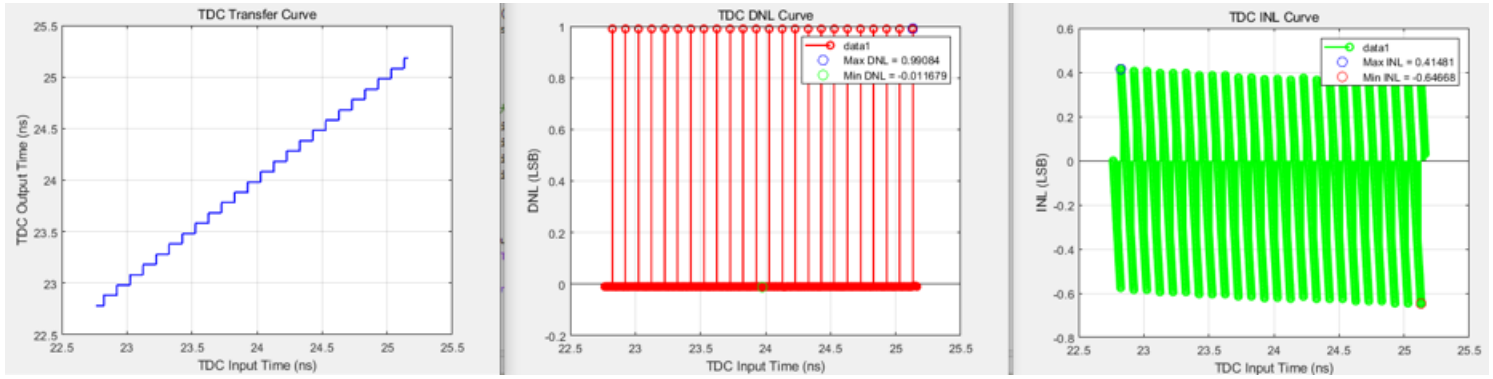
模块电路设计---TDC仿真



tt-27的转移曲线以及INL和DNL

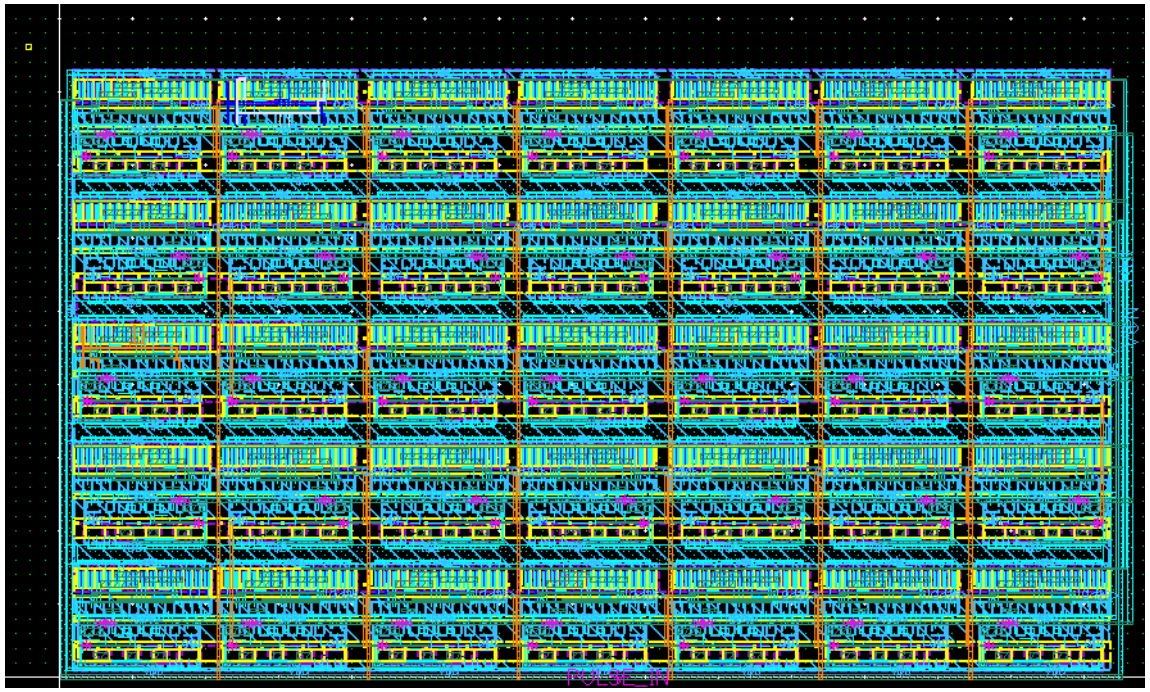


ss-40 的转移曲线以及INL和DNL



ff-85的转移曲线以及INL和DNL

模块电路设计---TDC layout & post-sim

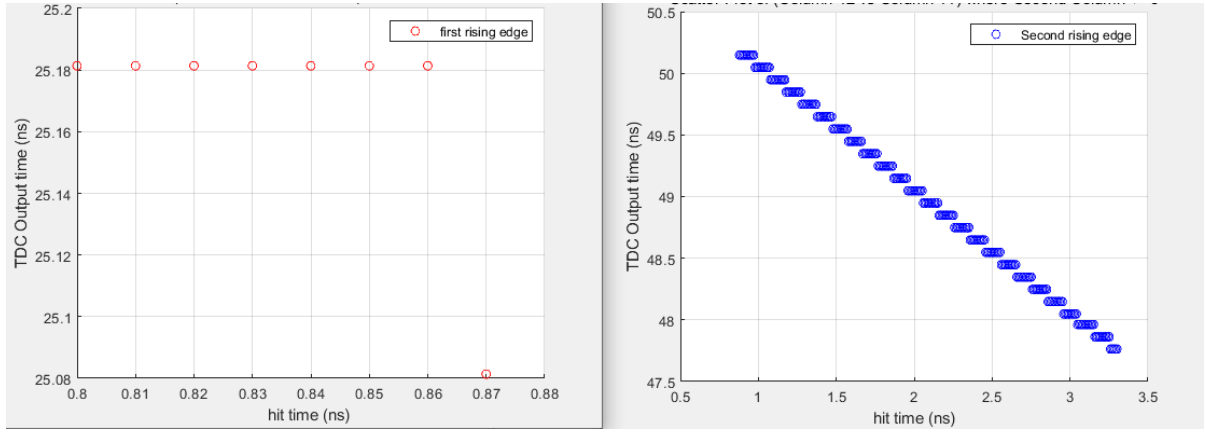


细计数部分版图

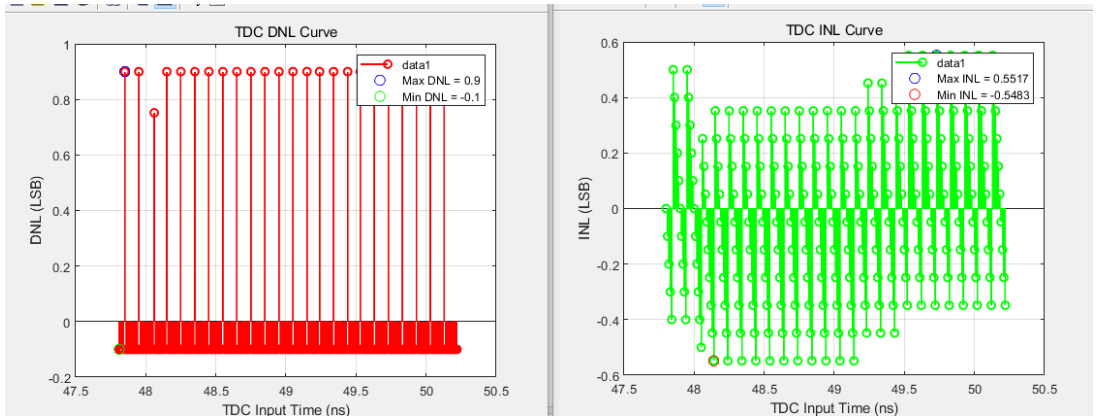
TDC在三个工艺角表现出的转移曲线均在设计的预期之内，三个工艺角最大的DNL为1.4LSB，其他的工艺角的INL和DNL均在1 LSB以下。TDC的细计数部分已经完成了版图设计，并进行了部分后仿真。

模块电路设计---TDC post-sim

– 细计数模块的layout决定了TDC的精度，因此对TDC进行了部分后仿真，以找到延迟单元合适的偏置电压以及确定layout是否影响了TDC的精度



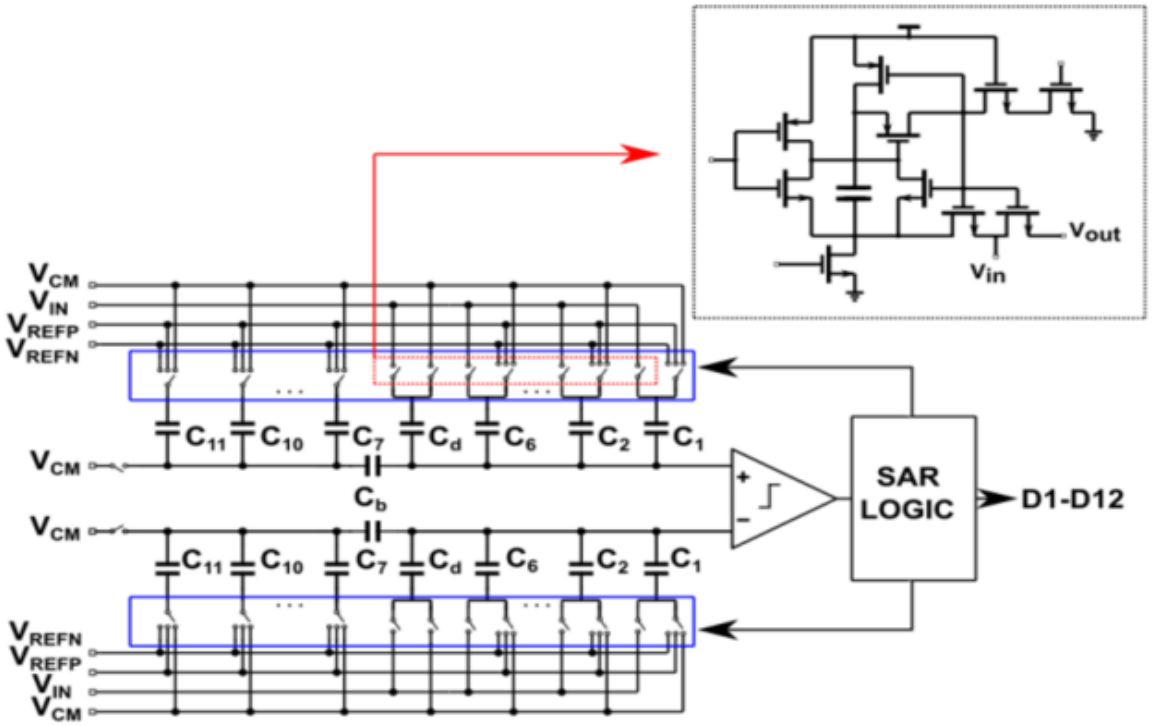
40M时钟下信号发生时间为0.8ns -3.3ns的TDC码字仿真@tt 27



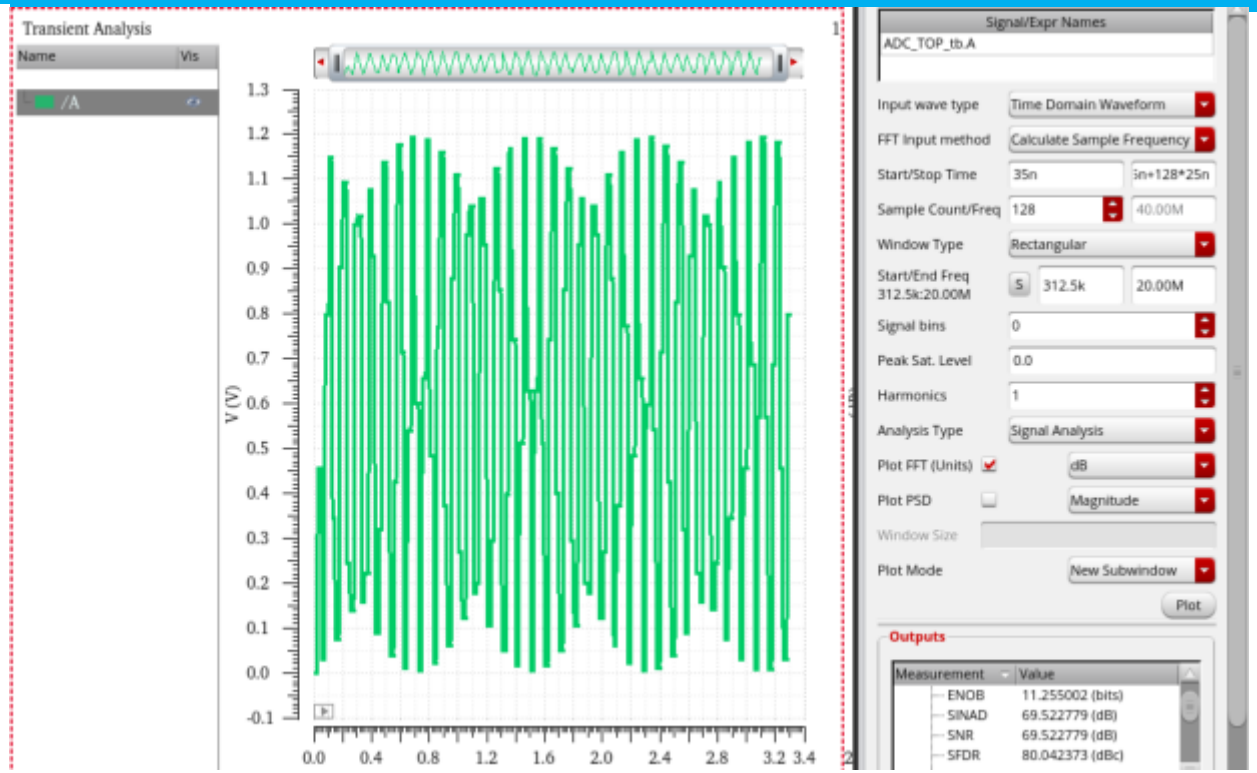
左图对应的INL和DNL

– 仿真结果表明，在延迟链采用后仿真参数的情况下，一个粗计数周期内的转移曲线的最大INL为0.55，最大DNL为0.9，证明该部分layout符合设计要求，ss，ff工艺角的数据正在仿真.

模块电路设计---SAR ADC



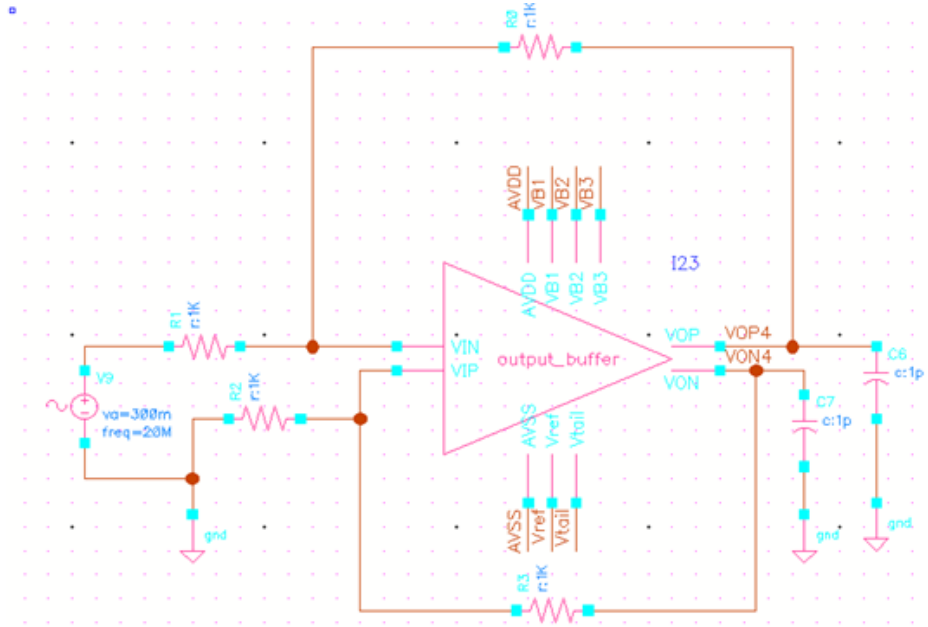
SAR ADC结构



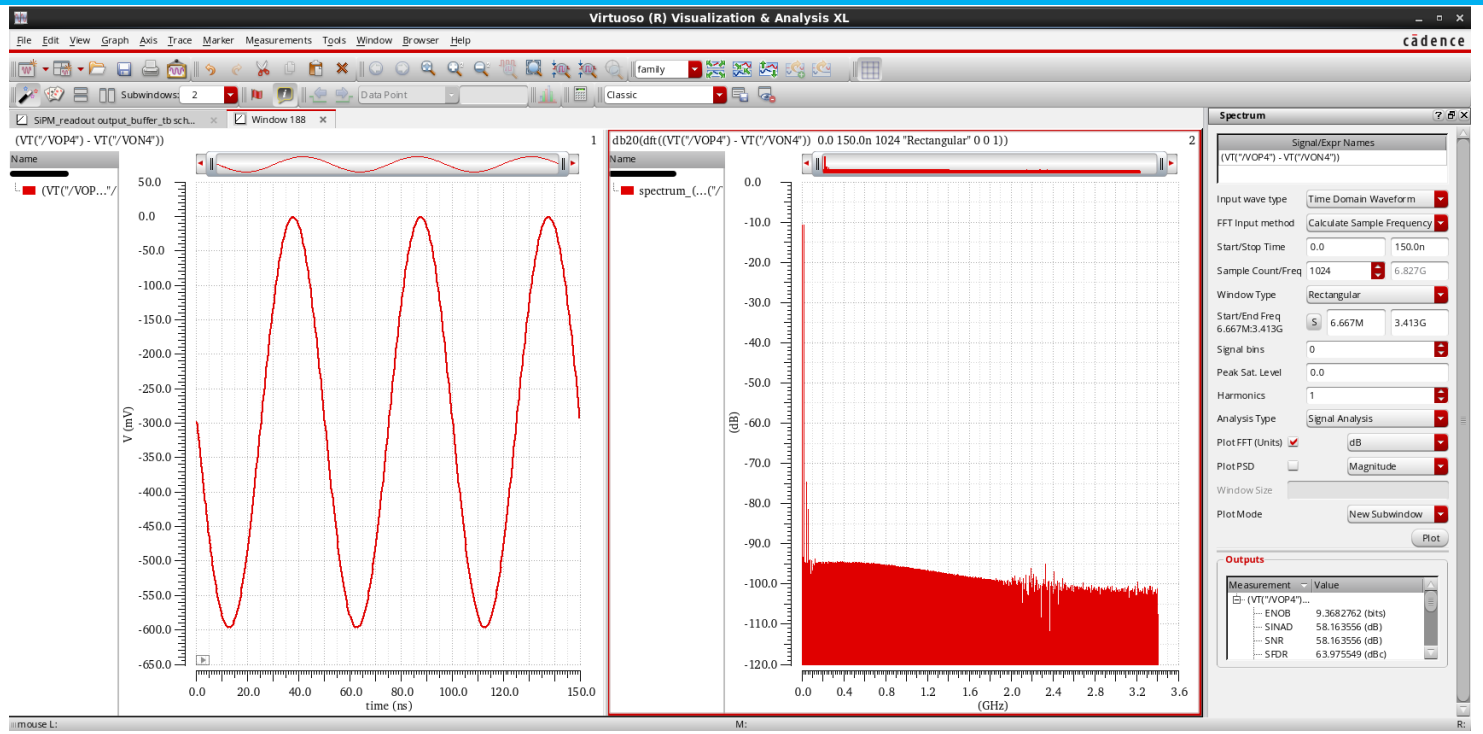
带噪声的ADC ENOB仿真
@40MSPS

ADC采用单级SAR结构，采用分段电容技术以及失调自校正技术，按照12位ADC来设计，目标最终的ENOB为10bit，在前仿有效位11.98bit，加$trannoise$噪声有效位为11.26bit，SNDR为69.52dB，SFDR为80.04dB，功耗为1.3mW，FOM值为20fJ。

模块电路设计---单转差放大器



单转差电路原理图（two-step folded-cascode common source）



单转差放大器ENOB仿真（20MHz输入情况）

开关电容采样电路输出为单端信号，与ADC连接时，需要单端转差分

按照20MHz为最大输入频率，输出ENOB目标为9bit

前仿真：Gain为50dB, 单位增益带宽1.3GHz，相位裕度78度，功耗9-10mA，ENOB为9.36bit

模块电路设计---Encoder考虑

- 数据量计算
  - 芯片包括4个通道
  - 每通道1个TDC，单个TDC的数据为72bit
  - 4通道共用1个ADC，电容采样深度为9，每通道2档，数据为72bit
  - TDC+ADC总数据为72bit*4+72bit=360bit
  - 按500KHz事例率考虑，信号需要在500KHz条件下传到后端，因此输出时钟的最低频率为180MHz
  - 加上帧头/尾、通道编码，拟采用346.4MHz的时钟传输数据
- 采用数字模块设计encoder以及serializer串行输出

整体进度

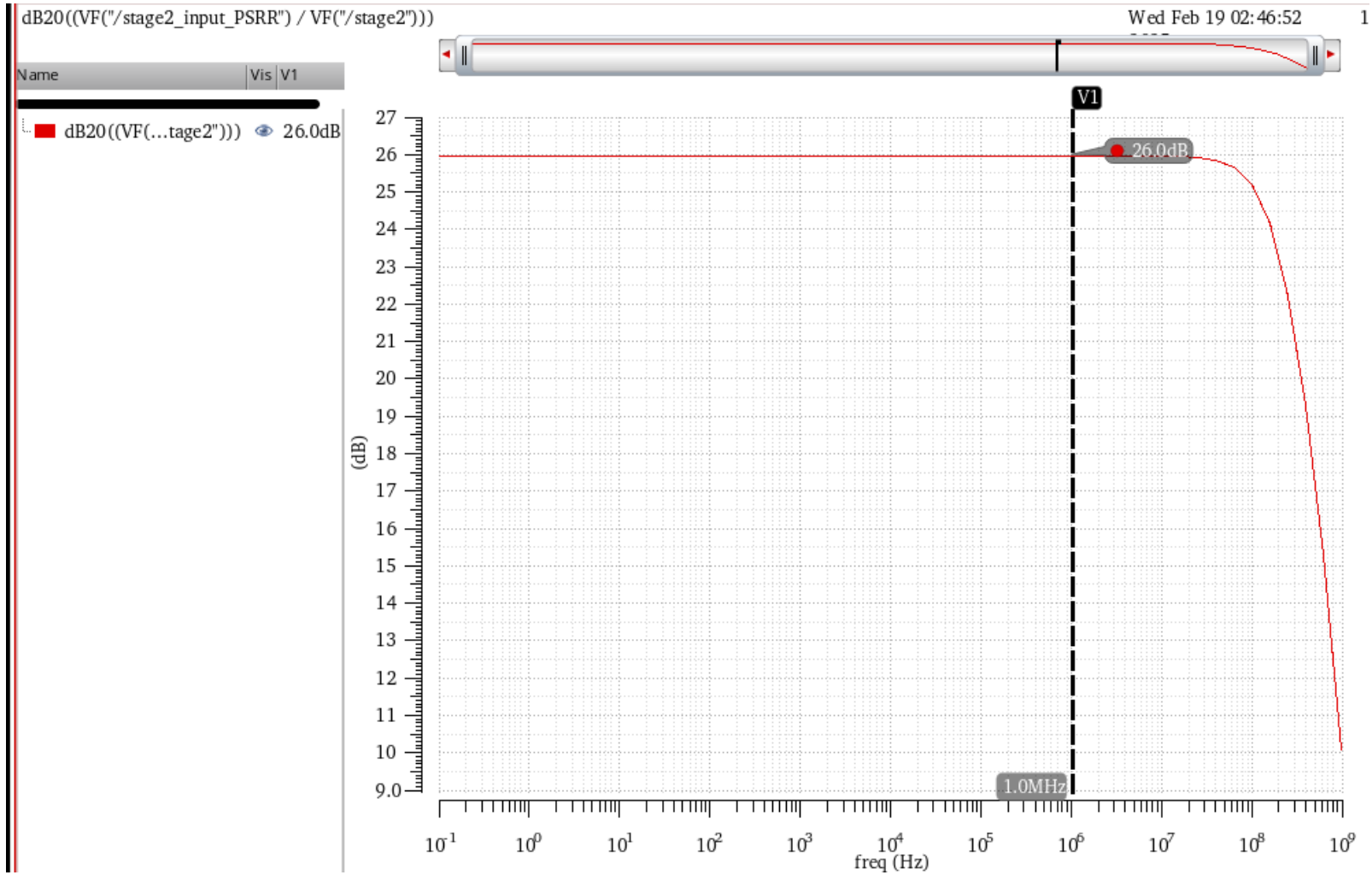
- ASIC各项指标参数已经确定
- 电路设计
  - Current Buffer、slow shaper、discriminator：前仿真完成
  - 开关电容采样电路：前仿真完成，与模拟部分的联合仿真完成
  - Calibration CSA/shaper：前仿真完成
  - Tuning DAC：前仿真完成，暂未与Current Buffer联调
  - TDC模块：前仿真，细计数部分的后仿真
  - ADC模块：前仿真完成，暂未联合仿真
  - 单转差放大器：前仿真完成，暂未联合仿真
- 4月份流片计划
  - 各关键模块的验证、4通道芯片的验证

Backup Slides

时间窗为bunch spacing 346 / 69 / 23 ns 阈值为0.1mip			平均计数率 [KHz/cell]	最大计数率 [KHz/cell]	最大占空比 [%]
带有4cm W以前的结果	ECAL Barrel	Higgs	4	87	---
		LZ	43	1,130	---
	ECAL Endcap	Higgs	9	469	---
		LZ	66	1,368	---
15mm不锈钢	ECAL Barrel	Higgs	11	424	0.57
		LZ	15	335	0.29
		HZ	77	2,104	0.29
	ECAL Endcap	Higgs	45	2,870	2.4
		LZ	65	6,699	0.78
		HZ	334	34,528	1.1
	HCAL Barrel	Higgs	0.2	5.8	0.00046
		LZ	0.7	12	0.00018
		HZ	2.2	44	0.00018
	HCAL Endcap	Higgs	5.3	221	0.013
		LZ	8.2	249	0.00458
		HZ	53	2,148	0.0085
15mm Ti+W	ECAL Barrel	Higgs	7	172	0.44
		LZ	11	212	0.16
		HZ	54	1,065	0.2
	ECAL Endcap	Higgs	23	1,746	1.74
		LZ	35	2,408	0.39
		HZ	187	15,209	0.57
	HCAL Barrel	Higgs	0.2	3.5	0.00052
		LZ	0.7	12	0.00012
		HZ	2.1	35	0.00015
	HCAL Endcap	Higgs	3.8	129	0.0084
		LZ	6	157	0.0037
		HZ	40	1,338	0.0063

Ref: https://indico.ihep.ac.cn/event/24786/contributions/178099/attachments/87639/112878/BIB_CAL_1.24.pdf

Current Buffer PSRR



频率小于10MHz时，PSRR为26dB（1/20）

按照电源纹波3mV@1-3MHz估算

---等效到输入端的电压为150uV

---CurrentBuffer的等效输入噪声为0.25MIP（1uA），等效为200uV

进一步优化该模块的PSRR