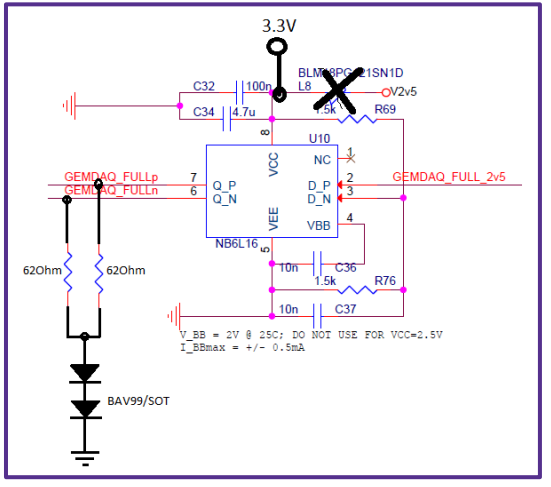
Status at Feb 24

- Recovered GEMROC 7 and tested
  - transceiver port was broken, now ok!

- Test of the full
  - FULL levels have separation also when connected to MTI board after changing the active termination network at FANOUT side to adjust the output levels to 1.6 V (high) and 1. V (low)
  - Change from 2.5 V to 3.3 V power supply of the fanout pECL driver, now levels are 2.3 V (high) and 1.8 V (low)
  - GUO Wenxuan verified that the signal is received by the MTI board
  - Changed something in the software (the FULL was masked?)
  - Differential lemo cable had inverted polarity, recovered to get direct polarity
  - Now FULL is working!



Thanks to DONG Sheng we can also prepare the spare fanout with the same scheme

Status at Feb 24 - II

- CHECK signal and data synchronization
  - It is our first priority now
  - In our understanding, CHECK signal arrives after the trigger –> Q: The 256th trigger, right?
  - Angelo modified the FANOUT firmware to take into account this in the logic
    - Originally we were told that the CHECK would arrive during the 256th trigger
  - Test is on-going with spare fanout first and then we will move to the “operation” fanout module. Plan is to test after dinner
  - After this test we can proceed to take data together

- Database for threshold
  - We shared the information of how the threshold are stored in GUFI with Tingxuan

Status at Feb 24 - III

- DAQ with GEMDC
  - We are focusing some effort on testing GEMDC1
  - Connect one-by-one the fibers of the GEMROCs and use Tingxuan's programs to acquire data
  - Two set of tests:
    - "Empty" packets tests
      - We configure channels to not transmit data, so only HEADER, TRAILER and UDP COUNTER are transmitted
    - "Standard" packets tests
      - Set the standard threshold and transmit data
  - Some results:
    - With "empty" packets we are able to acquire data with 9 GEMROCs
      - the remaining two are yet to be tested
    - With "standard" packets we successfully acquire data with 6 GEMROCs
      - Some more tests are planned
    - Some difficulties in achieving the interrupts are still present
    - Some discrepancy between the number of trigger recorded by GUFI and by the DCTest program
  - We keep Pawel updated, he prepared a small fimware fix

- Latency and delay
  - Q: We were told that the latency of L1 is 6.4 us, but from our readings it seems that is more close to 7.4 us. Are we missing something?

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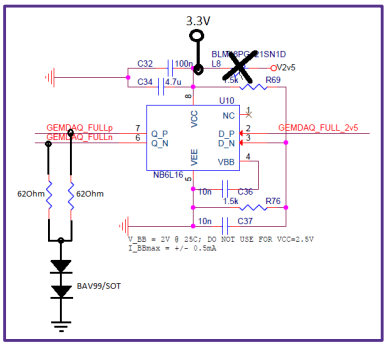

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