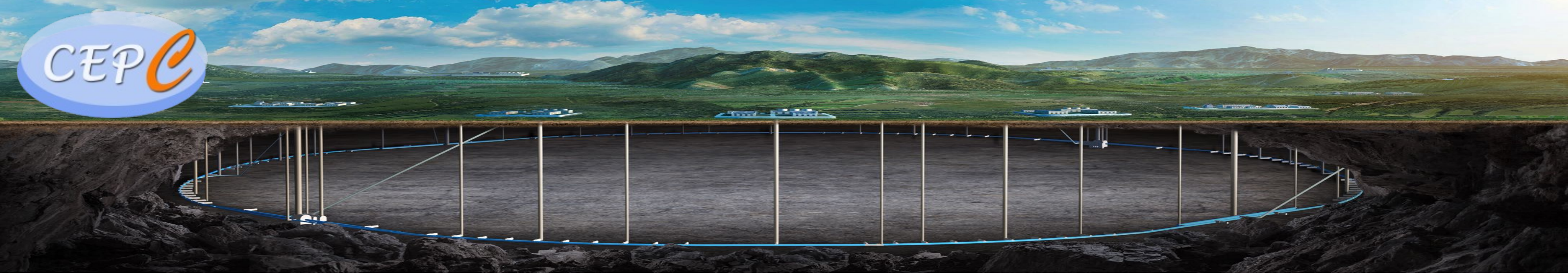

CEPC vertex Detector

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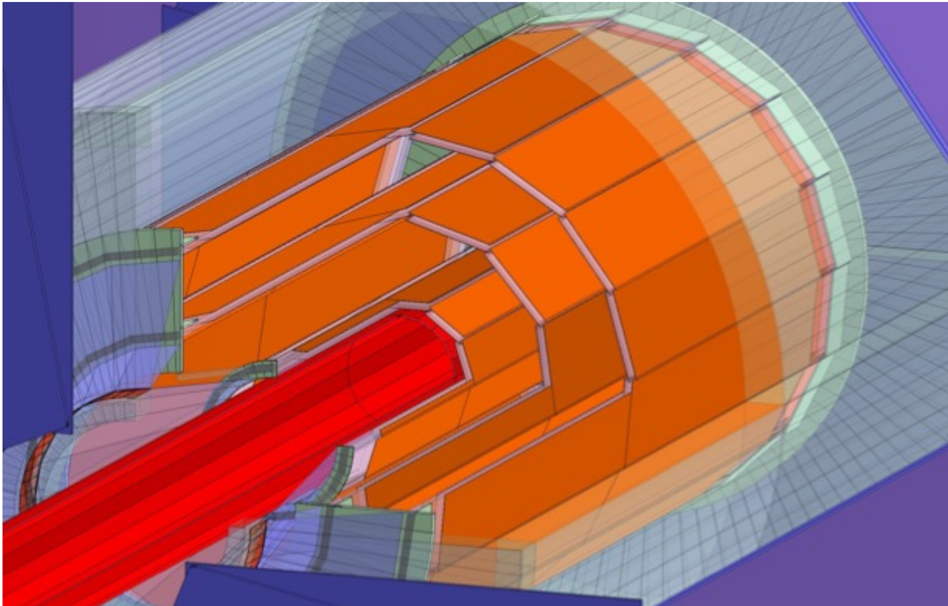
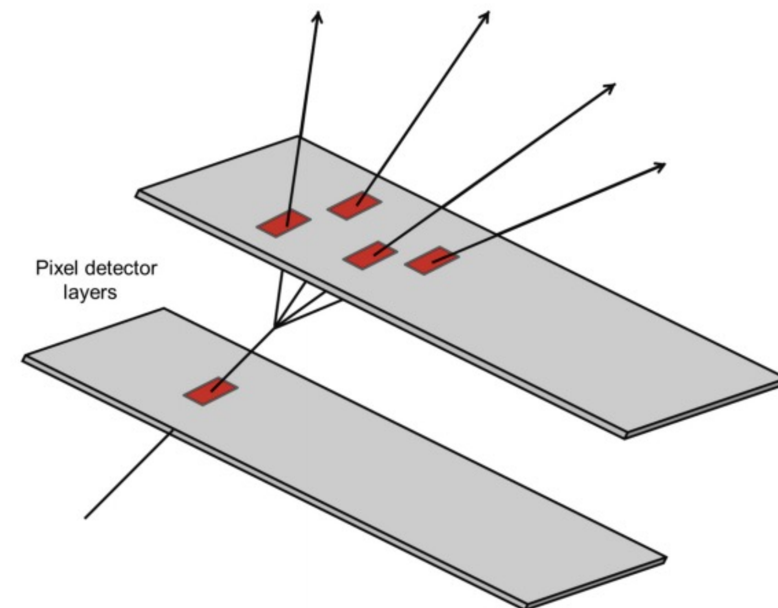
Content

- Introduction
- Requirements
- Technology survey and our choices
- Technical challenges
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics & BEC
- Performance from simulation
- Research team and working plan
- Summary

Introduction: vertex detector

- Vertex detector optimized for first 10 year of operation (ZH, low lumi-Z)
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for H → cc and H → gg physics, which is an important goal for CEPC





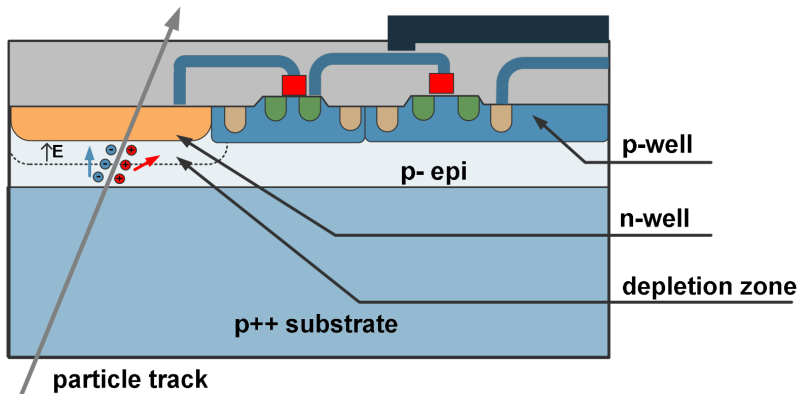
Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)
- High data rate: (especially at Z pole , ~43MHz, 1Gbps per chip)
  - **Challenges**: 1Gbps per chip high data rate especially at Z pole
- Low material budget (less than 0.15%X0 per layer)
- Detector Cooling with air cooling (power consumption<=40 mW/cm^2)
- Spatial Resolution (3-5 um)
- Radiation level (~1Mrad per year in average)

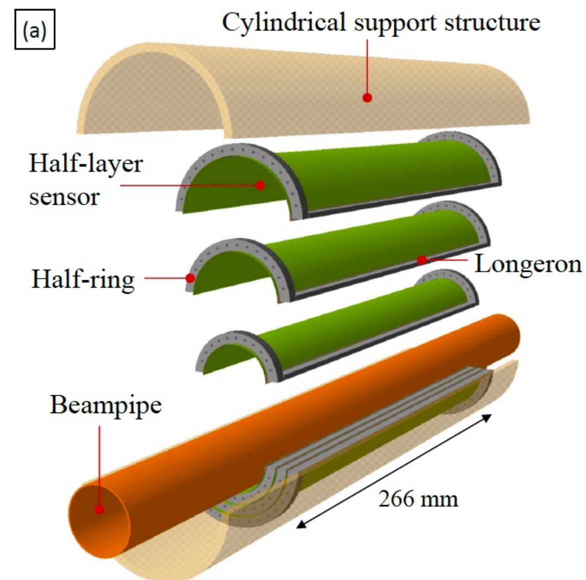
Technology survey and our choices

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

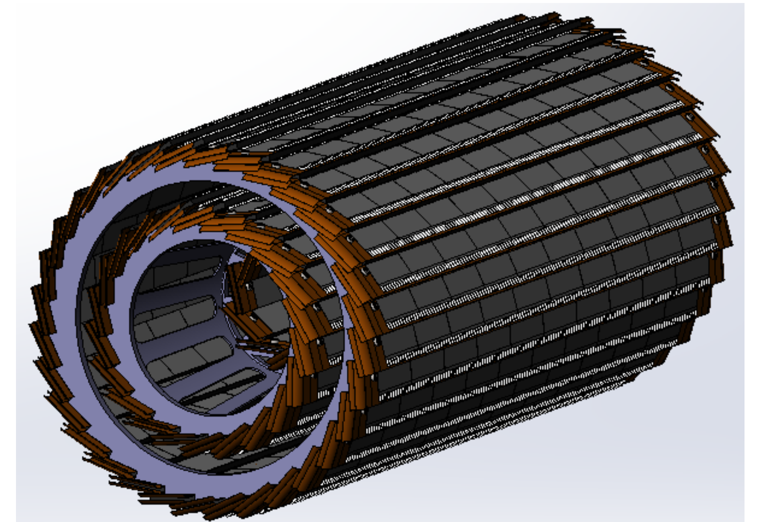
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS



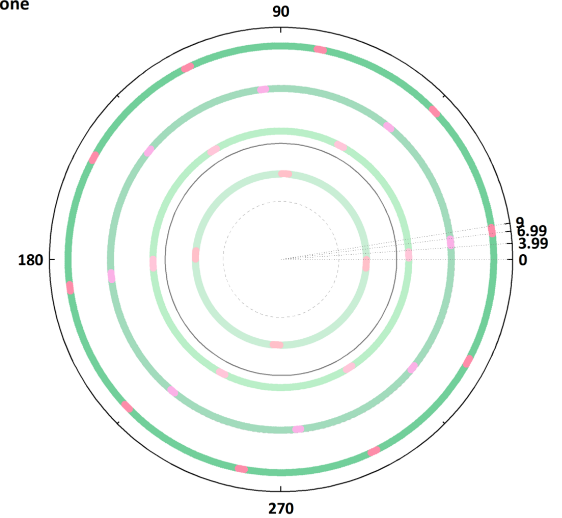
Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Baseline: bent MAPS

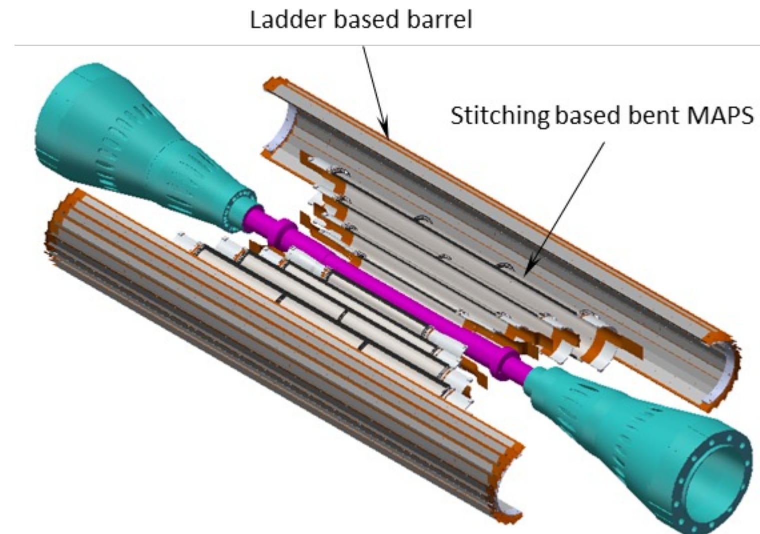
– 4 single layer of bent MAPS + 1 double layer ladder
  • Material budget is much lower than alternative option
– Use single bent MAPS for Inner layer (~0.15m^2)
  • Low material budget 0.06%X0 per layer
  • Different rotation angle in each layer to reduce dead area

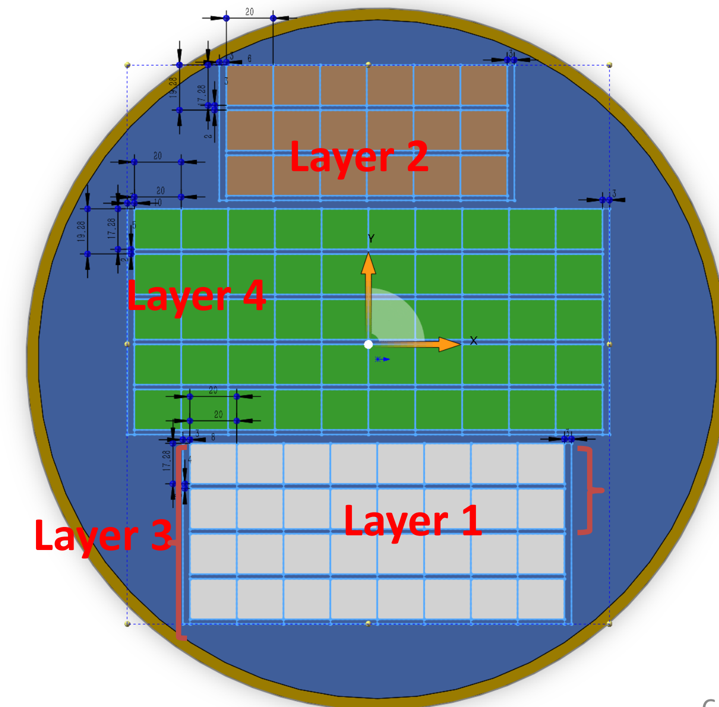


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Long barrel layout (no endcap disk)
to cover cos θ<=0.991

layer	Radius	Material
Layer 1	11mm	0.06% X0
Layer 2	16.5mm	0.06% X0
Layer 3	22mm	0.06% X0
Layer 4	27.5mm	0.06% X0
Layer 5/6 (Ladders)	35-40 mm	0.33% X0
Total		0.57% X0



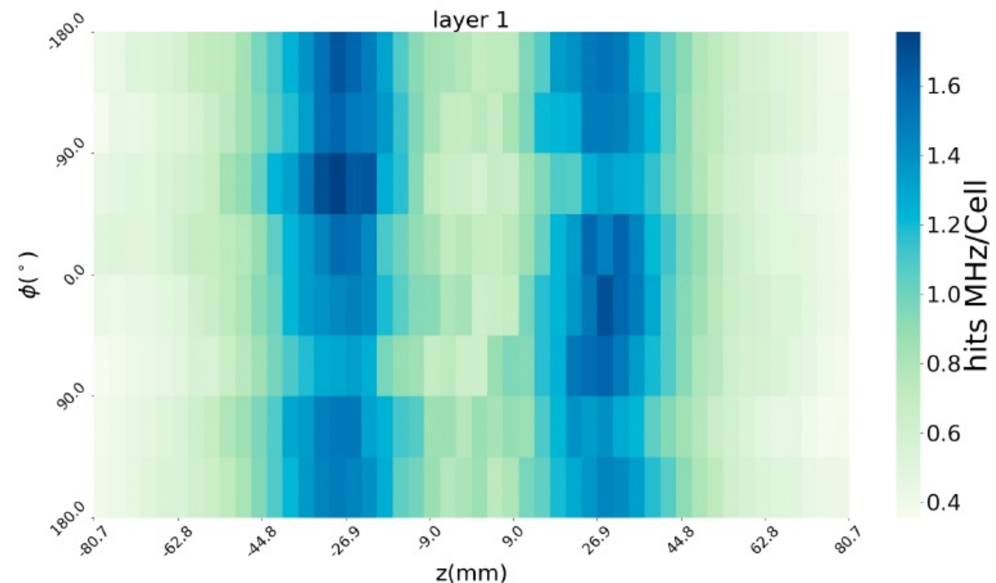


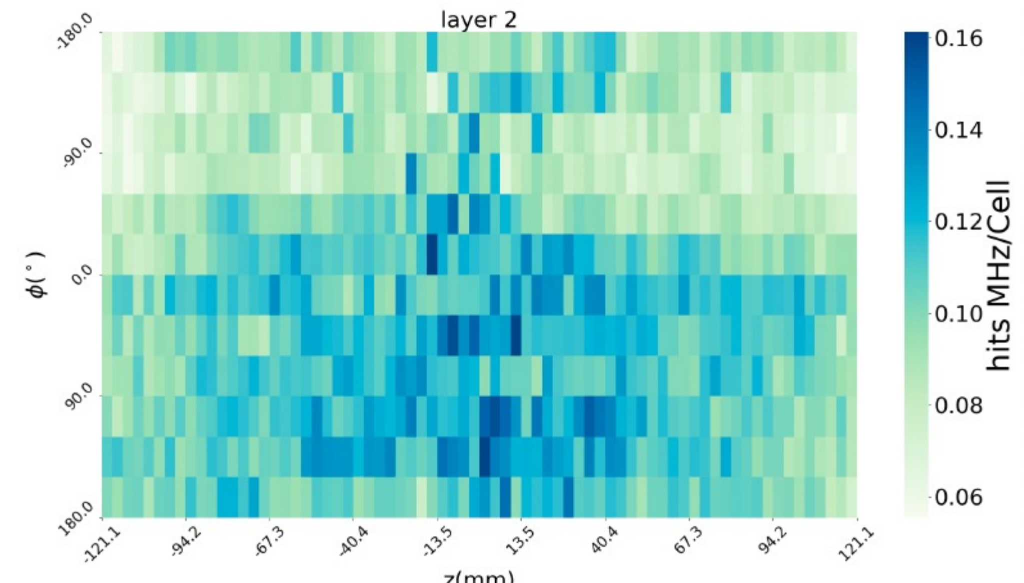
Data rate estimation of vertex detector

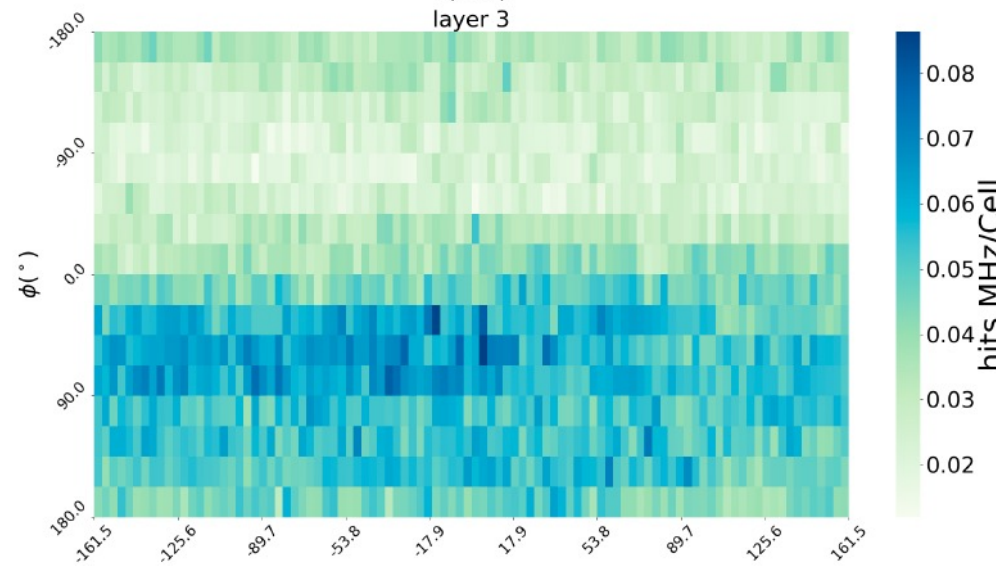
- Data rate @1.3Gbps/cm^2 per chip for triggerless readout at low-lumi Z

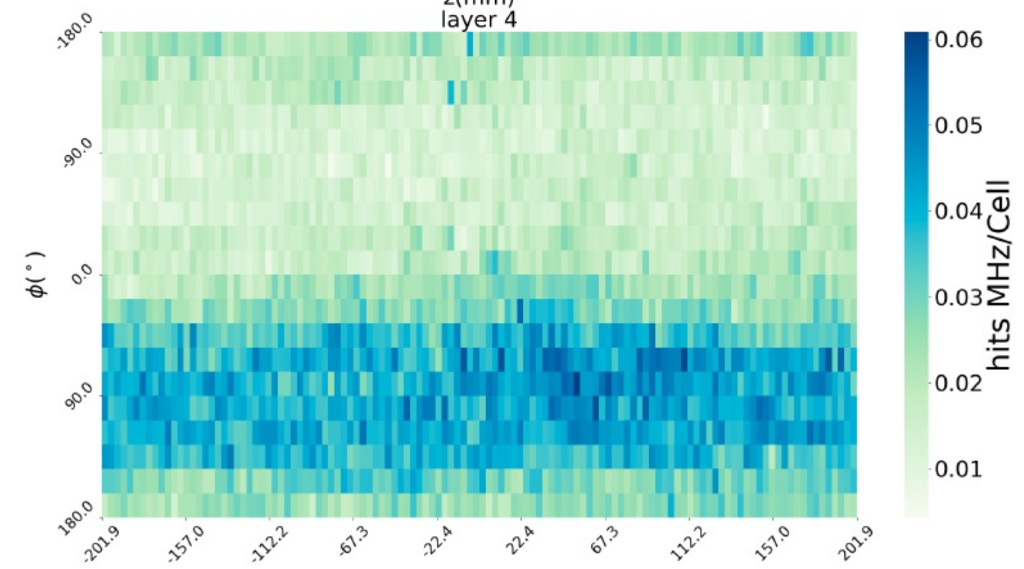
Layer	Ave. Hit Rate MHz/cm^2	Max. Hit Rate MHz/cm^2	Ave. Hit Rate×C MHz/cm^2	Ave. Hit Rate×C MHz/cm^2	Ave. Data Rate Mbps/cm^2	Max. Data Rate Mbps/cm^2
Higgs: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 346ns, 53%Gap, 25× 25 μm^2/ pixel)						
1	1.117	1.255	6.203	7.319	198.503	234.201
2	0.326	0.541	1.747	3.061	55.919	97.937
3	0.087	0.182	0.485	0.966	15.522	30.902
4	0.042	0.081	0.244	0.510	7.792	16.311
5	0.011	0.047	0.062	0.308	1.992	9.870
6	0.008	0.032	0.043	0.196	1.380	6.284
Low Lumi Z: DataRate = HitRate ×32 bit / pixel × ClusterSize @(Bunch Spacing: 69ns, 0%Gap, 25× 25 μm^2/ pixel)						
1	3.384	6.612	21.036	40.892	673.153	1308.556
2	0.384	0.608	2.469	4.388	79.000	140.410
3	0.154	0.326	1.057	2.620	33.834	83.853
4	0.097	0.229	0.658	2.401	21.050	76.834
5	0.015	0.038	0.098	0.246	3.141	7.887
6	0.012	0.025	0.075	0.173	2.393	5.527

Background Hit maps @ Low-lumi Z





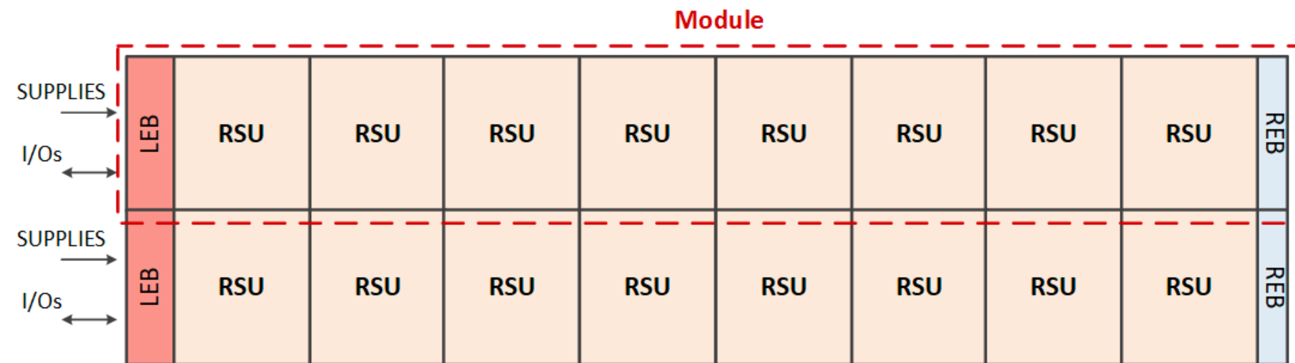


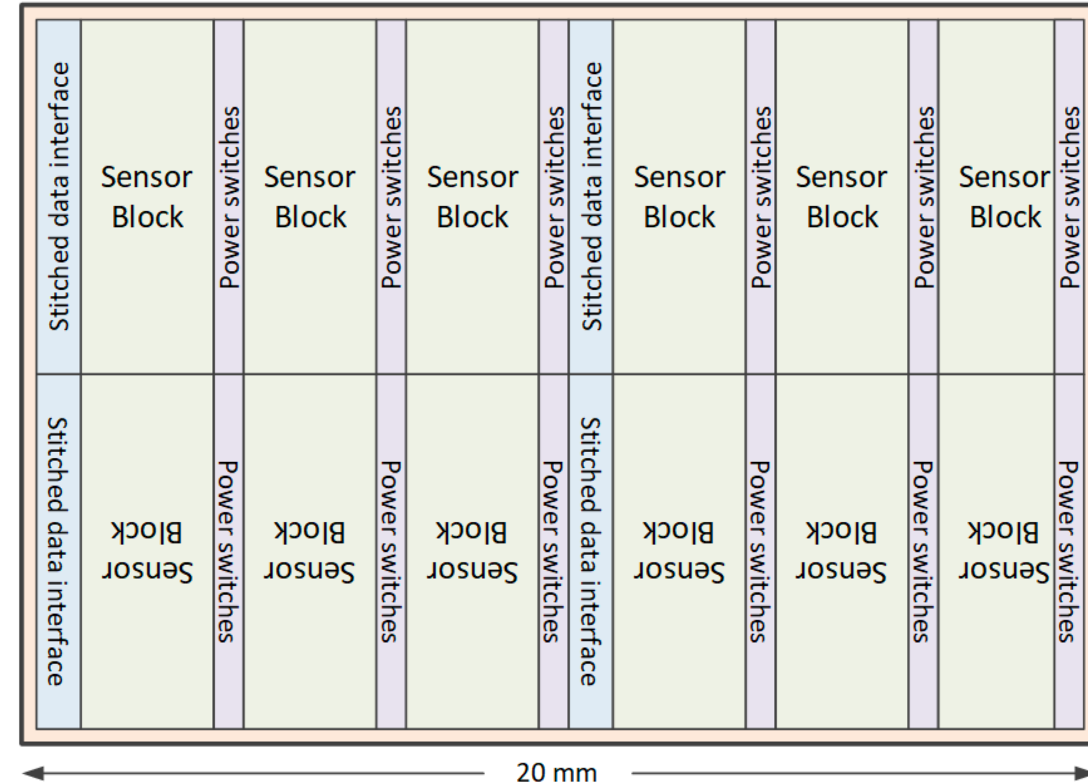


Stitching design

- Layer 1 has 8 repeated RSU.
- Power supplies and I/Os are from left side.

Top level floor-plan for a sensor of layer1





	Pixel Matrix	Biasing Block	Power Switches	Matrix readout	Stitched interface	RSU	LEB	REB
Width [mm]	8.409	0.053	8.409	0.177	8.409	17.277	17.277	17.277
Length [mm]	3.296	3.333	0.019	3.333	0.055	20.000	4.154	1.385

Ladder Electronics

– Layer 1-4 (stitching) : Stitching left-end Block

– Layer 5-6 (ladder) : flexible PCB

- Signal, clock, control, power, ground will be handled by control board through flexible PCB

Layer 1-4: stitching

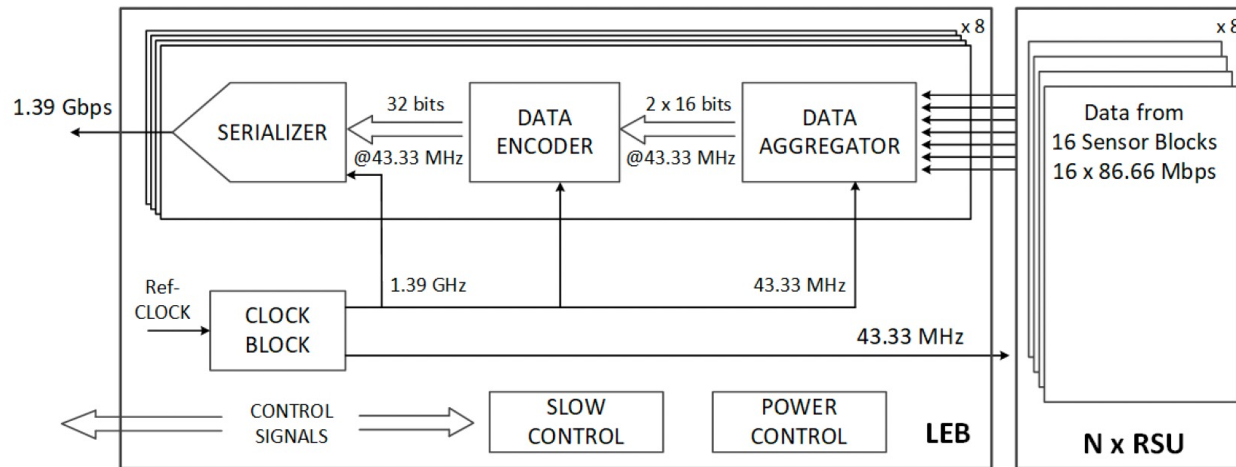
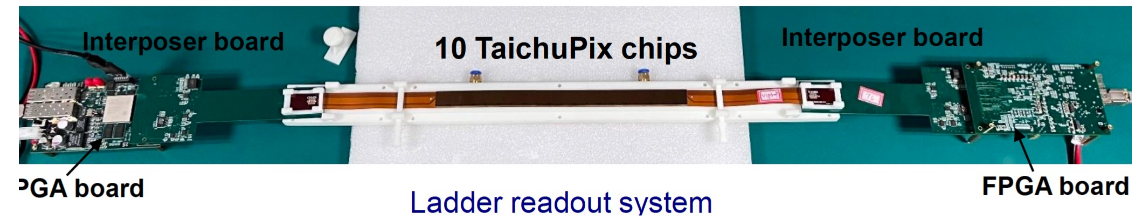


Figure 1.67: Proposed diagram of the Left-End Block (LEB). All data from RSUs of one moulde has to be transmitted to the LEB. 'N × RSU' labeled in the right part of the diagram represents that different layers in the detector contains a varying number of RSUs.

Layer 5-6: flexible PCB



叠层 **Stack Up**

Layer	Thickness	Unit	Material				Notes
	12.5	um	Coverlay (yellow)				
	20	um	Coverlay Adhesive			Soldmask (green)	
Layer 1	24	um	ED Base Copper	12	um	um + Plated 18 um	
	13	um	Polyimide (Adhesiveless)				
	12.5	um	Adhesive				
Layer 2	12	um	ED Base Copper	12	um		
	25	um	Polyimide (Adhesiveless)				Flex Thickness 绕折区
Layer 3	12	um	ED Base Copper	12	um		
	12.5	um	Adhesive				补强区
	13	um	Polyimide (Adhesiveless)				
Layer 4	24	um	ED Base Copper	12	um	um + Plated 18 um	
	20	um	Coverlay Adhesive				
	12.5	um	Coverlay (yellow)				

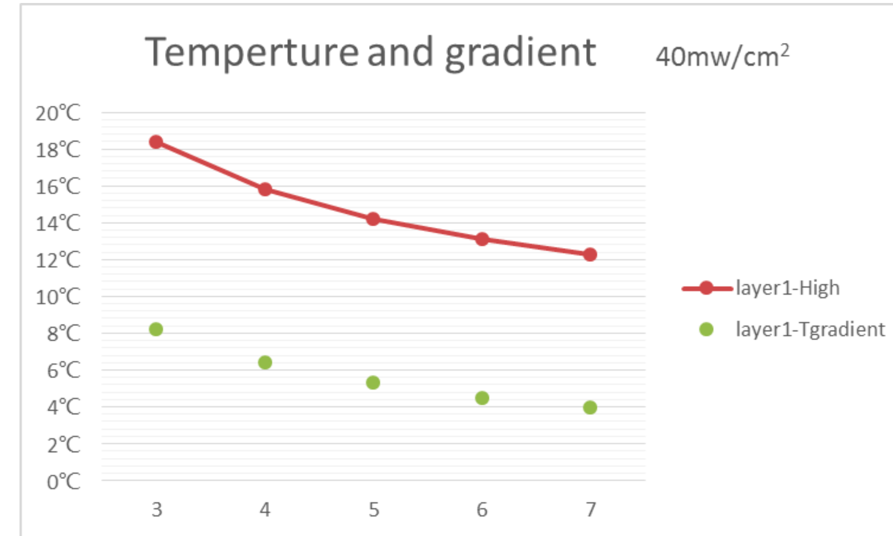
FPC厚度: 213 um Spec: 210 um +/- 50 um

Created By: HLJ

Date:

Chip design for ref- TDR and power consumption

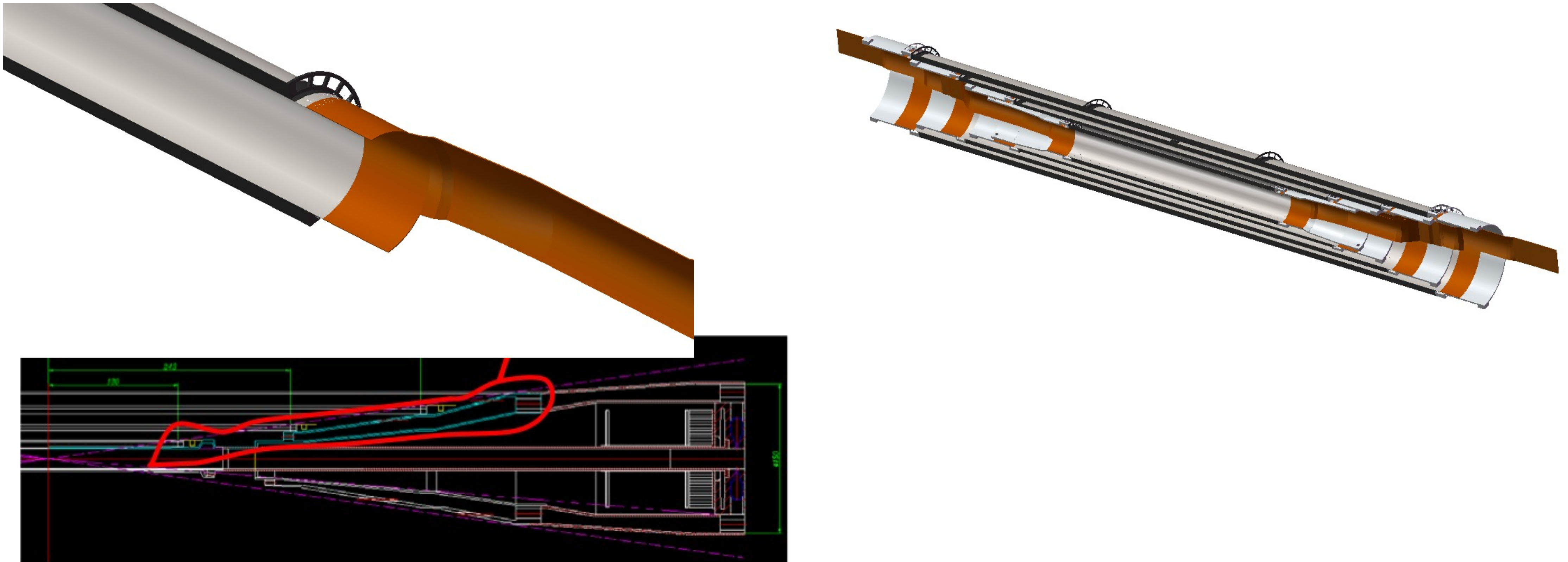
- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm^2
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 3 m/s air speed, estimated by thermal simulation



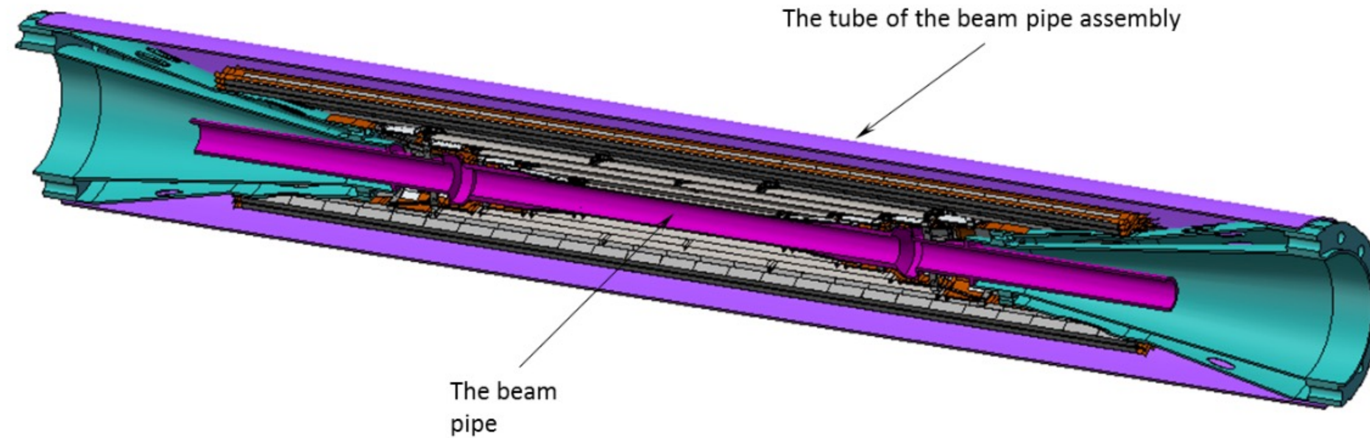
	Matrix	Periphery	DataTrans.	DACs	Total Power	Power density
TaiChu3 180nm chip @ triggerless	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm^2
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	~40 mW/cm^2

Vertex technologies: Cables and services

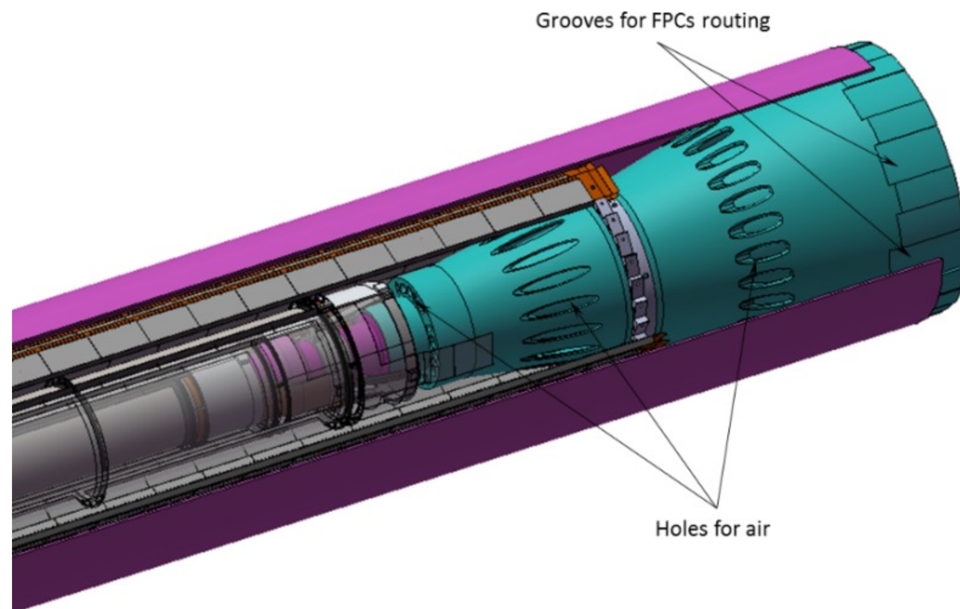
- Inner layer: flexible PCB connected to stitching layer with wire bonding
  - Power and Signal are transmitted through a long flexible PCB (~0.7m)
  - Signal converted to optical fiber (out of the MDI region)

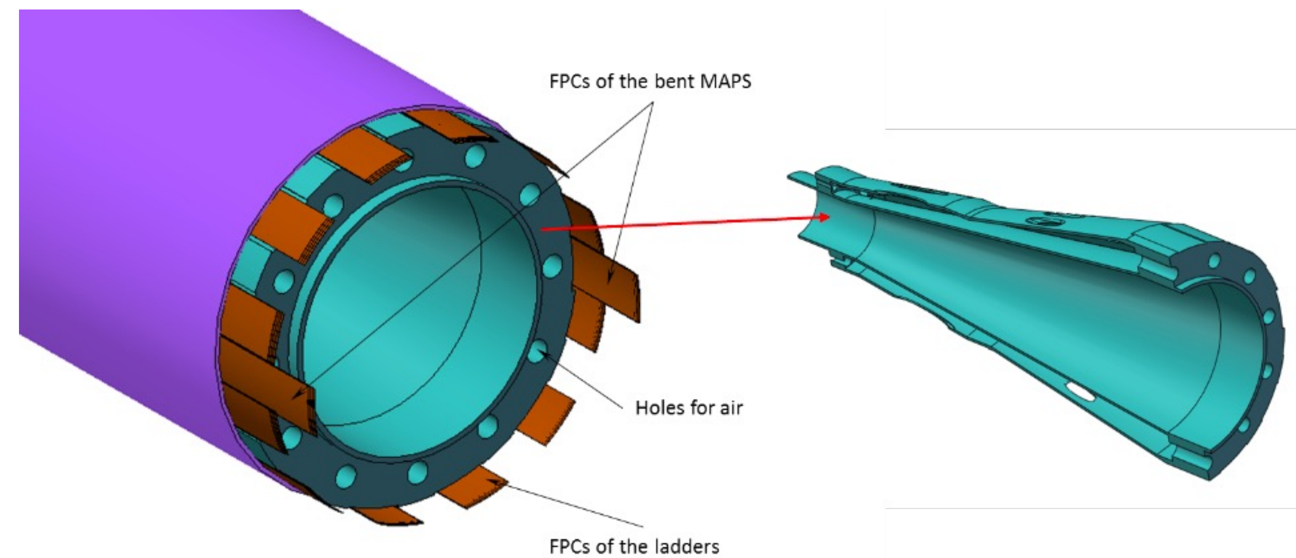


Vertex technologies: Integration with beam pipe



Flexible PCB routing

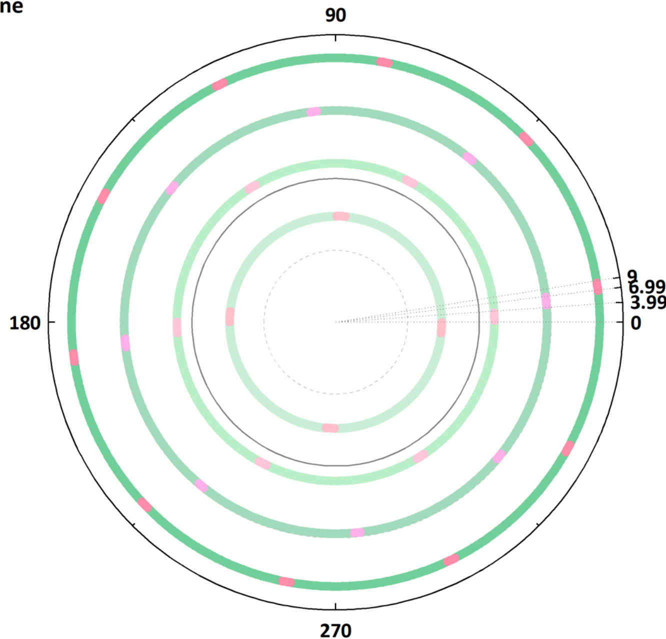




Performance: impact parameter resolution

- Compared to alternative (ladder) option
  - baseline (stitching) has significant improvement (~45%) in low momentum case

Different rotation angle in each layer to reduce dead area

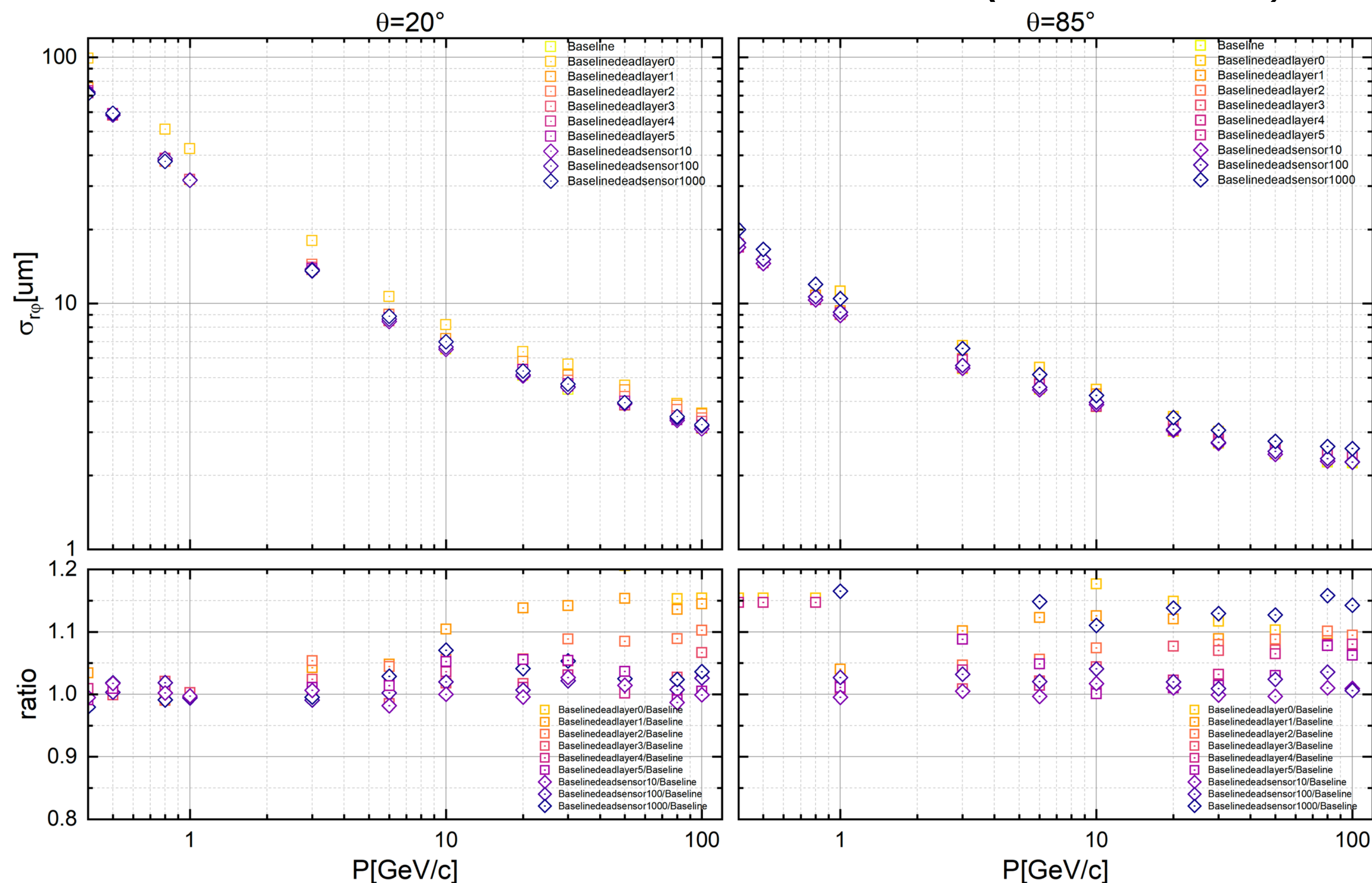


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

θ=85°
Barrel regions
θ=20°
Forward regions
Backup scheme
Baseline scheme(Four-layer bent MAPS)
Baseline scheme(Triple layer bent MAPS)
$\sigma_{r\varphi}$[um]
ratio
~45%
~40%
Baseline scheme(Four-layer bent MAPS)/Backup scheme
Baseline scheme(Triple layer bent MAPS)/Backup scheme
P[GeV/c]

Performance in case of dead sensors

- Study the performance in case of dead sensors, less than 20% impact
  - 1st case: one layer is dead
  - 2nd case: 10/ 100/1000 sensors block dead (0.1929% ,1.929%, 19.29%)



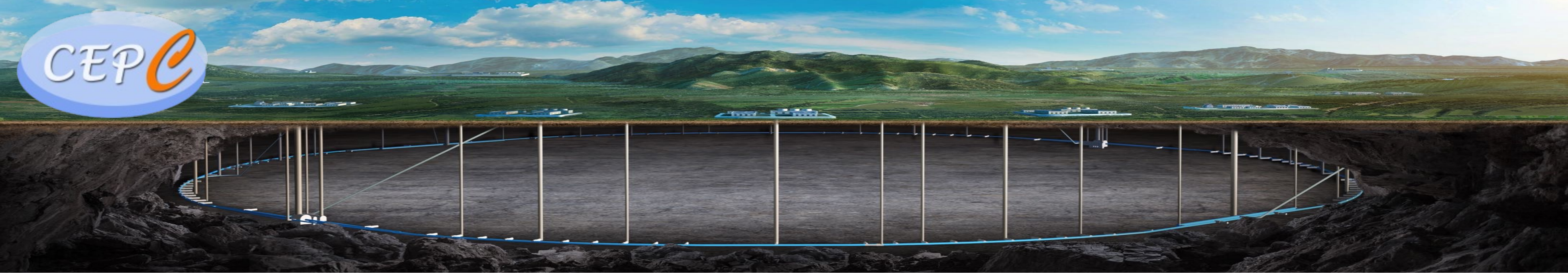
R&D status and final goal

Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 µm	3-5 µm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm
Stitching	11×11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

Summary: working plan

- CEPC vertex detector timeline is about 3-4 years after AlICE ITS3 upgrade
  - It will benefit from experience from AlICE ITS3 upgrade

	CEPC Final goal	CEPC Expected date	AlICE ITS3 schedule
CMOS chip technology	65nm CIS	2028 Full-size 65nm chip	2025
Spatial resolution	3-5 µm with final chip	2028	2025
Stitching	65nm CIS stitched sensor	2029	2026 wafer production
Bent silicon with small radius	Bent final wafer with radius ~11mm	2030	2027
Detector cooling	Air cooling with full power	2027： thermal mockup	2027
Detector integration	Detector with bent silicon design	2032	2028



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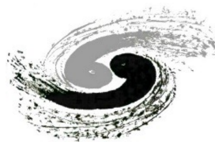

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Readout architecture of a RSU

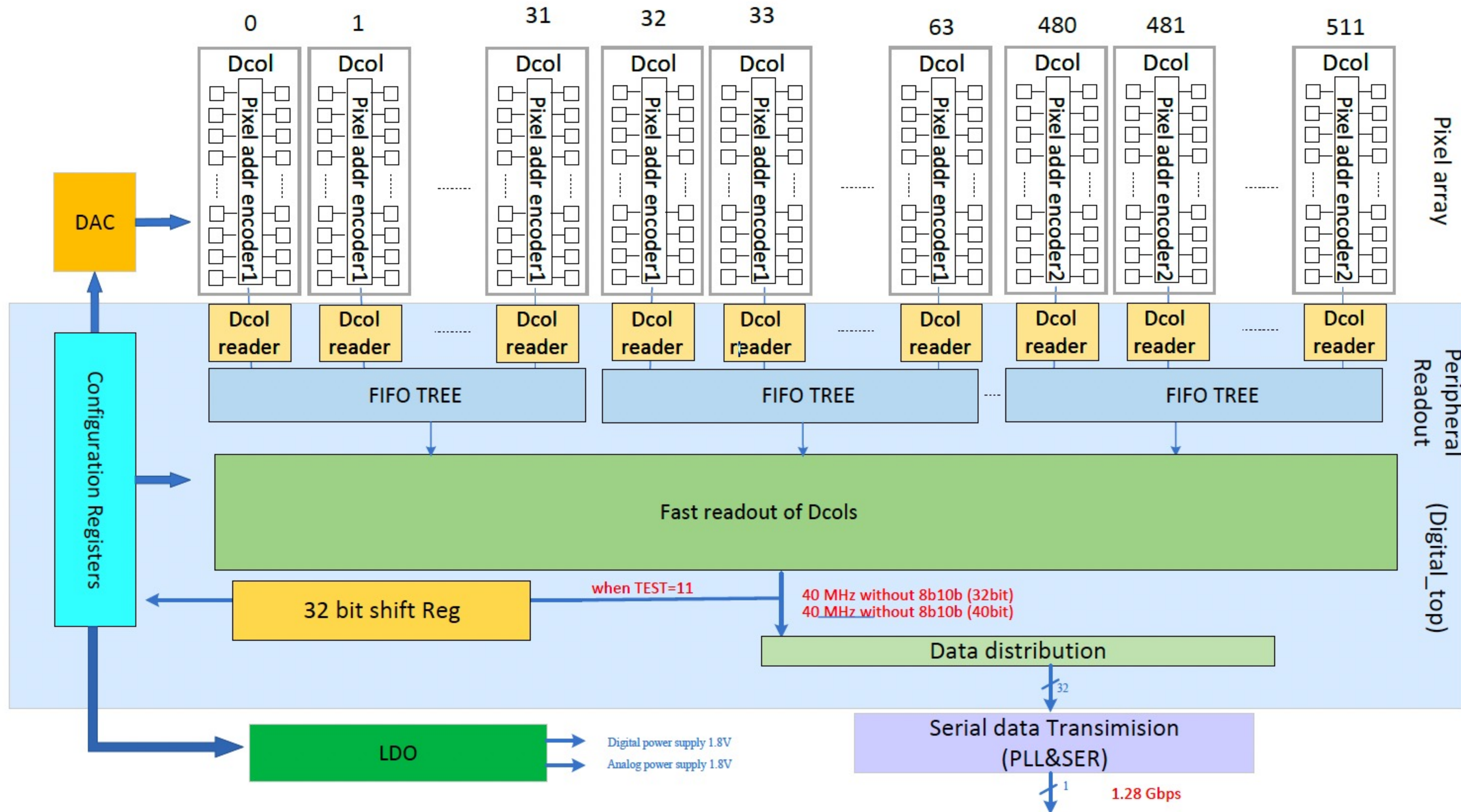
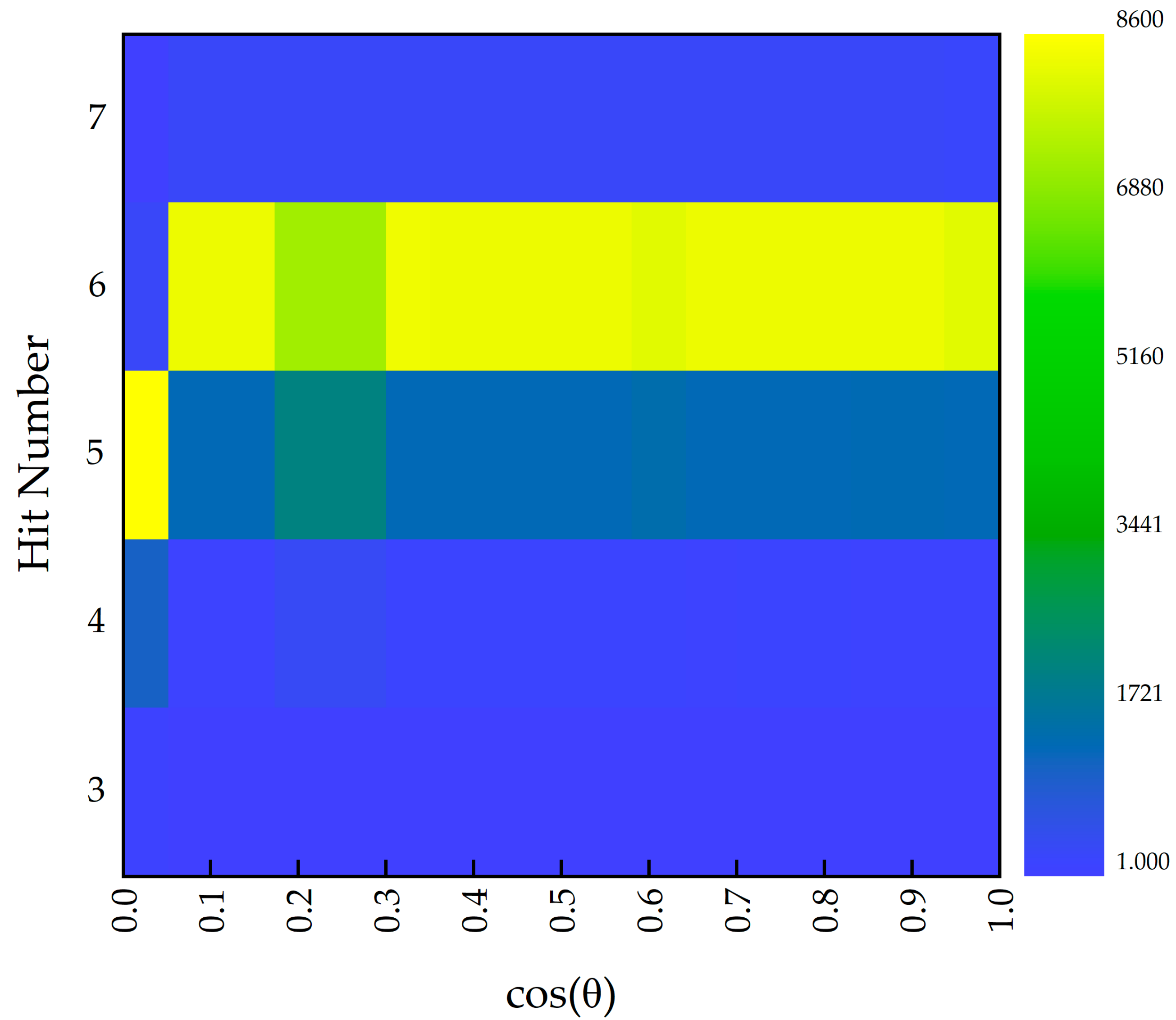
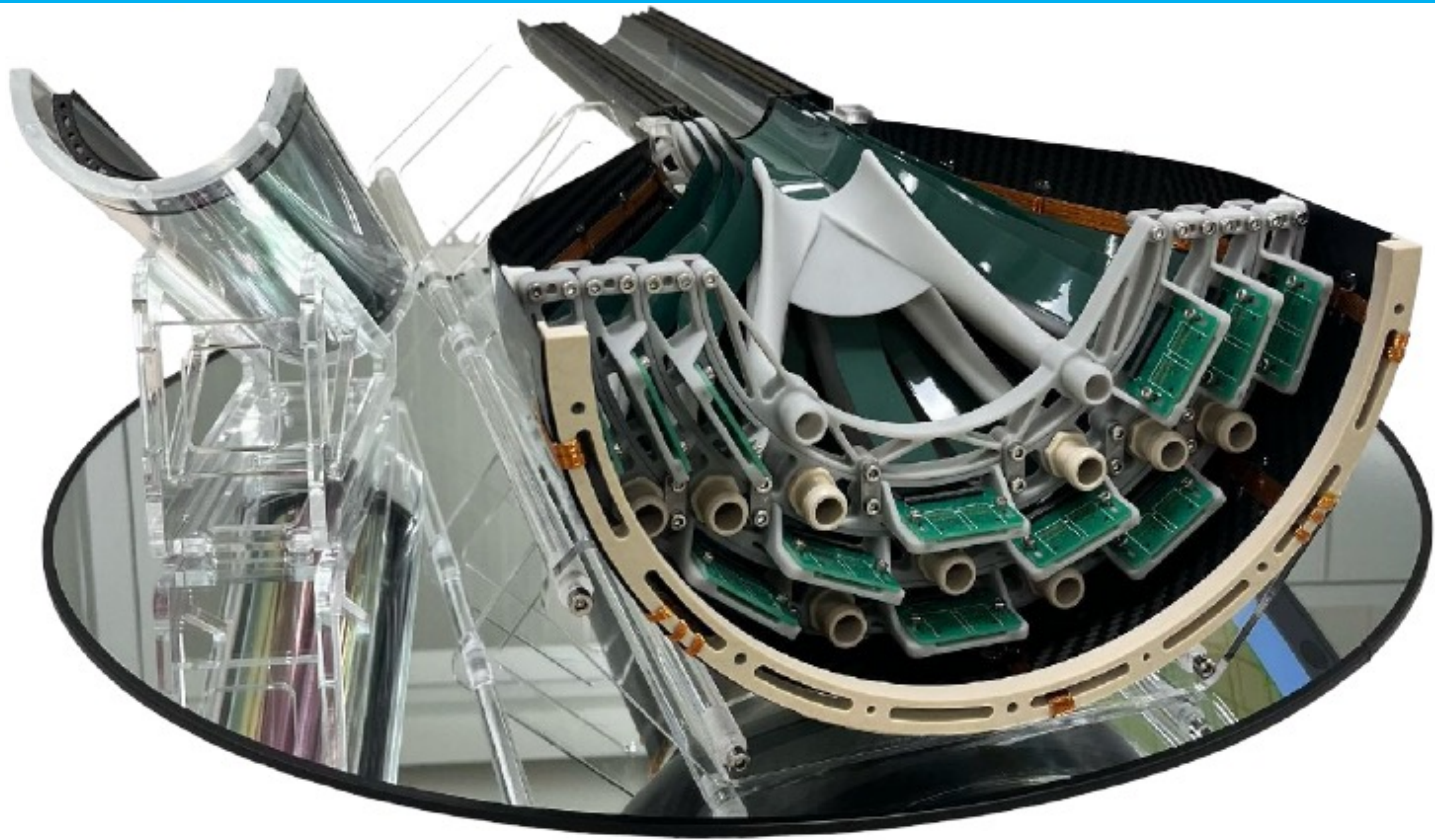


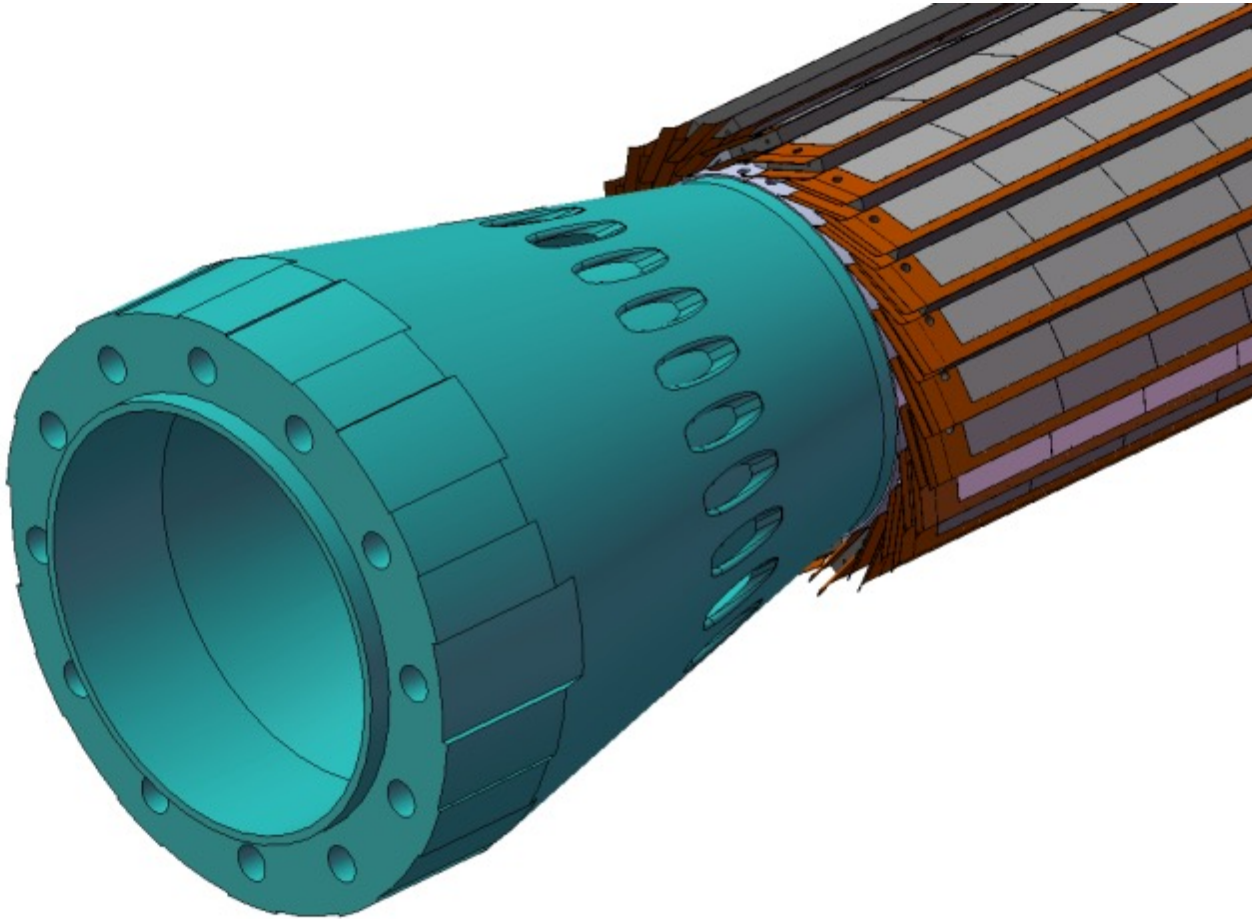
Figure 1.57: Readout architecture for a RSU

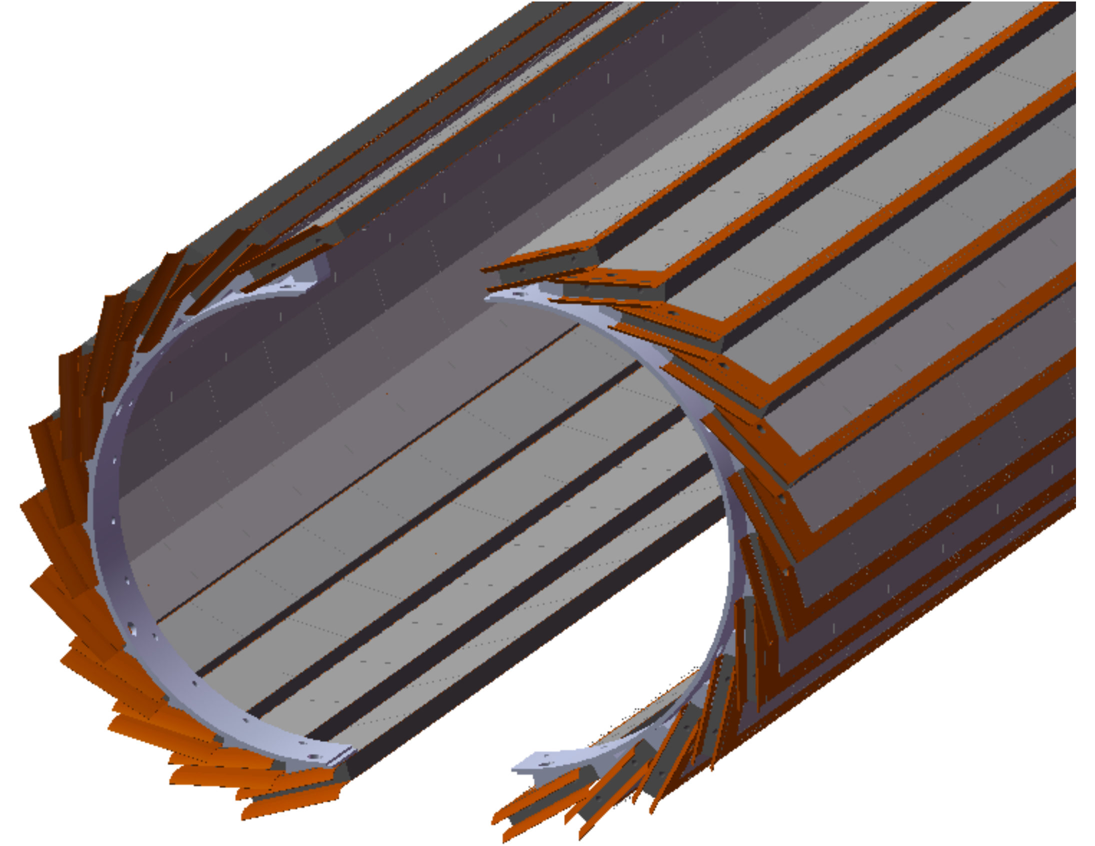
Performance





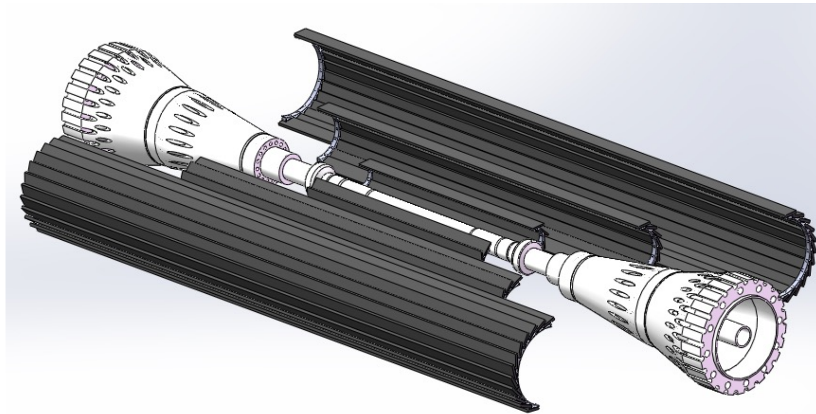
Layer 5-6 : ladder design



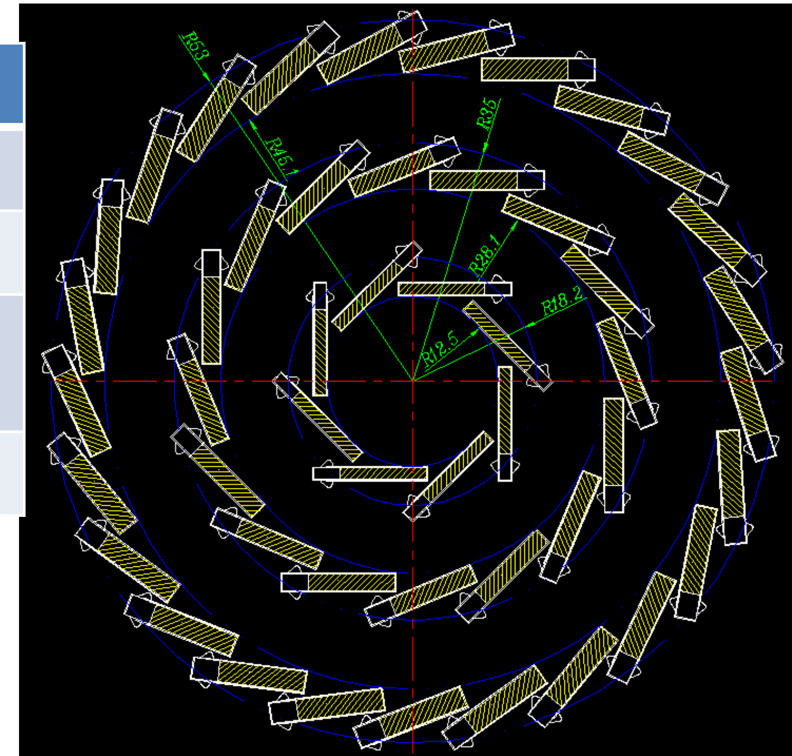


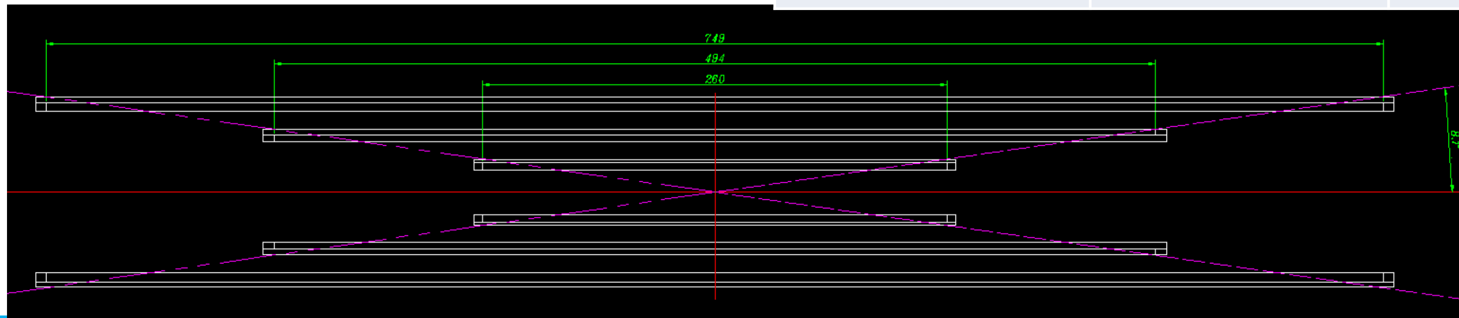
Alternative： CMOS ladder

- Alternative: CMOS chips with a long ladder layout
  - 3 double-side layer with long ladders design
  - We have built a vertex prototype based on the short ladders design
  - No effective solution for inner layer cooling yet.



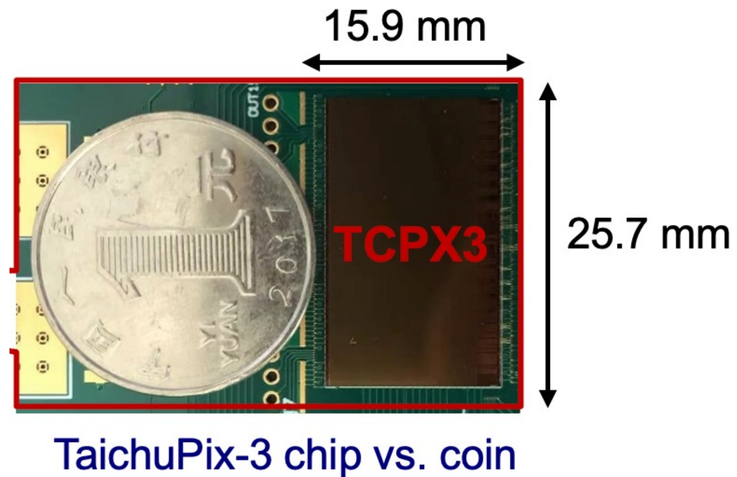
layer	Radius	Material
Layer 1/2	12.5 -18 mm	~0.33% X0
Layer 3/4	28 - 35mm	~0.33% X0
Layer 5/6 (Ladders)	45 - 53mm	~0.33% X0
Total		~1% X0



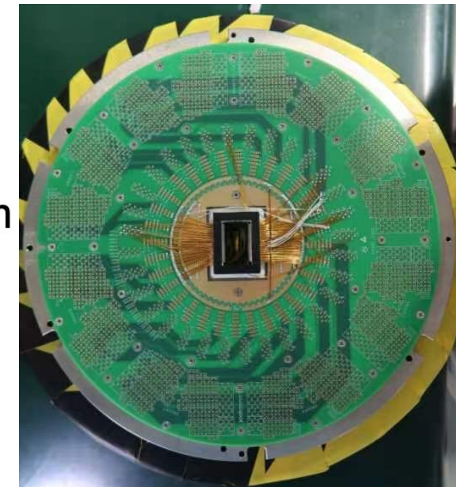


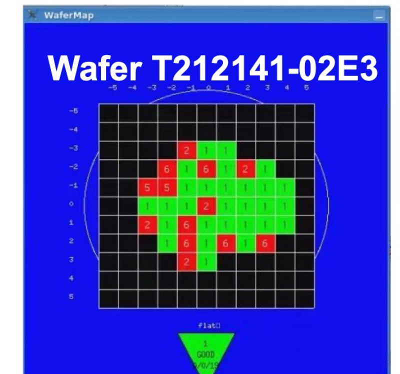
R&D efforts: Full-size TaichuPix3

- Full size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array, Chip Size: 15.9×25.7mm
  - 25μm×25μm pixel size with high spatial resolution
  - Process: Towerjazz 180nm CIS process
  - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)



TaichuPix-3 chip vs. coin





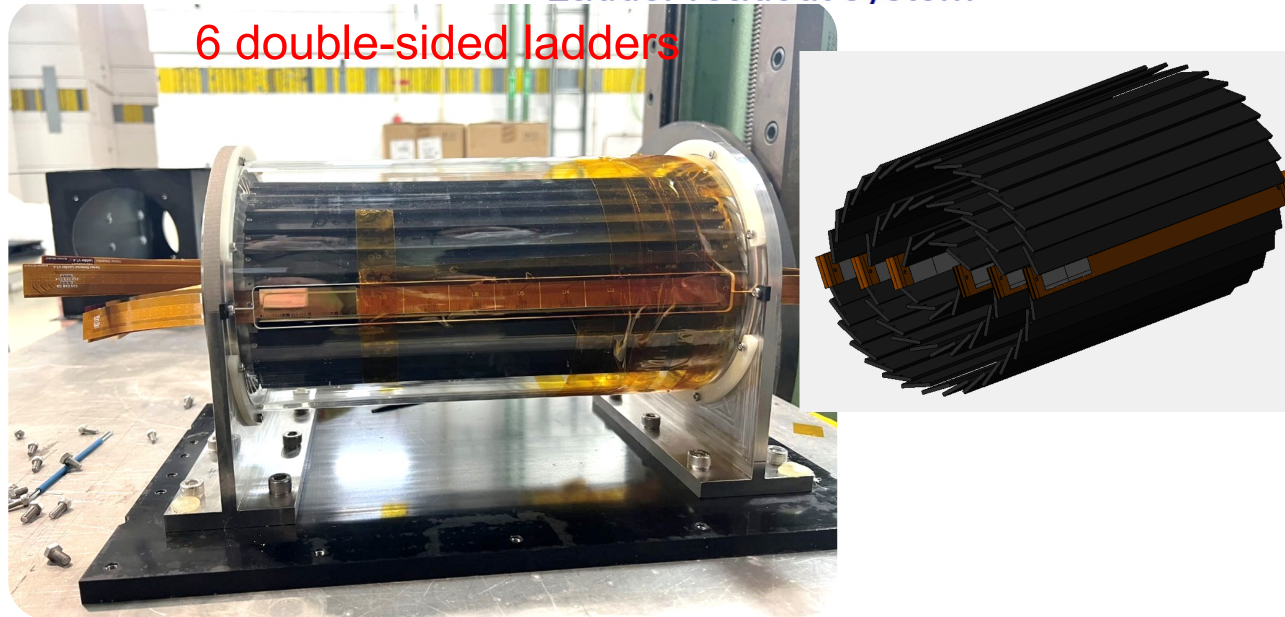
An example of wafer test result

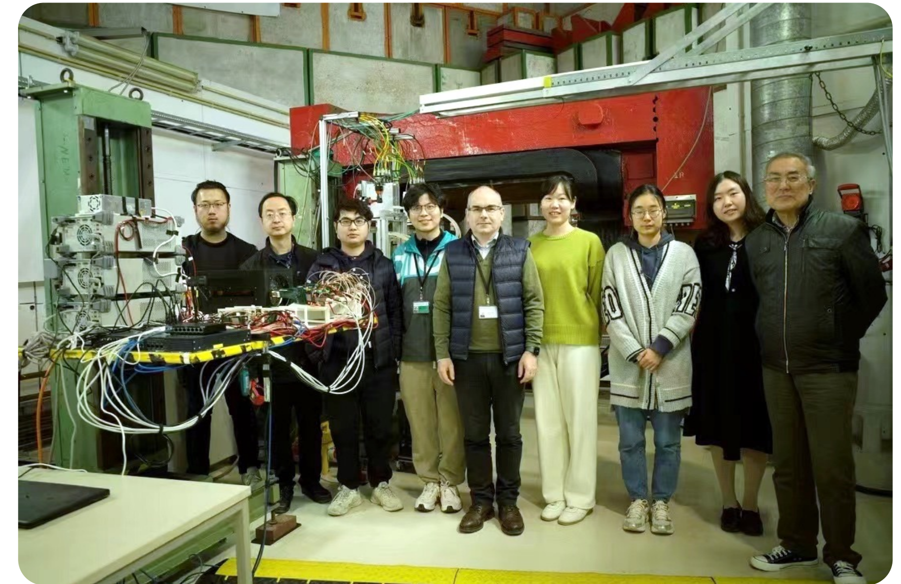
	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS

R&D effort: vertex detector prototype

TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 μm**



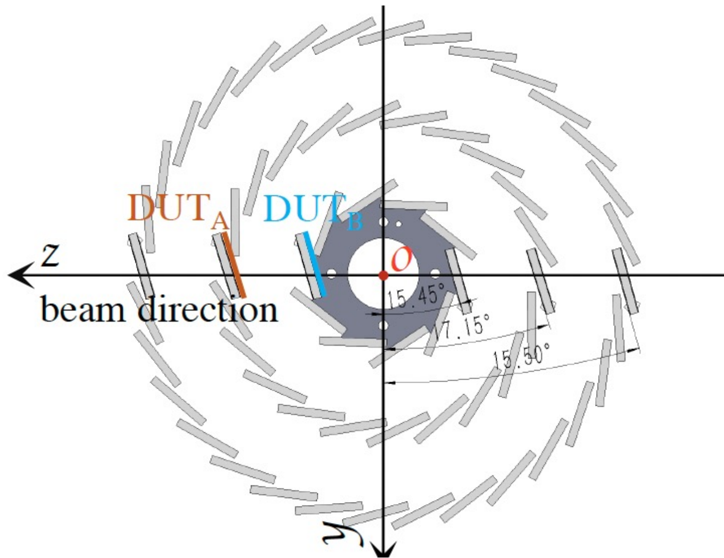


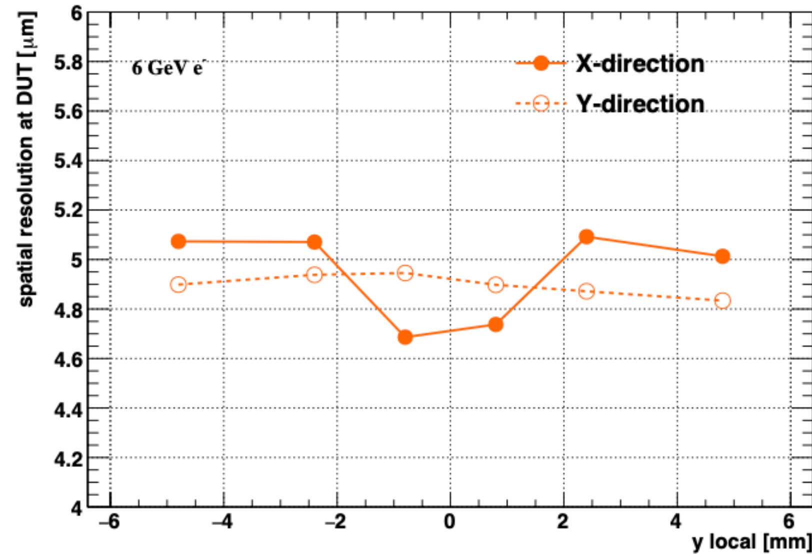
	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts and results: vertex detector prototype beam test

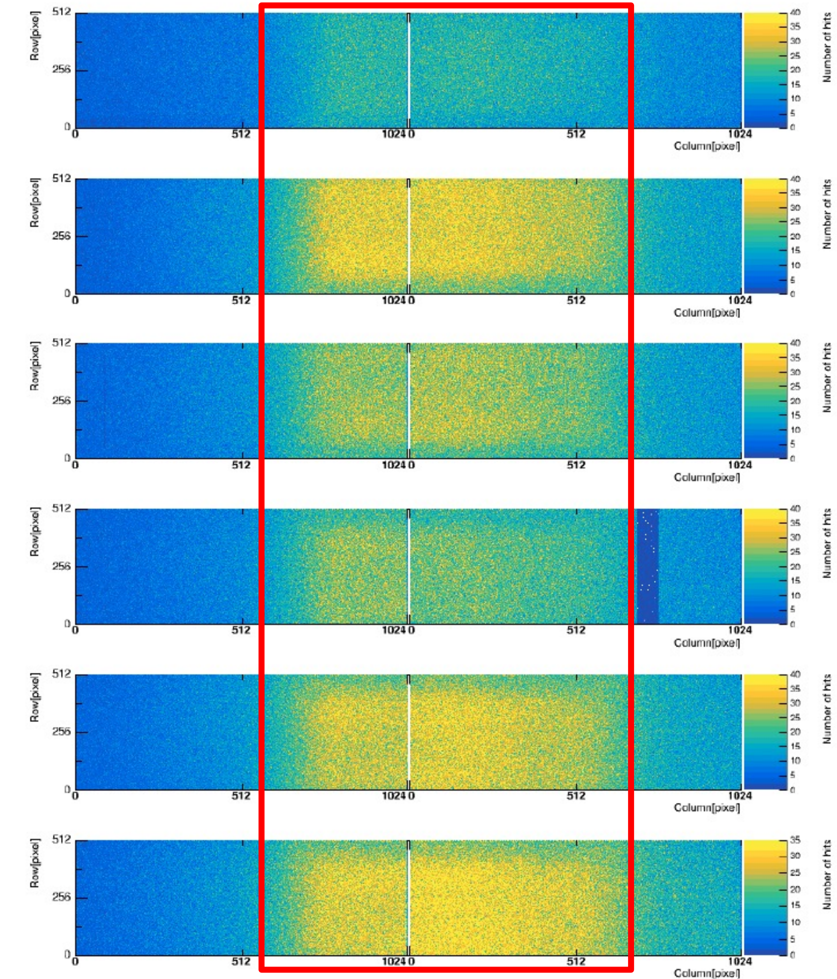
Hit maps of multiple layers of vertex detector

Spatial resolution ~ **5 μm**





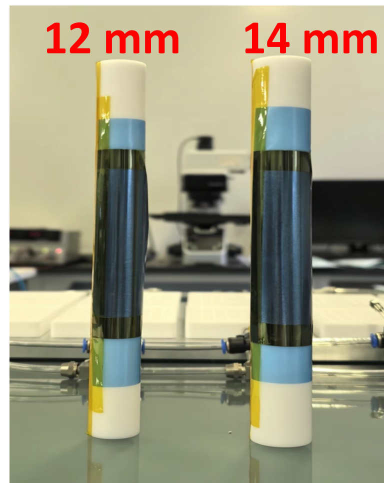
Beam spot

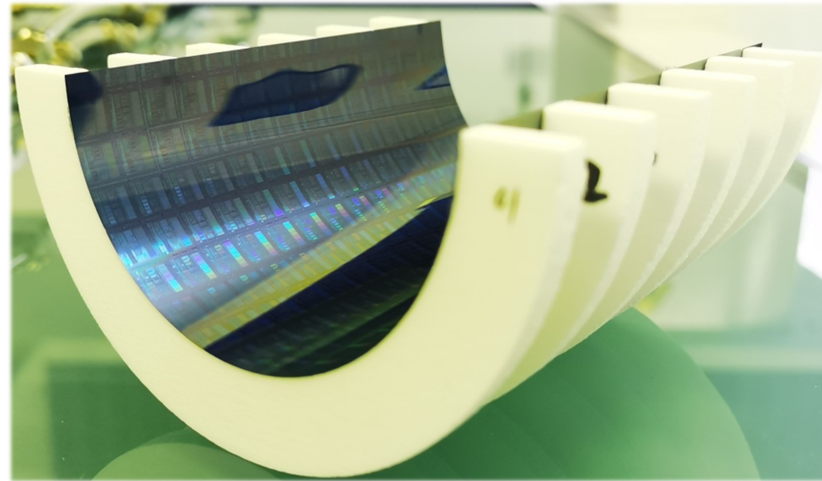


	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm



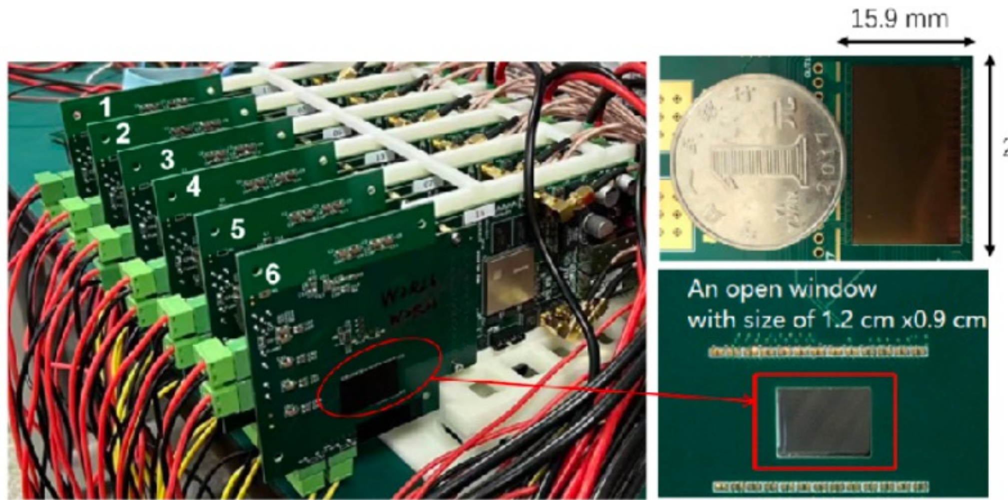


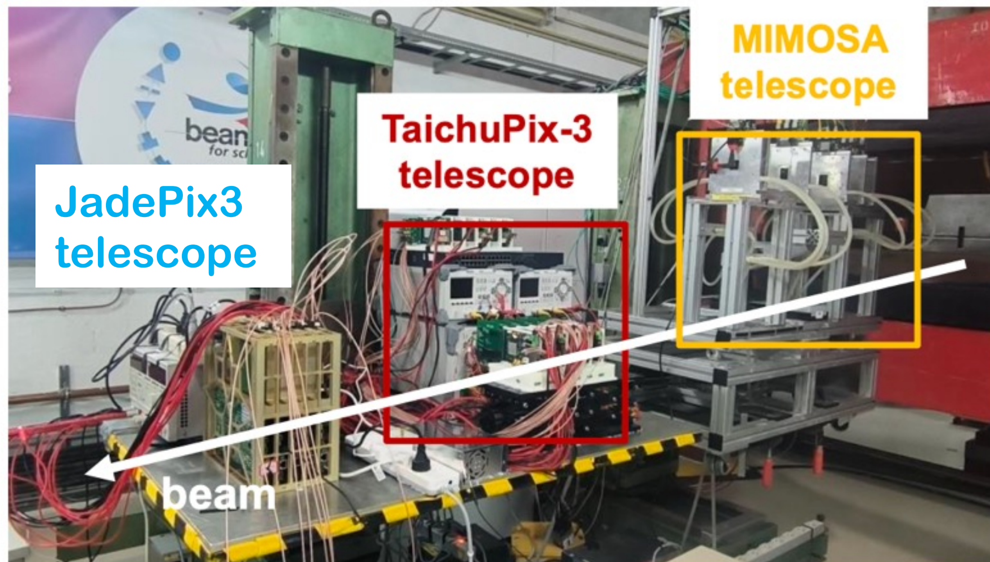
	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

Action item from meeting with IDRC chair

- Total area and Timeline for ALICE ITS3, should compare with CEPC vertex
  - ALICE ITS3 timeline is about 3~4 years earlier
  - Total area of ALICE ITS3 uprade: 0.06 m^2,
  - Total area of CEPC curved MAPS layers in vertex detector : 0.15 m^2
- Material budget for normal ladders is too conservative ?(especially for carbon fiber)
  - Material for mu3E ladders has 0.1% X0 per layer (we quoted 0.25% X0 per layer in last meeting)
  - Ladder material now reduce from 0.25% to 0.16%X0 per layer
    - Metal layer of flexible PCB now reduced from 6 to 4 layers
  - Carbon fiber thickness in CEPC prototyping can reach 0.12mm, on the same level as mu3e detector
- Accessibility for 65/55 nm technology in China
  - TowerJazz 65nm CIS can be submitted through TowerJazz agency in China
  - R & D of SMIC 55nm technology is on-going
- Serial powering is widely used in ATLAS/CMS upgrade, should look into it
  - DC-DC powering is preferred , MAPS silicon substrate needed a common negative bias

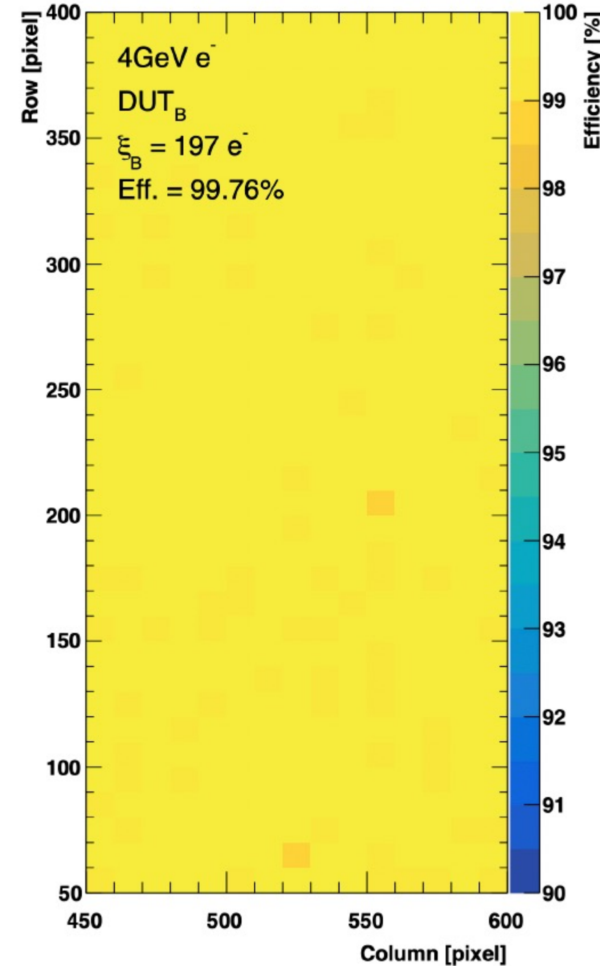
R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY



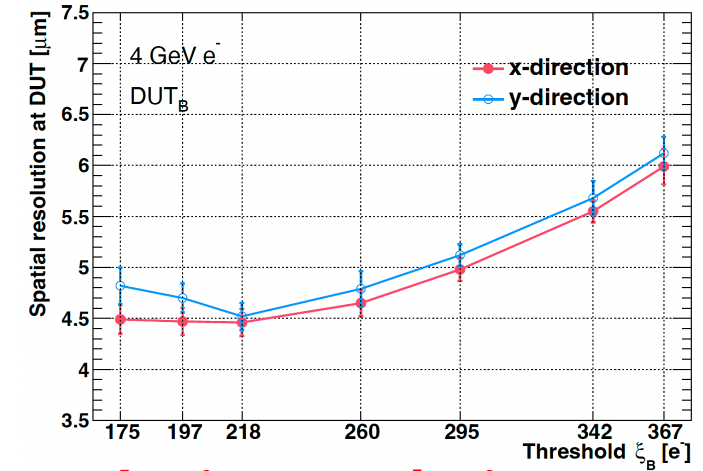


Spatial resolution 4~5um, Efficiency >99%

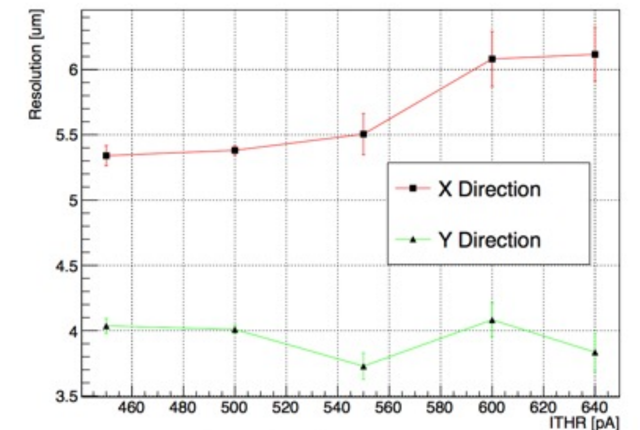
TaichuPix3 efficiency



TaichuPix3 resolution



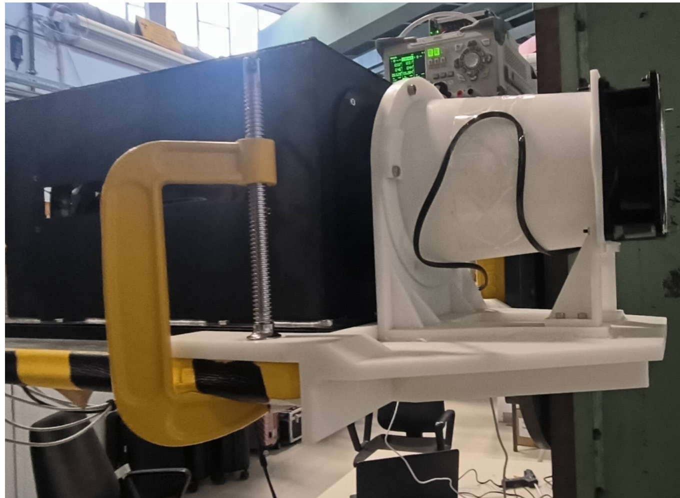
JadePix3 resolution



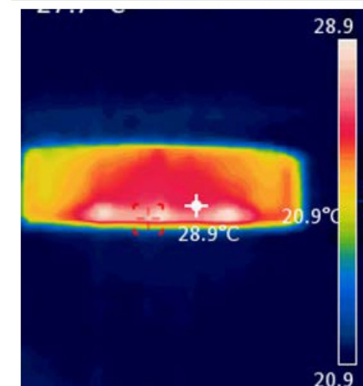
Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D

R&D efforts: Air cooling in vertex prototype

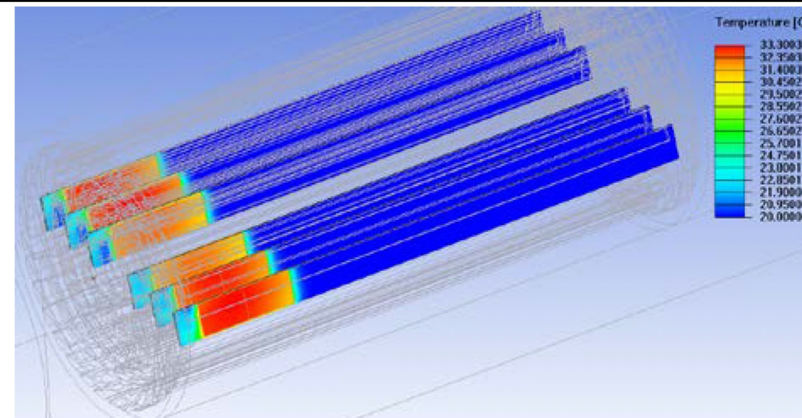
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm^2 (17.5 MHz in testbeam)
  - Before (after) turning on the cooling, chip temperature 41 °C (25 °C)
    - In good agreement to our cooling simulation
    - No visible vibration effect in spatial resolution when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃



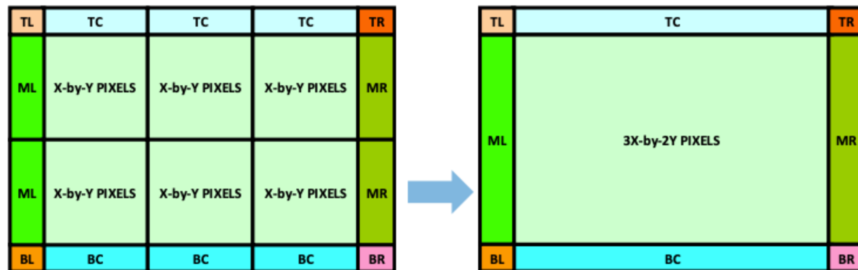
Prototype cooling simulation： Max 33.3 ℃



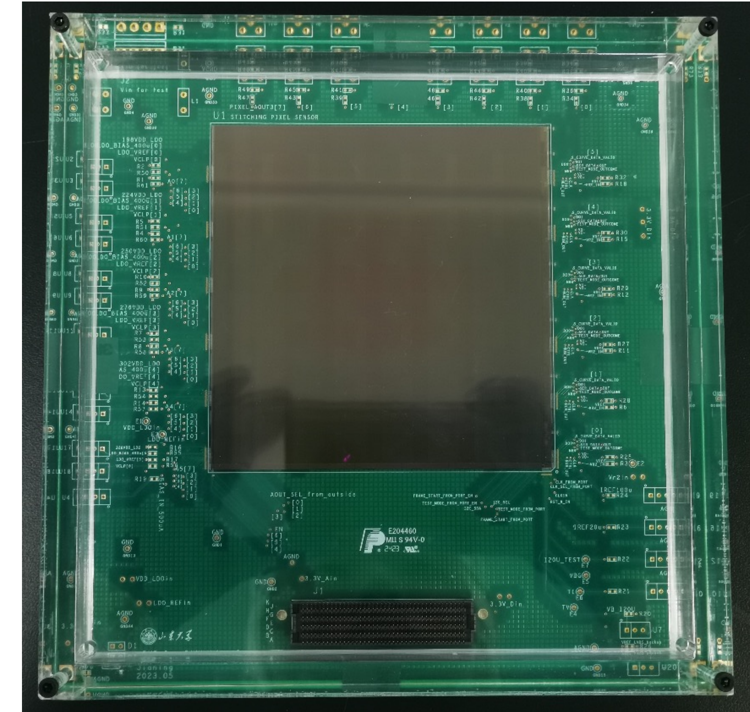
Key technology	Status	CEPC Final goal
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power

R&D efforts and results: R & D for curved MAPS

- Stitching chip design (by ShanDong U.)
  - 350nm CIS technology Xfabs
  - Wafer level size after stitching ~11 ×11 cm^2
  - reticle size ~2 ×2 cm^2
  - 2D stitching
  - Engineering run, chip under testing

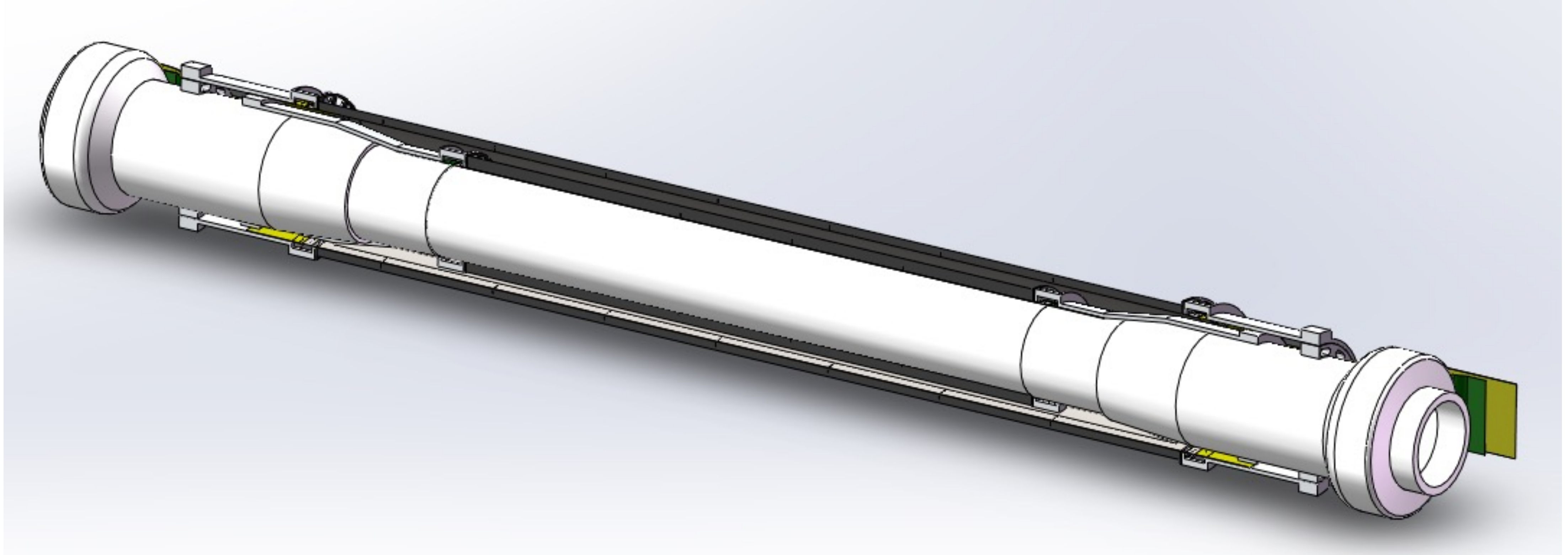


Stitching chip : 11 ×11 cm^2



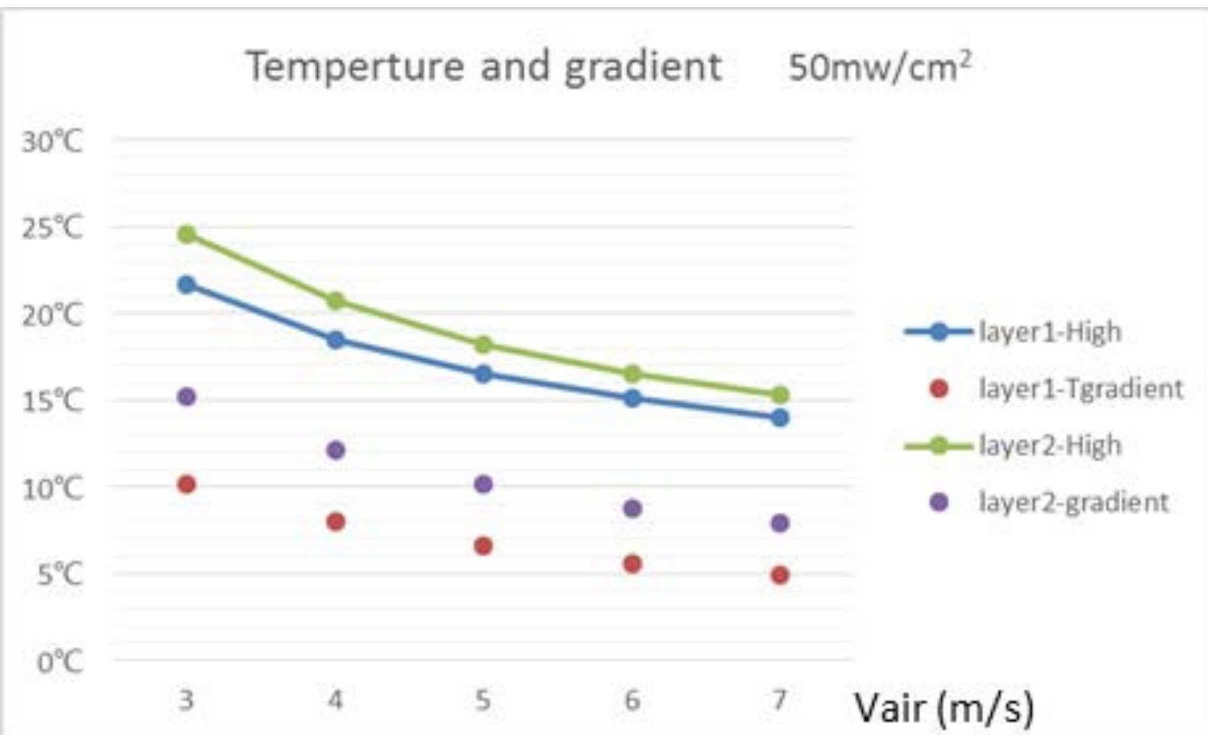
Key technology	Status	CEPC Final goal
Stitching	11*11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

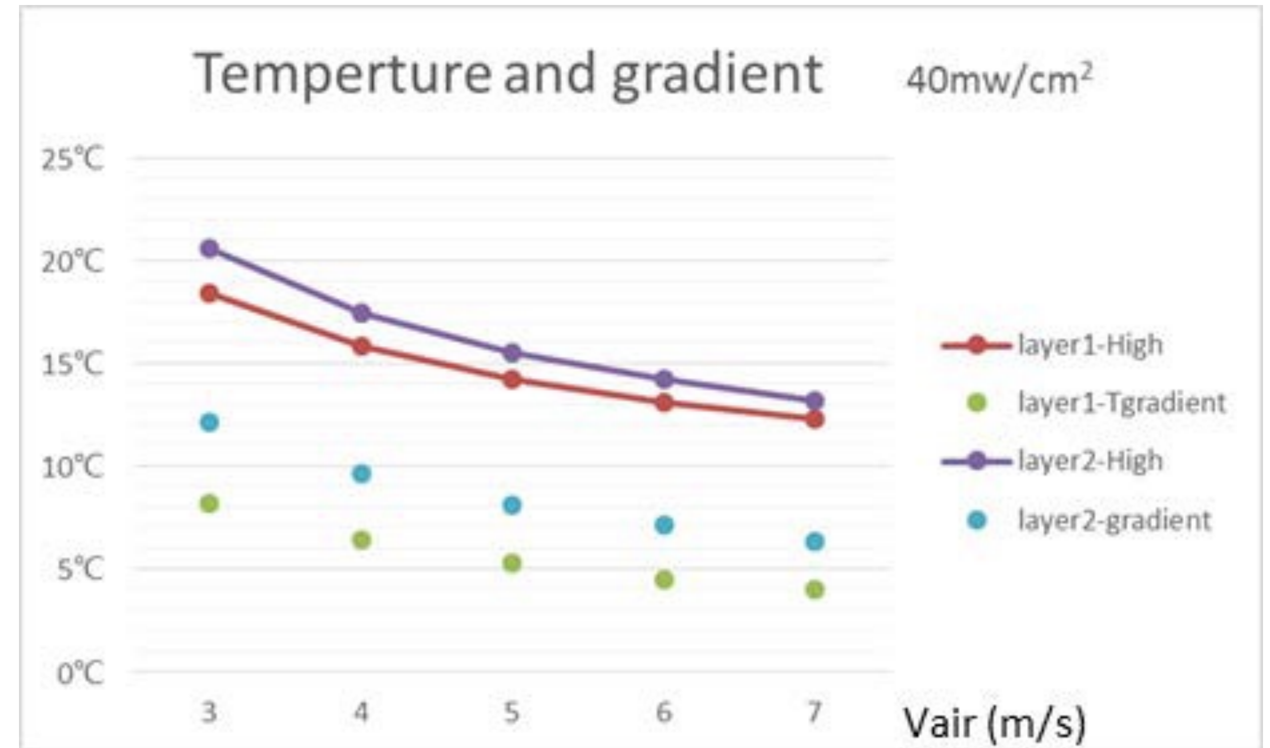
Backup: Mechanics



Backup : Cable and service

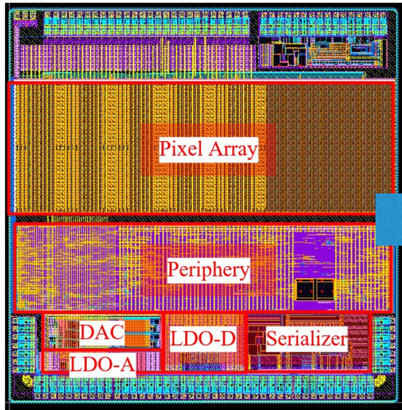
Backup : air cooling simulation

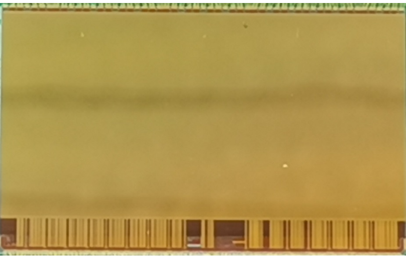




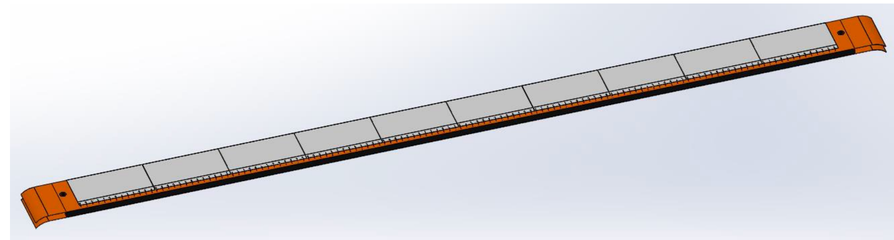
Overview of CEPC vertex detector prototype R & D

CMOS Sensor chip development



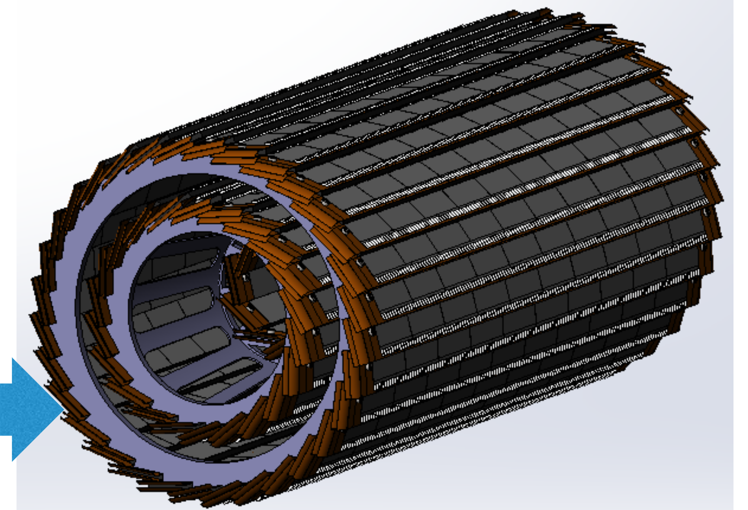


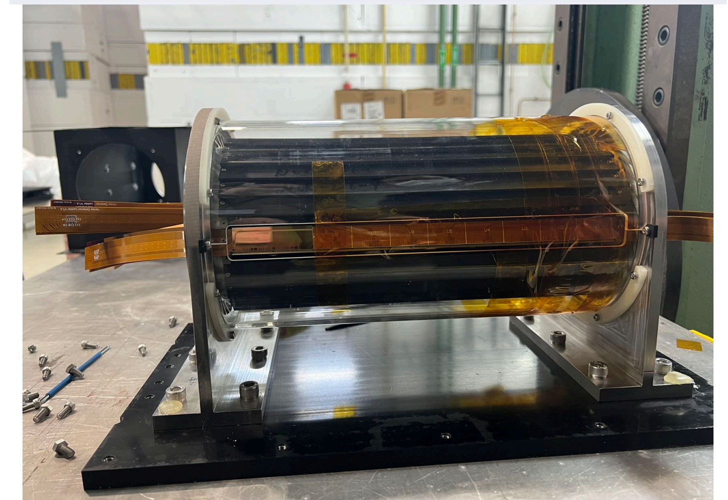
Detector module (Ladder) Prototyping



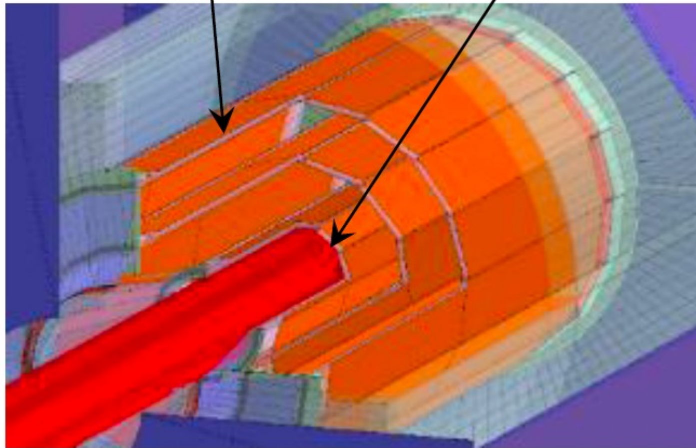
Ladder readout system

Vertex detector prototype





Silicon Pixel Chips for Vertex Detector



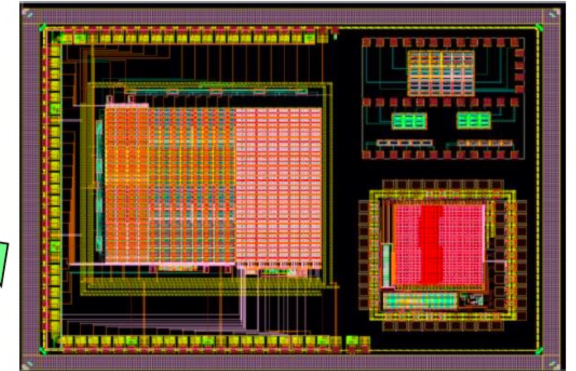
Goal: σ(IP) ~ 5 μm for high P track

CDR design specifications

- **Single point resolution ~ 3μm**
- **Low material (0.15% X_0 / layer)**
- **Low power (< 50 mW/cm²)**
- **Radiation hard (1 Mrad/year)**

Silicon pixel sensor develops in 5 series:
JadePix, TaichuPix, CPV, Arcadia, COFFEE

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process

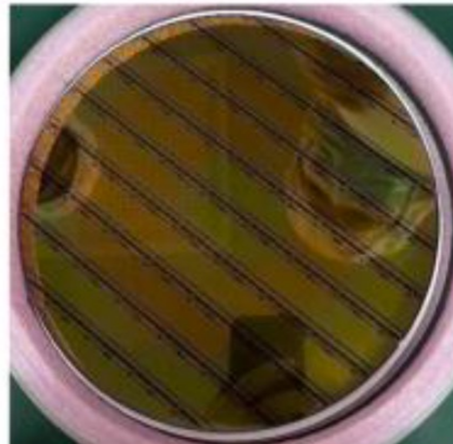


JadePix-3 Pixel size ~16×23 μm²

Tower-Jazz 180nm CiS process
Resolution 5 microns, 53mW/cm²

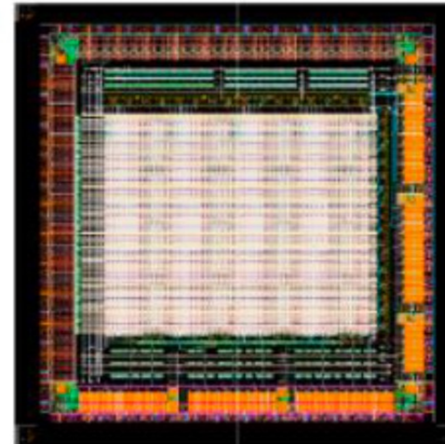
MOST 1

TaichuPix-3, FS 2.5x1.5 cm²
25×25 μm² pixel size

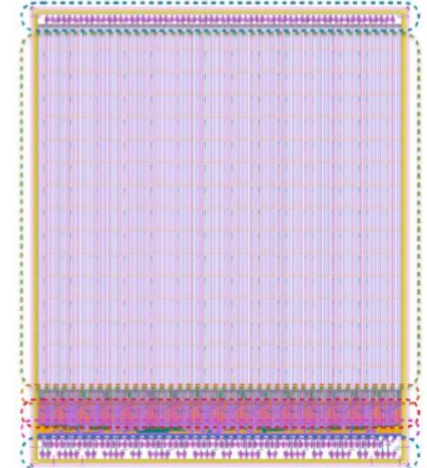


MOST 2

CPV4 (SOI-3D), 64×64 array
~21×17 μm² pixel size

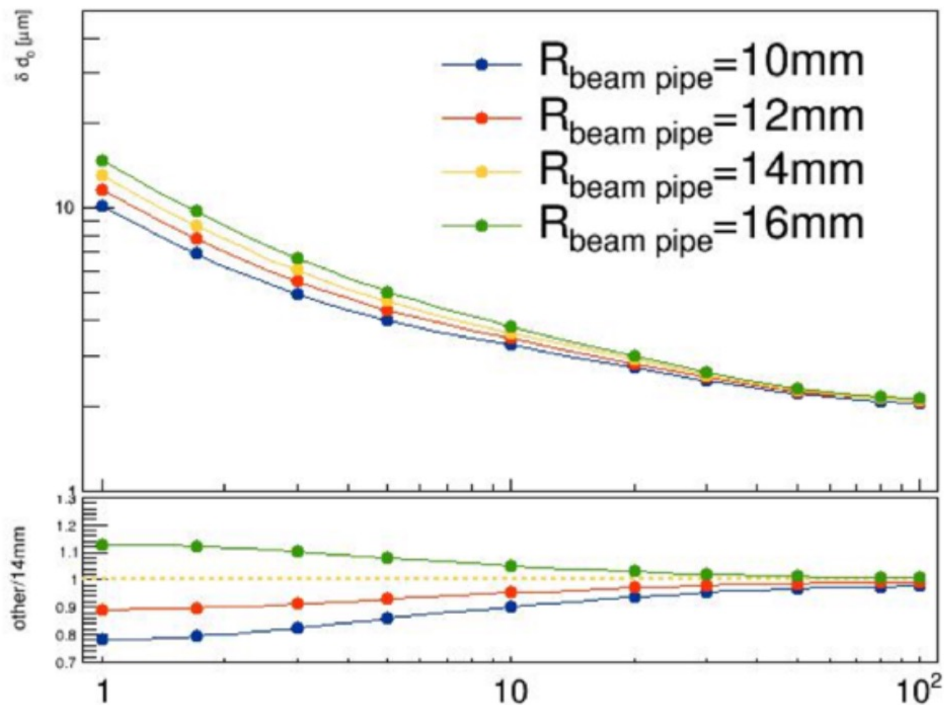


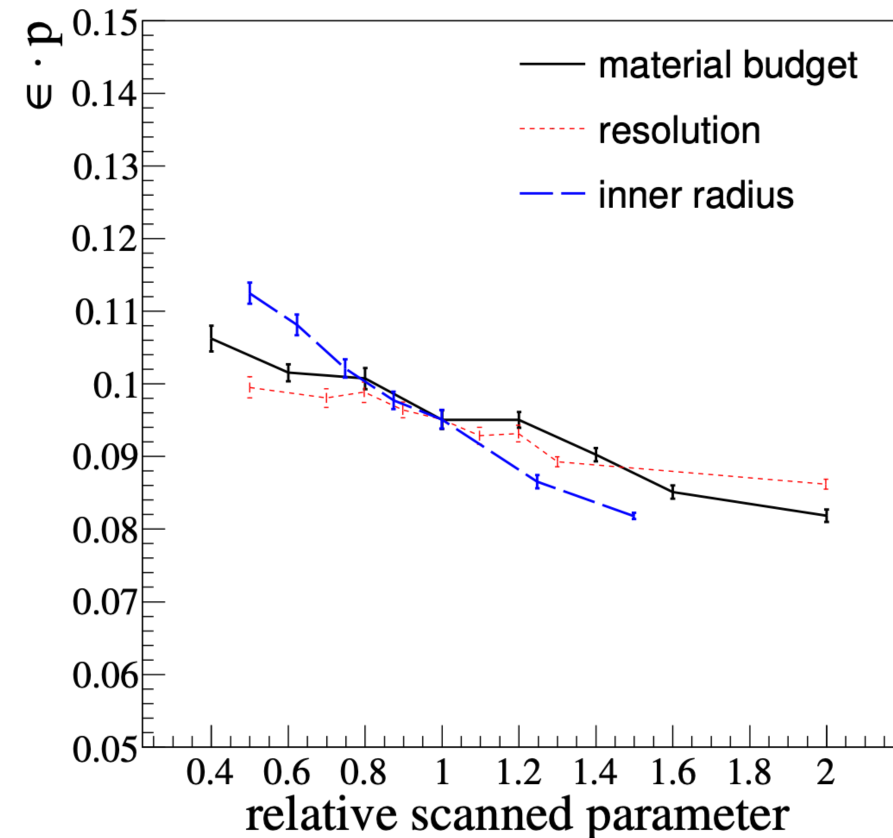
Arcadia by Italian groups for IDEA vertex detector
LFoundry 110 nm CMOS



Vertex Requirement

- 1st priority: Small inner radius, close to beam pipe (11mm)
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor： 3~5 μm

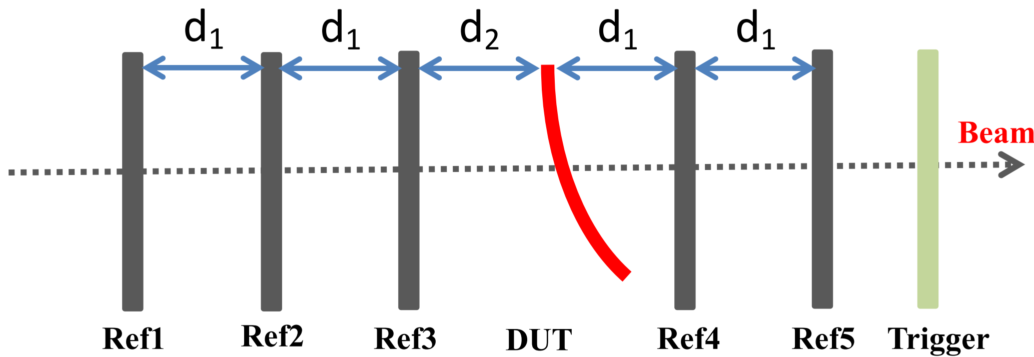


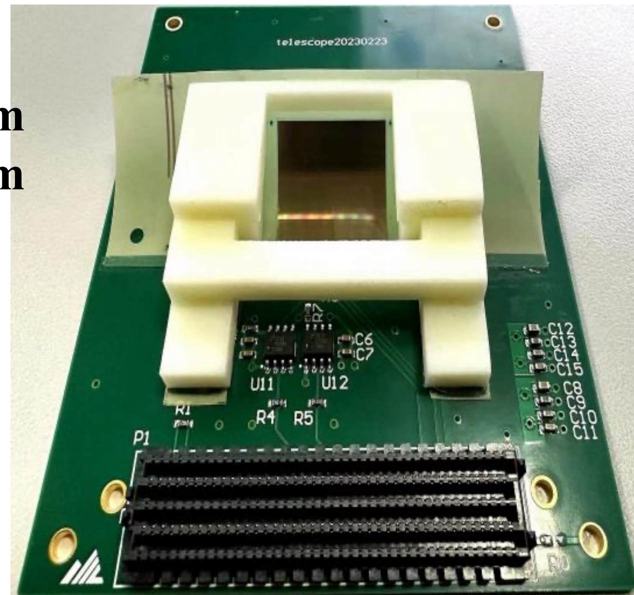


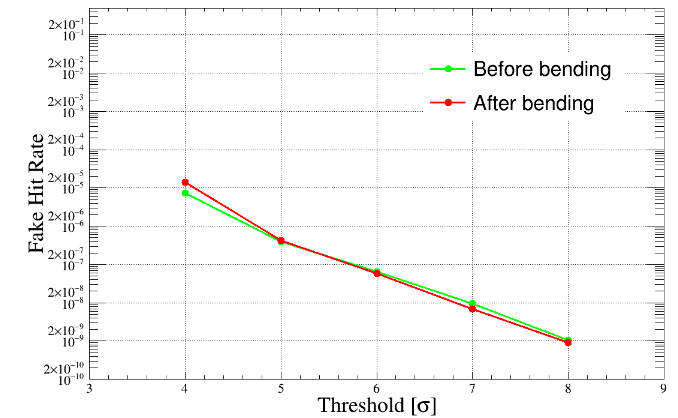
R&D efforts : Curved MAPS testbeam

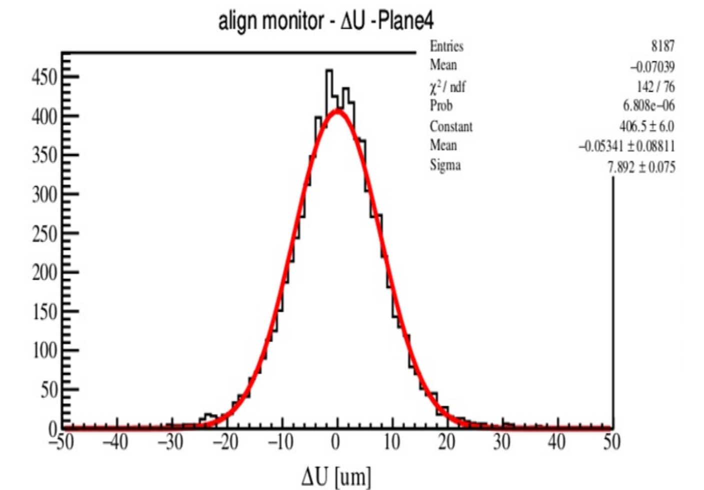
- R & D of curved maps with MIMOSA28 chip
  - No visible difference in noise level or spatial resolution before/after bending

d1 = 25 mm
d2 = 30 mm

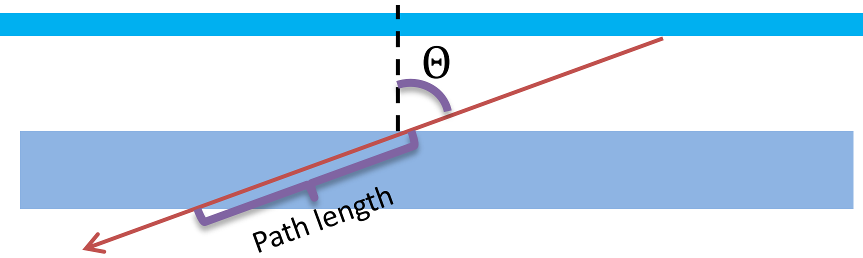




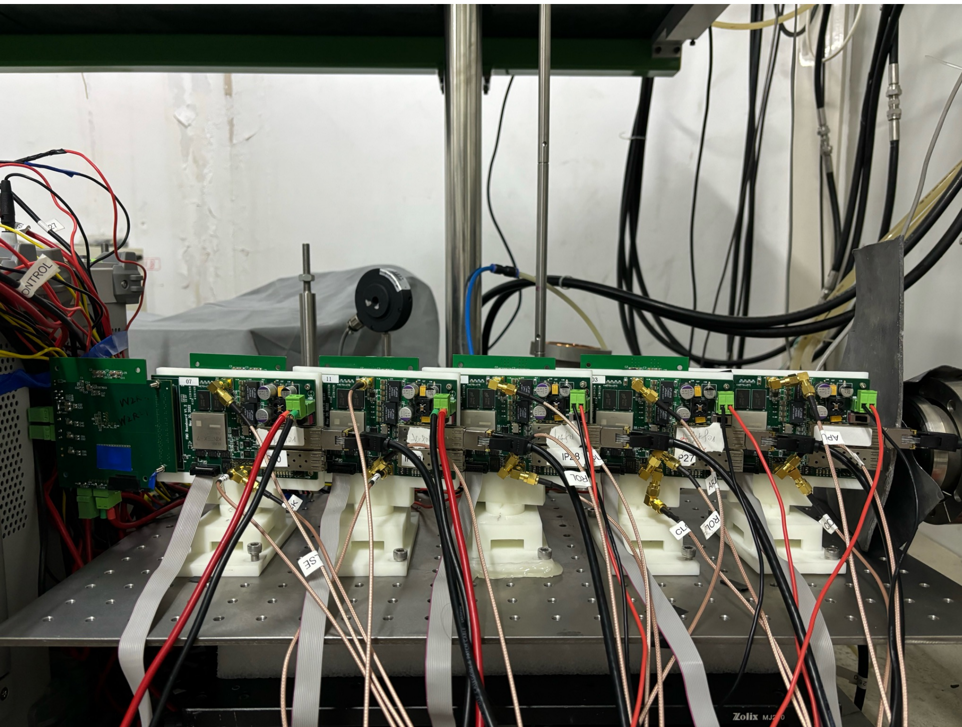


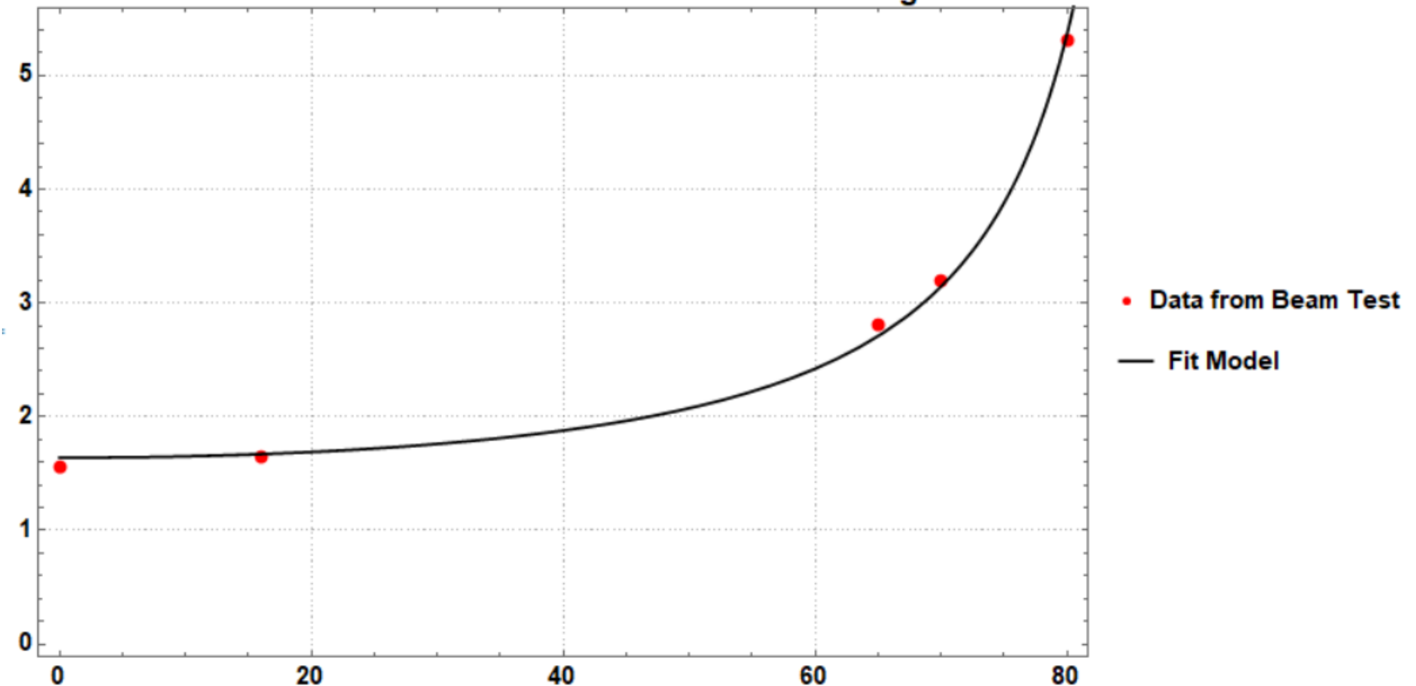


Long barrel : cluster size vs incident angle



Cluster size $= a \times sec\theta + b$

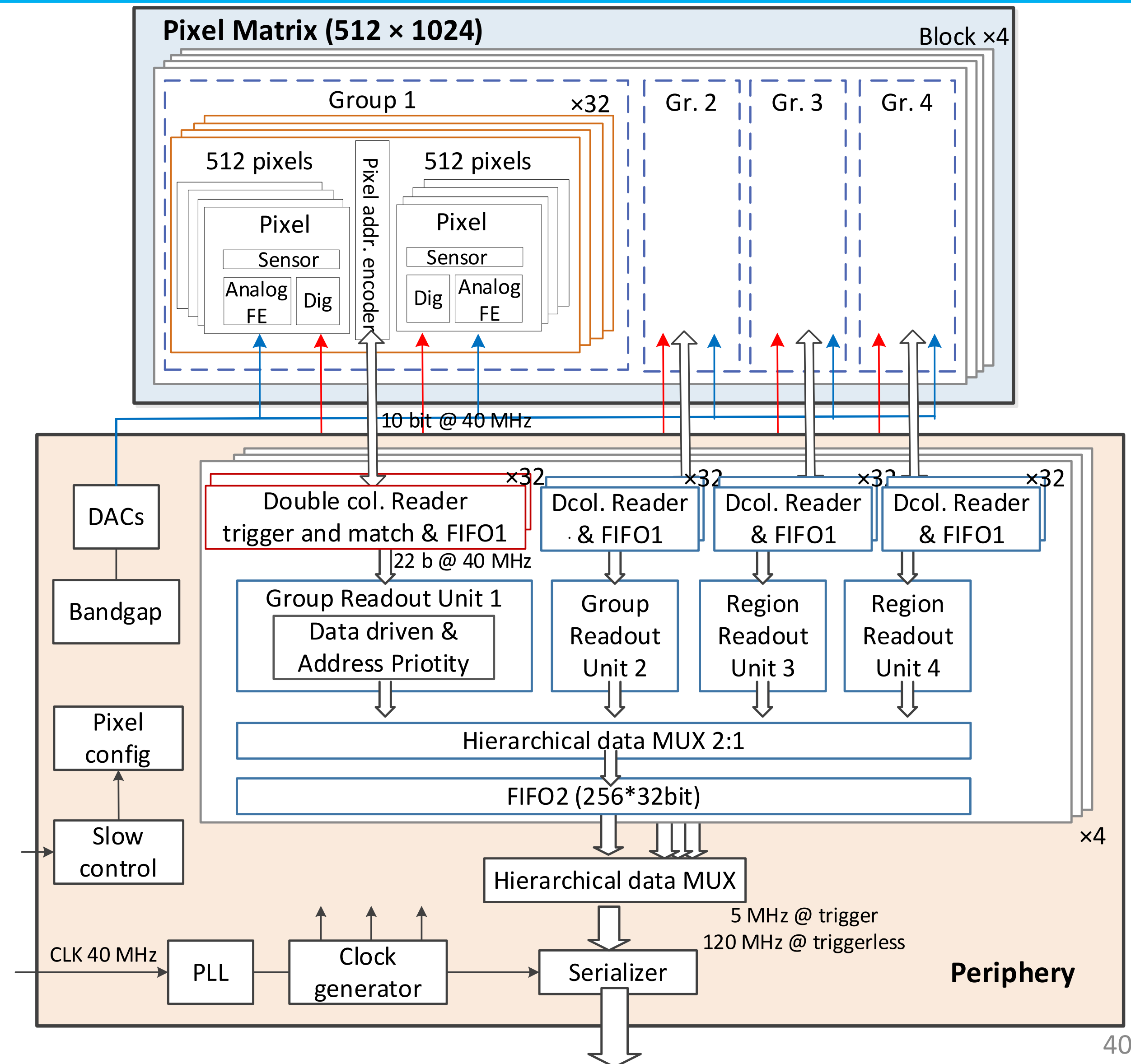




TaichuPix design

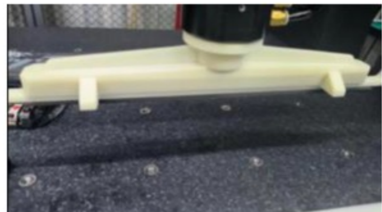
- Pixel 25 μm × 25 μm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Readout time: 50-100 ns for each pixel
- 2-level FIFO architecture
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp

    only matched event will be readout
- Features standalone operation
  - On-chip bias generation, LDO, slow control, etc



TaichuPix3 vertex detector prototype

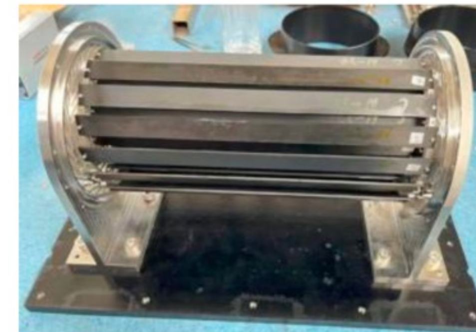
New pickup tools

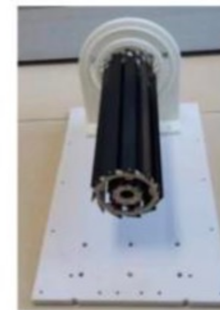


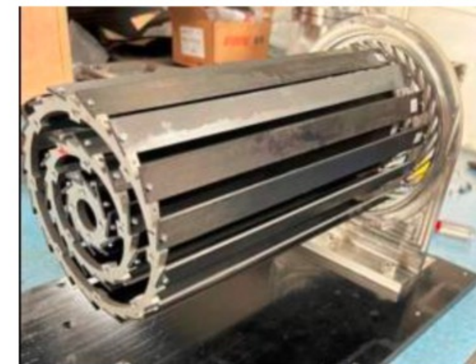
Dummy ladder glue automatic dispensing using gantry

Ladder on wire bonding machine

Dummy Ladder on holder







The first vertex detector (prototype) ever built in China

Ladder support tools

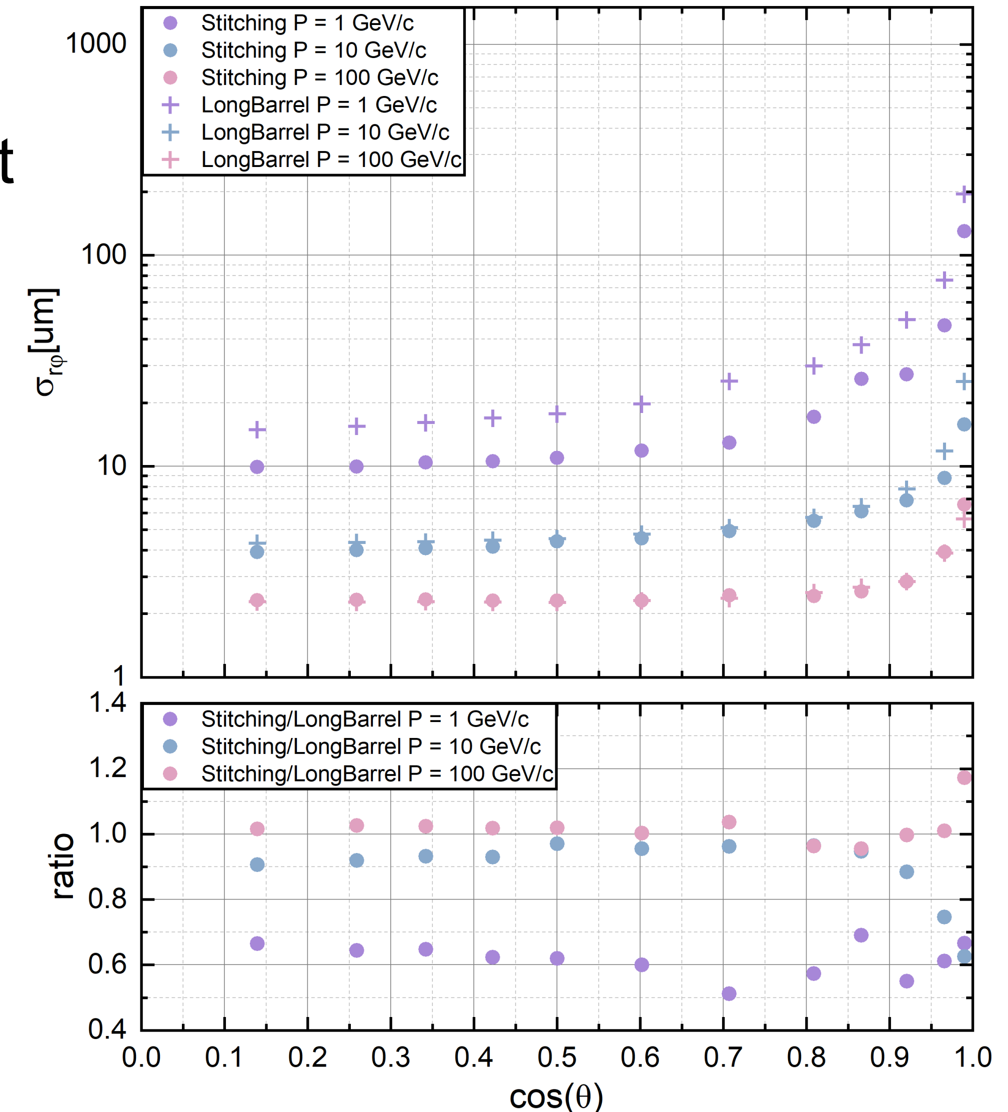
Ladder loaded on vertex detector

Research team

- IHEP: overall intergration, chip design, detector assembly, electronics, offline
  - Overall : Joao, Zhijun ,Ouyang Qun
  - Mechnical: Jinyu Fu
  - Electronics: Wei wei, Ying Zhang, Jun Hu, Yunpeng Lu , Yang Zhou, Xiaoting Li
  - DAQ: Hongyu Zhang
  - Detector assembly: Mingyi Dong
  - Physics: Chengdong Fu, linghui Wu, Gang Li
- IFAE: Chip design , Sebastian Grinstein, Raimon Casanova et al
- IPHC/CNRS: chip design , Christine Hu, Yongcai Hu et al
- ShanDong: chip design , Meng Wang, Liang Zhang, Jianing Dong
- CCNU: chip design, ladder assembly, Xiangming Sun, Ping Yang
- North West U. : Chip design Xiaoming Wei, Jia Wang, Yongcai Hu
- Nanchang U. : chip design, Tianya Wu
- Nanjing: irradation study: Ming Qi , Lei Zhang

Performance: impact parameter resolution

- Compared to alternative (ladder) option
  - – baseline (stitching) has significant improvement in low momentum case



Vertex detector Operation

- Vertex detector optimized for first 10 year of operation (ZH, low lumi-Z)
  - Low luminosity Z runs is ~20% instant luminosity of high luminosity Z runs

Table 1.4: Primary CEPC design objectives (@ 50 MW)

Parameter	Operation mode			
	H	Z	W	$t\bar{t}$
Colliding particles	e^+, e^-			
Center-of-mass energy (GeV)	240	91	160	360
Luminosity (10^{34} cm^{-2}s^{-1})	8.3	192	27	0.8
No. of interaction points	2			