Exploratory Development of 55 nm HV-CMOS Pixel Sensors

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On behalf of the CEPC Silicon Tracker Group

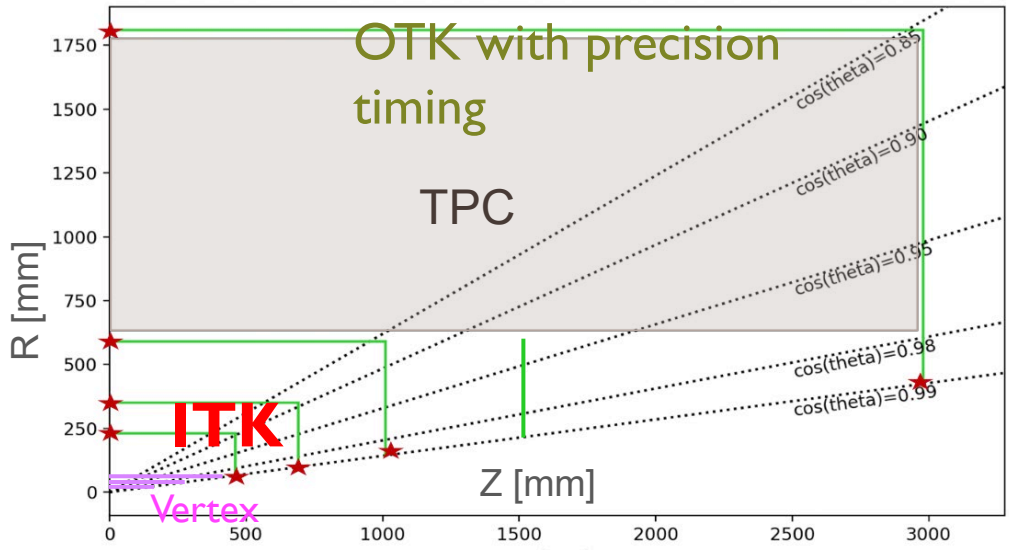
- **Background & Motivation**
- **COFFEE series outline**
  - Previous results from COFFEE2;
  - Design specifications, key simulation & preliminary test results of COFFEE3;
  - Process modification
- **Summary and Outlooks**
- **Acknowledgements**

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

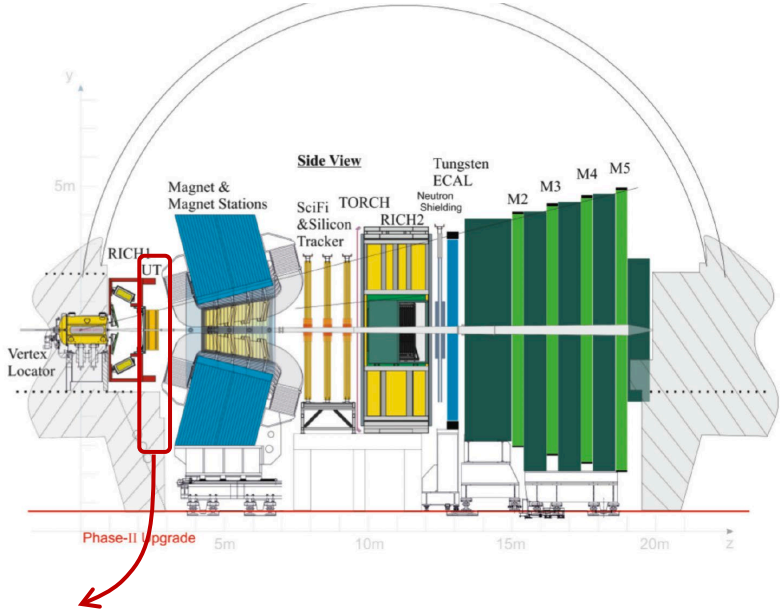
The 2025 CEPC International Workshop, Nov 5-10, 2025, Guangzhou, China

Background & Motivation

HV-CMOS sensors: current R&D targets for two applications



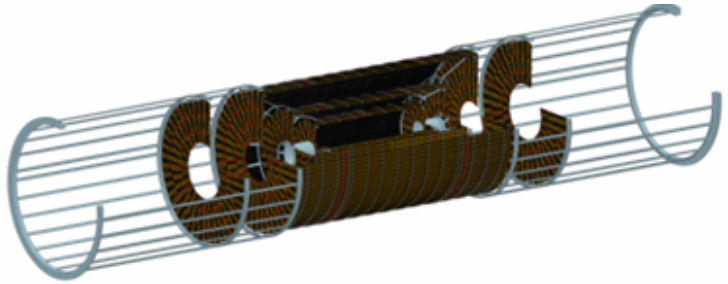
CEPC Inner Tracker (ITK)



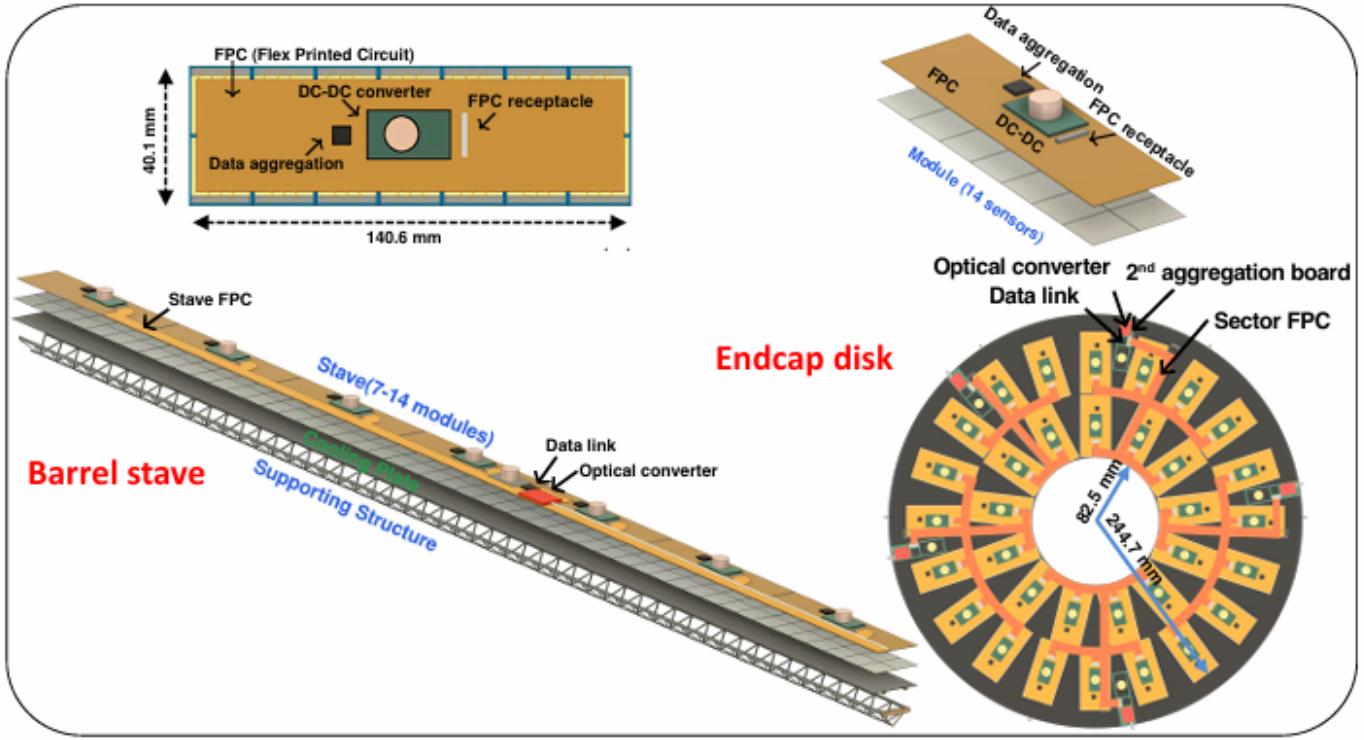
LHCb Upstream tracker upgrade (UP)

- **Requirements**: Time resolution ~ ns; Spatial resolution ~10 μm; Power dissipation < 200mW/cm^2 ;
- **Differences**:
  - LHCb requires higher hit density processing capability (~100 Mhz/cm^2) and higher radiation resistance (> 100 Mrad , >10^{15} N_{eq} /cm^2);

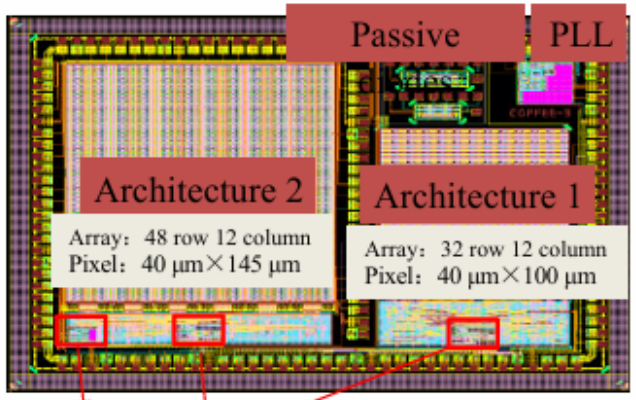
CEPC ITK Design Based on HV-CMOS Pixel Sensor



- The designed inner tracker comprises three barrel layers and four endcap layers, with a total active area of 20 m² and 47,024 sensors in total.



HV-CMOS sensor prototype (COFFEE3)



HV-CMOS sensor specification for ITK	
Sensor size	2 cm × 2 cm
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Timing resolution	3-5 ns
Power	200 mW/cm²
Process node	55 nm

Refer to Qi YAN's talk

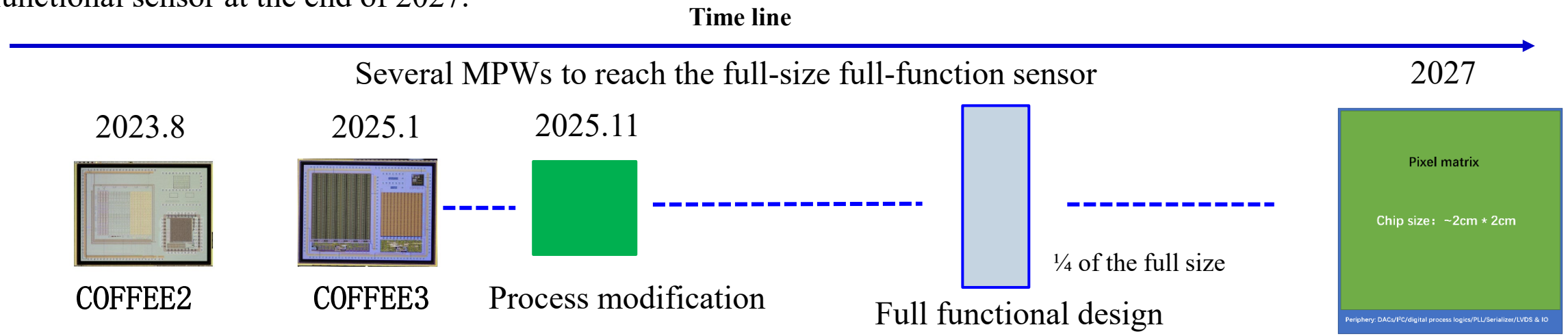
COFFEE Series Outline

We have completed two tape-outs in a commercial 55nm HV-CMOS process:

— **COFFEE2**: exploring and verifying the process characteristics;

— **COFFEE3**: verifying readout circuit structures and core performances;

The next submission will be at the end of this month; some **process modifications** will be made to enhance sensor performance. We aim have full functional design with ¼ of the full size sensor in the end of 2026, and a full size full functional sensor at the end of 2027.



Target: Time resolution ~ ns； Spatial resolution ~10 μm; Power dissipation < 200mW/cm² ;

Design Overview of COFFEE2

Three independent regions in COFFEE2:

1. **Passive diode arrays:**
   - Various sensing structures: PNW size, distances, with/without P-stop ;

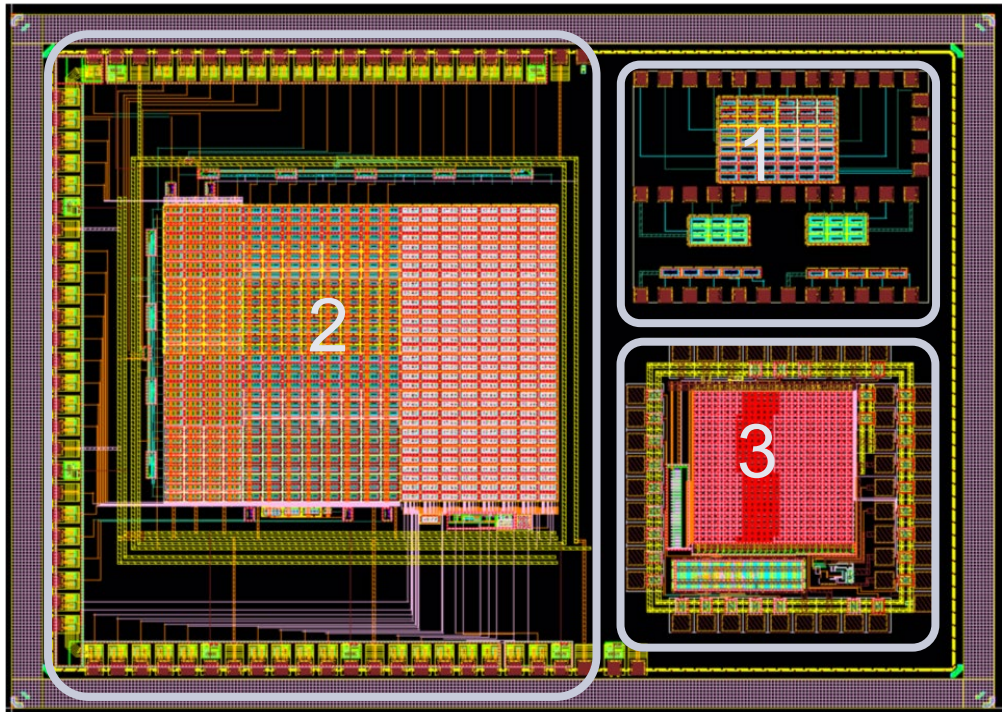
For the commercial process characteristics study

2. **An active pixel matrix including 3 variations of pixel design:**
   - To quantitatively evaluate the “cross-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip

For charge sensing diode + in-pixel AFE study

3. **An active pixel matrix with a new readout architecture:**
   - Very small pixel size 25×25μm^2 (for a HV-CMOS pixel sensor);
   - New matrix readout architecture;
   - Digital peripheral data processing included;

For new architectures in 55nm process @ Designed by KIT



The COFFEE2 design includes three independent regions.

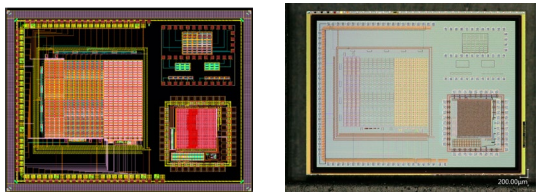
Published paper: 1. NIMA Volume 1069 P169905 (2024) https://doi.org/10.1016/j.nima.2024.169905;
2. 2025 JINST 20 C03023 . https://doi.org/10.1088/1748-0221/20/03/C03023;
3. 2025 JINST 20 C10011. https://doi.org/10.1088/1748-0221/20/10/C10011;

Results from COFFEE2

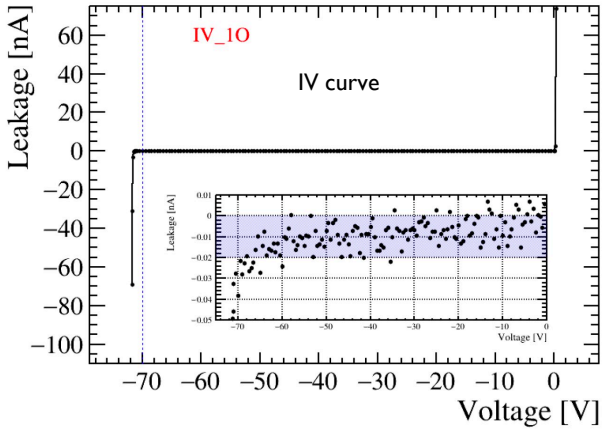
COFFEE
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

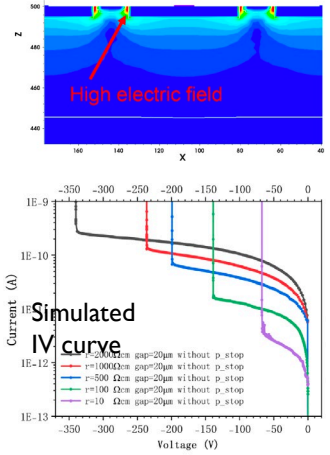
Feasibility study of a commercial 55nm HVCMOS process for future R&D

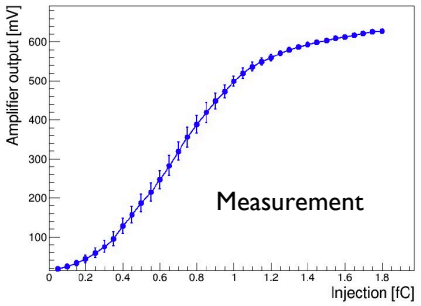
- For the sensor: breakdown voltage ~ -70V for regular resistivity wafer (10 Ω·cm)
- For electronics: the in-pixel amplifier & comparators work as the simulation predicts
- For the sensing diode + in-pixel amplifiers: clear response to laser/ ^{55}Fe / ^{90}Sr sources
- Leakage current increase from ~10pA/pixel to ~1nA /pixel after irradiation of 10^{14} n_{eq}/cm^2.

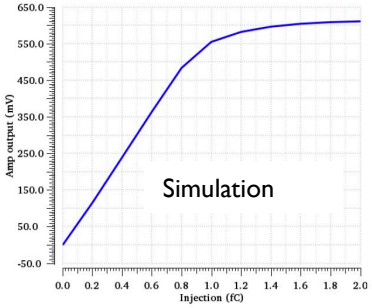


COFFEE2, the first prototype in 55nm HV-CMOS process

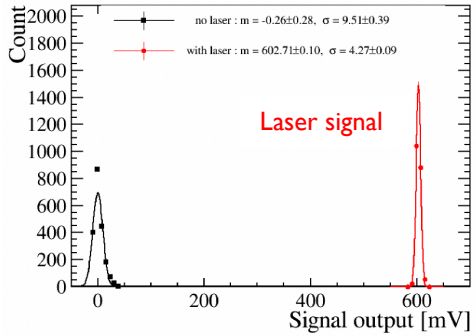


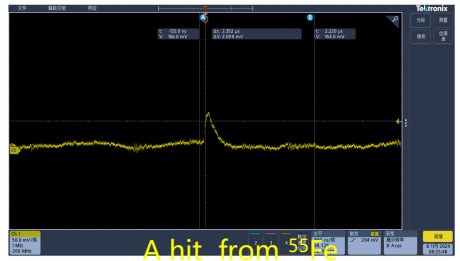




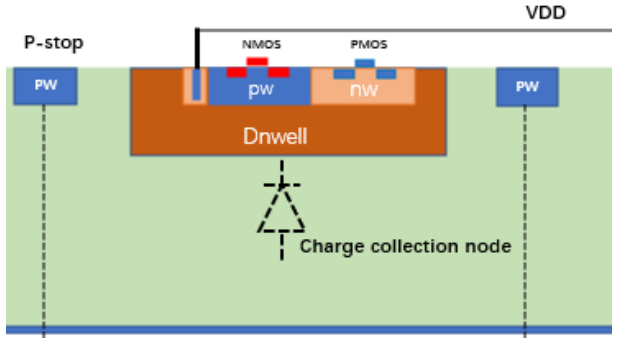


CSA output as function of charge injection

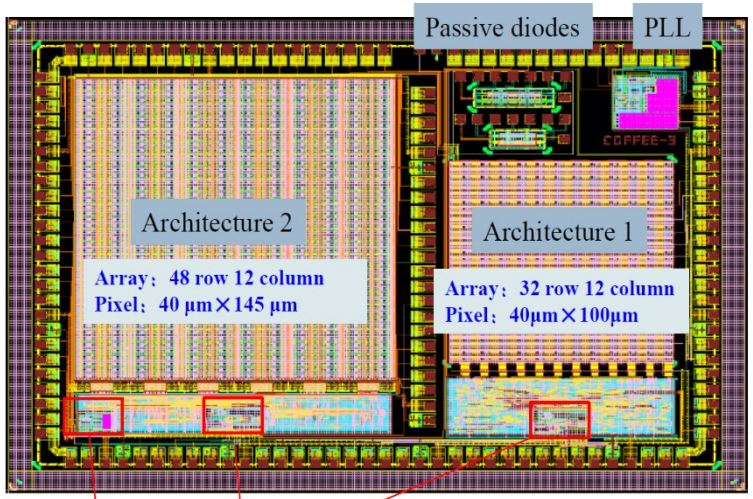




Layout and Floorplan of COFFEE3



Current process condition: triple-well, 10 Ω·cm substrate



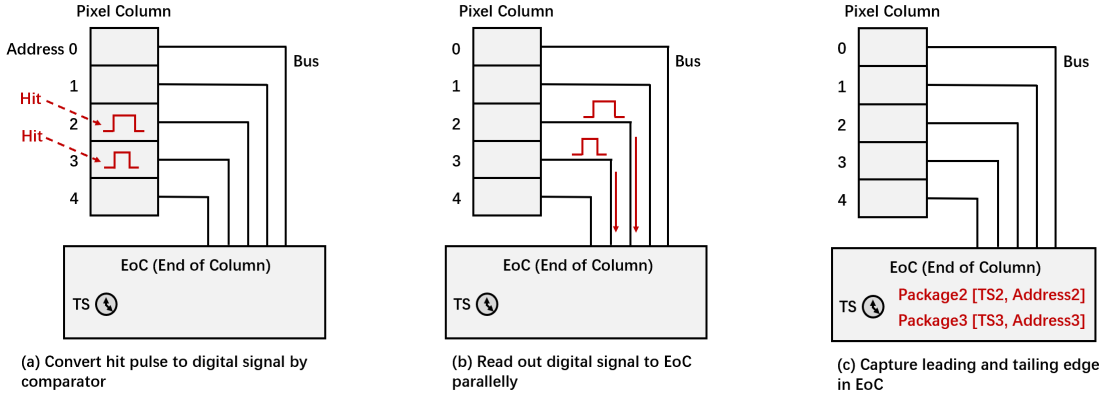
COFFEE3 layout，3×4 mm^2. 2025.1.Submitted Jan.2025. Returned May 2025.

Focus on verifying circuits and basic functionalities:

- **Two readout architectures**：with the expectation of process modifications
  - **Architecture 1**：NMOS design in-pixel, for current triple-well process；
  - **Architecture 2**：CMOS design in-pixel, for future quadruple-well process；
  - Peripheral digital readout matched with the pixel array；
- **Necessary Peripheral Function Modules**：DLL, LVDS, PLL, etc.； for IP accumulation and comprehensive assessment of overall power consumption；
- **Passive diode array**：for further research on the sensor and process；

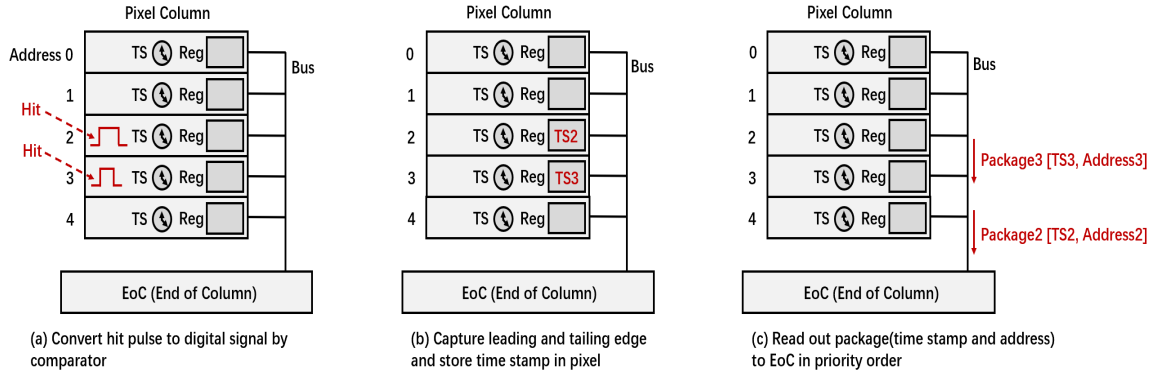
Readout Architectures

Architecture 1： In-pixel NMOS design, after digitization, each pixel data is transmitted in parallel to the bottom of the array, where time stamps are added.



Readout concept of Architecture 1, similar with ATLASPix, MightyPix, MuPix, etc

Architecture 2： employs a TDC within each pixel. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.



Readout concept of Architecture 2, similar with Timepix, RadPix, MonoPix, etc.

Advantages:

- *Low power consumption and high position accuracy*
- *High hit density processing capability*

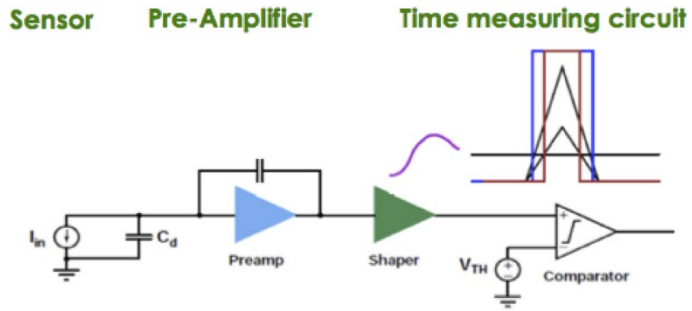
Some Key Design Simulation Performances

--- based on the expectation of using high-resistivity wafers in the future.

- Time resolution
  - Time walk;
  - Noise;
  - TDC bin size;
- Power & area estimate

C_{diode}	~200 fF （Estimated）
Signal distribution	2k - 20ke- （Assuming high-resistivity wafer）
Threshold set	5 times of noise values

Time Resolution



Typical time measurement detector structure.

$$\sigma_t^2 = \sigma_{TW}^2 + \sigma_J^2 + \sigma_{TDC}^2 .$$

（TOT compensation not included）

Signal charge distribution、analog front-end design、comparator threshold setting, etc.

Electronics noise、threshold inconsistency from pixel to pixel, etc.

TDC quantization noise：
Time stamp bin size/√12

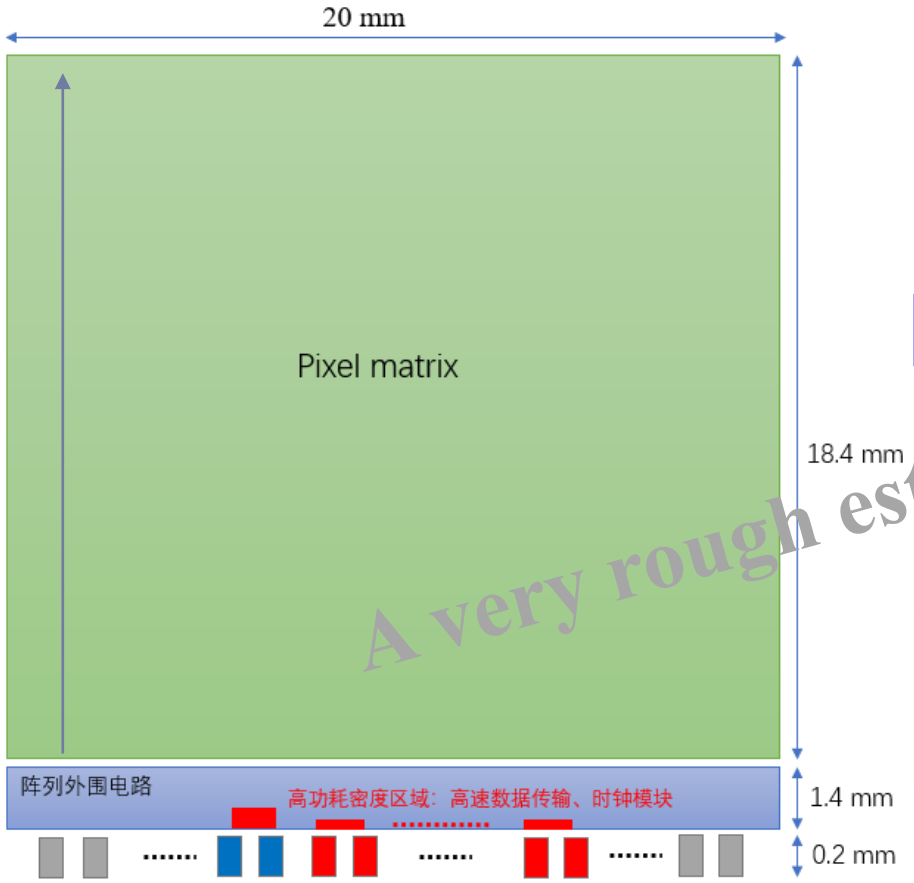
$(4\ \text{ns})^2$ $< (2\ \text{ns})^2$ $< (2\ \text{ns})^2$

Time resolution < 5 ns

The current analysis does not incorporate TOT compensation, clock delay (~1ns, compensable), or clock jitter (ps-level) effects.

The final performance needs to be verified through testing and highly depends on the final process condition we could access.

Power & Area Estimate



Estimated layout of a full size HV-CMOS sensor.

Estimated overall power consumption and area (based on architecture 2)

	Pixel matrix	Peripheral	Overall
Area	20 × 18.4 mm^2	20 × 1.6 mm^2	20 × 20 mm^2
Total power consumption	~580 mW	~ 22 mW (may overly optimistic)	~ 602 mW
Power density	**~158 mW/cm^2**	**~123 mW/cm^2** （estimate one data Transmitter channel）	**~ 150 mW/cm^2** （hit density related dynamic power not included yet）

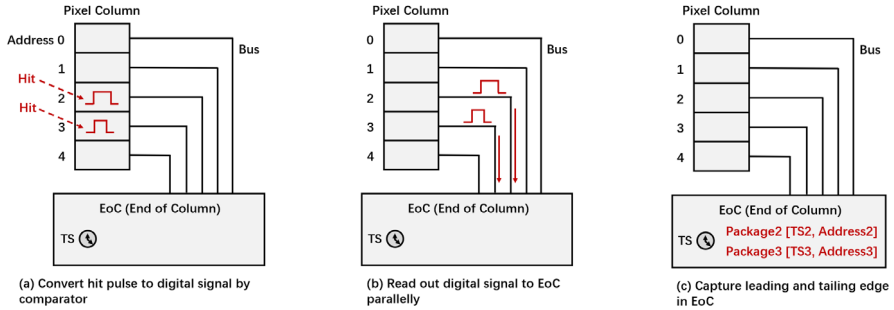
A very rough estimation

Leverage the Potential of 55nm Process Nodes

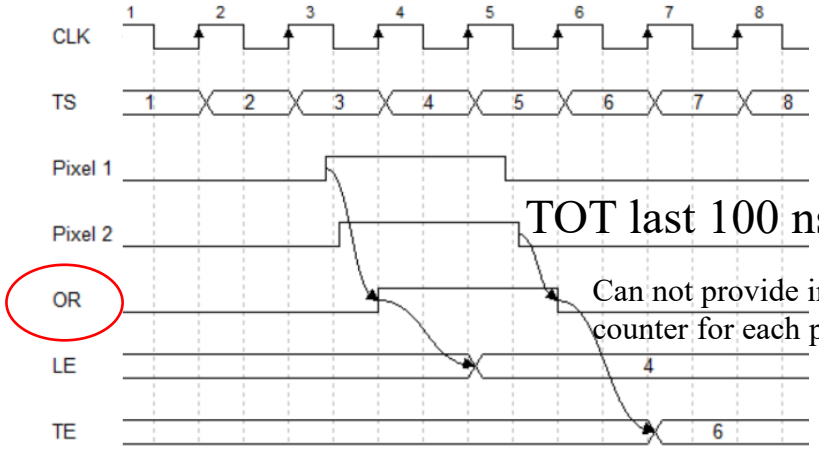
- enhance the performance upper limit of this technical type

Higher Hit Density Processing Capability: for Architecture 1

Architecture 1: Pixel Hit Parallel Transmission to Array Bottom



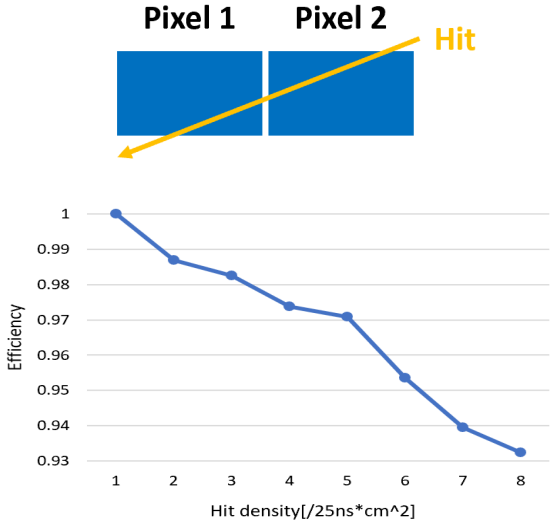
Each column shares an EoC module



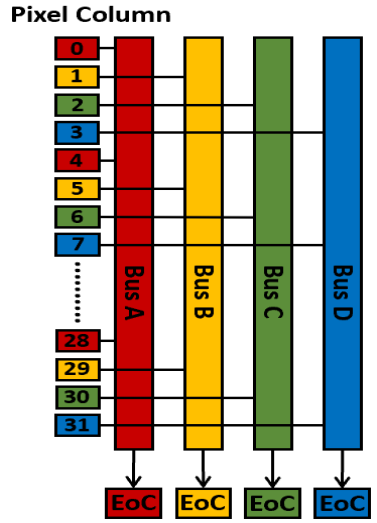
TOT last 100 ns -1.6 μs

Can not provide independent time stamp counter for each pixel at EoC

- This concept with 1 EoC for each column, while hit density increase, the timestamp information maybe inaccurate.



For high hit density, there will be some loss in efficiency.



One pixel column architecture in COFFEE3.

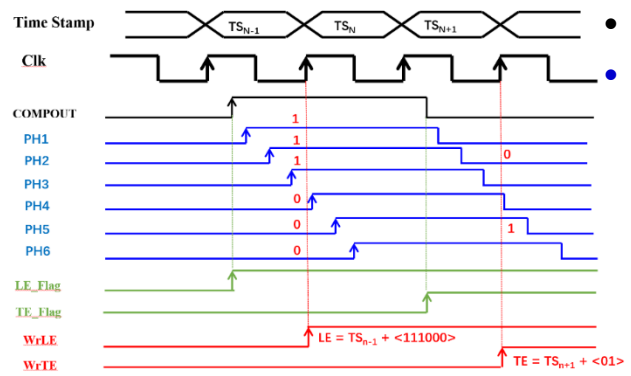
- **Limitation: while hit density increase (eg. > several tens of Mhz/cm^2)**
  - **Timestamp information inaccurate;**
  - **Efficiency loss;**
- **To handle higher hit rates: 4 EoC modules for each column, and two FSMs for each Eoc in COFFEE3.** The area of the peripheral digital circuits does not significantly increase (still less than 10% of the whole sensor).

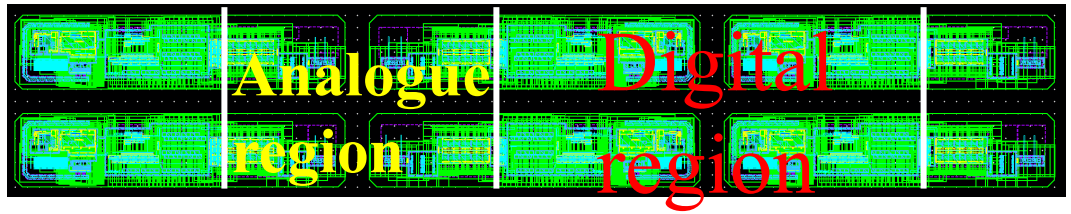
More Possibilities: for Architecture 2

Architecture 2: the event time information are recorded within each pixel.

Time stamp bin size:

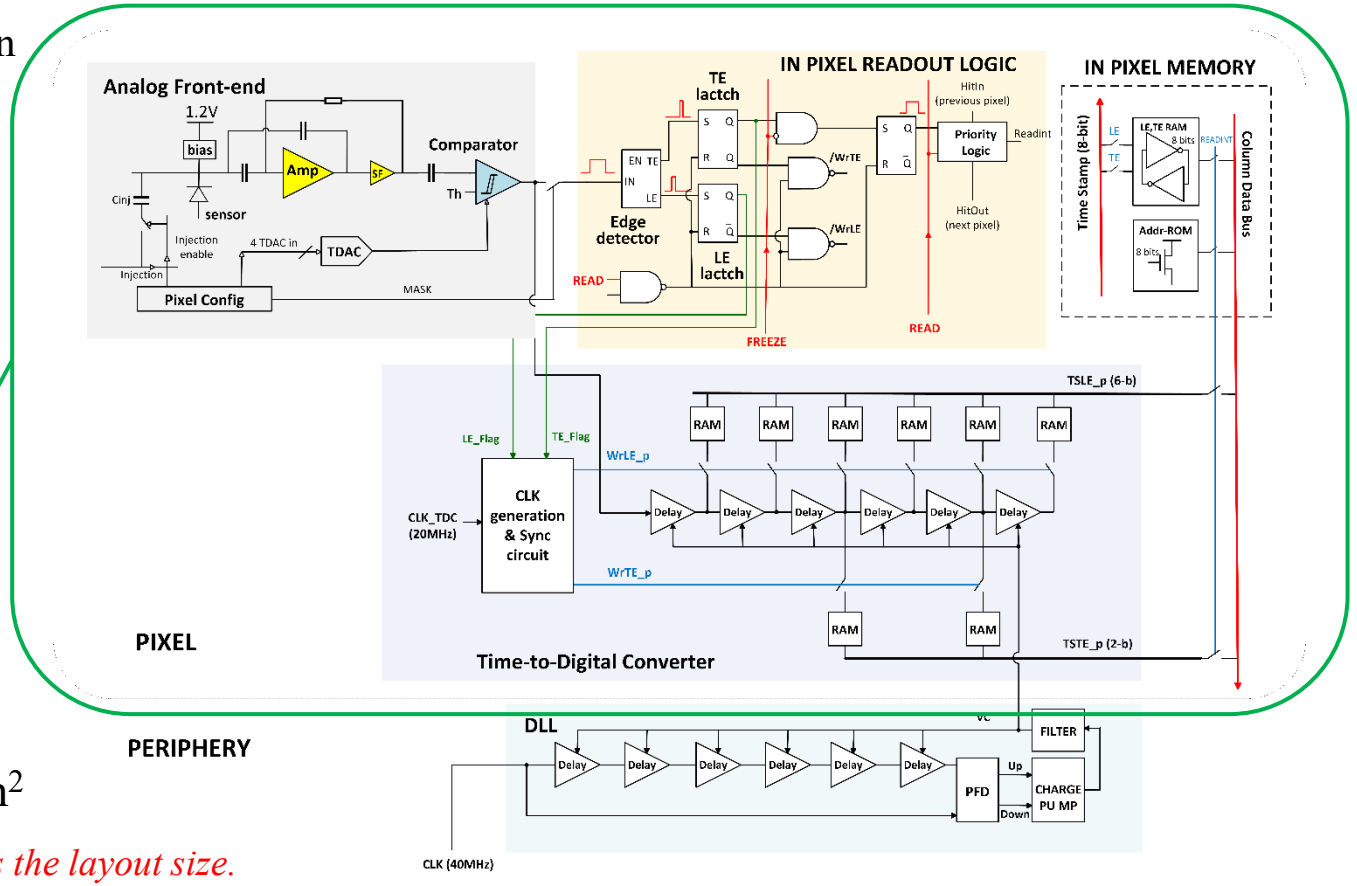
- Coarse: 25ns
- Fine: 25ns/6 = 4.16ns





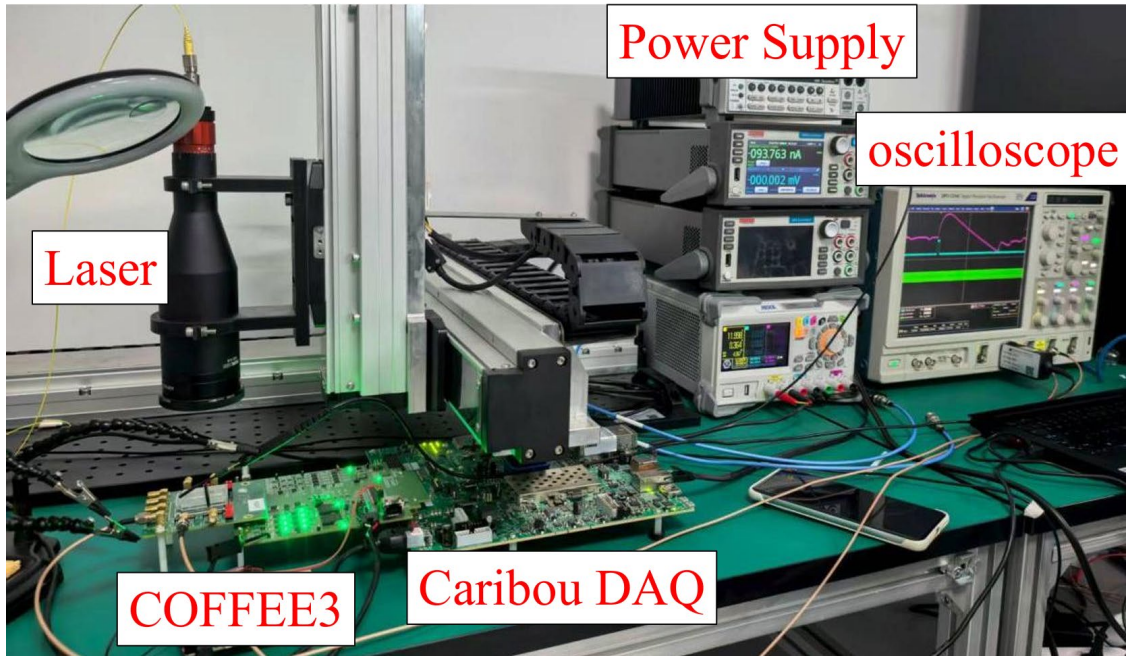
Layout of 2×3 pixels， signal pixel size is 40×145 μm²

**The actual manufacturing size will be scaled down to 0.9 times the layout size.*



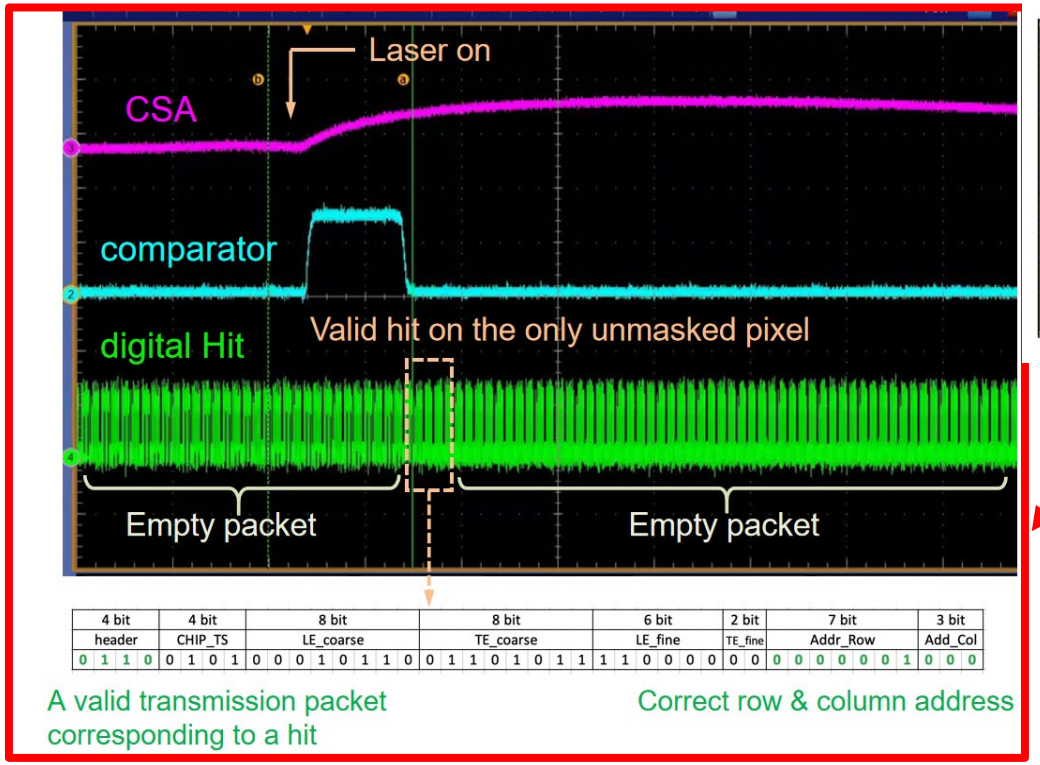
➢ More integration in-pixel: The analog front-end, comparators, in-pixel DACs, priority readout structure, memories, and TDCs have all been integrated within a limited pixel area. This further enhances the capability of HV-MAPS to provide high-precision hit information in high hit density applications.

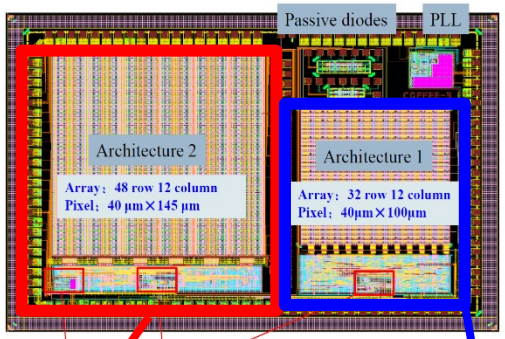
The Preliminary Test Results of COFFEE3



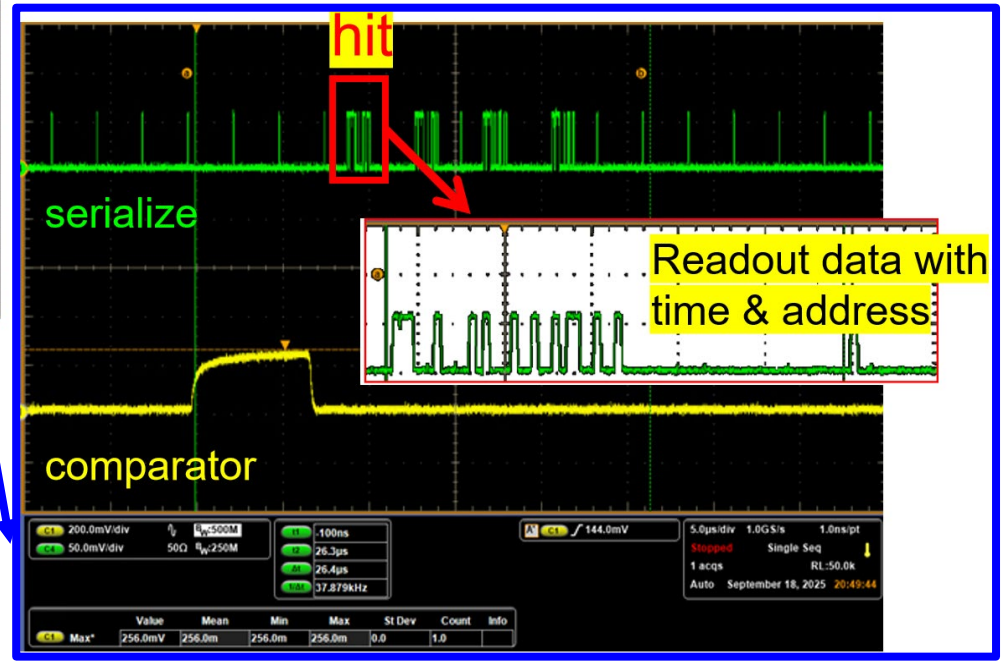
Response of Full Readout Chain with Laser Test

Architecture 2: in-pixel TDC





Architecture 1: in-pixel NMOS design



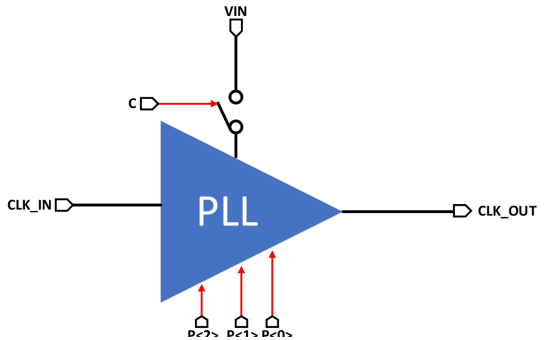
The full readout chain works for both of the two readout architectures.

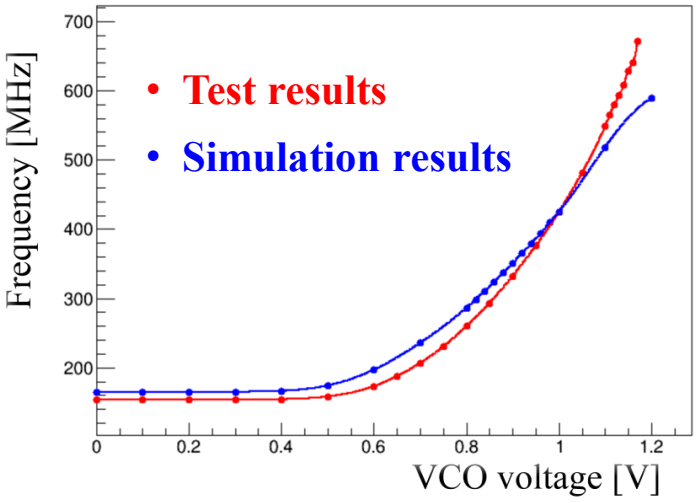
Sensing diode → in-pixel (CSA\comparator\TDC) → EOC (digital peripheral) -> data link-> DAQ

Test Results of Functional Modules

All the functional modules designed in COFFEE3 work:

- PLL works ups to 640Mhz





- LVDS driver/receiver works at 640 Mhz support 1.28 Gbps data link

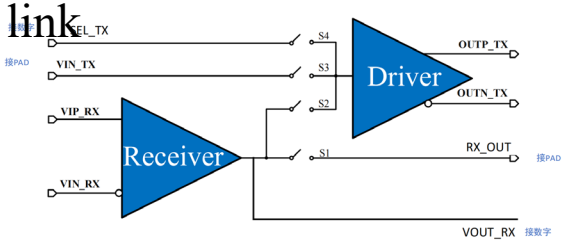
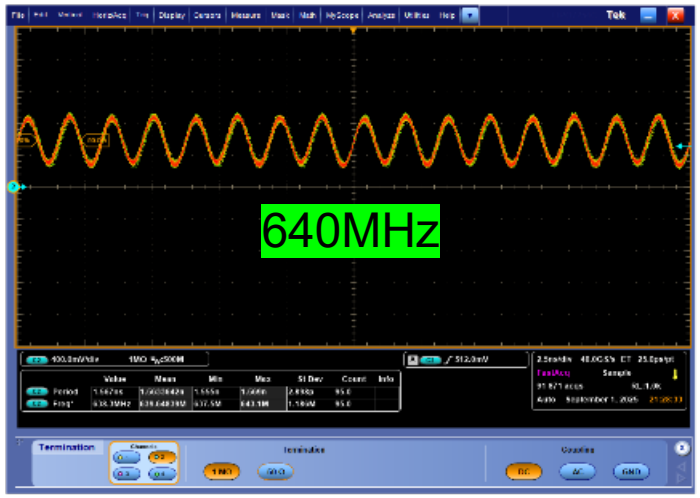
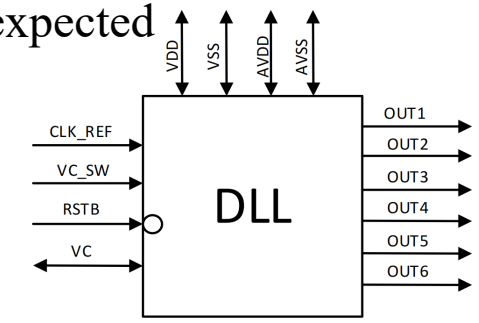


Fig 3.1.1 LVDS block diagram



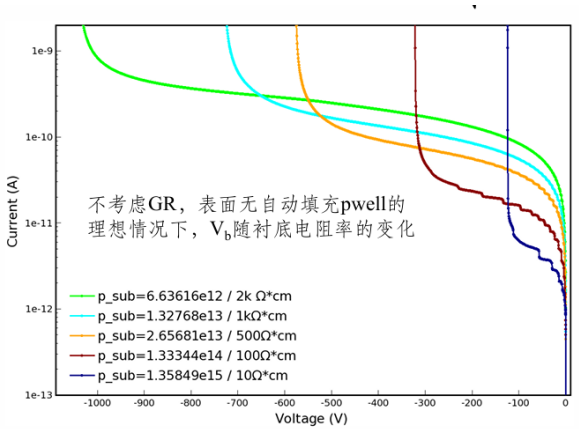
- Delay line for in-pixel TDC works as expected



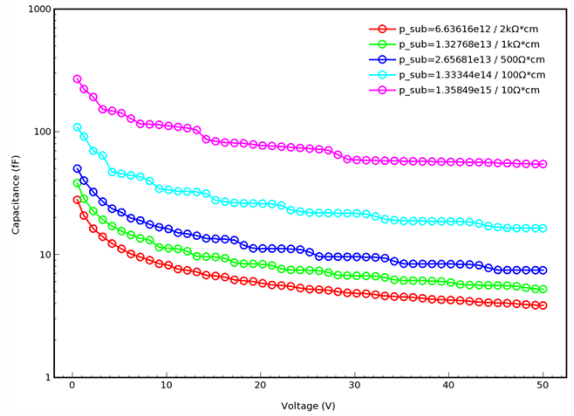
Process modifications for HV-CMOS pixel sensors

Process Modification for Next Tape-out

Modifications :

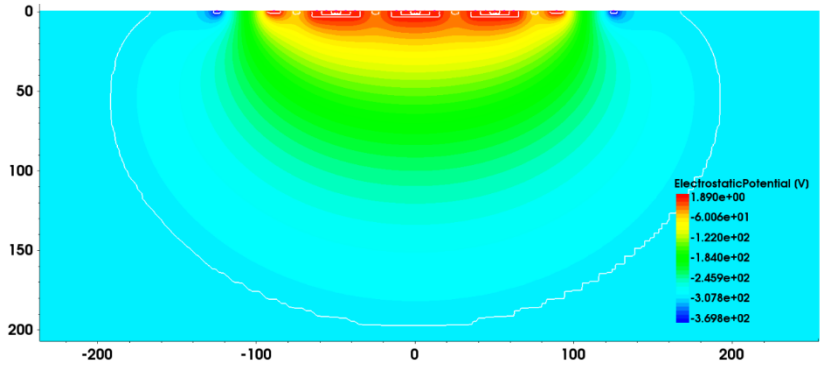


➢ Breakdown V: **70 --> > 400V**



➢ Capacitance of VDNW/p-sub:
~ hundreds fF --> ~ tens of fF

- Deep-PW & Very-deep-NW added;
- Use >1k Ω·cm wafer;
- Change doping rules affecting breakdown voltage;



➢ Depletion depth: ~10 μm → >200 μm

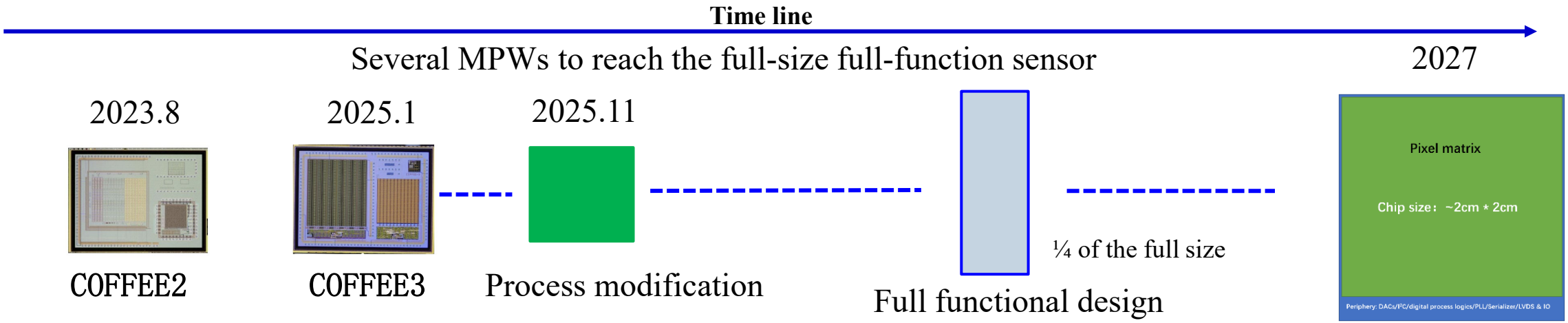
The first submission will be in this month!

Answers to many key questions can be expected!

Huge S/N gain: Signal increase >10 times, while C_{diode} reduce

Summary and Outlook

- We have complete the design of COFFEE2/3 in a commercial 55nm HV-CMOS process;
- The preliminary test results are positive, more performance tests are in progress;
- The first submission to validate the **process modification for HV-CMOS pixel sensors in 55nm process** will be in the end of this month. A key step for the final chip.
- Future designs will be based on the readout architecture validated by COFFEE3 and the modified process characteristics, to complete the full-function and full-size chip design as soon as possible.



Target: Time resolution ~ ns; Spatial resolution ~10 μm; Power dissipation < 200mW/cm^2 ;

Acknowledgements

- **Chip design:**
  - **COFFEE2**：Weiguo LU, Mei ZHAO, Kunyu Xie, Leyi Li, Ruoshi DONG, Yang CHEN, Xuekang LI，Xinyang GUO, Zhuojun CHEN, Yang ZHOU;

  & **Independent KIT design**: Hui ZHANG, Ruoshi DONG, Ivan PERIC；
  - **COFFEE3:** Leyi Li, Xiaoxu ZHANG，XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang CHEN，Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI，Yang ZHOU;
- **Chip test and validation:**
  - Zhiyu Xiang, Zijun Xu, Zeng CHENG，Menke Cai, Boxing Wang, Yuman Cai, Weiguo LU, Mingjie FENG, Hui ZHANG, Jianpeng DENG, Pengxu LI , Hongbo ZHU, Yiming Li …….

……more details could also refer to the posters of this workshop

For the design:

- Xiaoxu Zhang et al. *"55 nm HVCMOS Pixel Sensor: Readout Architecture Simulation, Hit Loss Analysis, and Data Transmission Optimization"*
- Leyi Li et al. *"A 55 nm HV-CMOS Pixel Sensor Design for High-Energy Particle Tracking with High Hit Rate and Precise Time Resolution"*
- Bingchen Yan et al. *"A Low-Power 55 nm HV-CMOS Pixel Sensor Readout Architecture for the CEPC Inner Tracker"*

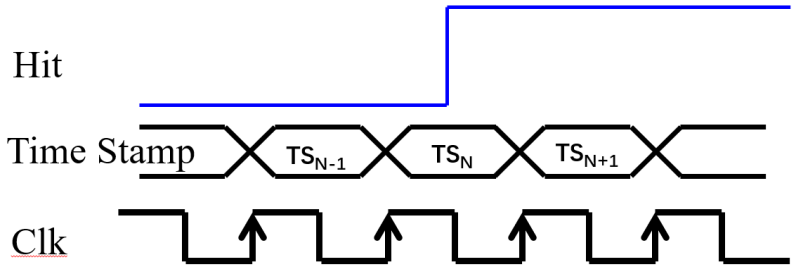
For the tests:

- Boxin Wang et al. *"Current Testing Results of the Sensing Diode, PLL, NMOS Comparator and Readout Circuit of COFFEE3 Pixel MAPS Prototype for CEPC"* ;
- Yuman Cai et al. *"Current Testing Results of the In-Pixel CSA, Discriminator, TDC, and Readout Circuit of COFFEE3 Pixel MAPS Prototype for CEPC"*

Back ups

TDC bin size

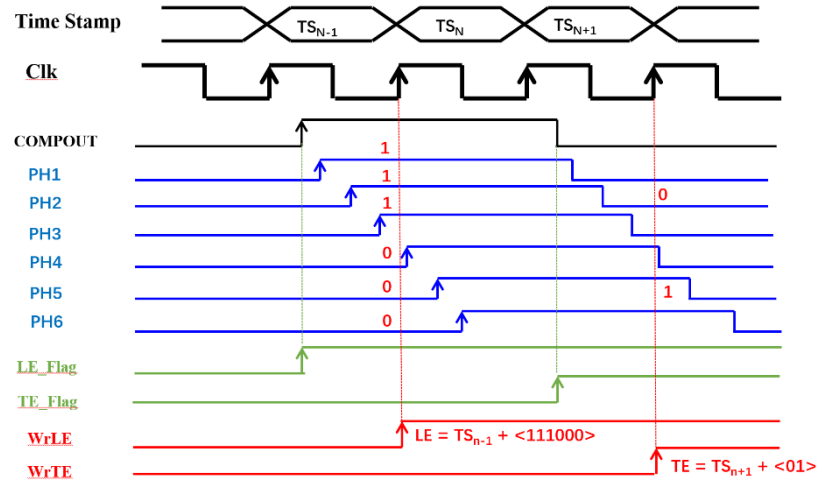
Architecture 1: Timestamp marking at the end of pixel array



- The timestamp can use any of the 40MHz 160MHz or 320MHz, corresponding to **timestamp widths of 25ns, 6.25ns, and 3.125ns** respectively.

Architecture 2: integrates pixel level coarse-fine TDC based on delay-line structure.

Working Principle of In-Pixel Coarse-fine Time Information Provision



- The pixel array employs a 40MHz coarse timestamp (25ns period). Within each pixel, a delay-line structure processes the comparator output to subdivide each coarse period into 6 bins, providing **a 4.16ns fine timestamp** for the leading edge (LE) of hit events.

Power Dissipation

Architecture 1：

- in pixel matrix: ~10μW/pixel

Architecture 2：

- in pixel matrix：
  - Two analogue FE design：11 μW/pixel and 9 μW/pixel；
  - Power for time-stamp distribution：~ 20 mW/cm^2;
  - Fine time TDC：only work in fired pixel;
  - Hit density related dynamic power consumption：not yet evaluated；

Layout area and simulated power consumption of the peripheral functional modules

Peripheral modules	area	Frequency	Power consumption
Digital module	/	40 Mhz	~ 40 mW/cm^2
PLL	360×360 μm^2	160/320/640 Mhz	0.98/1.76/2.66 mW
LVDS Receiver	70×140 μm^2	40/160/320/640 Mhz/	1.13/1.58/2.18/3.38 mW
LVDS Transmitter	112×250μm^2	40/160/320/640 Mhz	4.87/5.04/5.27/5.73 mW