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Exploratory Development of 55nm HV-CMOS Pixel Sensors: Design of the COFFEE Series Chips

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High-Voltage CMOS (HV-CMOS) pixel detectors, with excellent radiation hardness and fast signal collection enabling nanosecond-level timing and micron-level spatial resolution, are chosen as the baseline for the CEPC Inner Silicon Tracker. Our R&D using a 55 nm process has produced the COFFEE series of prototype chips. Following verification with COFFEE2, the COFFEE3 chip was designed and submitted for tape-out in spring 2025. COFFEE3 implements two readout architectures: one digitizes within each pixel and transmits data in parallel to the array bottom for time stamping, while the other uses a pixel-level Time-to-Digital Converter (TDC) with column-level readout. Both aim for sub-5 ns timing, optimized differently for hit-rate handling and power. This talk will present the COFFEE series R&D, the COFFEE3 design and performance, preliminary test results, and future plans.

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