Contribution ID: **52** Type: **Poster**

[C02] Current testing results of sensing diode, PLL, NMOS comparator and readout circuit of COFFEE3 pixel MAPS prototype for CEPC

COFFEE3 prototype chip were fabricated with 55-nm HV-CMOS process to aim for the requirements of CEPC inner tracker.COFFEE3 including 4 sectors: 1) passive sensing diode array; 2) standalone PLL block; 3) pixel matrix with in-pixel CSA and half part of discriminator, while other circuits at the end of column; 4) pixel matrix with full in-pixel CSA, discriminator, TDC, while readout circuit at the end of column. The readout out architecture of sect.3 has less cross-talk effect between digital and analog circuit, which is more suitable with the current triple-well HV-CMOS process. The sect.4 could handle higher hit density rate, while need more R&D effector. The current testing results of the first 3 sectors are presented in this poster.

Primary authors: WANG, Boxin (Institute of High Energy Physics, CAS); WANG, Jianchun (Institute of High Energy Physics, CAS); WEI, Xiaomin (Northwestern Polytechnical University); ZHOU, Yang (Institute of High Energy Physics, CAS); XIANG, Zhiyu (Institute of High Energy Physics, CAS); ZENG, Cheng (Institute of High Energy Physics, CAS); LI, Leyi (Institute of High Energy Physics, CAS); CAI, Mengke (Institute of High Energy Physics, CAS); LU, Weiguo (Institute of High Energy Physics, CAS); ZHANG, Xiaoxu (Nanjing University); LI, Yiming (Institute of High Energy Physics, CAS); CAI, Yuman (IHEP); XU, Zijun (Institute of High Energy Physics, CAS)

Presenter: WANG, Boxin (Institute of High Energy Physics, CAS)

Session Classification: Poster

Track Classification: Detector and System: 12: Silicon Detector