Contribution ID: **59** Type: **Poster**

A low-power 55 nm HV-CMOS pixel sensor readout architecture for the CEPC Inner Tracker

The Inner Tracker (ITK) for the Circular Electron Positron Collider (CEPC) has identified High-Voltage CMOS (HV-CMOS) pixel detectors as the most promising technical solution. Driven by the stringent performance requirements of the CEPC ITK, we have launched the COFFEE (CMOS sensOrs in Fifty-FivE nanometer procEss) series of design explorations, leveraging a commercial 55 nm HV-CMOS process. Building on the initial validation results of the COFFEE2 prototype, we proposed a pixel readout architecture specifically designed to minimize the sensor’s power consumption—an optimization that enables the adoption of a simplified cooling system, thereby facilitating the development of a detector system with low material budget. To validate this design concept, a 32×12 pixel array (integrated with corresponding peripheral digital modules and high-speed low-voltage differential signaling (LVDS) data transmission modules) was designed and implemented in the COFFEE3 prototype. This paper presents the detailed design of COFFEE3 and its preliminary test results, while also discussing strategies for further optimization

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Session Classification: Poster

Track Classification: Detector and System: 12: Silicon Detector