

Current testing results of the in-pixel CSA, discriminator, TDC, and readout circuit of COFFEE3 pixel MAPS prototype for CEPC

To address the requirements of CEPC inner-tracker, the COFFEE3 chip was developed using an advanced 55nm High Voltage CMOS (HV-CMOS) process for high spatial and time resolution and low power consumption. COFFEE3 is designed to validate two distinct readout architectures integrated on a single chip, focusing on verifying circuit functionality and core performance. This poster presents the preliminary test results for the left-side array, which features a more complex in-pixel design incorporating a full CMOS-based CSA, discriminator, TDC, and priority-based readout, targeting higher hit-rate environments. Bench tests utilizing laser and radiation sources successfully demonstrate the basic functionality of the in-pixel circuits and the full readout chain at digital peripheral which also including the serializer and LVDS transceivers.

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