SIPAC：A SiPM readout ASIC for the CEPC Detector

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Outline

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- Introduction
- Circuit Design
- Test Result
- SIPAC1 Design
- Conclusion

Introduction

◆ Application:

- CEPC: readout ASIC for E-CAL & H-CAL

◆ Protype ASIC requirement:

Characteristics	Value
Charge Dynamic Range	1.28 pC~3.84 nC
Charge resolution	10%@1.28pC, 1%@128pC 1%@100 MIPS
Time resolution(RMS)	200 ps @1.28pC, 100 ps @12.8pC
Detector Capacitance	≤ 100 pF
Max signal rate/channel	500 kHz/ch
ADC	10-bit
TDC resolution	8-bit
TDC bin width	100 ps
Power consumption	15mW/channel
Num. of channels	4

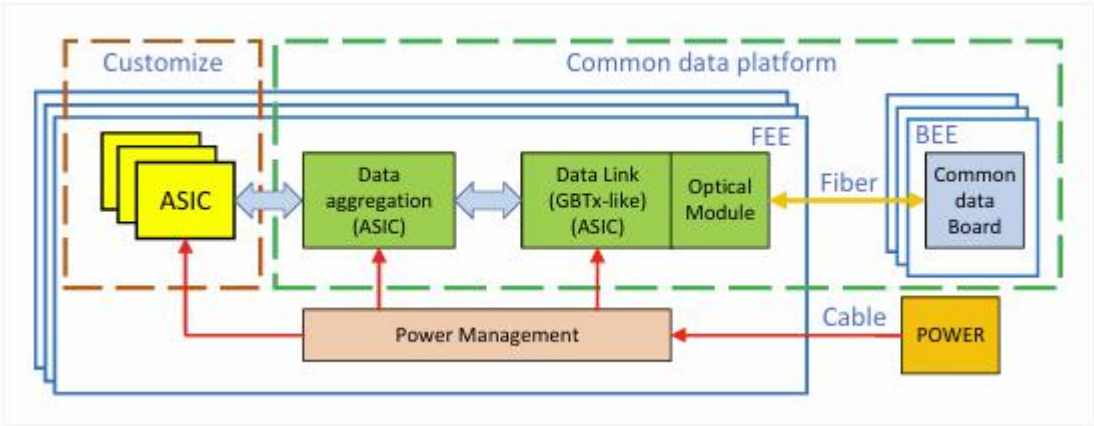


Fig. 0 : Connection diagram of the chip in CEPC

- Dynamic Range : 1 MIPS – 3000 MIPS (Prototype chip)

Introduction

◆ Architecture:

- DAC: 6 bits DAC to adjust SiPM BIAS
- Pre Amplifier : Voltage Amplifier
- Shaper : The peaking time of the output signal after shaper is approximately 150ns.
- SCA: Sampling depth 9
- SAR ADC: 10 bits SAR ADC
- Serializer:128 bits 320 MHz
- TDC : 2 Step TDC 100 ps resolution

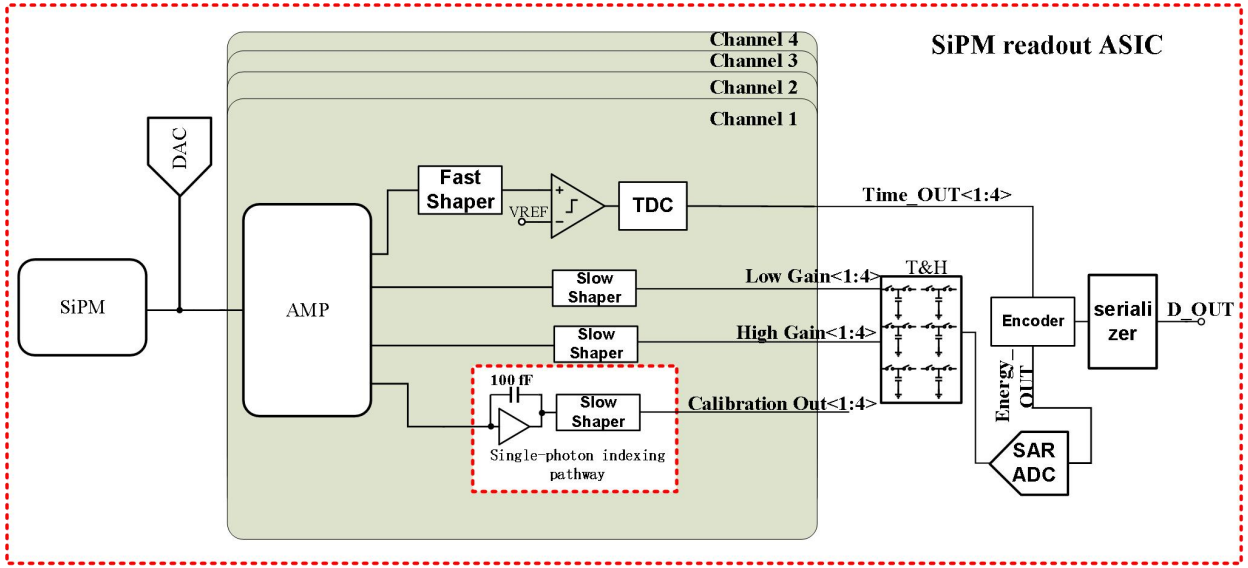
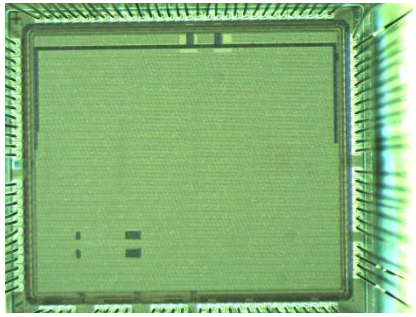


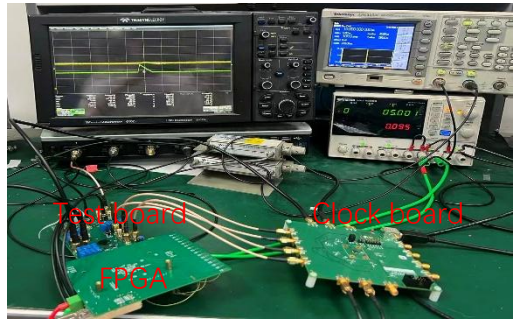
Fig. 1 : SIPAC Architecture

◆ Submitted in April 2025

◆ Tested in September 2025



The prototype of the SIPAC chip



SIPAC test system

Circuit Design

■ Amplifier and Shaper Design:

➢ Voltage Amplifier:

- AC Coupling to isolated the DAC Voltage
- Preliminarily amplify the signal

➢ Shaper:

- Use second-order RC slow shaper
- The peaking time of the output signal after shaper is approximately 150ns.

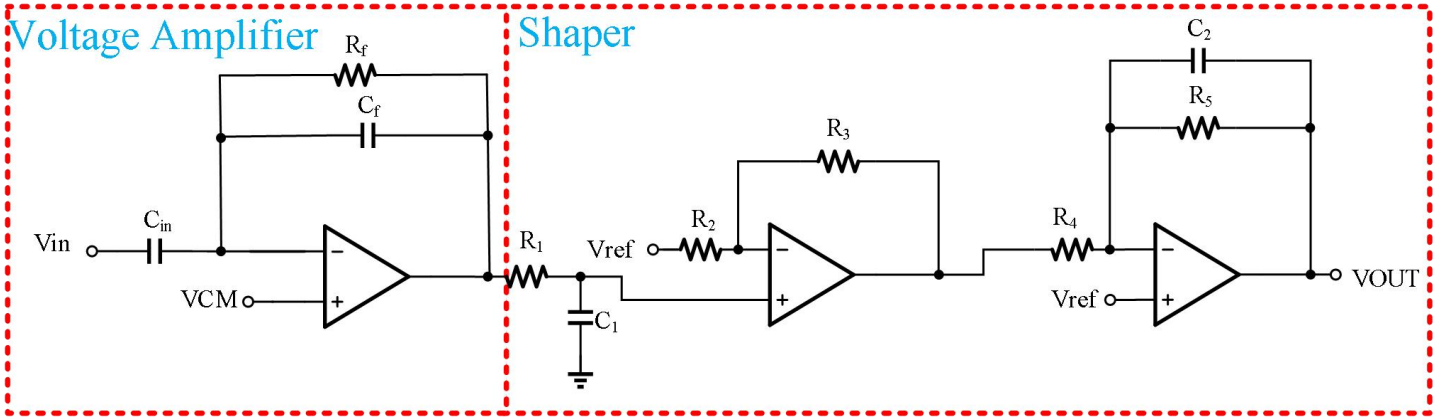


Fig. 2 : Amplifier and Shaper Design

Circuit Design

■ Discriminator:

- Positive feedback forms a hysteresis window
- Hysteresis window to prevent noise inversion
- Hysteresis window : 2 mV
- PMOS input to decrease noise

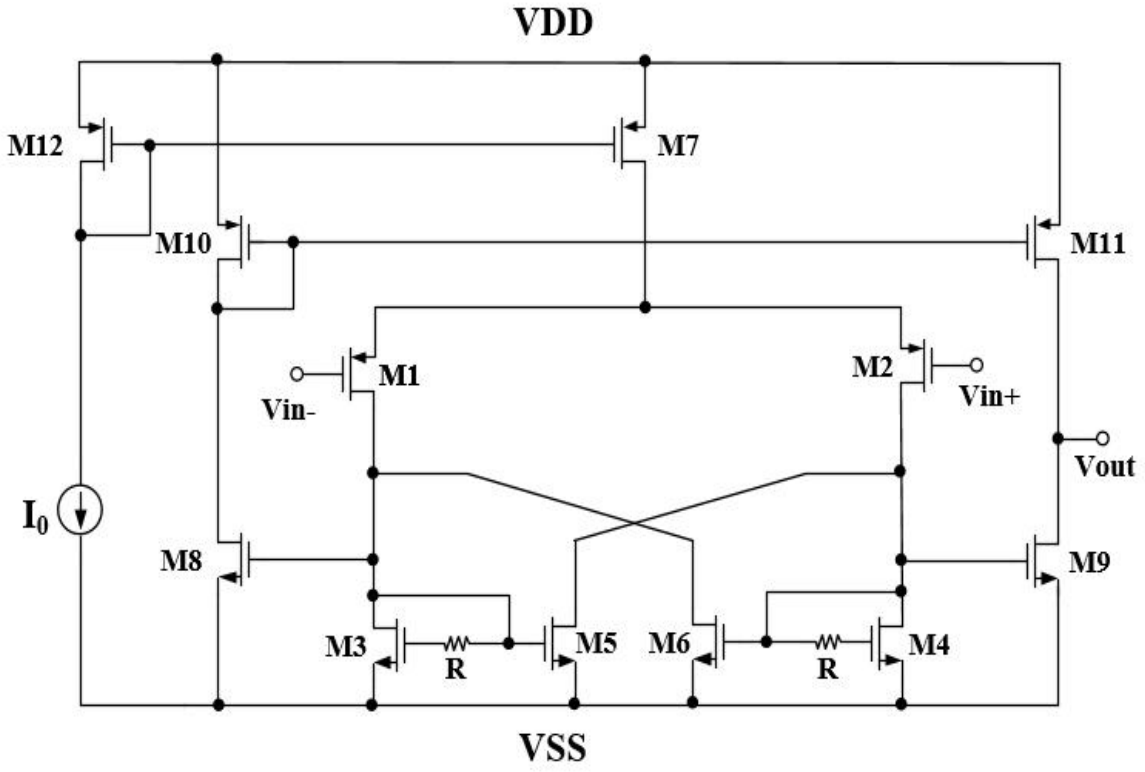


Fig. 3 : Hysteresis comparator

Circuit Design

■ TDC:

➢ Two Step TDC:

- The two-step TDC achieves coarse counting through a counter, and fine counting by combining with a delay chain. By combining the characteristics of the two structures, time measurement is realized.
- An external 320M clock is used as a refernce of the coarse counter to measure the coarse time
- The delay chain measures the fine time as a fine counter
- The delay chain is used to measure the undercounting time d_{t1} and overcounting time d_{t2} in the coarse counting period

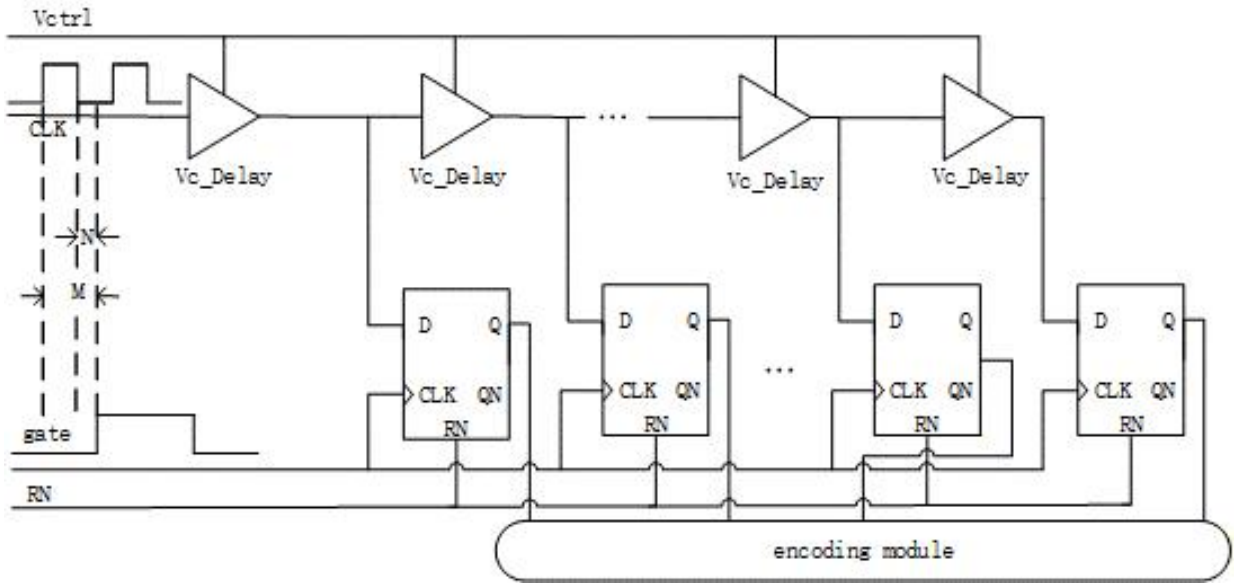


Fig. 4 : Delay Chain Circuit

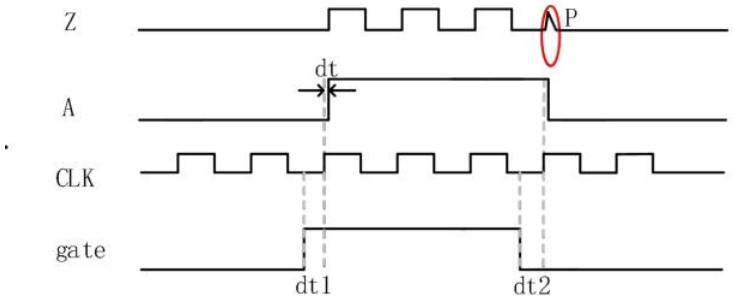


Fig. 5 : Measurement logic diagram

Circuit Design

■ ADC:

➢ SAR ADC:

- 12 bit SAR ADC ENOB 10 Bit
- Use single to differential amplifier to convert the input signal into a differential signal.
- Use segmented capacitors and offset auto-interpolation counting
- Based on the design requirements, the ADC uses a SAR ADC structure, with four channels sharing a single SAR ADC for quantization.

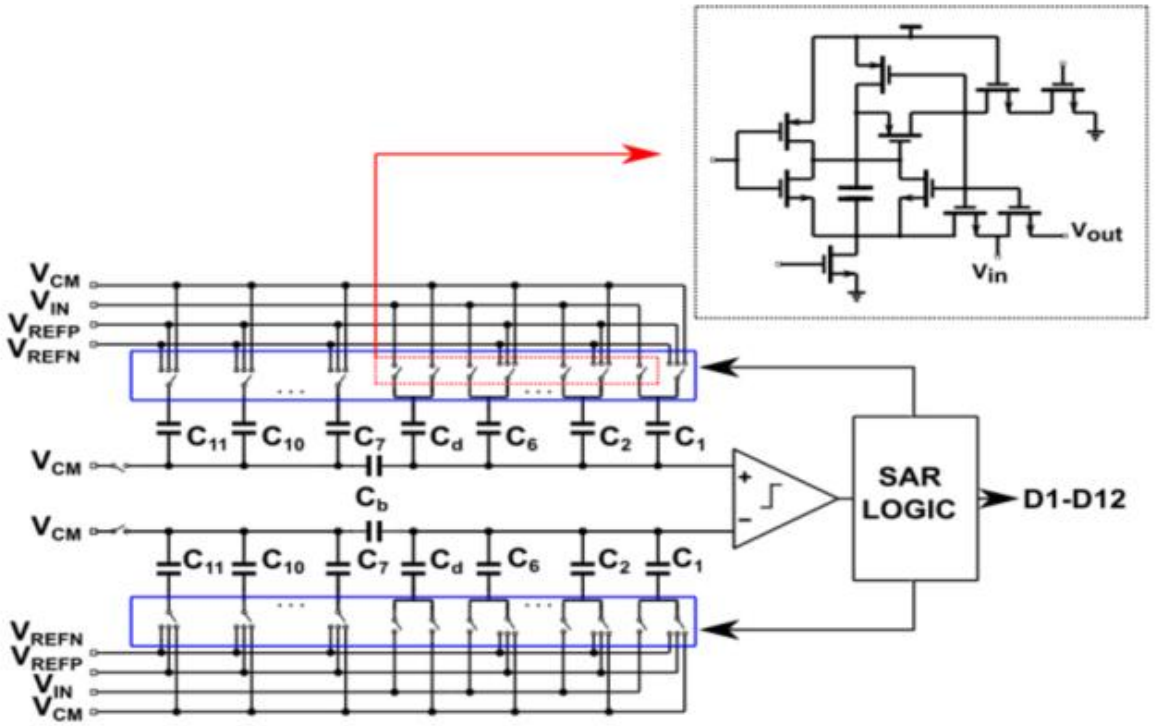


Fig. 6 : SAR ADC diagram

Test Result

■ Performance of the Amplifier:

- The Output Noise is 0.93 mV@High Gain (Fig 7(a)), equal to 0.45 pC input noise.
- The high-gain setting has a nonlinear error of less than 1%, with a dynamic range of 2.13 pC-213 pC(Fig 7(b))
- The low-gain setting has a nonlinear error of less than 3%, with a dynamic range of 213 pC-4.68 nC(Fig 7(c))

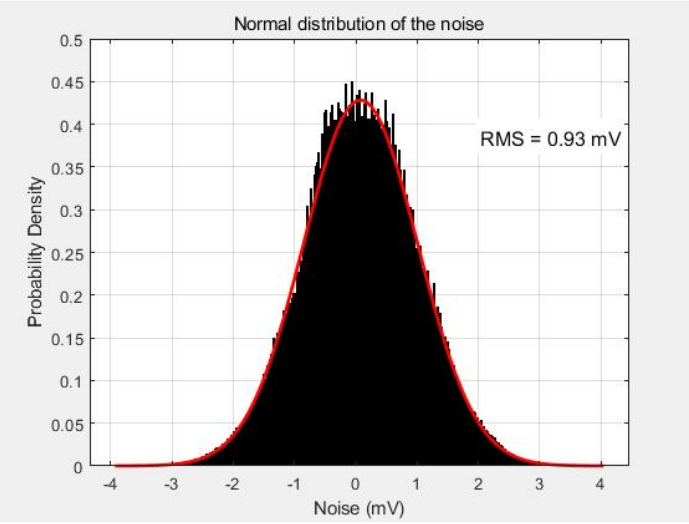


Fig. 7(a) : Output Noise
SNR=8.6@ 1 mV(4.26 pC) input

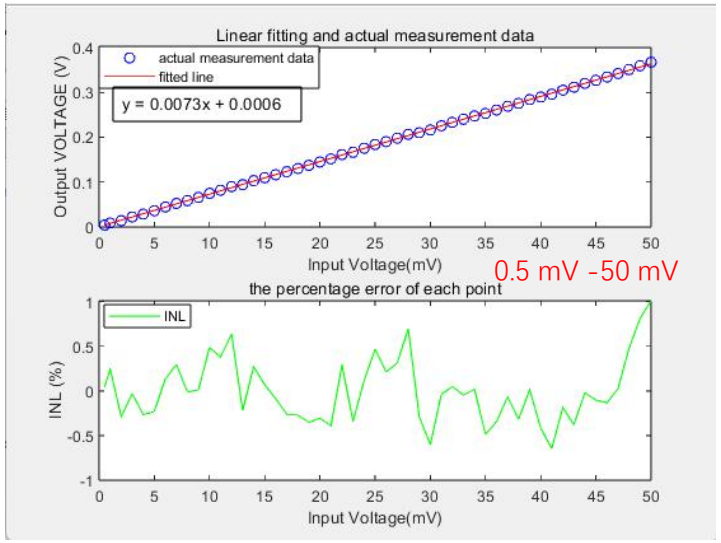


Fig. 7(b) : High Gain Nonlinear error

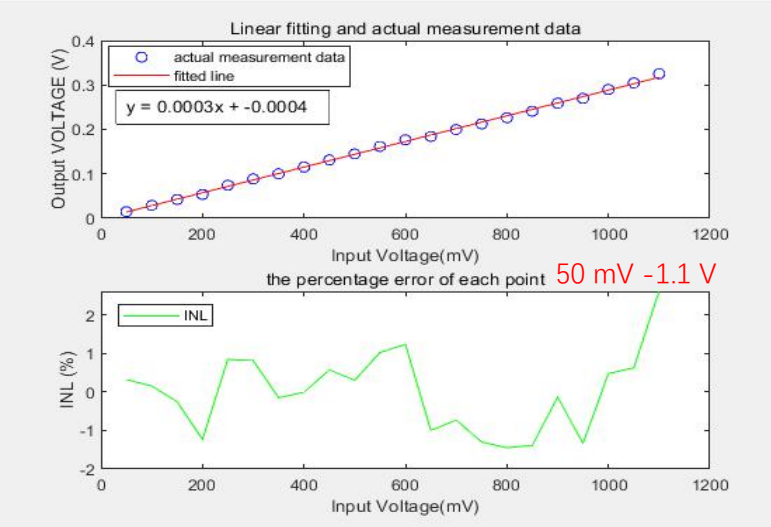


Fig. 7(c) : Low Gain Nonlinear error

Test Result

■ Performance of the TDC:

- The transfer curve of TDC shows that the LSB of TDC is 142ps which is caused by packing density and process corner and the maximum INL is 0.6 LSB(Fig 8(a))
- During multiple measurements, the TDC measurement code fluctuates within 1 LSB (Fig 8(b)).

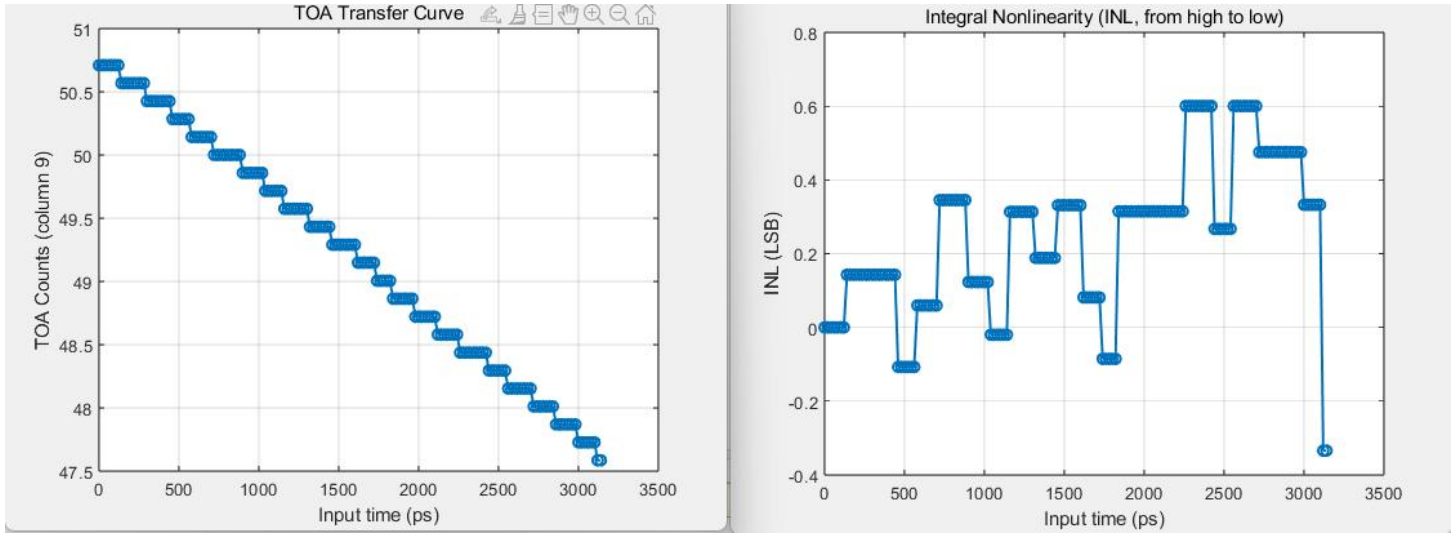


Fig. 8(a) : Transfer Curve (20 ps step)

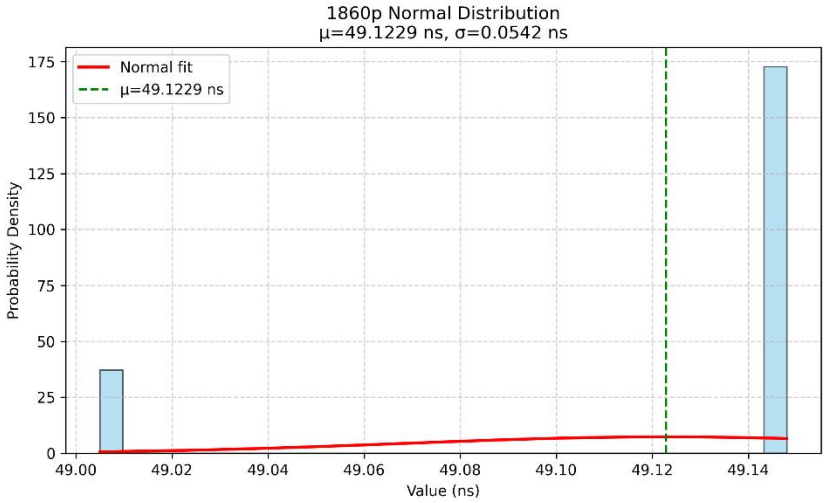


Fig. 8(b) : The normal distribution of multiple measurements

Test Result

■ Performance of the chip:

- After the codewords output by the encoder and shaper are decoded, comparing the points with the original waveform shows that some points differ significantly from the waveform.(Fig 9)
- From the diagram, we can see that the triangular portion of the ADC output deviates slightly from the shaper output. During testing, we identified the issue and traced its cause. It was due to charge sharing during sampling, which caused charge from the previous sample to remain on the buffer.

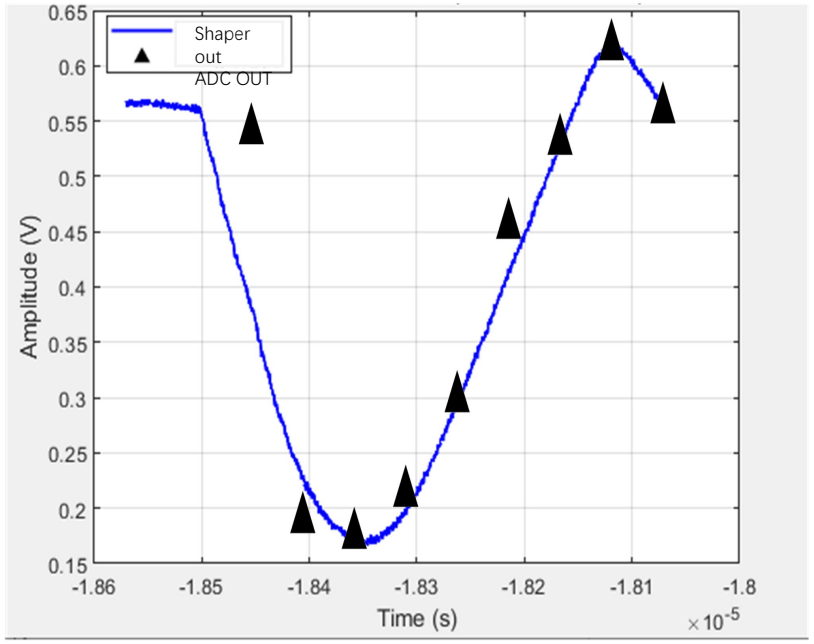


Fig. 9: Comparison between the ADC code words output by the serializer and the output of the shaper

Table. 1 : Chip Specifications Comparison

Chip Specifications Comparison		
Design Specifications		**Test result**
Input dynamic range	300 μV- 900 mV	0.5 mV - 1.1V
High gain gear gain	8	7.3
Low gain gear gain	0.5	0.3
SNR	5@300 μV(1MIP)	4.3@0.5mV(1.5 MIPS)
TDC resolution	100 ps	142 ps
ADC resolution	ENOB 10bit	testing

- As can be seen from the table, there are still many areas where our chips need improvement

SIPAC1 Design

■ SIPAC1 Design:

◆ Submitted in Oct 2025

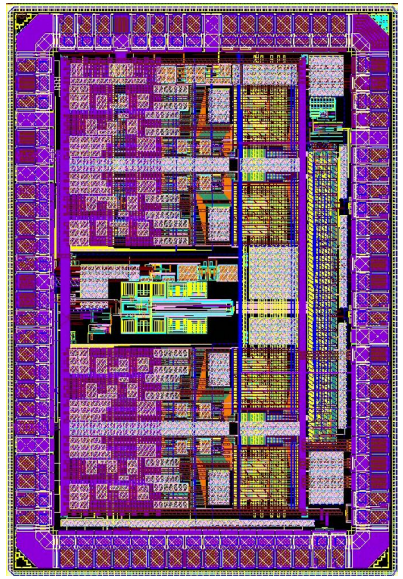


Fig. 10: The layout of the SIPAC1 chip

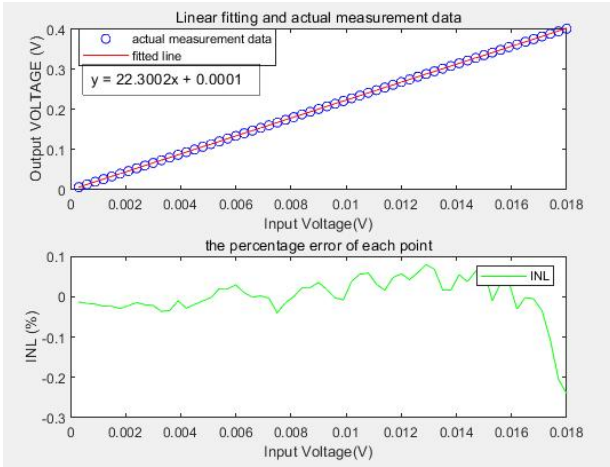


Fig. 11: The Linearity of high gain gear

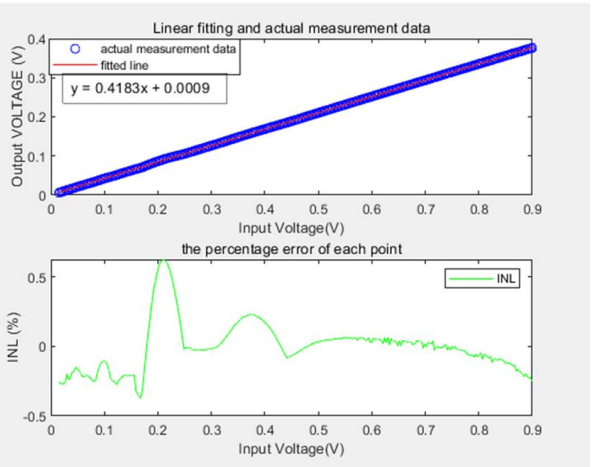


Fig. 12: The Linearity of low gain gear

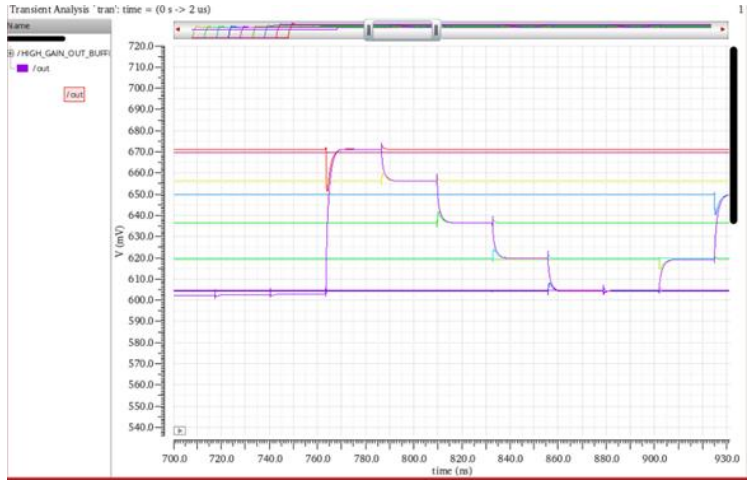


Fig. 13: Comparison between switched capacitor sampling signal and ADC quantization signal

- In the design of SIPAC1(Fig. 10), the following two main changes were made:

- Change the gain of the front-end circuit : 22.3 for high gain (Fig. 11), 0.42 for low gain(Fig. 12),which will increase the SNR to 7.
- An isolation buffer has been added to the switched capacitor output to prevent charge accumulation caused by switching between different capacitors. The simulation results (Fig. 13) show that the issue of charge accumulation during capacitor switching has been significantly reduced.

Conclusion

- We designed a SiPM readout circuit, which integrates TDC and ADC internally, with fully digital output. As the first version of the chip test, the overall functionality of the chip is normal, and all modules are working properly.
- The chip has been jointly tested with the SiPM of NDLEQR20-3030 as well as with 4mm*4mm glass and 3mm*3mm BGO. The chip can respond to the SiPM signals, and the source energy spectrum is under testing.
- Some issues were also found during the testing. The issues found in this test have been resolved. The chip is taped out again in October. The chip will be tested in March 2026.

Thank You ！