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SIPAC A SiPM readout ASIC for the CEPC Detector

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The Circular Electron Positron Collider (CEPC) is proposed for Higgs boson research, and will includes several detectors, such as the Electromagnetic Calorimeter (ECAL), Hadronic Calorimeter (HCAL), and Muon detector. Silicon photomultiplier (SiPM) is widely used in these detectors for light conversion. This paper presents a prototype design of SIPAC (SiPM readout ASIC for calorimeter).

Table 1 outlines the readout requirements of the ECAL and HCAL. Given the limitations of existing commercial chips and the CEPC detector’s requirement for a large-scale deployment of SiPM and their associated readout circuits, a dedicated SIPAC readout chip has been developed. With a maximum input charge of 3.84 nC, employing a CSA as the front-end amplifier would necessitate an impractically large input capacitor. To realize SiPM voltage adjustment, AC coupling is implemented between the preamplifier and the SiPM. Furthermore, given the slow response of the SiPM signal after passing through the crystal, SIPAC utilizes voltage amplifier as the front-end solution. Given the critical impact of the noise on time and energy resolution, the design of the shaper is critical. The energy path employs a slow shaper with two stages of low-pass filters, achieving an SNR of 8, while the timing path uses a fast shaper with a Bandpass filter, achieving an SNR of 12. Signals after shaping are sampled or compared, then quantized by the ADC or TDC and read out by the digital module. The four channels’ switched capacitor sampled signals are processed by a shared ADC and serializer for conversion and output, with each channel featuring a dedicated TDC. Figure 1 shows the overall architecture.

To address the gain variations between different SiPMs, an on-chip DAC is integrated into each channel for precise gain calibration of each SiPM. AC coupling is implemented for signal transmission, effectively isolating the adjustment effects of the DAC from the readout circuit. The signal after shaper is sampled by a switched-capacitor circuit and digitized by the SAR ADC for energy measurement. As shown in Figure 2, the post-simulation results indicate that within the input dynamic range of 1.28 pC to 3.84 nC, the nonlinearity errors are 0.4% for the high-gain path and 0.3% for the low-gain path. Furthermore, the SAR ADC achieves an ENOB of 10 bits.

For the time measurement path, the TDC employs a hybrid measurement structure combining coarse counting and fine counting. The coarse counting is derived from a counter, while the fine counting is determined by a delay line. The TDC is designed to measure the time of arrival (TOA). The digital codes generated by the TDC and ADC are encoded and serialized by the digital module for data transmission.

In summary, SIPAC, a dedicated SiPM readout ASIC for the CEPC detector, features a wide dynamic range (1.28 pC to 3.84 nC), supports a 500 kHz event rate, and achieves a 200 ps time resolution at 1.28 pC. The integrated TDC delivers 100 ps resolution with INL and DNL below 1 LSB, while the ADC achieves a 10-bit ENOB.

Currently, the chip is undergoing functional testing. The front-end circuit and TDC are working normally, and the ADC is under testing. It is expected that the accuracy of the TDC will reach 100ps, and the dynamic range of the front-end meets the design requirements. Detailed performance tests will be conducted after the functional tests are completed.

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