A Low-Power Timing Chip Prototype for Strip LGAD Readout

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Outline

- Introduction
- Circuit design
- Test results
- Conclusion

Introduction

◆ OTK

- The outermost detector of the tracking system in the reference detector of the CEPC;
- Uses AC-LGAD microstrip sensors;
- Provides both high spatial resolution (10 μm) and high time resolution (50 ps).

◆ LATRIC

- A 128-channel timing chip for LGAD readout;
- Requirement:
  - High time resolution (30ps) & self-calibration;
  - 100-μm channel height to match the pitch of strip LGAD;
  - Low power consumption for thermal management (strip capacitance leading to power consumption issues).

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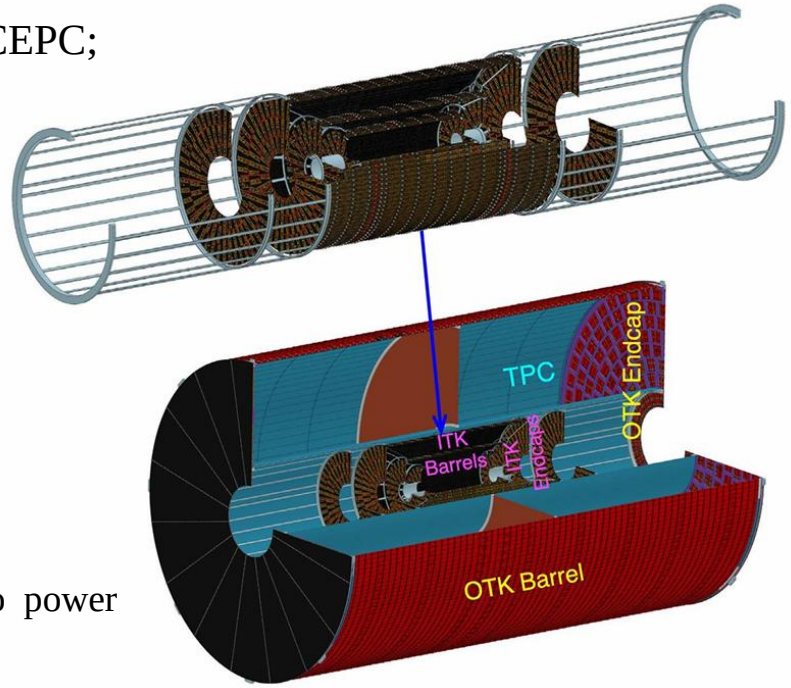


Fig 1. Layout of the Silicon tracker

- LATRIC0 (single-channel, April, 2025)
- LATRIC1 (8-channel, October, 2025)

Circuit Design

◆Architecture

- Front-End (FE)
  - An amplification and a discrimination.
- TDC core
  - *Timing controller;*
  - *Event-Driven RO & Quantization logic;*
  - Encoder.
- Output logic
  - Output the Measured CAL, TOT, TOA codes;
  - 128-bit Serializer for 111-bit raw data;
  - 40-bit Serializer for 36-bit encoded data;

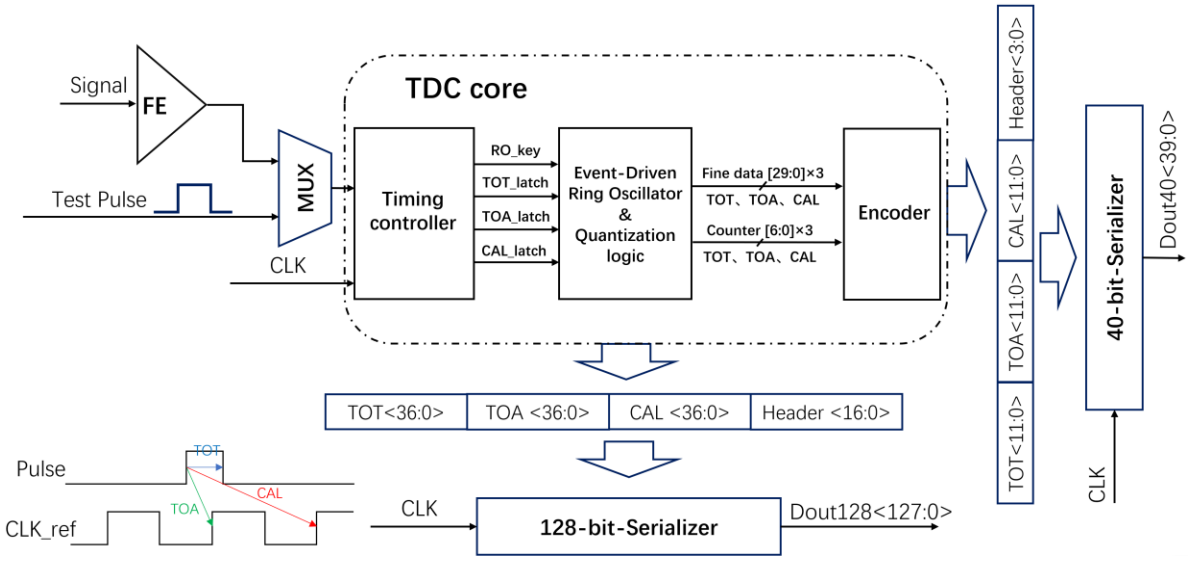


Fig 2. The overall block diagram

■ Self-calibration

- An additional period of CLK_ref is measured for calibration: $LSB_{Cal} = T_{CLK\_ref} / (CAL_{code} - TOA_{code})$;
- $TOA_{time} = LSB_{Cal} * TOA_{code}$;
- $TOT_{time} = LSB_{Cal} * TOT_{code}$.

Circuit Design

TDC core

- RO & Quantization logic
  - The RO employs 15 NAND-based delay cells, each providing an average delay of about 30 ps;
  - The 15 S2D converters transform both the rising and falling edges into **differential** signals for the three groups of SR latches;
  - The **symmetric** structure of SR latch ensures a consistent response to both rising and falling edges from the delay cells.

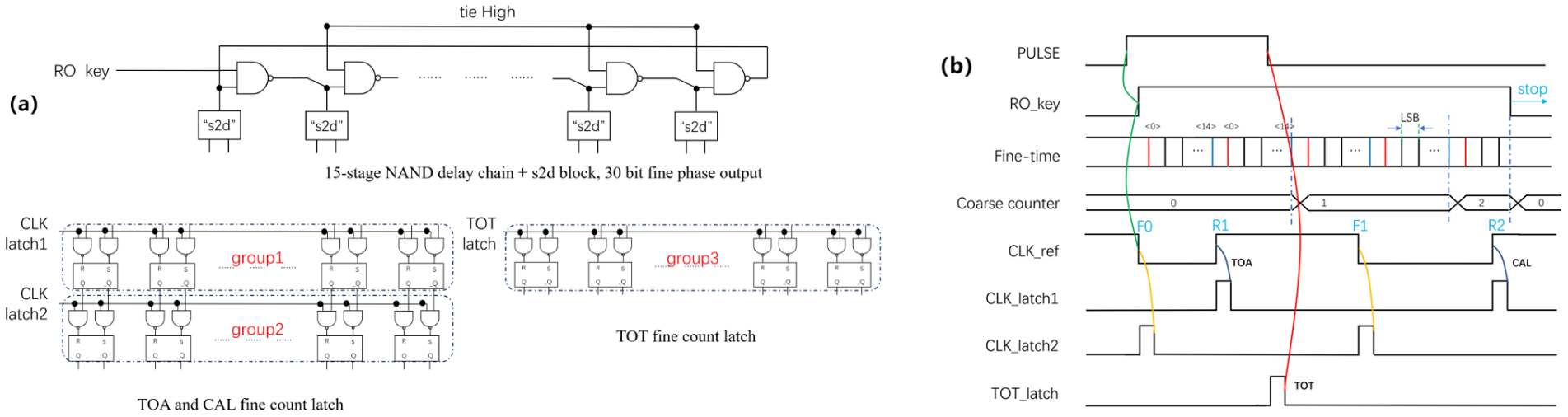


Fig 3. (a) Event-Driven RO & Quantization logic; (b) Quantization timing

Circuit Design

TDC core

- Controller
  - PULSE signal reception;
  - Reference clock, RO control; latch signal generation.
- Quantization timing

1. When the leading edge of the PULSE signal arrives, the RO is activated, the CLK_ref is enabled, coarse count starts;
2. The first rising edge (R1) of CLK_ref generates the CLK_latch1, which captures the TOA information in the latch group1;

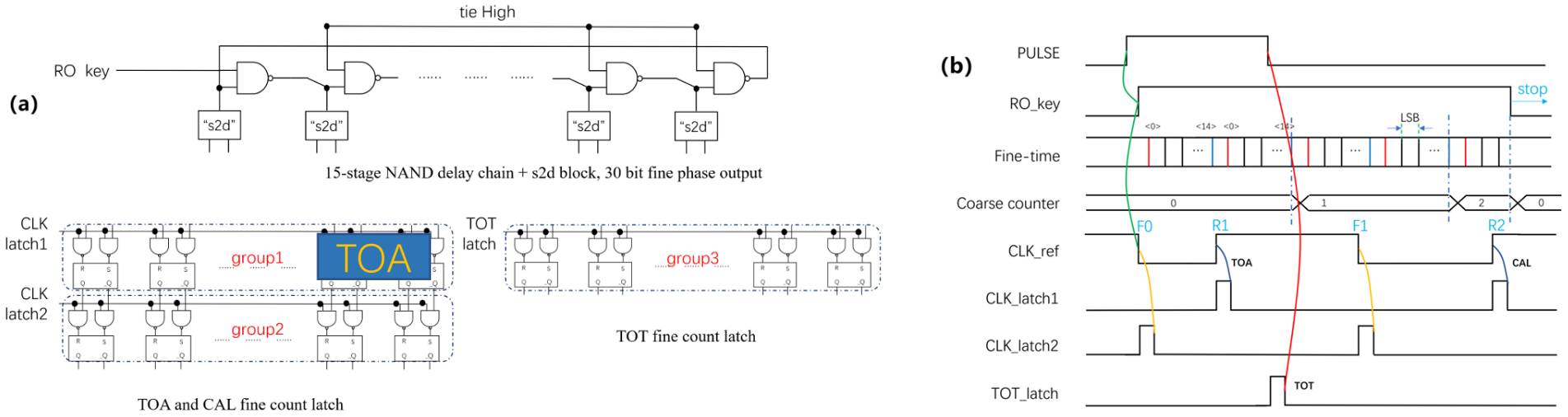


Fig 3. (a) Event-Driven RO & Quantization logic; (b) Quantization timing

Circuit Design

TDC core

- Quantization timing

3. The falling edge (F1) generates CLK_latch2, transferring the TOA codes to the latch group2;
4. The rising edge (R2) of CLK_ref generates the second CLK_latch1 pulse, which latches the CAL information into the latch group1, overwriting the previous TOA codes;
5. The trailing edge of the PULSE signal generates the TOT_latch signal to capture the TOT information in the latch group3;

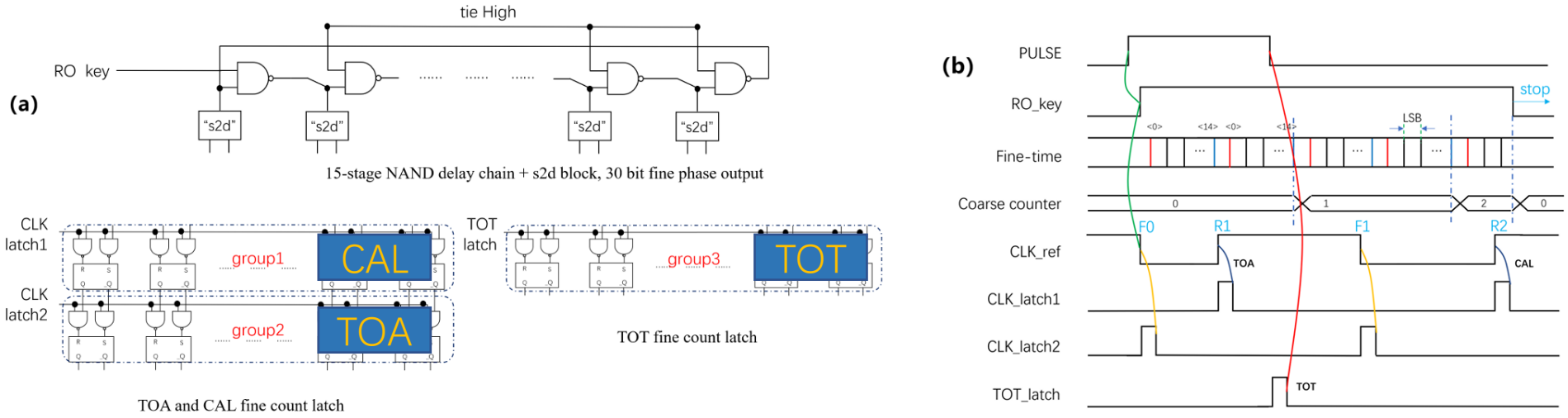


Fig 3. (a) Event-Driven RO & Quantization logic; (b) Quantization timing

Circuit Design

TDC core

- Quantization timing

6. After all the three measurements , RO_key is pulled low, stopping and resetting the RO, clearing the coarse counter, and returning the CLK_ref to high state.
7. The TOA, TOT, CAL value will be held in the three groups of latches, until the next event occurs.

(In the LATRIC1, these value will be latched into *Event builder* when RO_key is pulled down.)

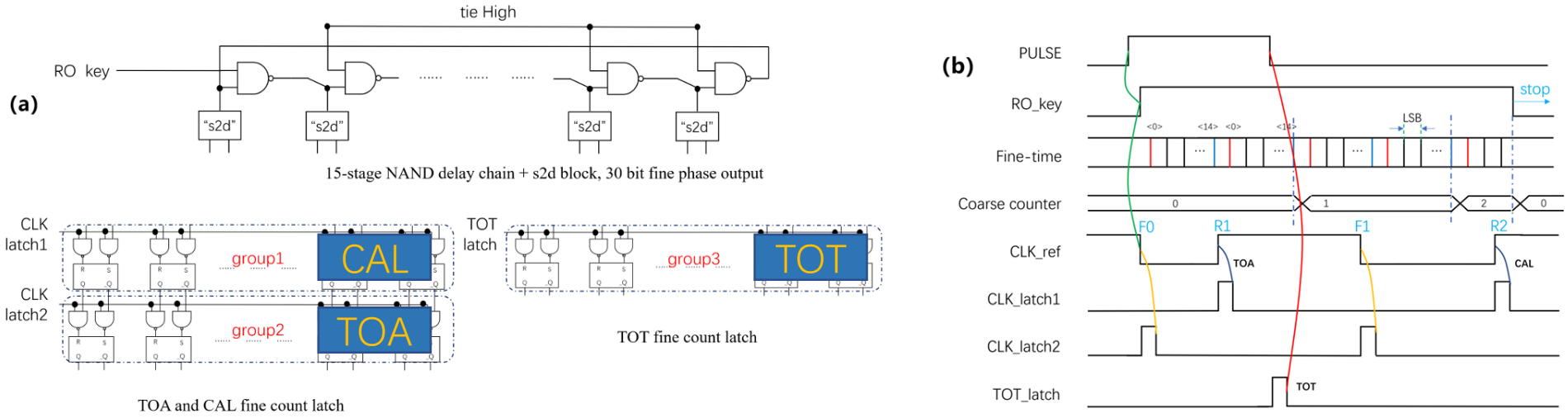
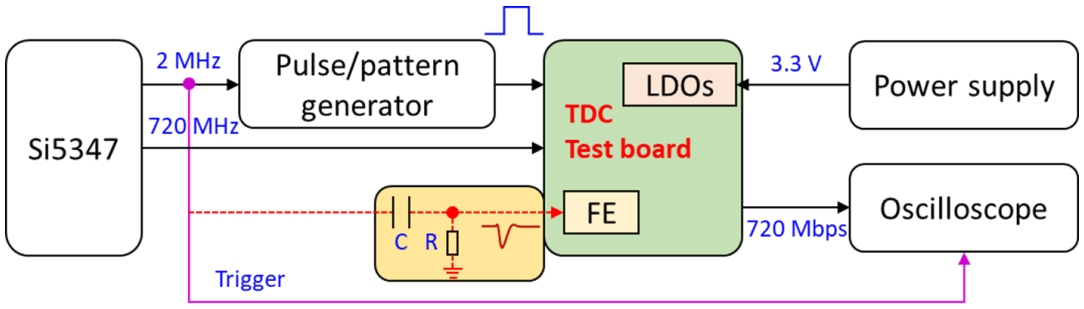


Fig 3. (a) Event-Driven RO & Quantization logic; (b) Quantization timing

Test Results

Test Setup

- Test-pulse mode
  - A 720-MHz clock (Si5347) for both serializer and TDC. Inside the TDC, the 720-MHz clock is divided down to 18 MHz and used as the reference clock for TOA measurement.
  - A 2-MHz clock (Si5347) to trigger a pulse/pattern generator (81130A). Both the pulse width and relative delay of pulse signal are independently adjustable. This function enables scanning of TOT and TOA transfer curves;
  - The measured standard deviation is 15.8 ps for the pulse width and 14.2 ps for the relative delay.
  - The averaged and rounded TDC output code from repeated measurements are used to plot the transfer curve.
- FE-mode
  - For functional verification of the FE-TDC integration, a passive RC differential circuit is used to generate an analog signal as input of FE.



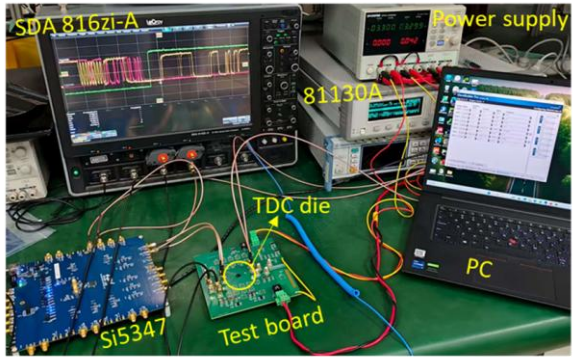


Fig 3. Test setup

Test Results

Timing performance (test-pulse mode)

- The TOA DNL and INL without FE are measured less than ± 1 LSB;
- $LSB_{toa} \approx 31.1$ ps;
- The TOT DNL and INL without FE are measured less than ± 1 LSB;
- $LSB_{tot} \approx 31.0$ ps ;

- $LSB_{cal} \approx 31.1$ps ;
- These three LSB are very close, indicating the effectiveness of the self-calibration.

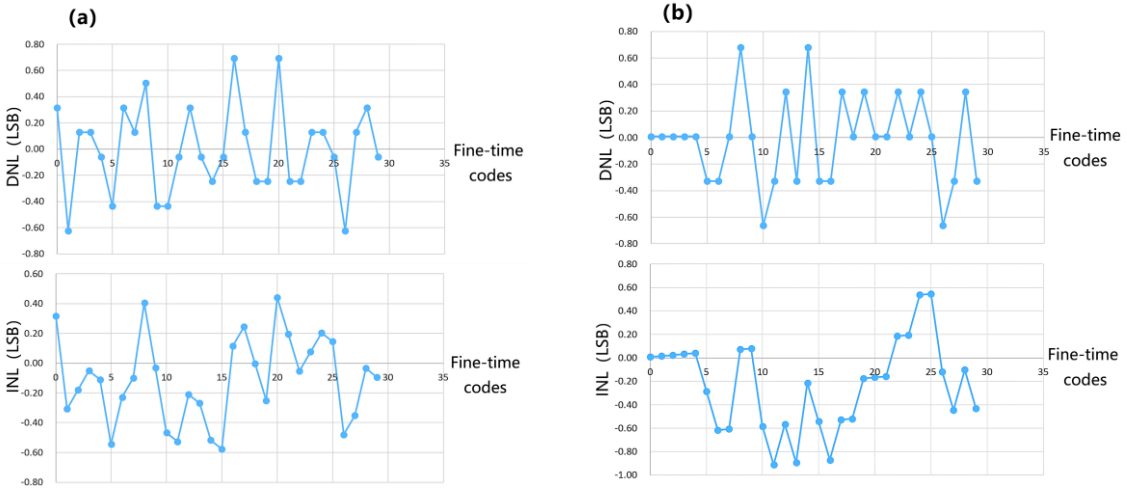


Fig 4. DNL & INL of: (a) TOA; (b) TOT

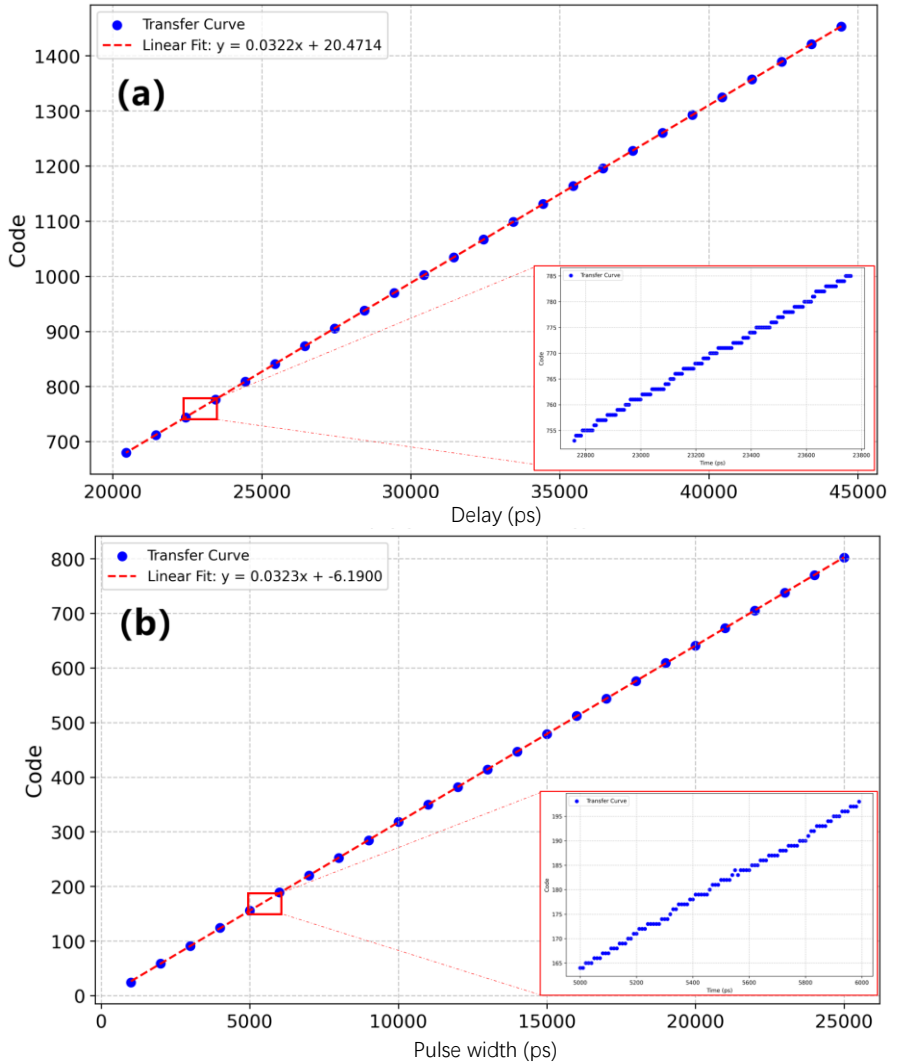
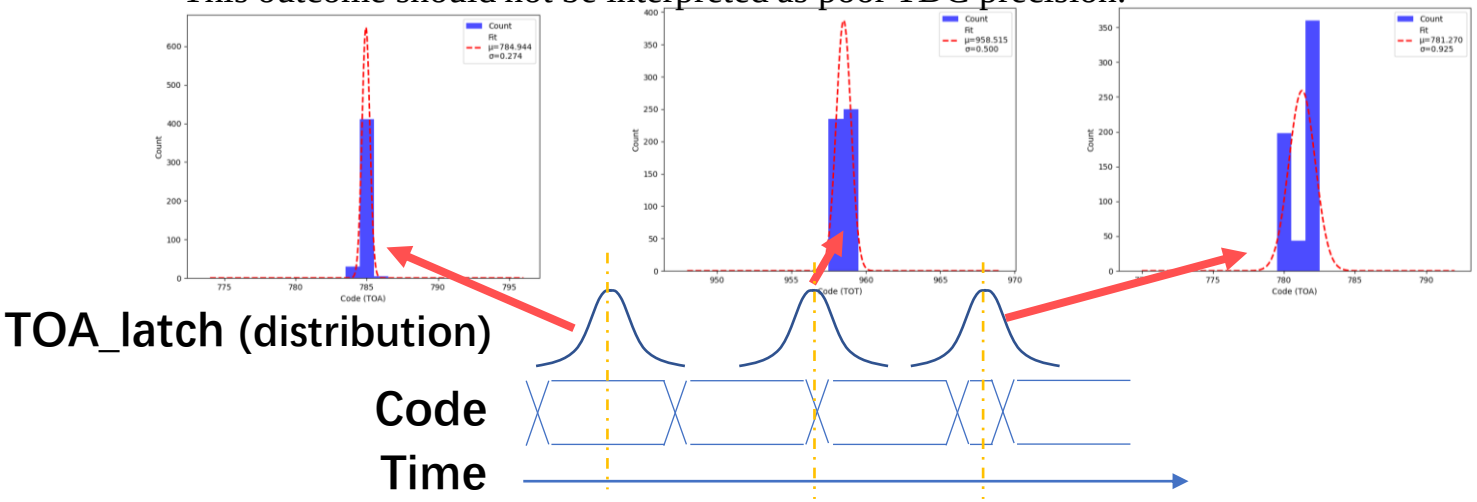


Fig 5. Measured transfer curves of: (a) TOA; (b) TOT

Test Results

Timing performance (test-pulse mode)

- Figure 6 shows the distribution of the standard deviation of TOA from multiple measurements, *obtained without removing the influence of the signal source* (σ = *14.2 ps, The relative magnitude between σ and the code width significantly dictates the statistical results*).
- The standard deviation for the most of delay values is better than 0.5 LSB;
- The standard deviation of a few points is significantly greater than 0.5 LSB:
  - These points correspond to the regions with smaller code width in the transfer curve.
  - The jitter of the signal introduces a larger influence when the code width is smaller.
  - This outcome should not be interpreted as poor TDC precision.



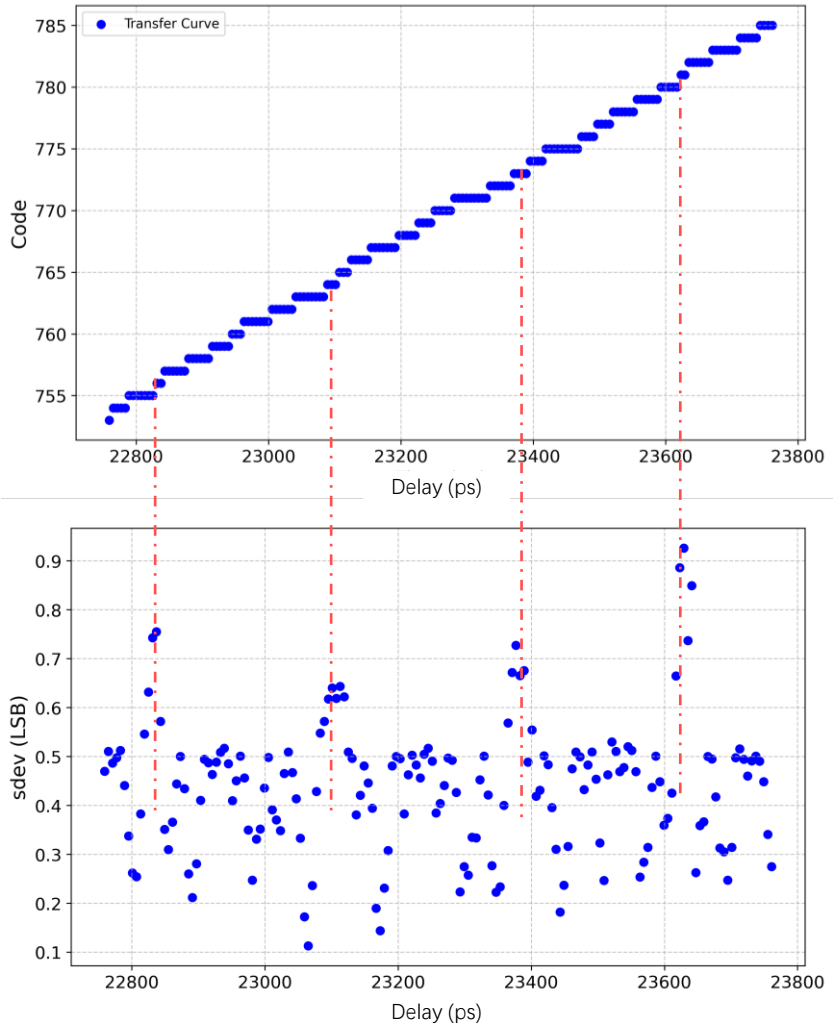


Fig.6 The standard deviation of repeated measurement corresponding to the transfer curve

Test Results

Timing performance (FE-mode)

- To perform functional verification of the FE-TDC integration (Futher test with LGAD is ongoing).
- Figure 7 shows the FE-TOA and FE-TOT distributions for a 13.0 mV input signal.
- Preliminary results indicate standard deviations of less than 0.9 LSB and 1.1 LSB, respectively.

Power consumption

- The FE consumes 4.9 mA (1.2V).
- The power consumption of the TDC core varies with event rate.
- The total power consumption is measured to be 6.24 mW at an event rate of 1 MHz.

Blocks	Event rate	Operating current
TDC part	2 MHz	~ 0.5 mA
	1 MHz	~ 0.3 mA
	500 kHz	~ 0.1 mA
Pre-amplifier		~4.9 mA

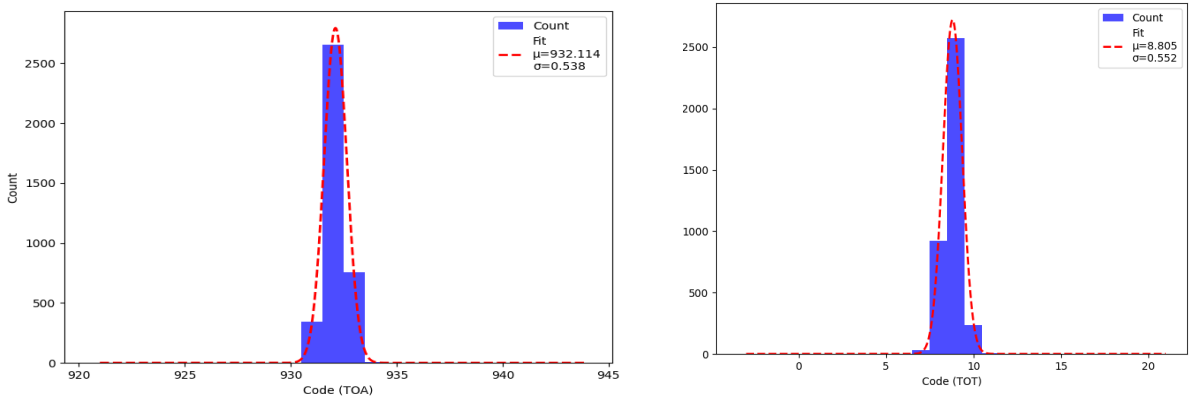
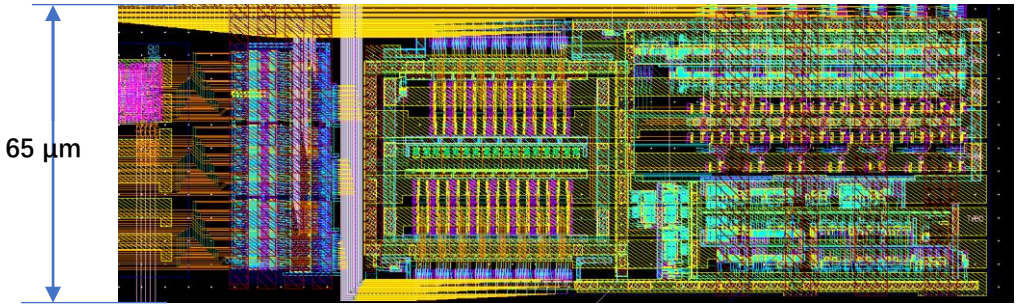


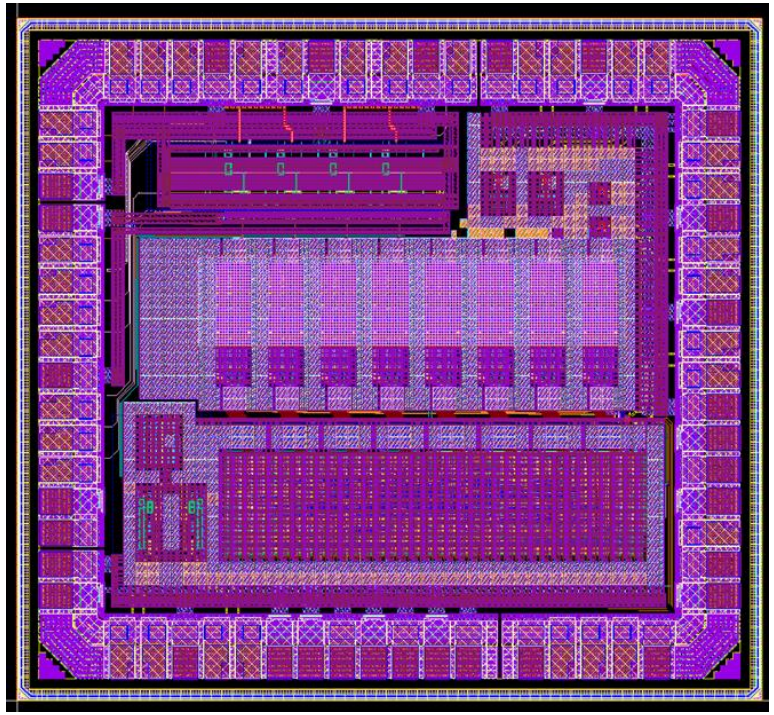
Fig.7 The statistical standard deviation corresponding to the transfer curve

Conclusion

- Successful integration of FE and TDC in LATRIC0
- High timing precision with low power consumption
- Effective self-calibration with consistent LSB values
- Meets CEPC requirements for OTK readout，including the height constrain of layout.



- Submitted for tape-out in October
  - 8 channels TDC; 4 channels with front end;
  - Increase the gain of preamplifier;
  - Improve the encoder logic;
  - Add event builder and timestamp;
  - 100 μm channel pitch match the LGAD.



Thank you!

Conclusion

- The figure shows the transfer curve between the set pulse width and the measured pulse width of signal generator.
- The nonlinearity at the marked region may cause a jump in the TOT transfer curve.