

## A Low-Power Timing Chip Prototype for Strip LGAD Readout

*Saturday, 8 November 2025 14:50 (20 minutes)*

AC-coupled Low Gain Avalanche Detector (AC-LGAD) based microstrip, achieving 30 ps timing resolution with a 100  $\mu\text{m}$  pitch, is proposed for the OTK in CEPC. The inherent capacitance of AC-LGAD presents significant challenges for power optimization. To match the strip pitch, a LGAD Timing Readout Integrated Chip (LATRIC) integrating 128 channels with a height of less than 100  $\mu\text{m}$  per channel is proposed. A single-channel prototype, LATRIC0, is fabricated in a 55 nm process for functional verification and integrates a front-end amplifier, a time-to-digital converter (TDC) core, and two serializers for outputting encoded and raw data. For analysis and debug, both a 128-bit low-speed serializer and a 40-bit high-speed serializer are included to output raw and encoded data, respectively.

The TDC core is implemented with a compact layout height under 65  $\mu\text{m}$ , including a timing controller, an event-driven ring oscillator with quantization logic, and an encoder. Upon an event trigger, the timing controller produces an enable signal to start the ring oscillator, along with separate latch signals for measuring the time of arrival (TOA) and time over threshold (TOT). A calibration (CAL) mechanism is incorporated via an additional clock cycle in the latch signal. The ring oscillator, which consists of 15 delay cells, supports simultaneous TOA, TOT, and CAL measurements.

Test results show that the TDC achieves an average bin-size of about 30 ps for both TOT and TOA. Both the tested integral and differential non-linearity are below 1 LSB.

Measurement results indicate that the average power consumption for the TDC measurement is below 0.12 mW at a 500 kHz event rate. The power consumption of the pre-amplifier and TDC block combined is less than 5.88 mW.

More detailed testing is in progress.

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**Session Classification:** Electronics

**Track Classification:** Detector and System: 16: Electronics