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First RISC-V–Based System-on-Chip for CEPC Readout ASICs

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High-Energy Physics (HEP) experiments increasingly rely on complex ASICs, driving a growing need for flexible, programmable architectures. We present a RISC-V–based System-on-Chip (SoC) that serves as a versatile control and configuration hub for CEPC ASICs. The SoC integrates tiny_riscv, a lightweight 32-bit processor with a 3-stage pipeline, capable of executing C programs to manage registers and implement communication protocols such as I²C and SPI via firmware. Its application will first be demonstrated in LATRIC, an ASIC for Low-Gain Avalanche Diode (LGAD) readout, with fabrication planned in a 55 nm CMOS process in October. This talk will present the SoC design, its implementation for CEPC ASICs, and prospects for future development and applications.

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