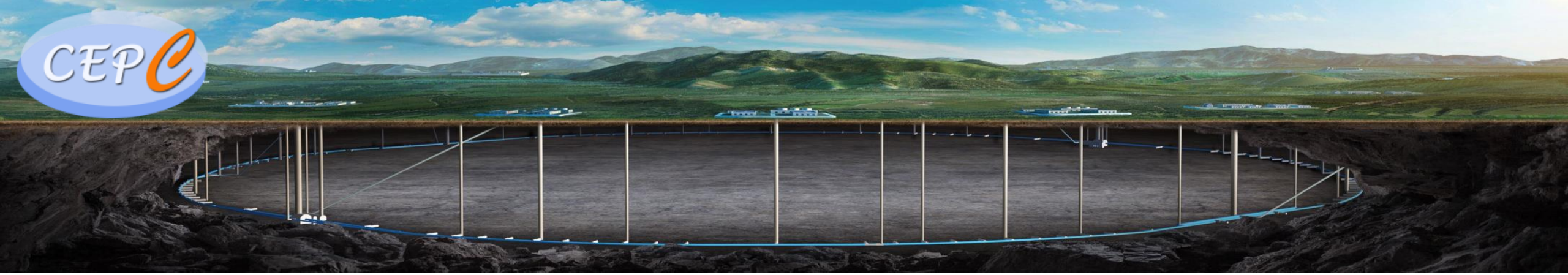


Overview of the CEPC Vertex Detector

Zhijun Liang, Ying Zhang
(On behalf of the CEPC vertex detector group)

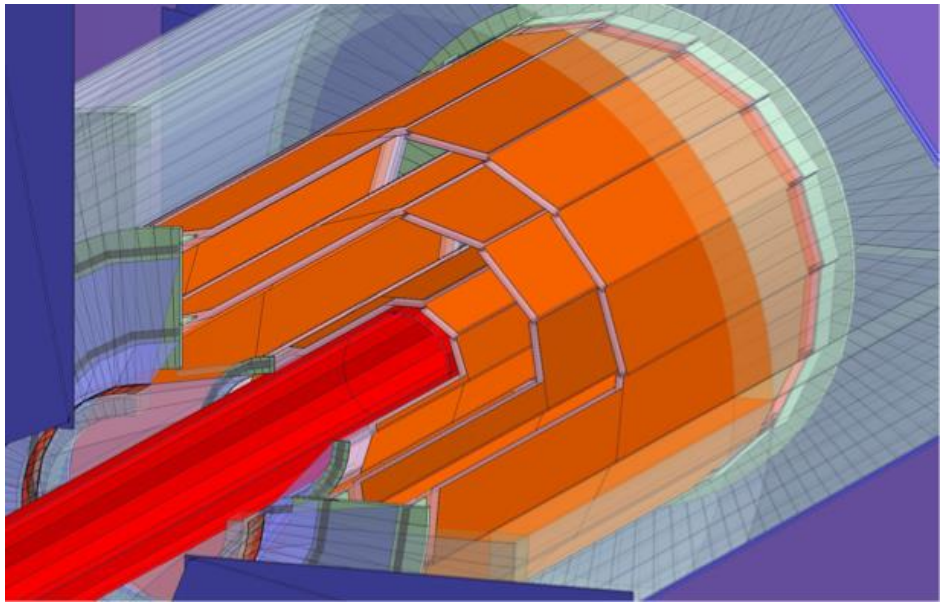
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Content

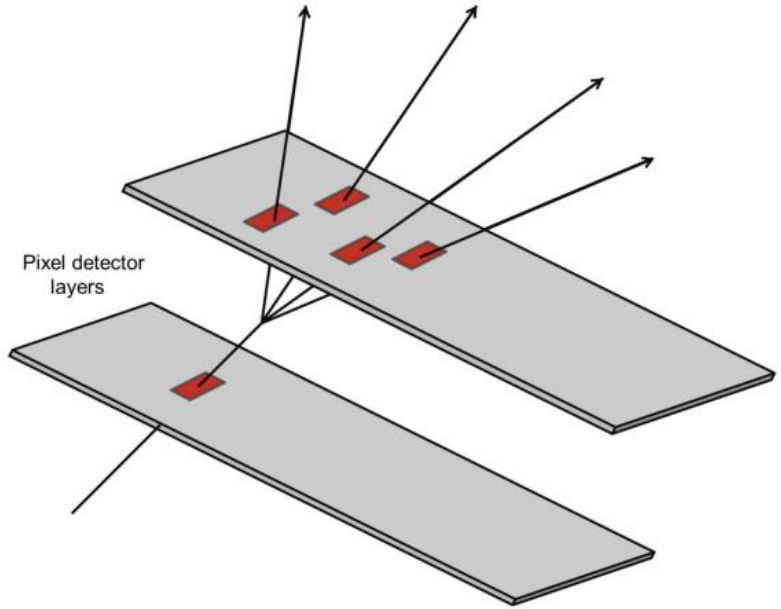
- Introduction
- Requirements
- Technology for CEPC reference TDR
- R&D efforts and results
- Detailed design including electronics, cooling and mechanics
- Readout electronics
- Performance from simulation
- Research team and working plan
- Summary

Introduction: vertex detector

- Vertex detector optimized for first 10 years of operation (ZH, low lumi-Z)
- Motivation:
  - Key detector for H → cc and H → gg physics, which is an important goal for CEPC
  - Aim to optimize impact parameter resolution and vertexing capability



CEPC vertex conceptional design (2016)



Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - Challenges: Radius (11.1 mm) is smaller compared with ALICE ITS3 (18 mm)
    High background hit rate up to 39 MHz/cm^2 for low-luminosity Z mode

Table 4.2: Vertex Detector Design Parameters

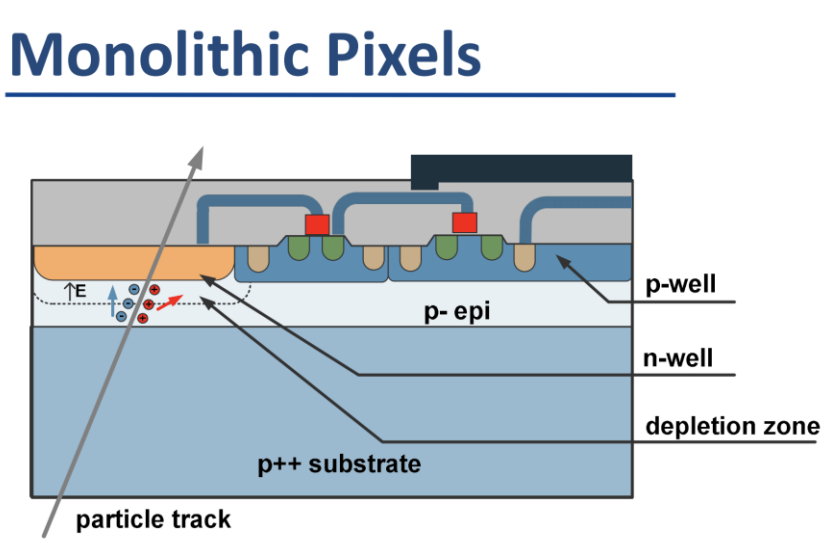
Parameter	Design
Spatial Resolution	~ 5 μm
Detector material budget	$\sim 0.8\% X_0$
First layer radius	11.1 mm
Power Consumption	< 40 mW/cm^2 (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}$ Neq/cm^2 (for first 10 years)
Operation Temperature	~ 5 °C to 30 °C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

Ref: CEPC Detector Ref-TDR

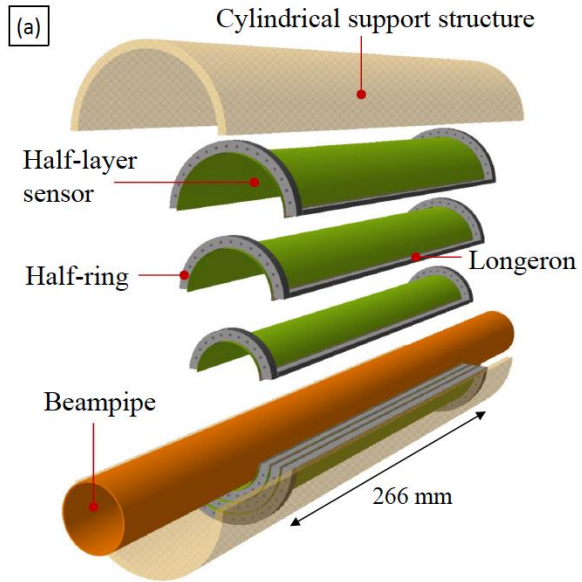
Technology for CEPC Reference TDR

- Vertex detector technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design [1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

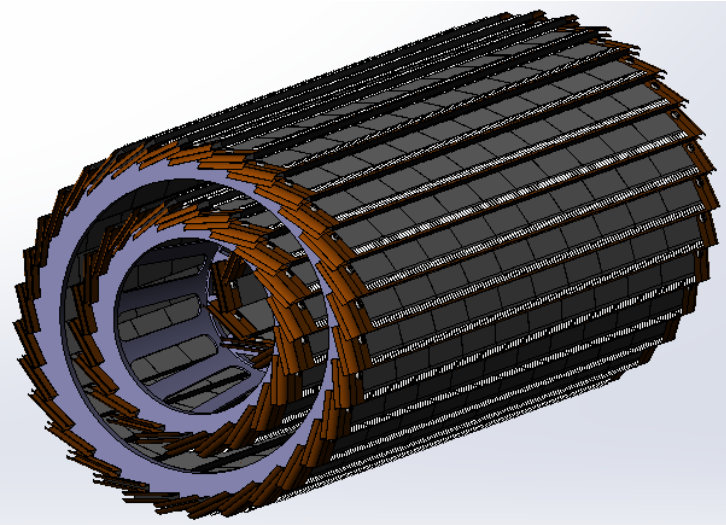
Monolithic active Pixel Sensor (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

R&D status and final goal

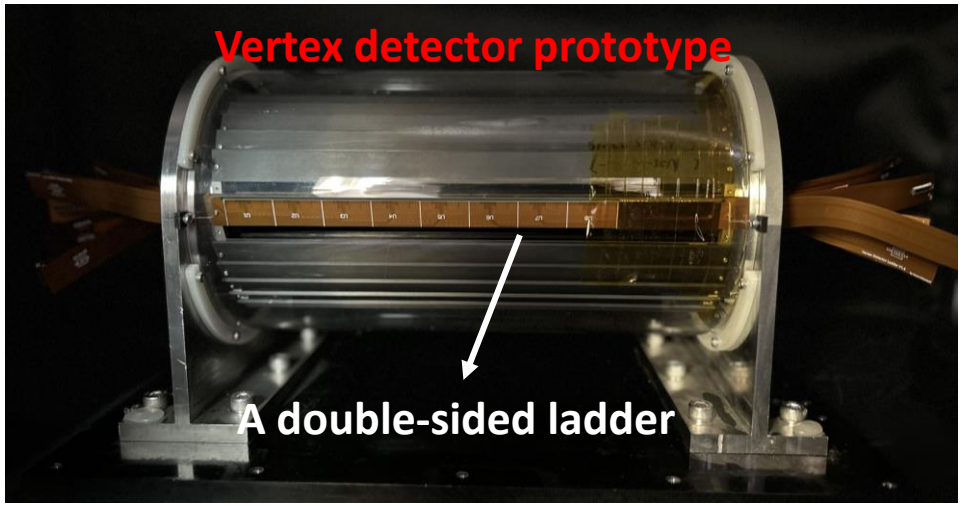
Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with 180 nm CIS (TaichuPix-3)	65/55 nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon sensor
Spatial resolution	4.9 μm	3-5 μm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12 mm	Bent final wafer with radius ~11 mm
Stitching	11×11 cm^2 stitched chip with 350 nm CIS	65/55 nm CIS stitched sensor

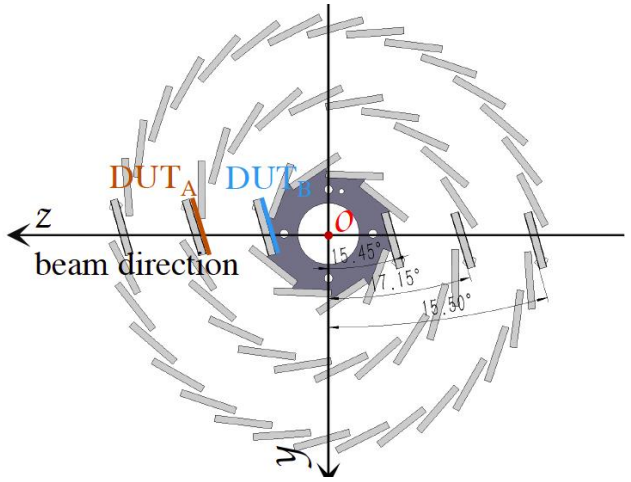
Talk on sensor chip and electronics: 11:30 AM, 8th Nov., Ying Zhang

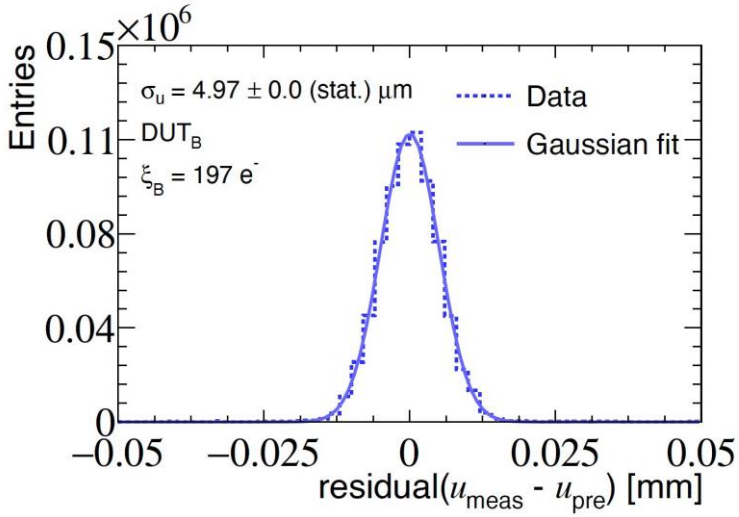
R&D effort: vertex detector prototype

Ladder readout system

TaichuPix-based prototype detector tested at DESY in April 2023
Spatial resolution ~ **4.9 µm**
@ Detection efficiency > 99%



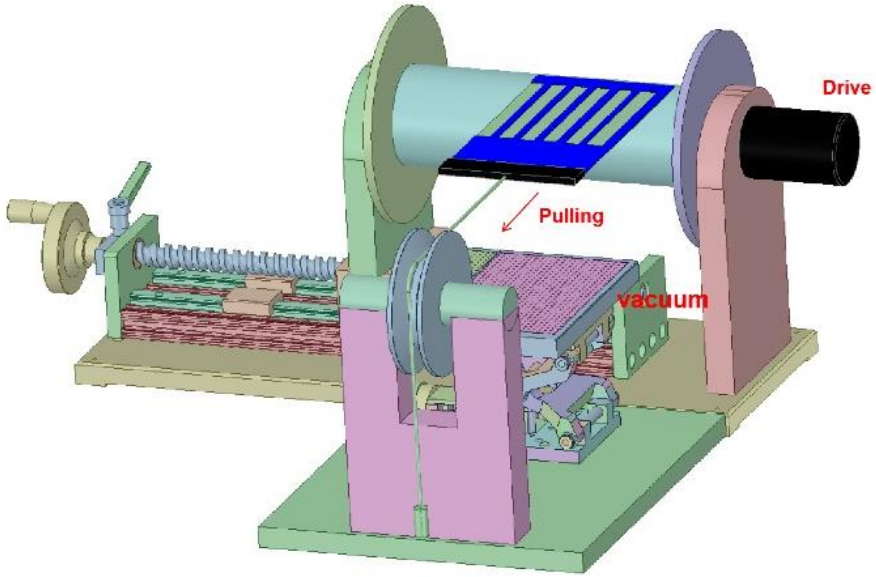


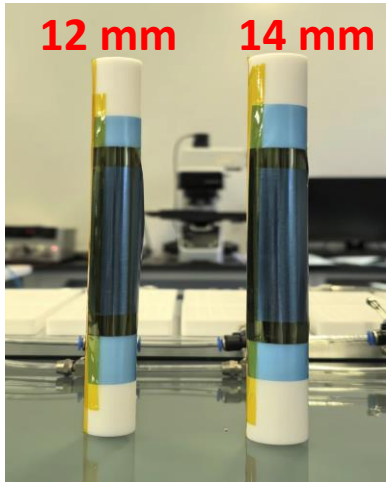


	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts curved MAPS

- CEPC b-layer radius (11 mm) smaller compared with ALICE ITS3 (radius = 18 mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12 mm
  - The dummy wafer has been thinned to 40 µm





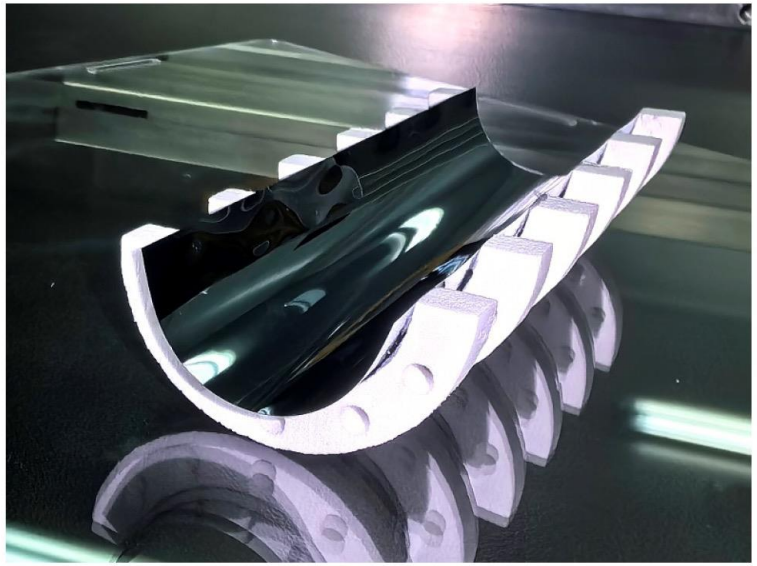
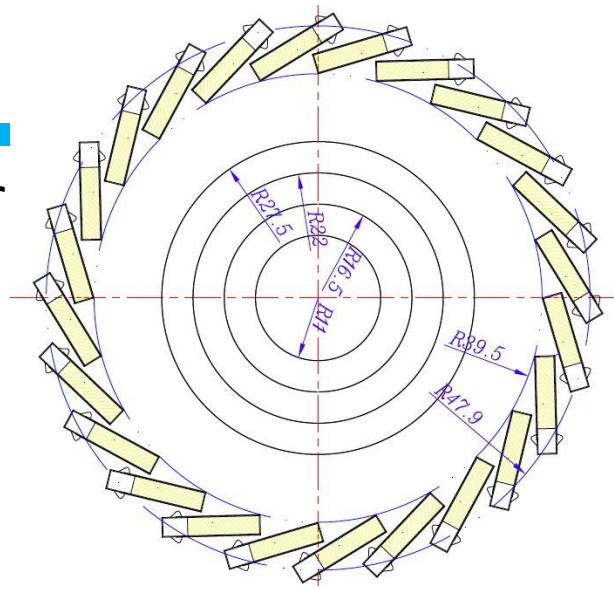


Figure 4.26: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12 mm	Bent final wafer with radius ~11 mm

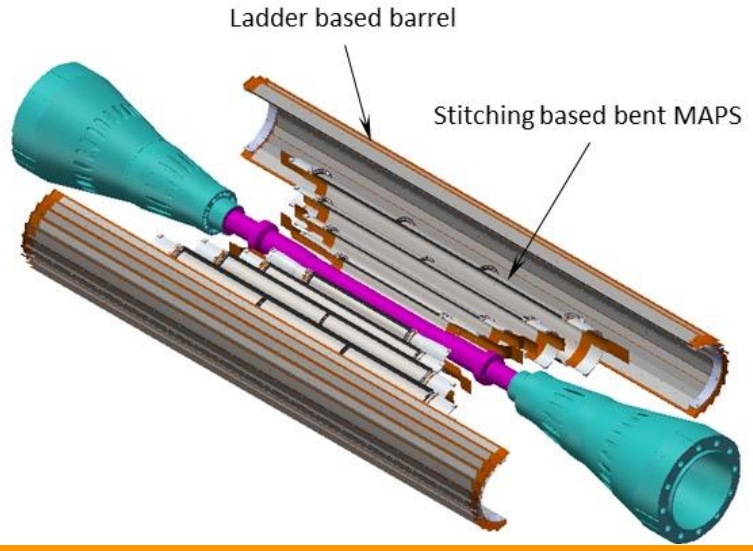
Baseline layout

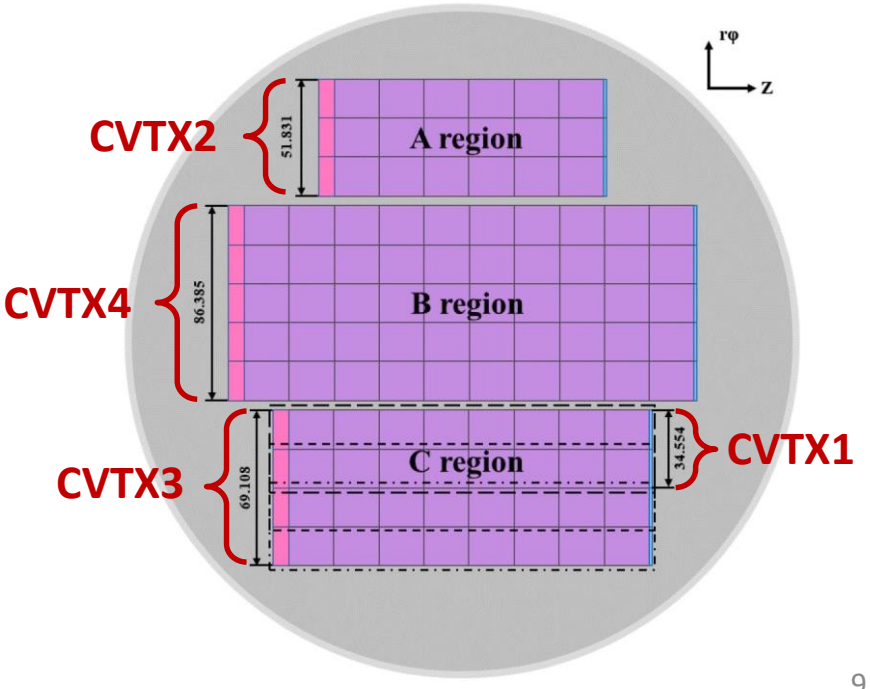


- Baseline: 4 single layer of bent MAPS + 1 double-sided ladder layer
  - Alternative option: 3 double layer ladders
- Inner layer: using single bent MAPS (~0.15 m^2)
  - Low material budget 0.06% X_0 per layer
  - Different rotation angle in each layer to reduce dead area
- Outer layer: using double layer ladder (~0.3% X_0/layer)

CVTX/ PVTX X	radius mm	length mm
CVTX 1	11.1	161.4
CVTX 2	16.6	242.2
CVTX 3	22.1	323.0
CVTX 4	27.6	403.8
PVTX 5	39.5	682.0
PVTX 6	47.9	682.0

Long barrel layout (no endcap disk)





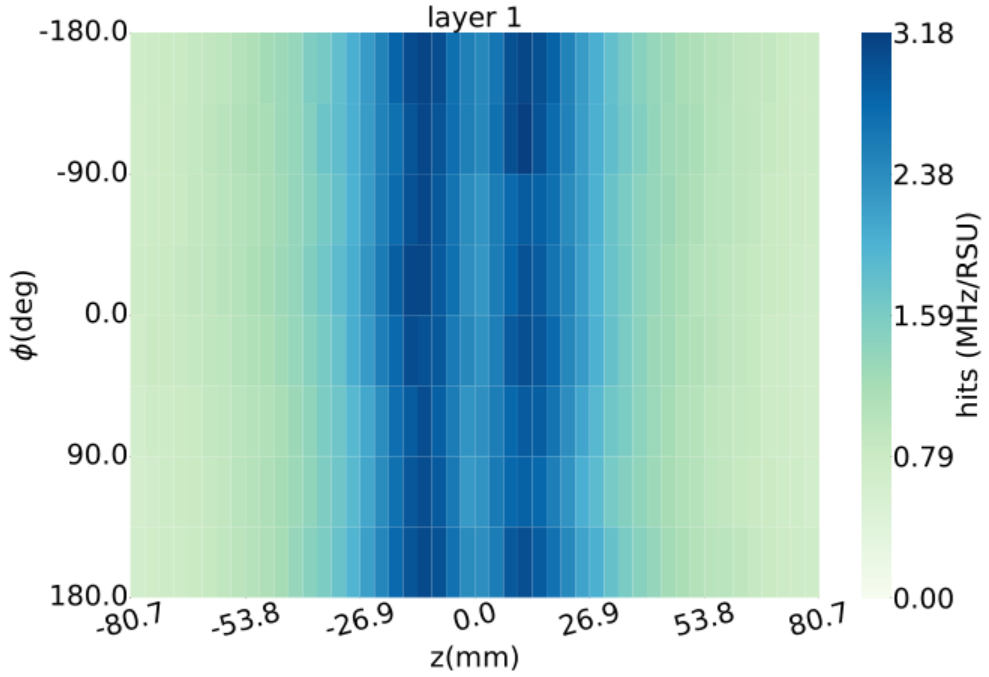
Background estimation

- The various sources of beam-induced backgrounds are simulated
  - The data rate at low-lumi Z pole is about ~Gbps level in b-layer

Background rate for Higgs and low-lumi Z runs

Layer	Ave. Hit Rate (MHz/cm^2)	Max. Hit Rate (MHz/cm^2)	Ave. Data Rate (Mbps/cm^2)	Max. Data Rate (Mbps/cm^2)
Higgs mode: Bunch Spacing: 277 ns, 63% Gap				
1	6.2	12	760	1500
2	0.84	1.6	87	160
3	0.17	0.36	19	38
4	0.067	0.16	8.4	19
5	0.017	0.037	2.1	4.2
6	0.013	0.026	1.6	3.7
Low-luminosity Z mode: Bunch Spacing: 69 ns, 17% Gap				
1	15	39	2700	8100
2	1.7	2.6	240	400
3	0.72	1.2	110	240
4	0.43	0.94	70	210
5	0.10	0.19	14	31
6	0.078	0.15	11	23

Hit rate map for 1st layer @ Higgs mode



Electronics

- Inner layers (L1-L4): stitching and RDL metal layers on wafer to transfer signal and power
  - Flexible Printed Circuit (FPC) connecting stitched sensors and Front-end Electronics Board (FEE)
  - FEE is installed in the service area outside of fast-LumiCal
- Outer layers (L5-L6): ladder on FPCs (also used in alternative design)
  - Signal, clock, control, power, ground will be handled by control board through FPCs

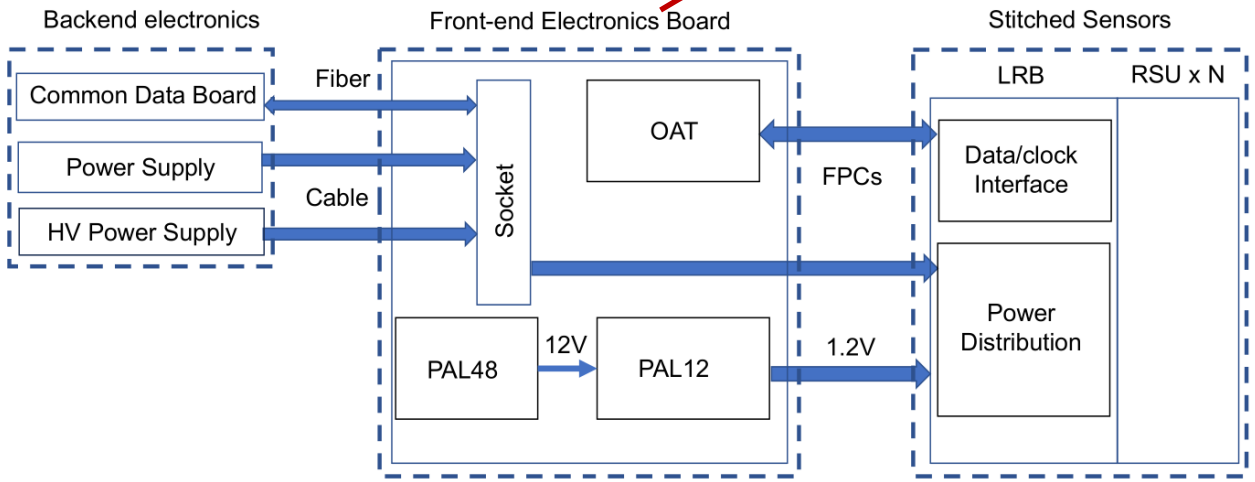
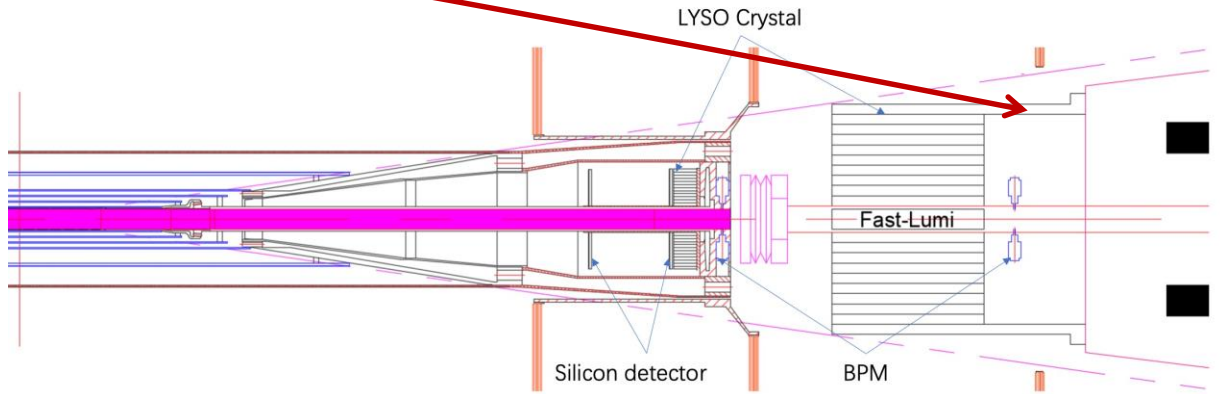


Diagram of the VTX readout electronics

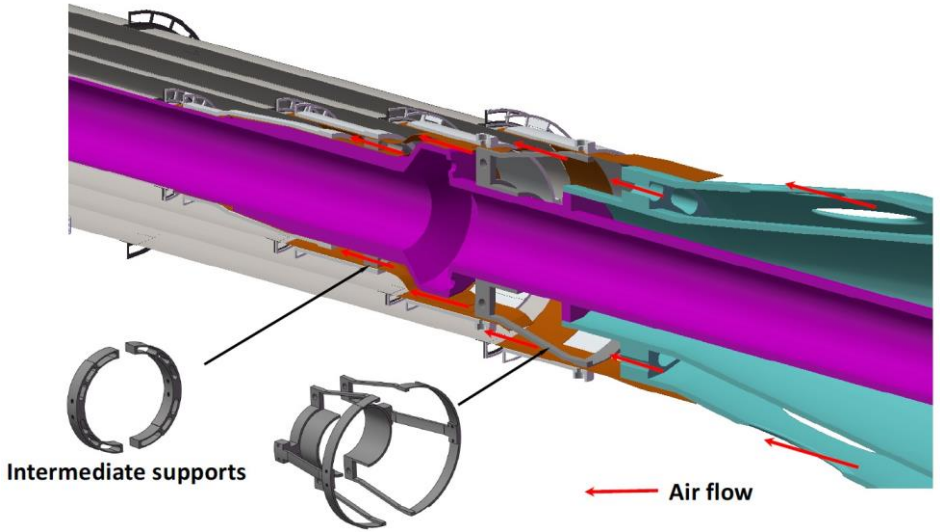


Location of the VTX service area

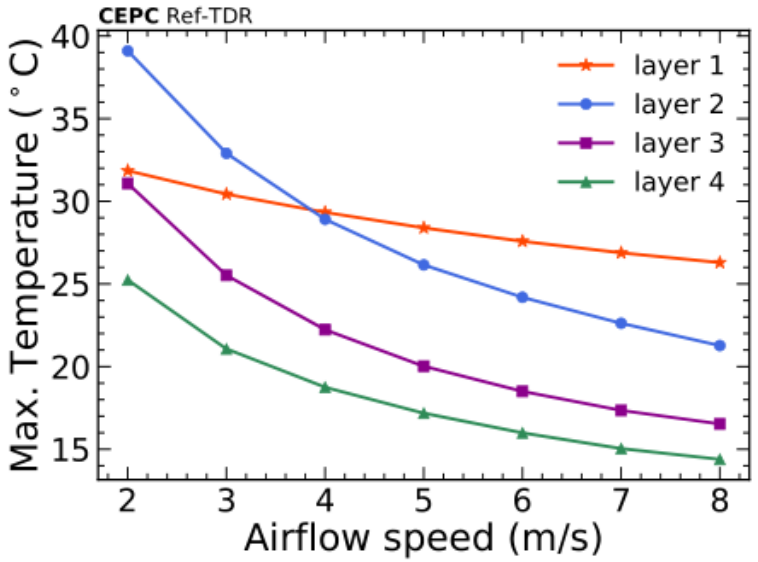
Talk on sensor chip and electronics: 11:30 AM, 8th Nov., Ying Zhang

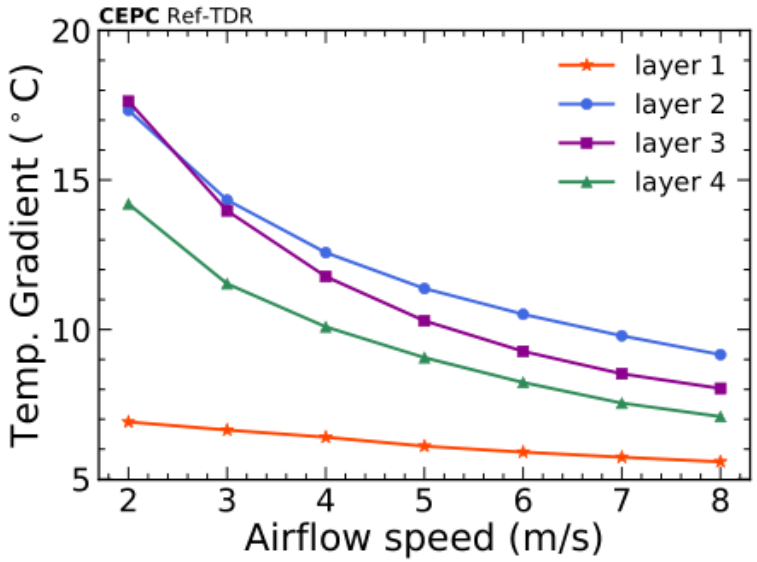
Mechanics and cooling

- For the sensitive area of stitched sensor, power consumption estimated to ~40 mW/cm^2
- Air cooling feasibility study
  - Effective airflow cross section of 12.6 cm^2
  - Baseline layout can be cooled down below 30 ℃ with 7 m/s air speed for stitching layers



Installation of the half layers and intermediate support



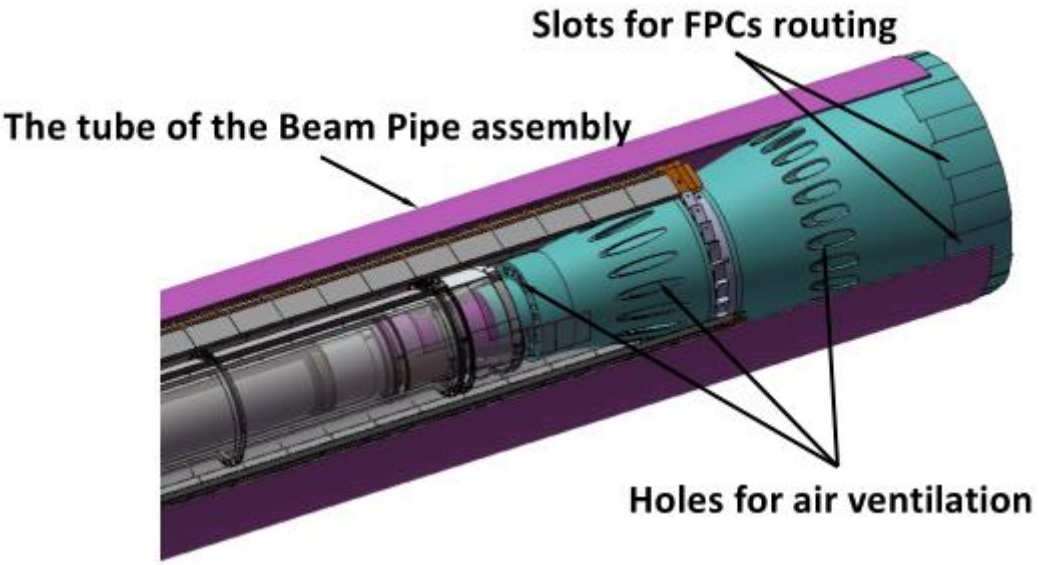


Thermal simulation results for the curved layers

Talk on Mechanics: 11:44 AM, 7th Nov., Jinyu Fu

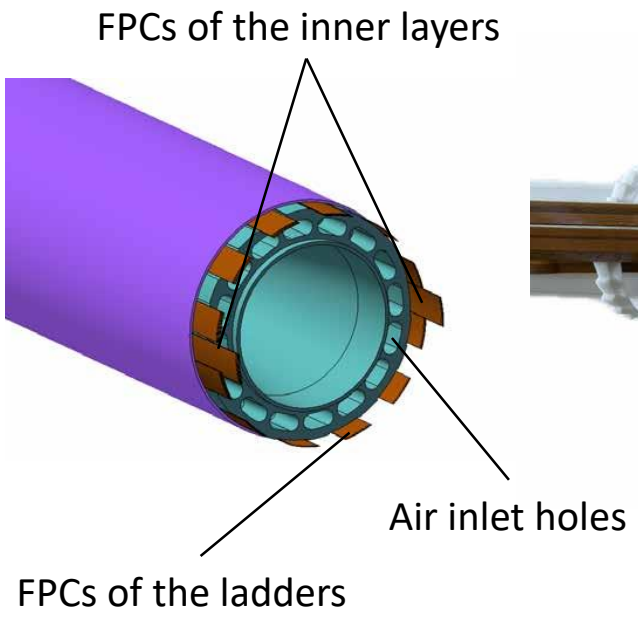
Vertex technologies: cables and services

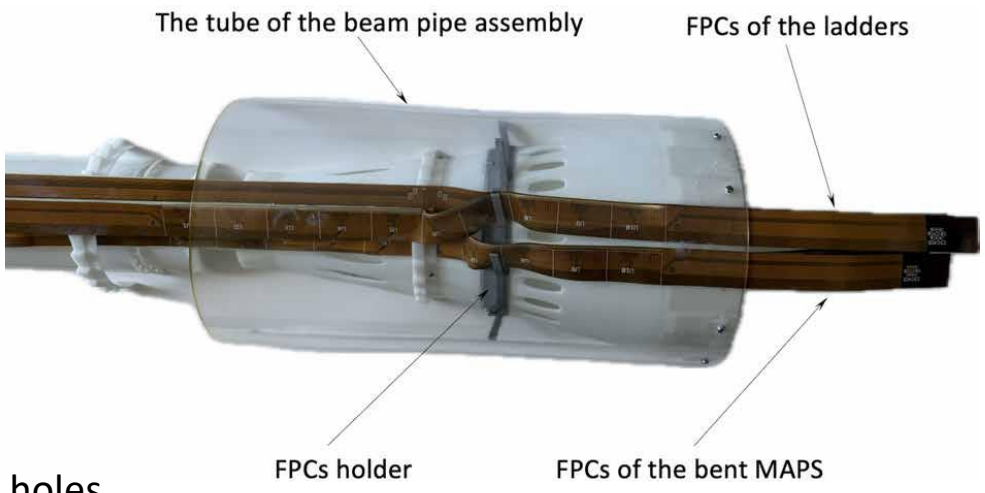
- A hollow conical structure integrated into the beam pipe assembly to serves as air distributor.
- A half-dummy 3D printed mechanical mockup was constructed
  - Validated there is enough space for cable routing and air cooling channel
  - The effective area for air cooling is 12.6 cm^2 (stitching layers)+ 28 cm^2 (between L4/L5)



Cross-sectional view of the full assembly

Dummy mockup of the VTX structure

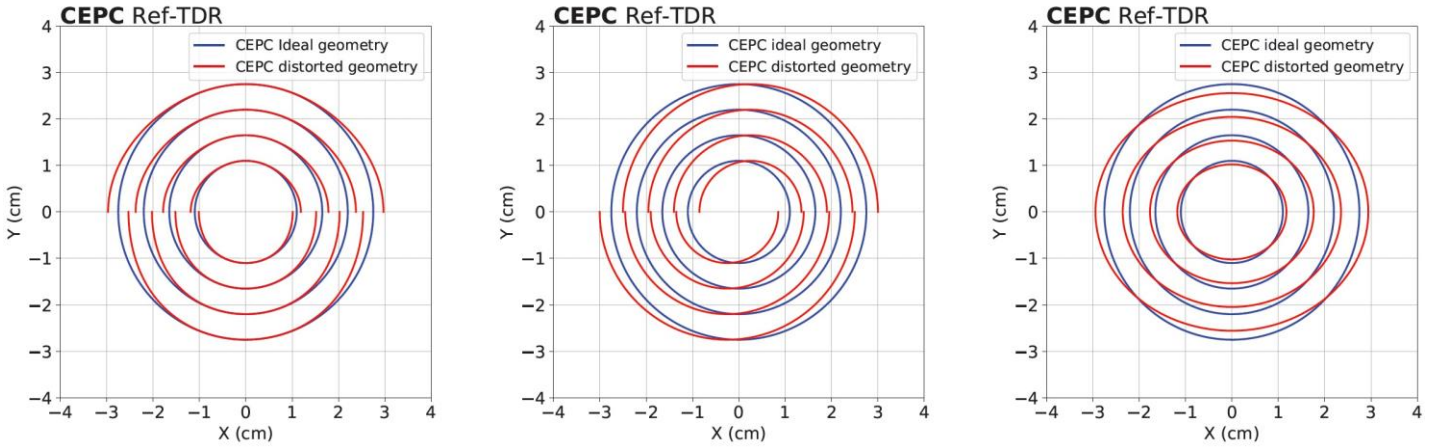




Alignment in stitching layer

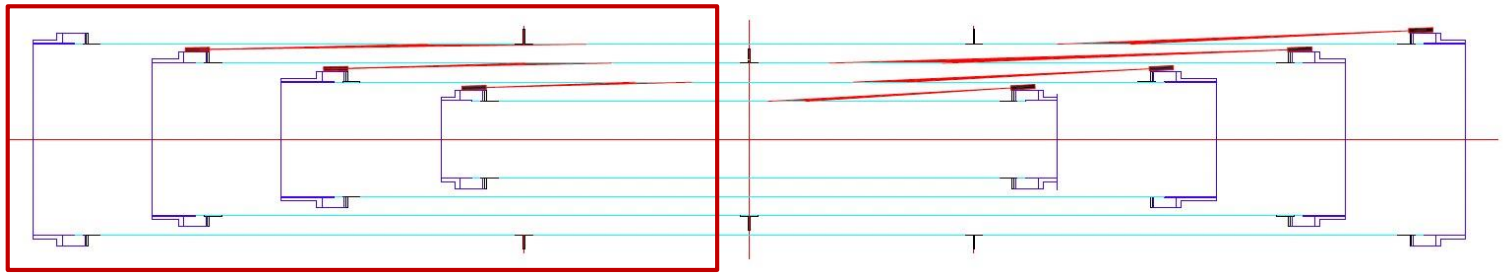
- Deformation modes simulated by FEA

Hit positions with three deformed geometries

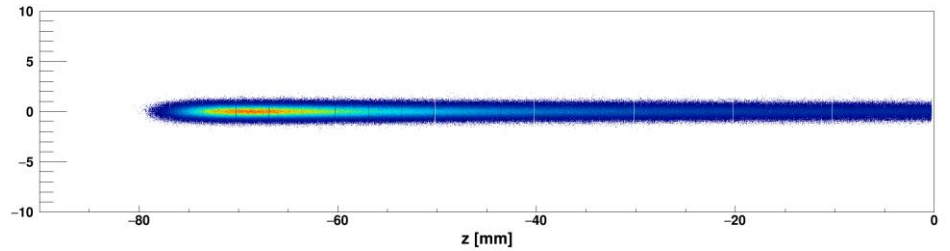


- Real time deformation monitoring by a infrared laser alignment system
  - laser sources are placed at both sides of the inner three layers and right side of the Layer 4

Back-side illuminations

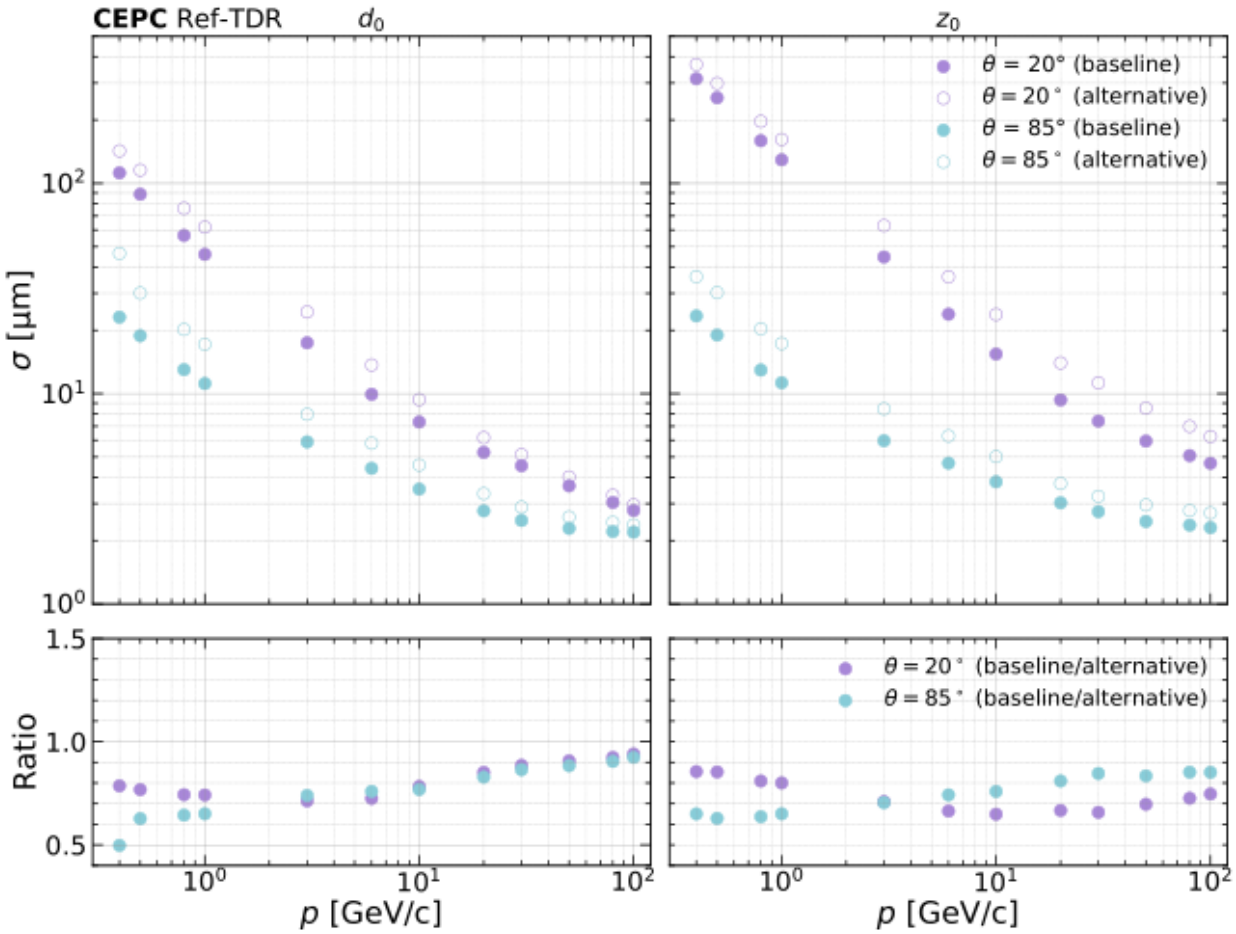


Laser beam spot on the Layer2 from (13 mm, 0, -85 mm)

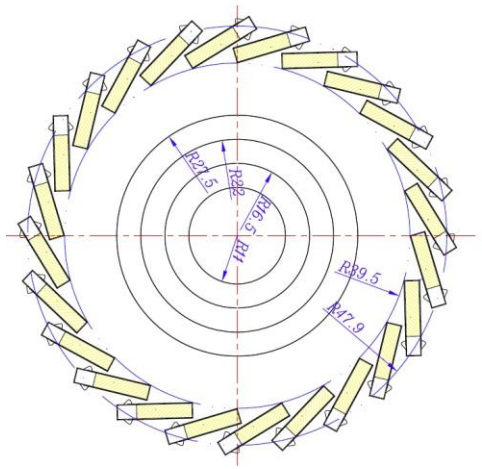


Performance: impact parameter resolution

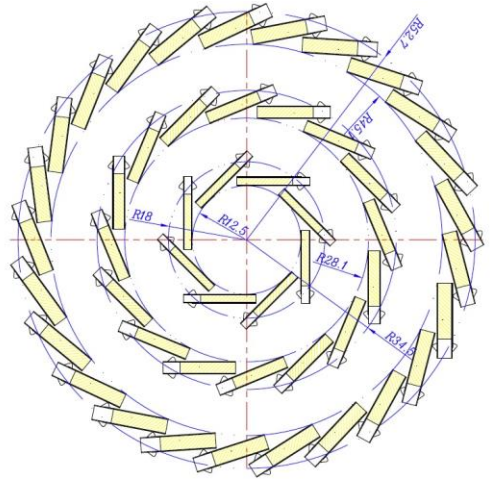
- Baseline has better resolution than alternative (ladder) (10-40%) in 0.4 GeV to 100 GeV



Baseline scheme
4 stitched curved sensor +
1 double layer ladders



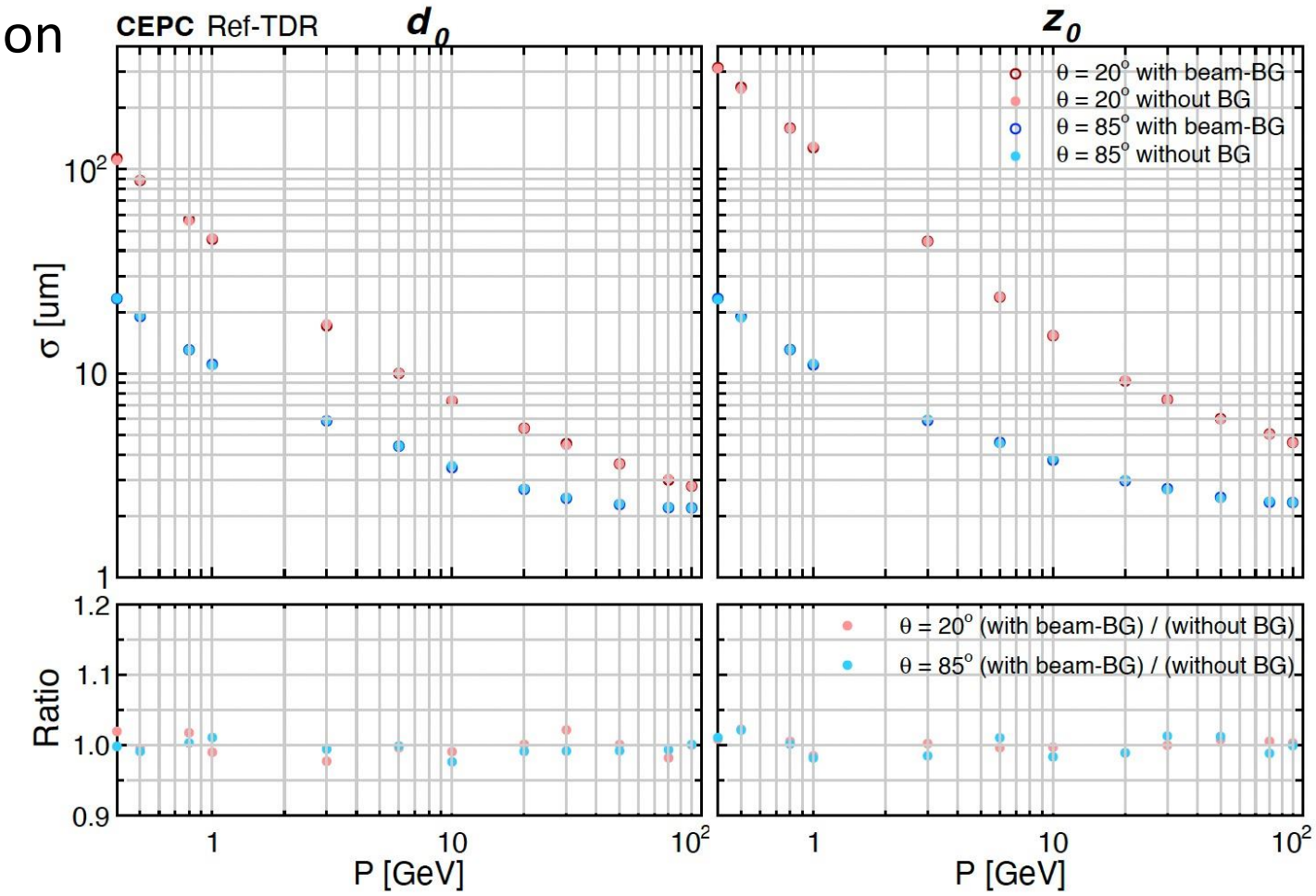
Alternative scheme
3 double layer ladders



Impact parameter resolutions of d_0 and z_0 for the baseline and alternative

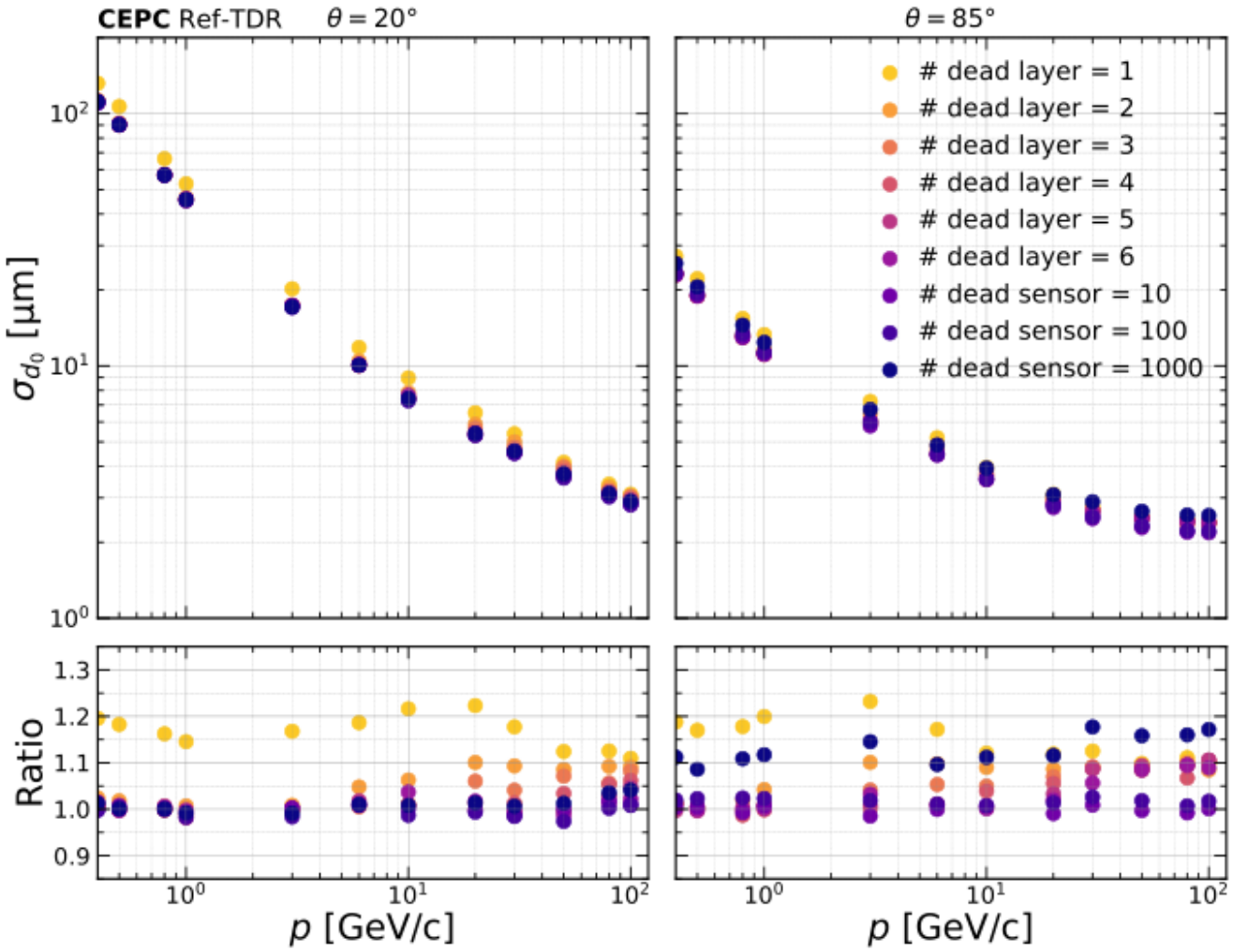
Performance with beam background

- The impact of beam background to performance has been studied.
  - No visible effect in d_0/Z_0 resolution
  - SR photons not accounted yet
    - Expected to be negligible



Performance: Efficiency

- Simulations assuming the complete loss of signal from one layer at a time.
- Any single layer loss leads to performance drop <= 25%, with the innermost layer contributing the most.
- VTX expected to maintain stable performance.



Poster on VTX Detector: C12, 7:00 PM, 7th Nov., Tianyuan Zhang

Research team

- IHEP: 8 faculty, 2 postdoc, 5 students
- IPHC/CNRS: 3 faculty, collaboration in framework of FCPPL and DRD3
  - CEPC Jadepix design, ALICE/BELLE2 upgrade (especially on MAPS design, stitching)
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty)
  - CEPC TaichuPix chip design, ATLAS upgrade
- ShanDong U.: Stitching chip design (3 faculty, 1 postdoc, 3 students)
- CCNU: Chip design, ladder assembly (2 faculty, 3 students)
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 students)
- Nanchang U. : Chip design, (1 faculty, 1 student)
- Nanjing U.: Irradiation study, chip design : (2 faculty, 4 students)
- NanKai U.: Physics performance (1 faculty, 1 student)
- CERN: Recent joint R&D collaboration aiming for ALICE3 upgrade

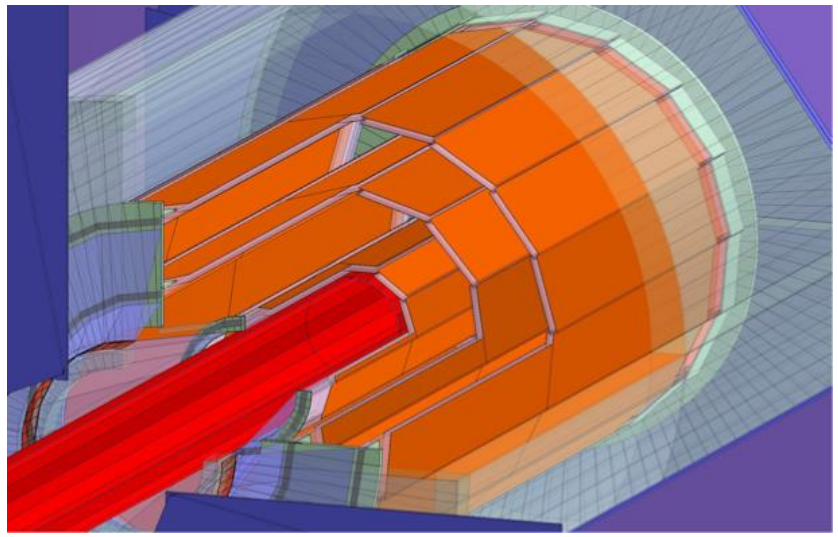
Working plan

- Development of wafer-scale stitched MAPSs.
  - Develop wafer-scale stitching with 180 nm technology
  - The second-generation stitched chip will transition to 65 nm/55 nm
    - Baseline: TPSCo's 65 nm technology
    - Alternative: HLMC's 55 nm technology
- Ultra-thin mechanical supports and low-mass integration techniques.
  - Start with prototype with dummy silicon wafer
- Construction of a full-scale VTX prototype to address challenges in mechanical precision, cooling performance, laser alignment, and system-level integration.

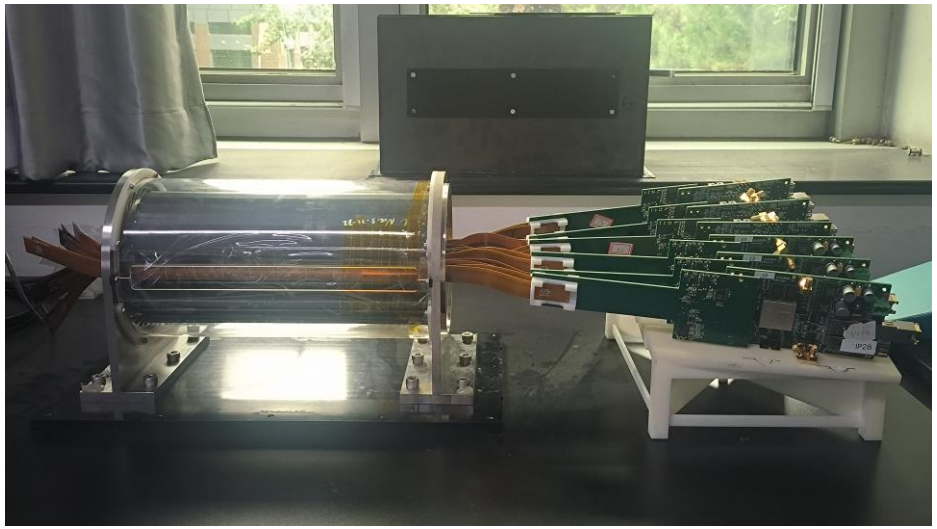
Summary

- Completed reference TDR for CECP vertex detector
  - Aiming for stitching technology as baseline design for reference TDR
- We active expanding international collaboration and explore synergies with other projects
  - Recent collaboration with CERN on ALICE3 tracker upgrade
  - We are members of ECFA DRD3 collaboration

CEPC vertex conceptional design (2016)



CEPC vertex prototype (2023)



Thank you for your attention!

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Institute of High Energy Physics
Chinese Academy of Sciences