CMOS Sensors with internal gain

CASSIA = **C**MOS **A**ctive **S**en**S**or with **I**nternal **A**mplification

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On behalf of the CASSIA collaboration in DRD3:

DRD 3
SOLID STATE DETECTORS

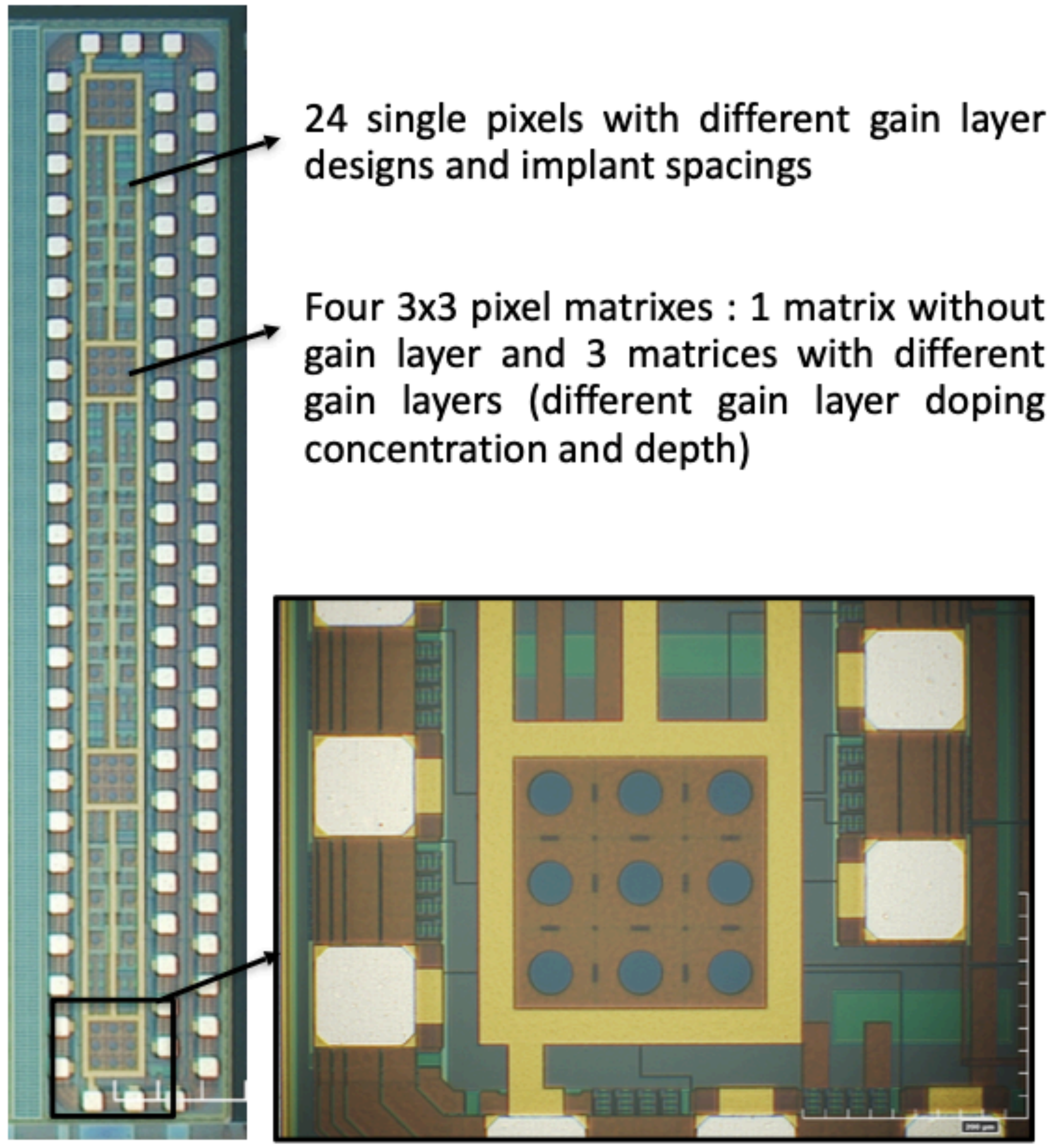
- Technical University Athens
- University Bonn
- CERN
- CPPM Marseille
- University Zagreb/FER
- IPHC Strasbourg
- KEK
- Tsukuba University
- Kyushu University
- IIT Madras/ Chennai
- University of Glasgow
- GSI Darmstadt
- University Zürich
- University Bern

CASSIA Sensor with internal gain in CMOS imaging process

- The CASSIA project aims to implement a **pixel implant structure with internal gain** in a **CMOS imaging process** for future use in MAPS for **tracking, timing or time-tagging**
- **This addresses a major goal of DRD3 CMOS research plan and is a DRD3 WG1 project**
- Design the **pixel implant structure with internal gain** in a way that it can be **implemented in commonly used MAPS pixel matrix** (either existing or future sensors)
- **Internal gain** for
  - Much higher signal-to-noise in thin monolithic sensors (simplification of circuits)
  - Substantial improvement of time resolution for tracking sensors
  - Aim at limited gain in linear amplification range to keep noise rate low enough for HEP trackers
- **Discussion with Tower Semiconductor** Research director indicated that this **can be done in TJ180nm CIS imaging process** on which many HEP sensors are based and we have substantial experience for tuning implant profiles
- A **transfer of results to finer-pitch processes** (e.g. 65nm) is envisaged for a future stage after initial developments in 180nm

CASSIA sensor design variants with different electrode and gain layer designs

- **CASSIA1 design jointly by CERN and University Zagreb /FER**
  - Main focus : demonstrate that internal gain can be achieved in 180nm CIS with existing doping profiles
  - voltages necessary to achieve gain are within process capabilities



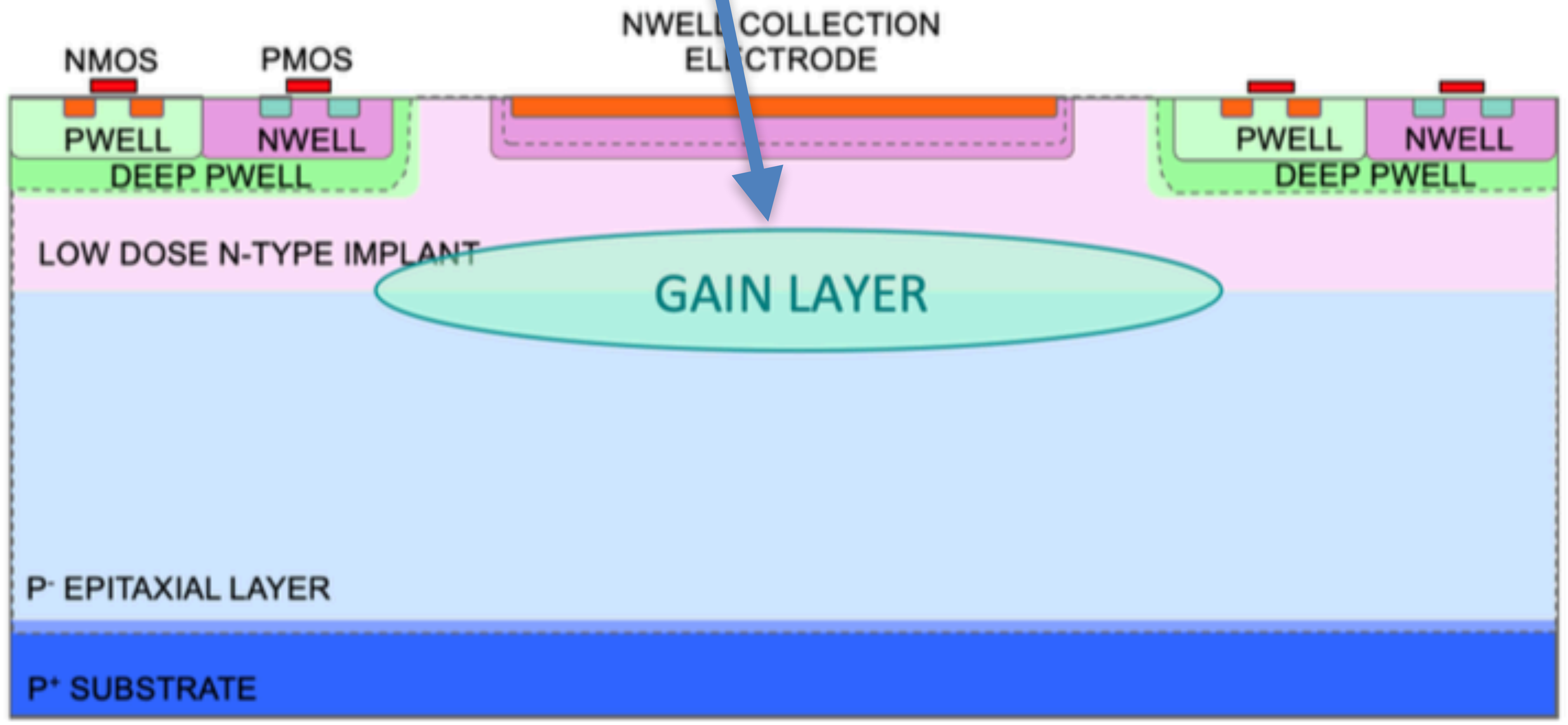
24 single pixels with different gain layer designs and implant spacings

Four 3x3 pixel matrixes : 1 matrix without gain layer and 3 matrices with different gain layers (different gain layer doping concentration and depth)

- **Implemented low-gain avalanche (LGAD)/SPAD-type sensor in Tower 180nm CIS imaging process**
  - top biased electrode, substrate and PW on GND
  - pixel pitch 80um

Electrode and gain layer configurations:

A. no gain layer (reference)
B. NW electrode + p-type GL depth 1
C. NW electrode + p-type GL depth 2
D. Shallow electrode + p-type GL depth 2
E. Deep electrode + p-type GL depth 2

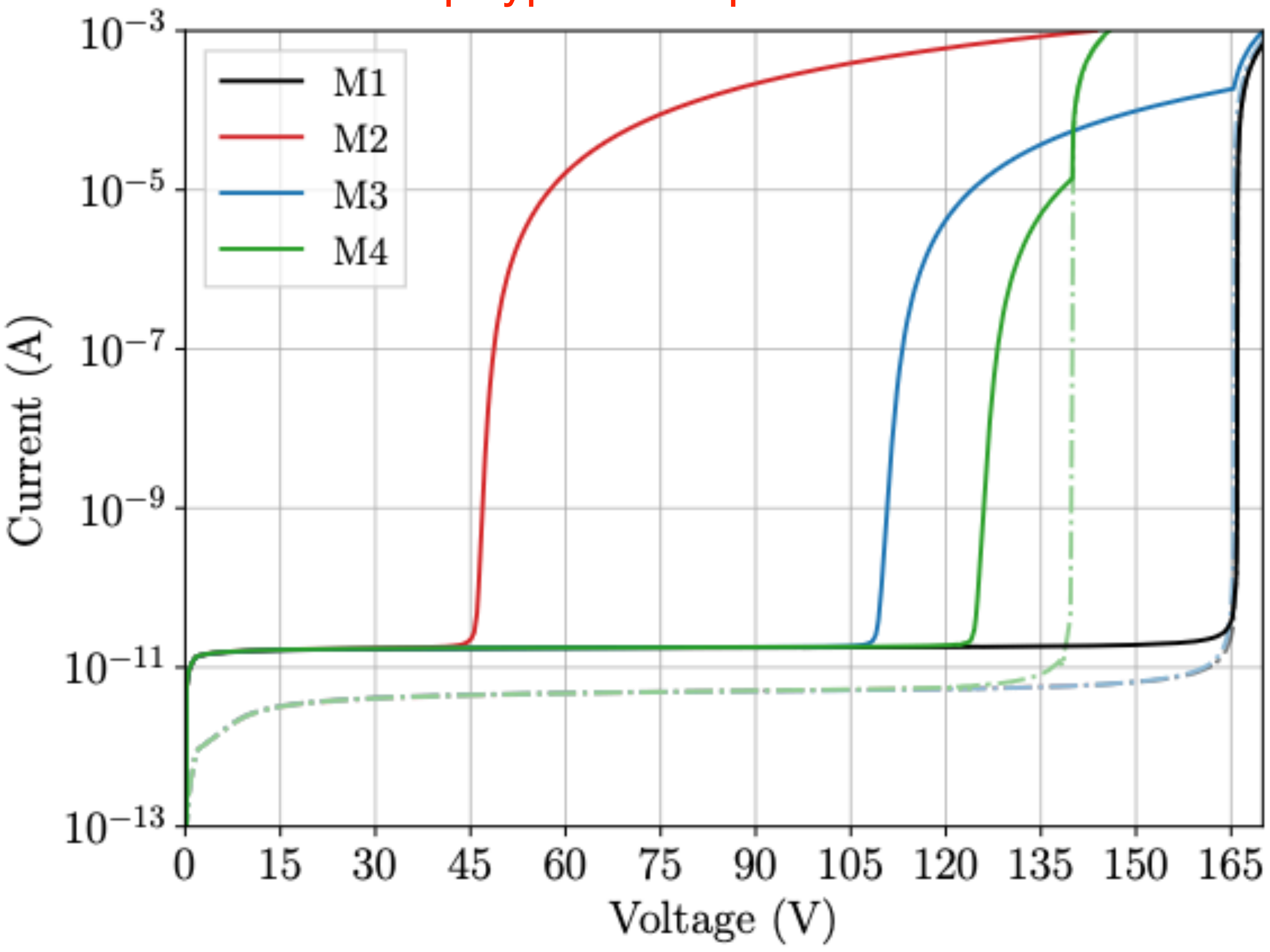


General structure of the CASSIA sensors

TCAD simulation

- TCAD in 2D cylindrical
- Use Okuto-Crowell model for charge multiplication
- bias electrode, substrate/PW on GND
- current electrode/GL (solid) and electrode-surrounding p-well (dashed)

NW electrode + p-type GL depth 1 20um



Shallow electrode + p-type GL depth 2 12um

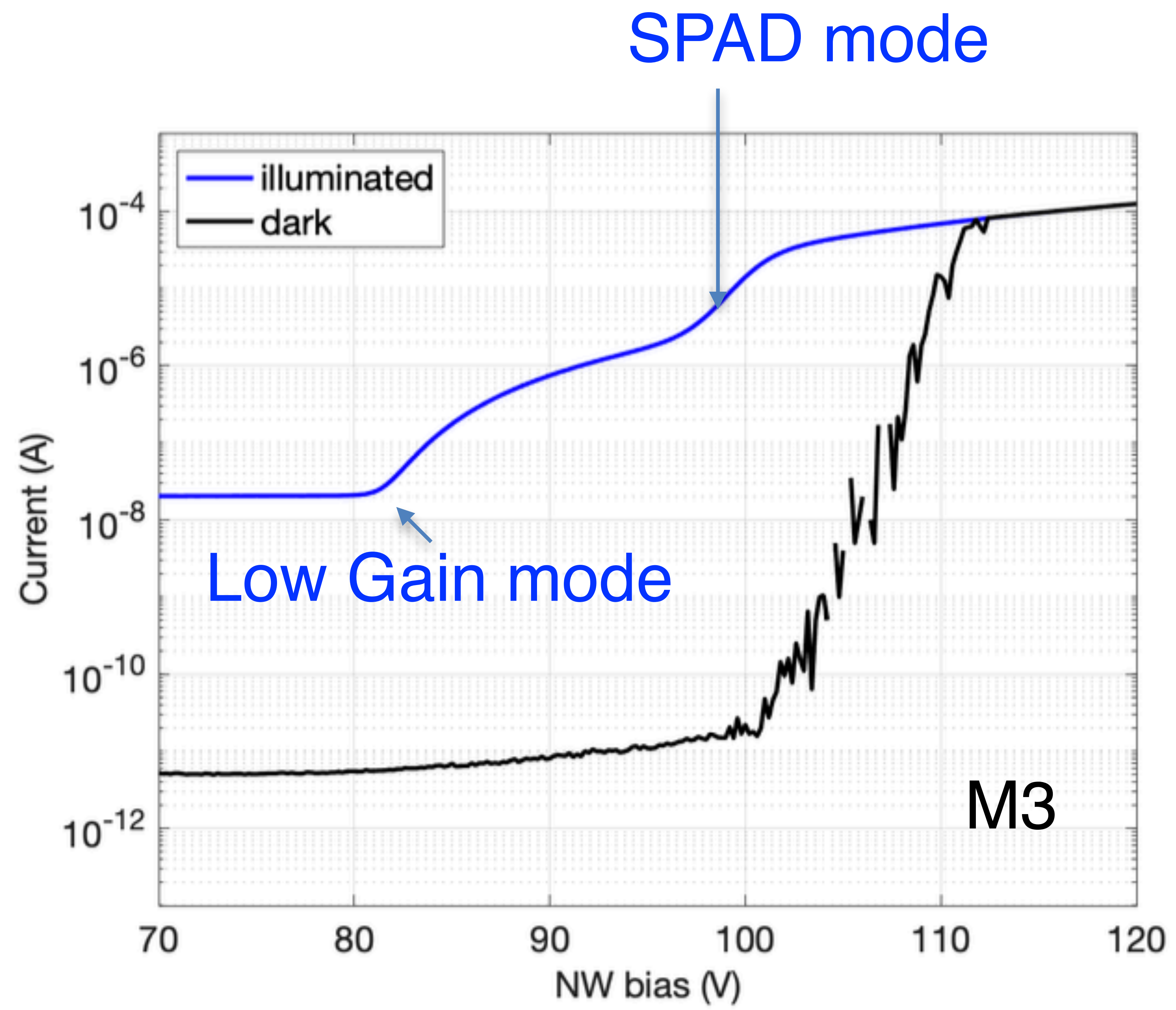
No GL (breakdown to PW @165V)

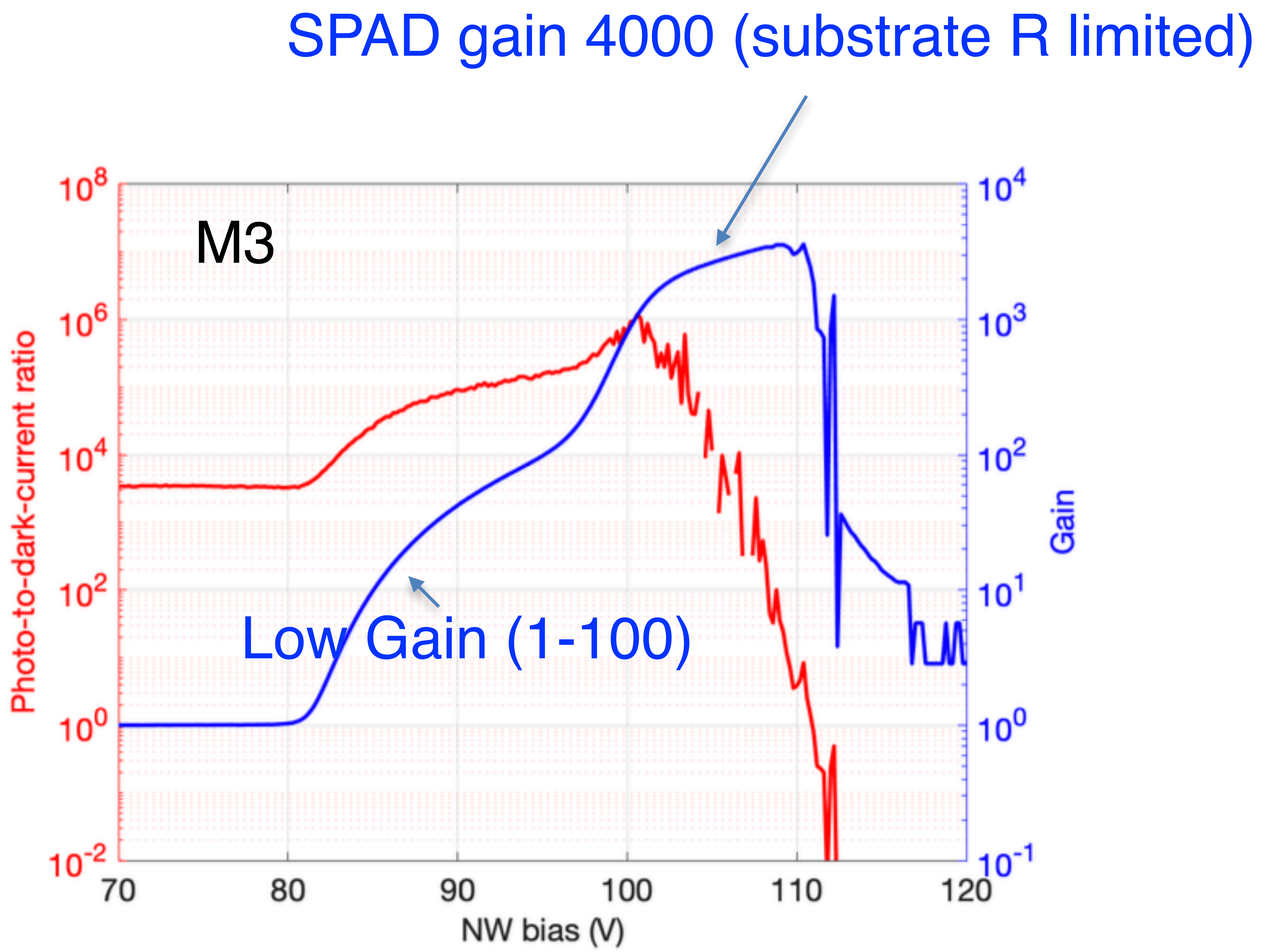
NW electrode + p-type GL depth 2 12um

TCAD matches measurement results very well

Dark and illuminated visible light : IV curve and gain

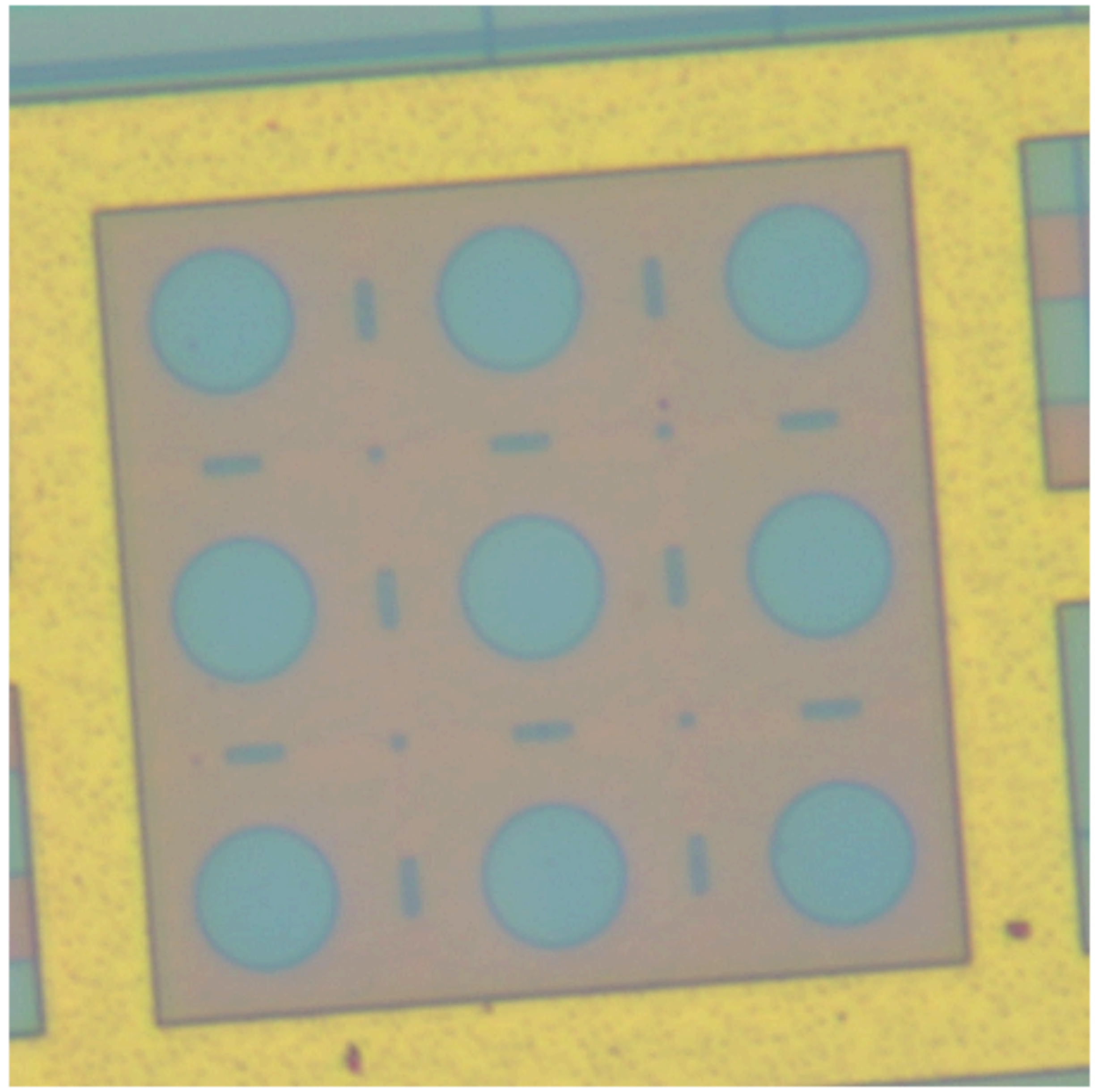
- bias voltage applied on n+ electrode & illuminated with visible light
  - very well controlled gain modes : LGAD mode 82V to 98V , SPAD mode >100V



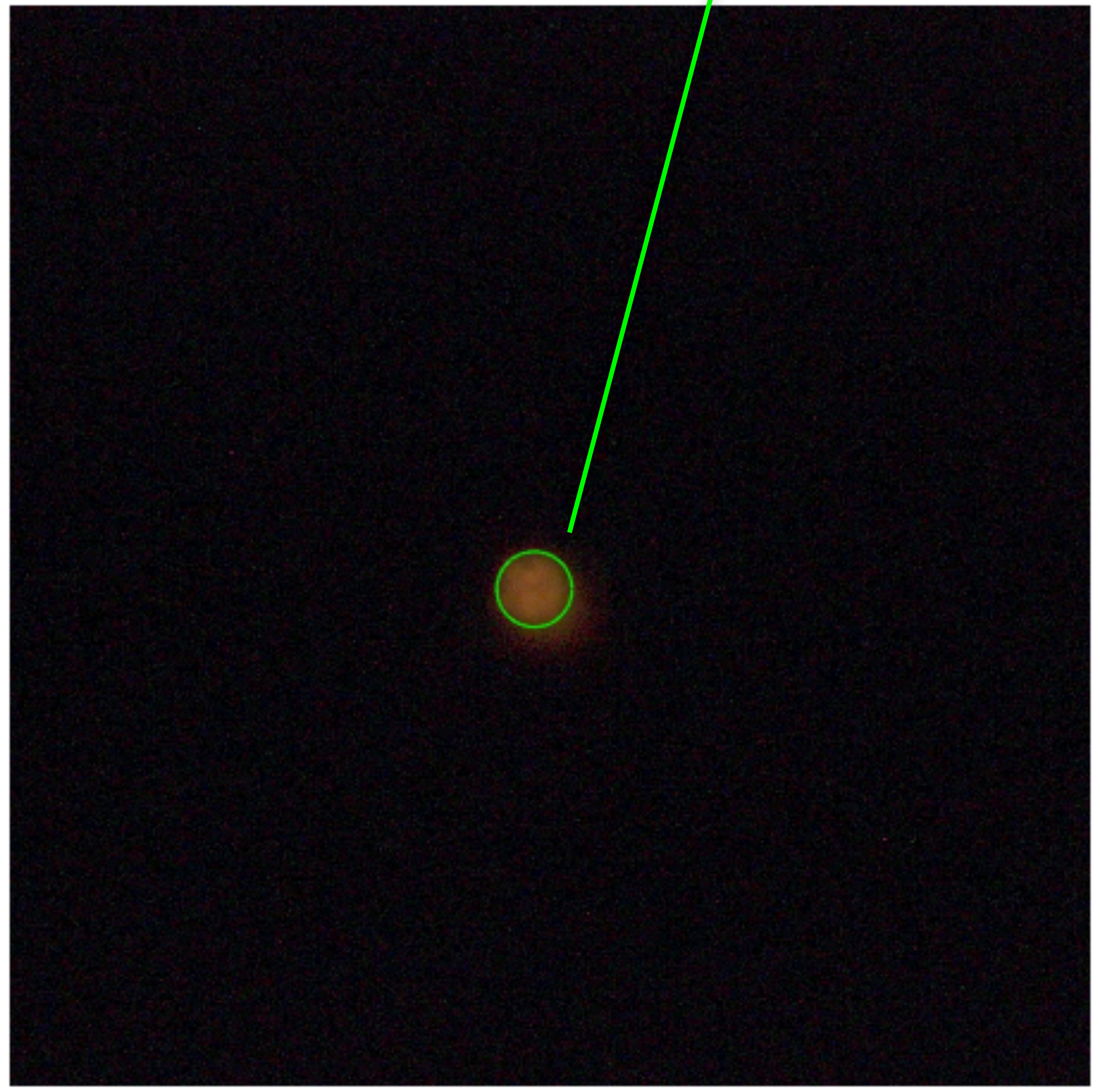


Break down in GL area or edge ? Light emission measurements

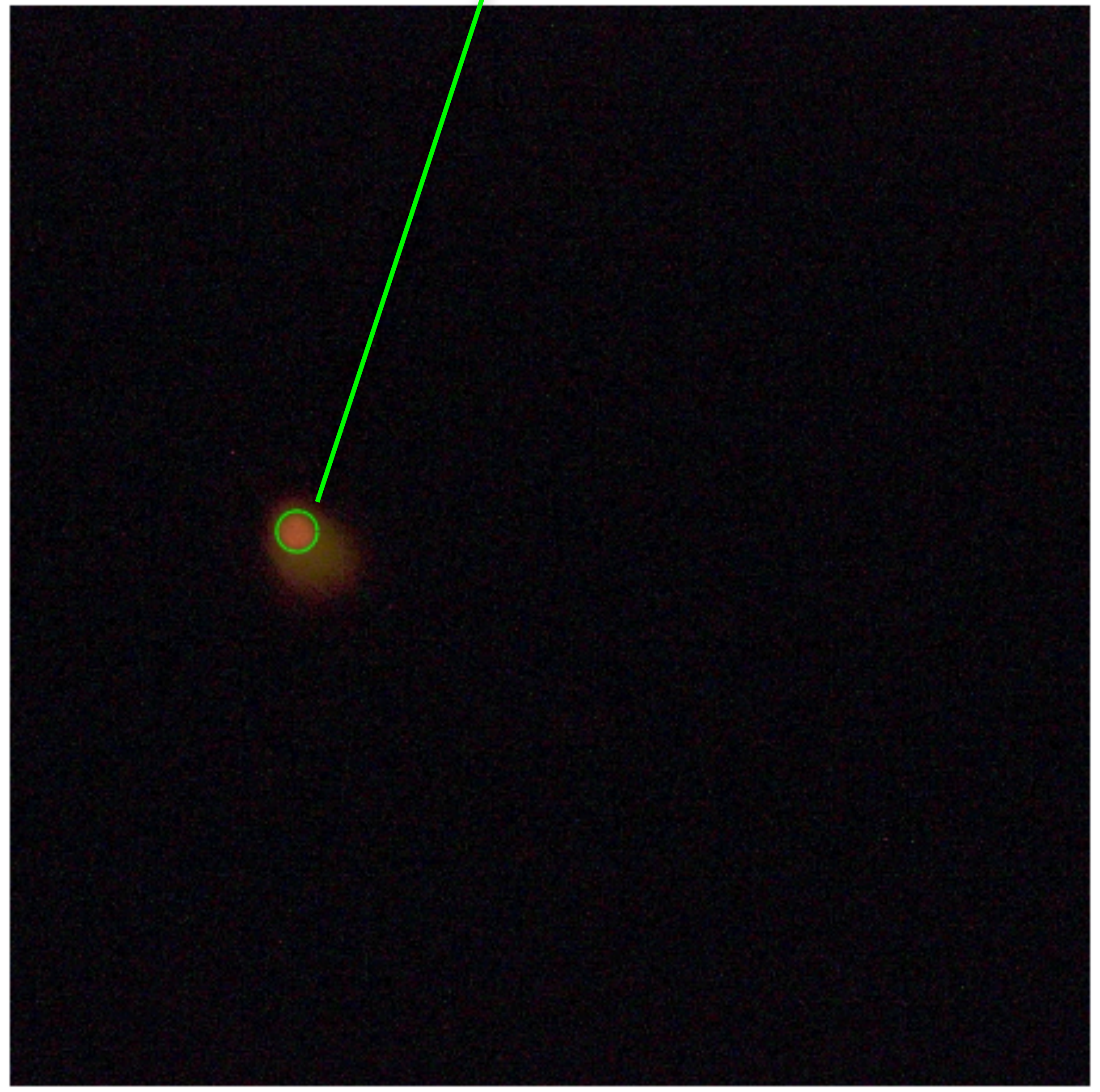
- bias electrode >100V and record light emission
  - Light emitted uniformly across GL and spot size matches GL diameter



M2 - 20um GL diameter



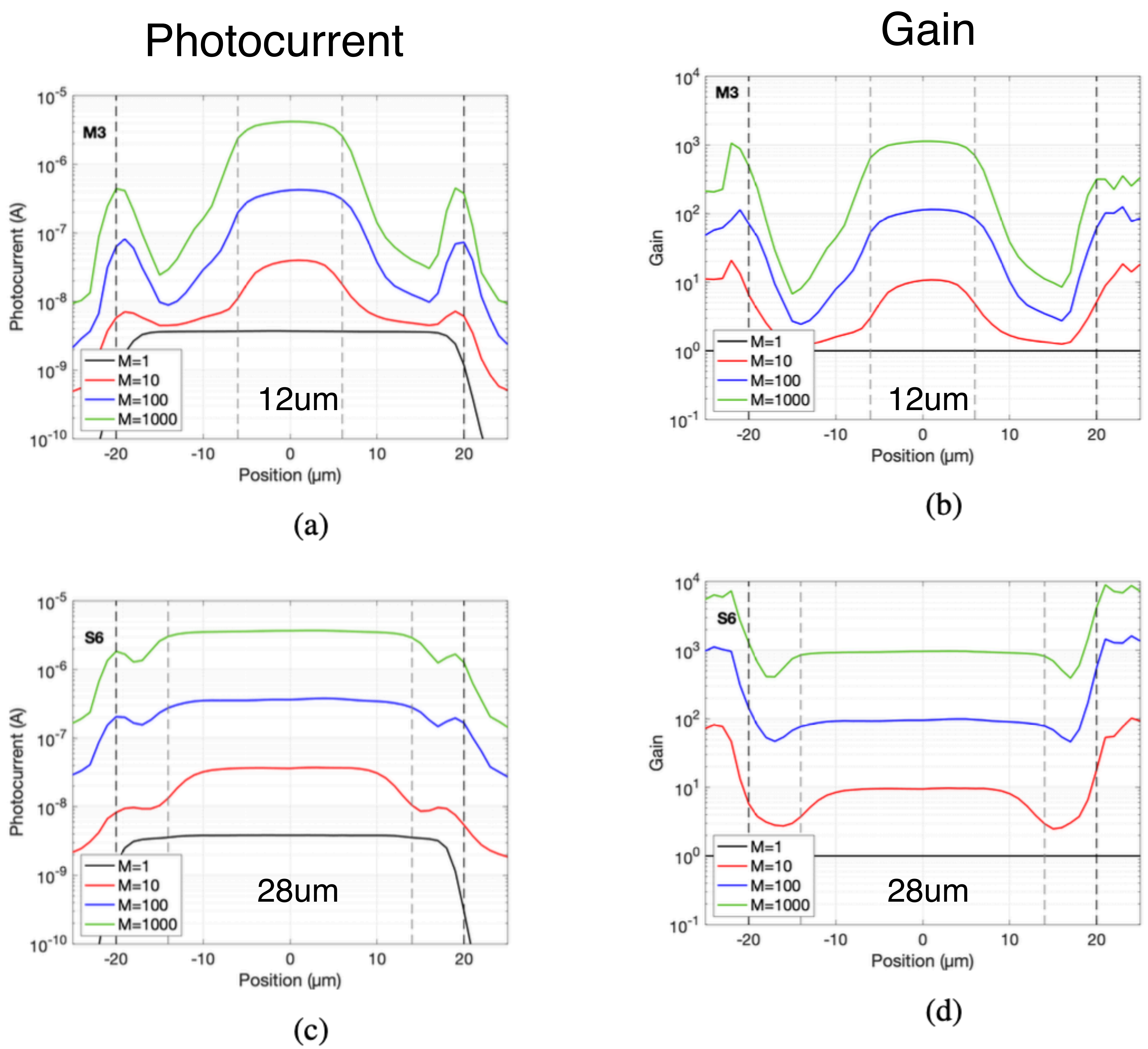
M3 - 12um GL diameter



Photocurrent and gain uniformity across pixel

- focused 2um FWHM laser beam 782nm scanned across pixel
  - Light emitted uniformly across GL and spot size matches GL diameter
  - compare GL diameter 12um (M3) and GL diameter 28um (S6)

- Very uniform gain across gain layer area
- Still significant gain outside GL area (~x2 in fill factor)

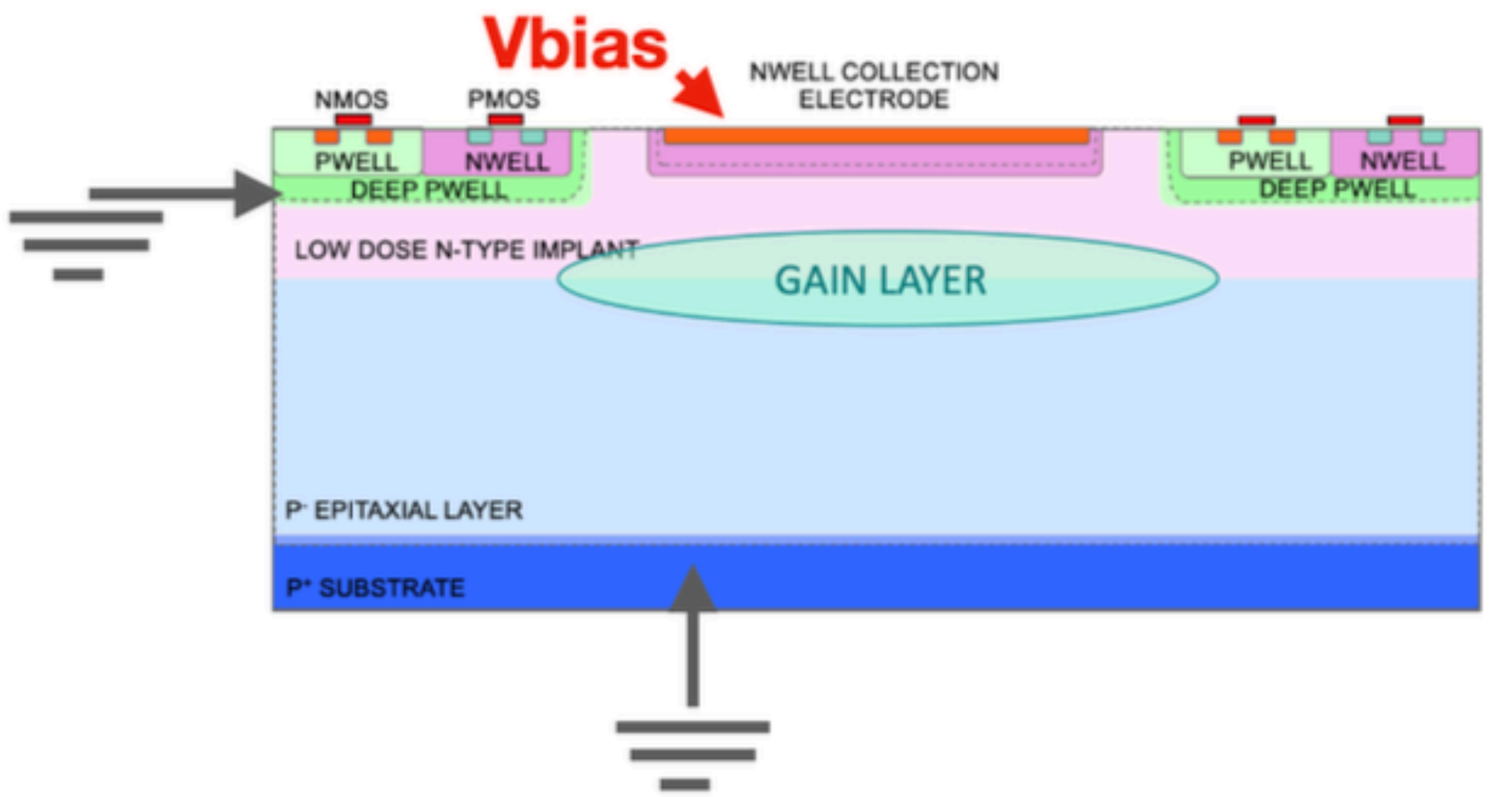


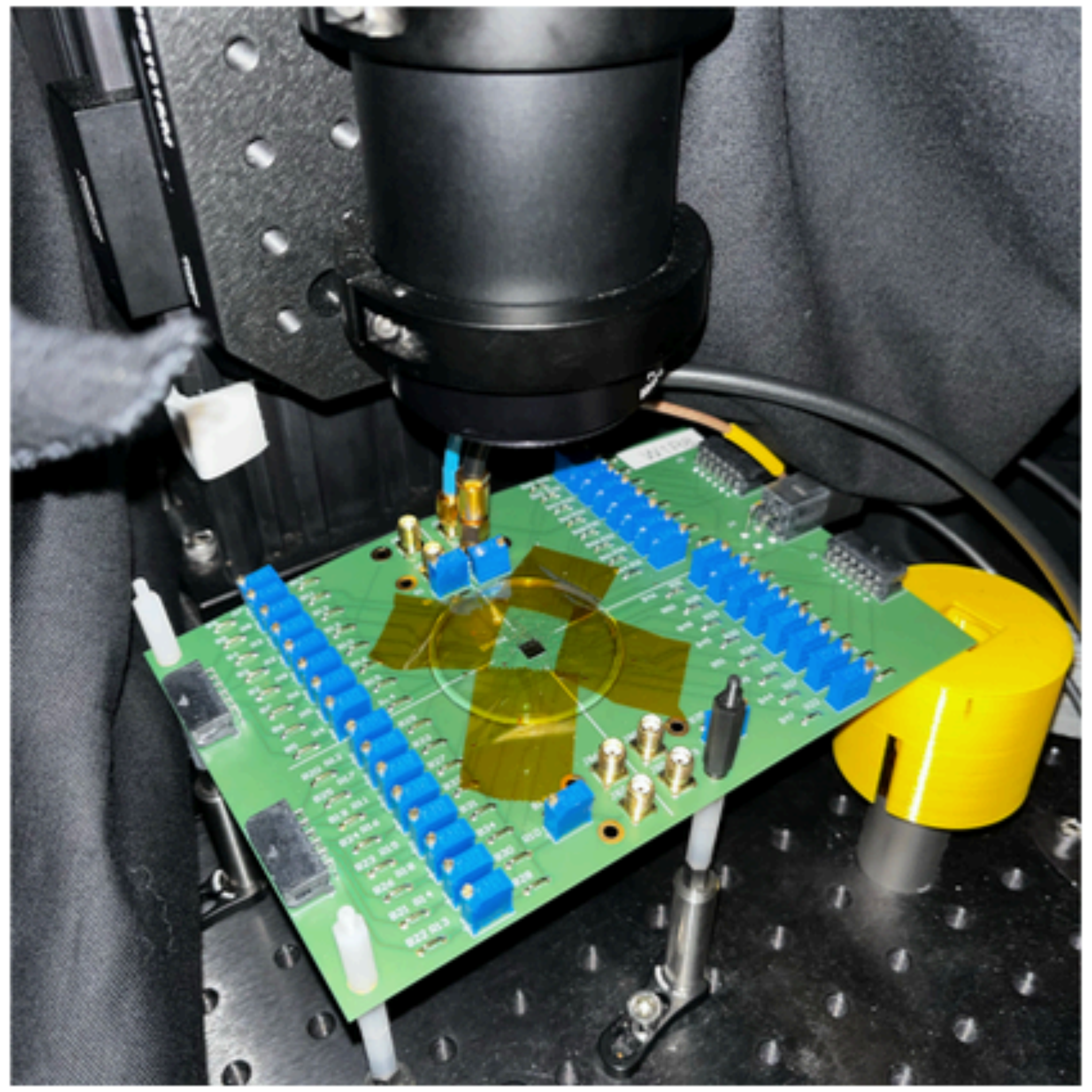
Pulsed laser measurements (triggered 1060nm laser)

- Pixel matrix exposed to triggered pulsed laser
  - pulse width <100ps
  - laser not focused (expose area>pixel)
- Pixel connected to external amplifier
  - bias electrode through amplifier
  - record single pulse waveform to analyse amplitude and arrival time wrt to external trigger
  - record electrode current as function of pulse frequency
  - record electrode current without laser (dark current)

Laser setup

- Laser source (1060nm)
- Used for timing and gain measurements



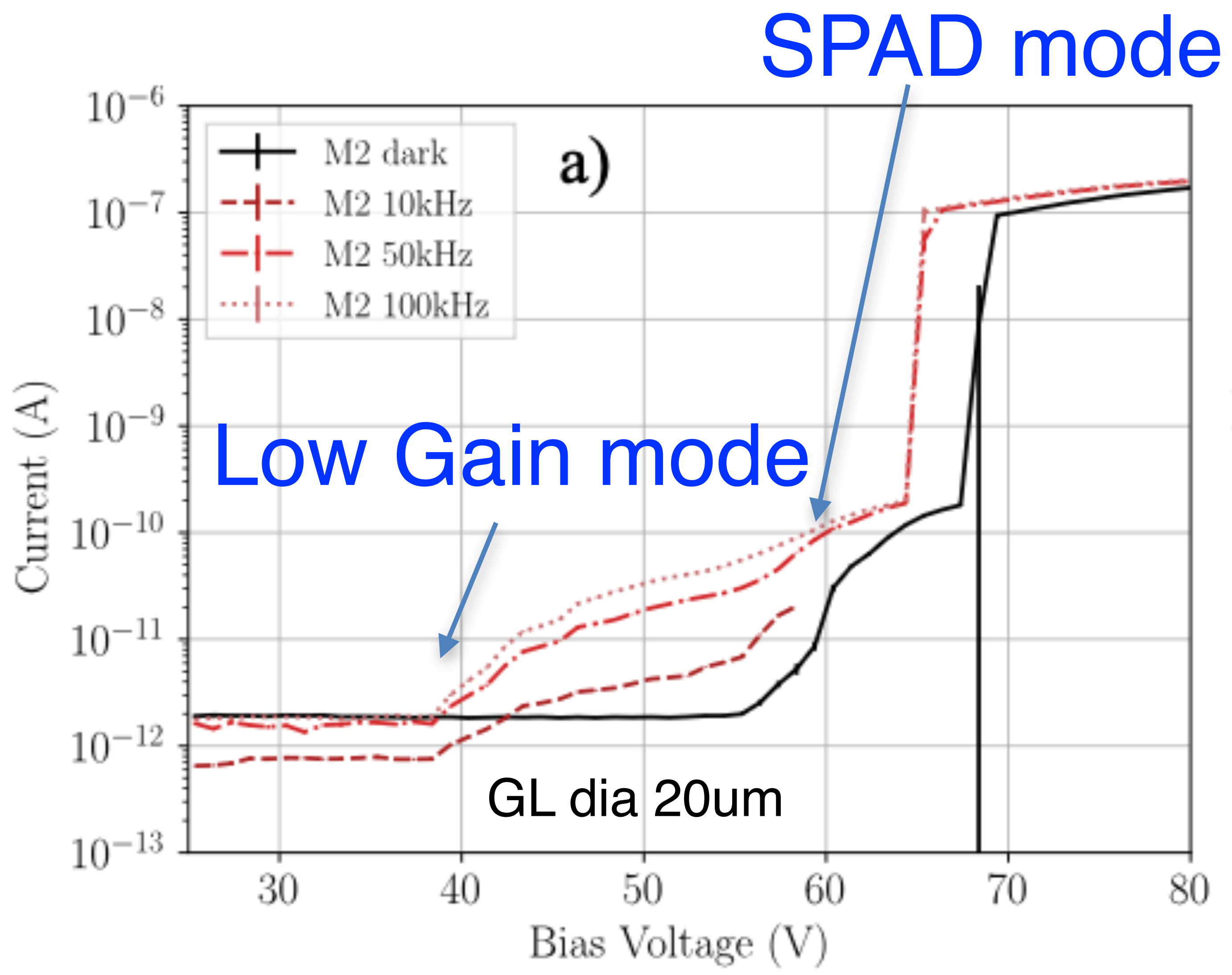


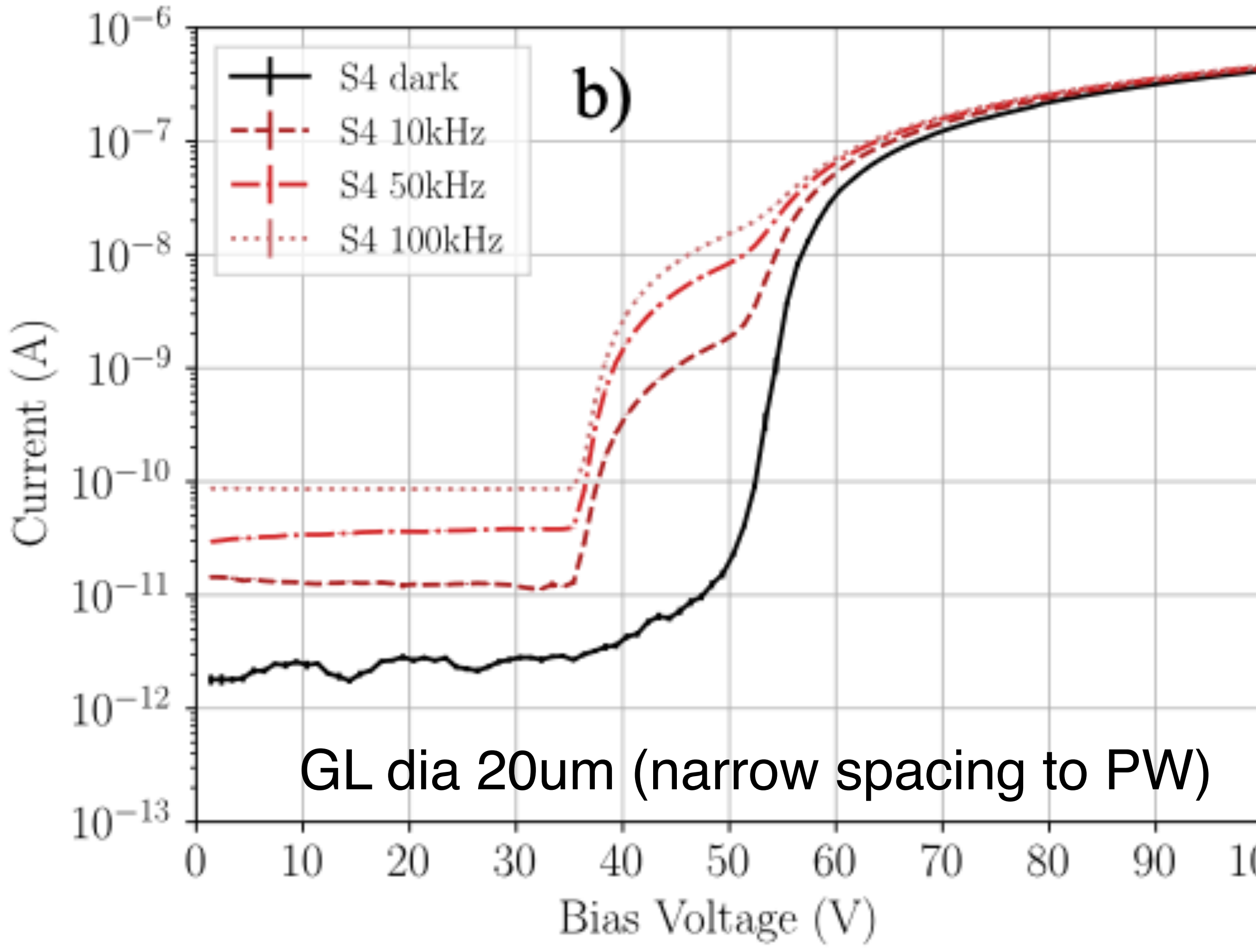
I-V in pulsed laser measurements (triggered 1060nm laser)

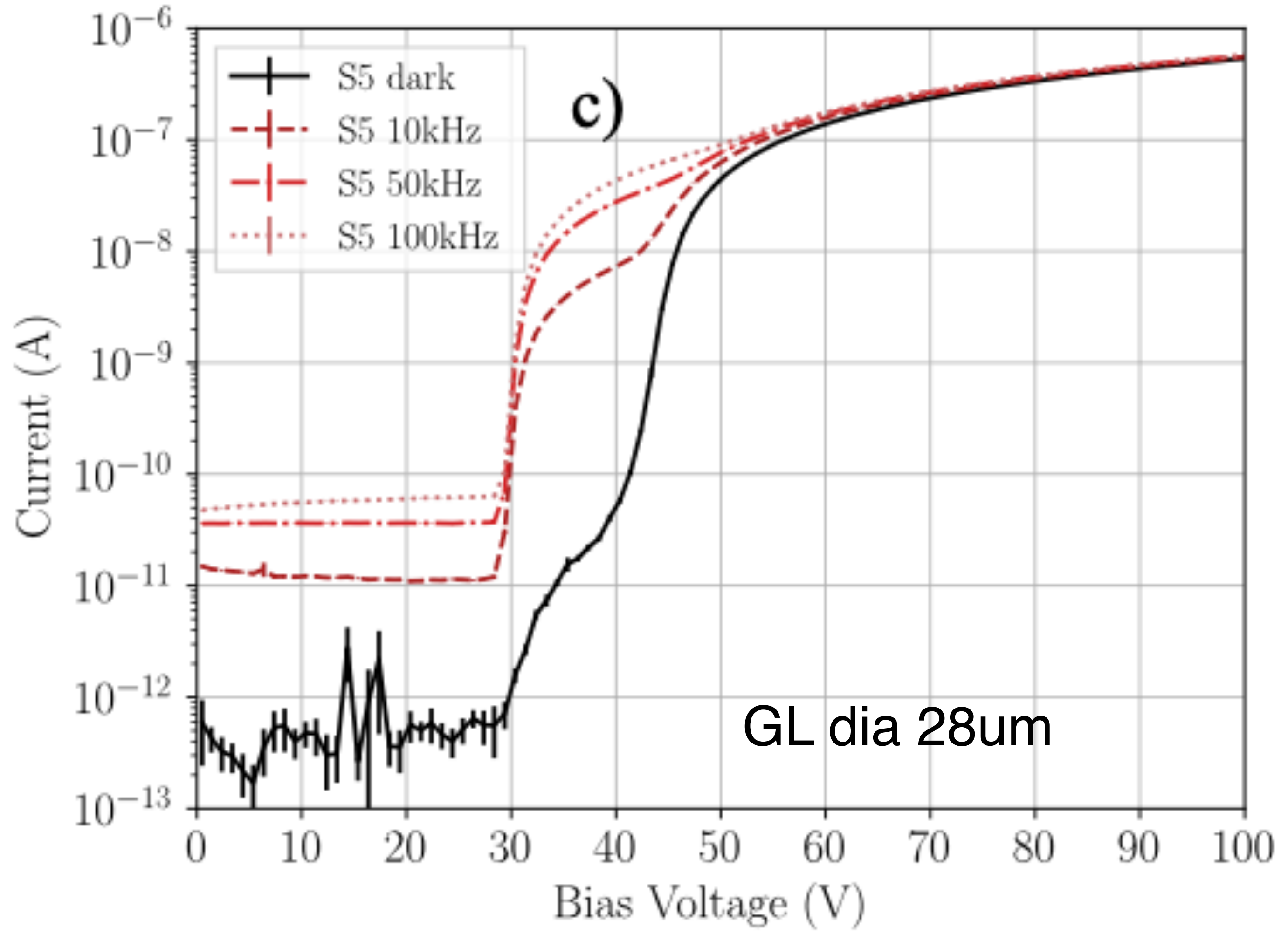
- I-V in dark, 10kHz, 50kHz and 100kHz
  - substrate and PW GND
  - n+ electrode bias to +V
  - matrix without GL 1pA/pixel until 160V

- Study charge amplification as function of electrode and GL implant configuration
  - different gain layer diameter for each configuration

A. NW electrode + p-type GL depth 1: CASSIA M2/S4/S5
B. NW electrode + p-type GL depth 2: CASSIA M3/S6
C. Shallow electrode + p-type GL depth 2: CASSIA M4/S19
D. Deep electrode + p-type GL depth 2: CASSIA S13/S14



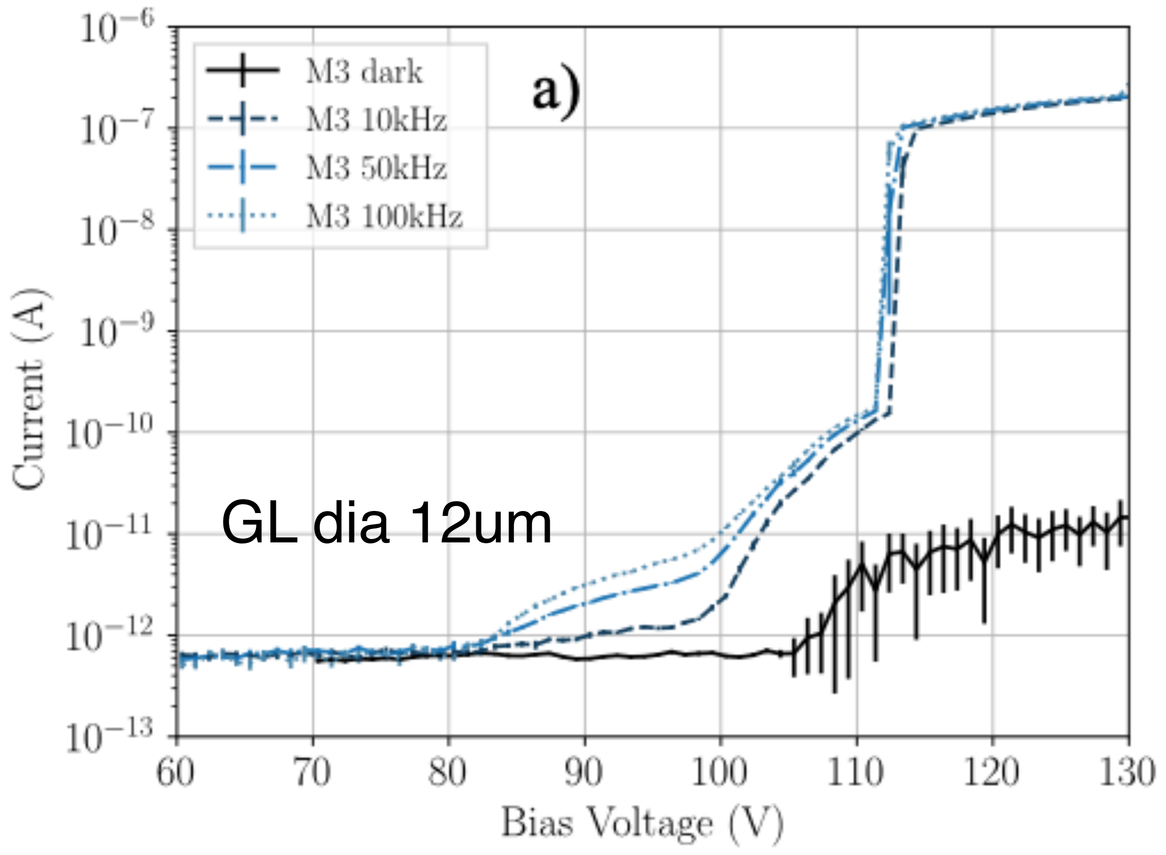




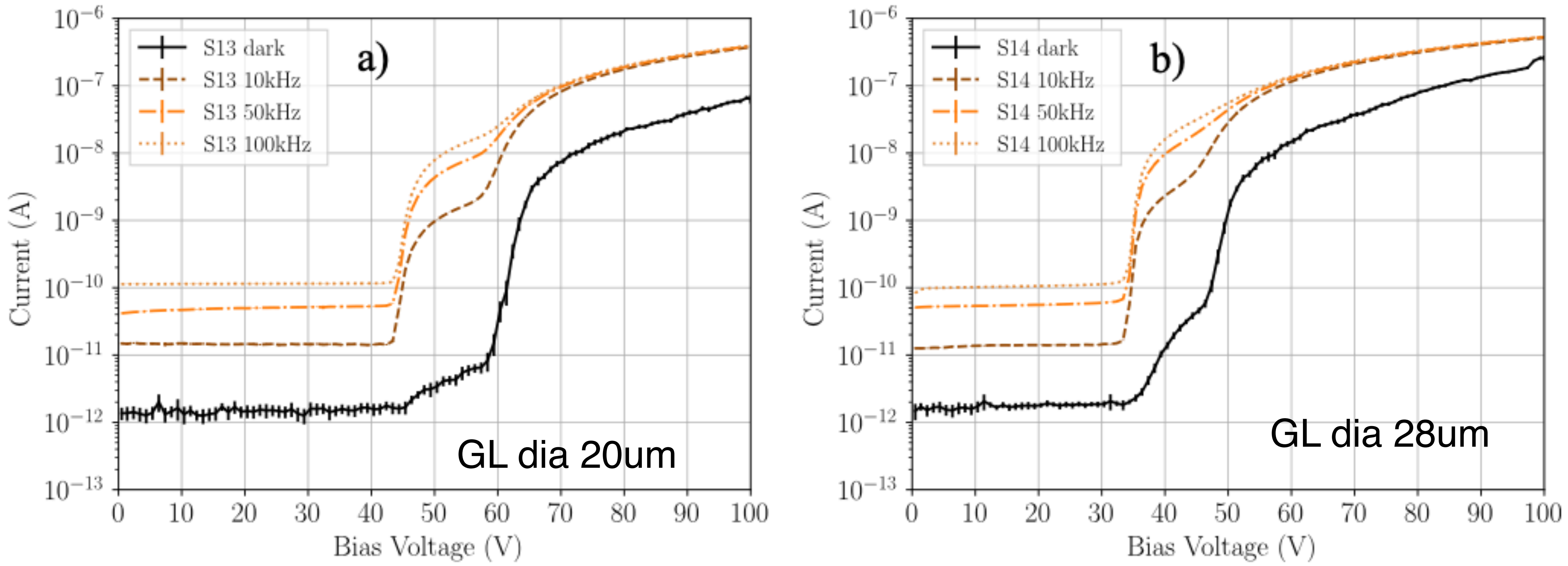
- NW electrode + p-type GL depth 1
  - LGAD mode starts at 30V to 40V
  - Transition to SPAD mode about 15V later
  - larger GL area reduces amplification voltages

I-V in pulsed laser measurements (triggered 1060nm laser)

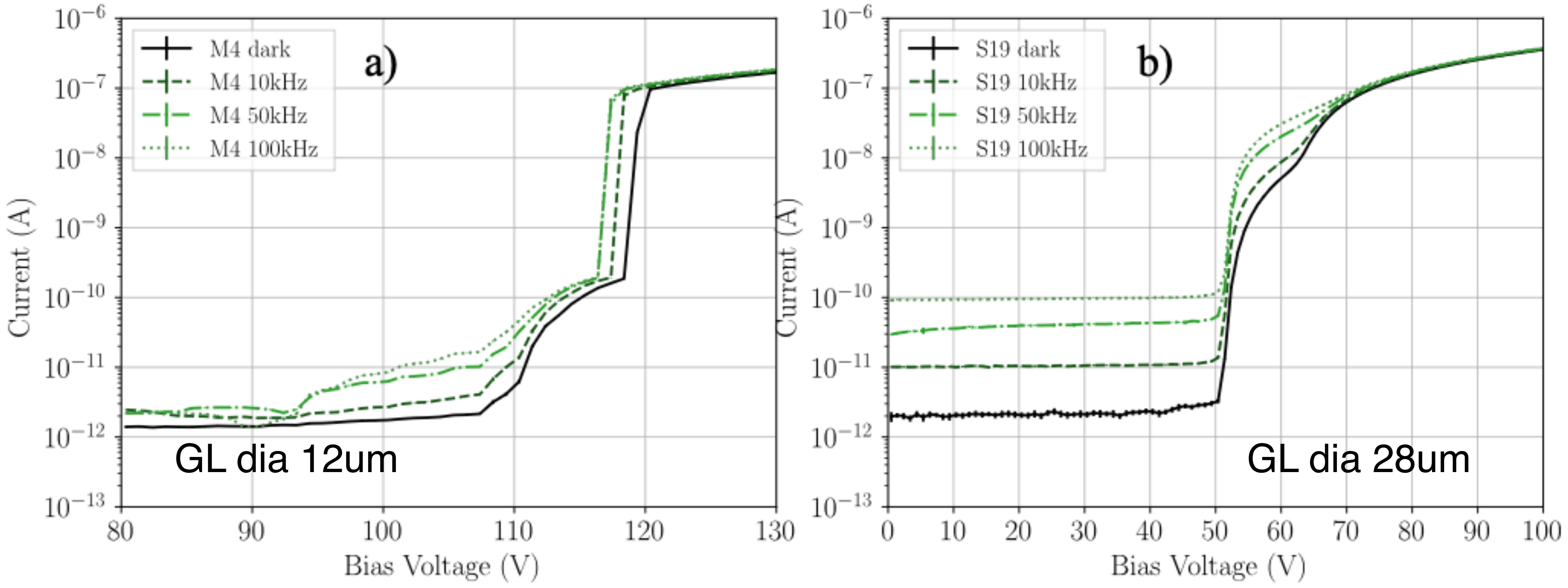
NW electrode + p-type GL depth 2



Deep electrode + p-type GL depth 2



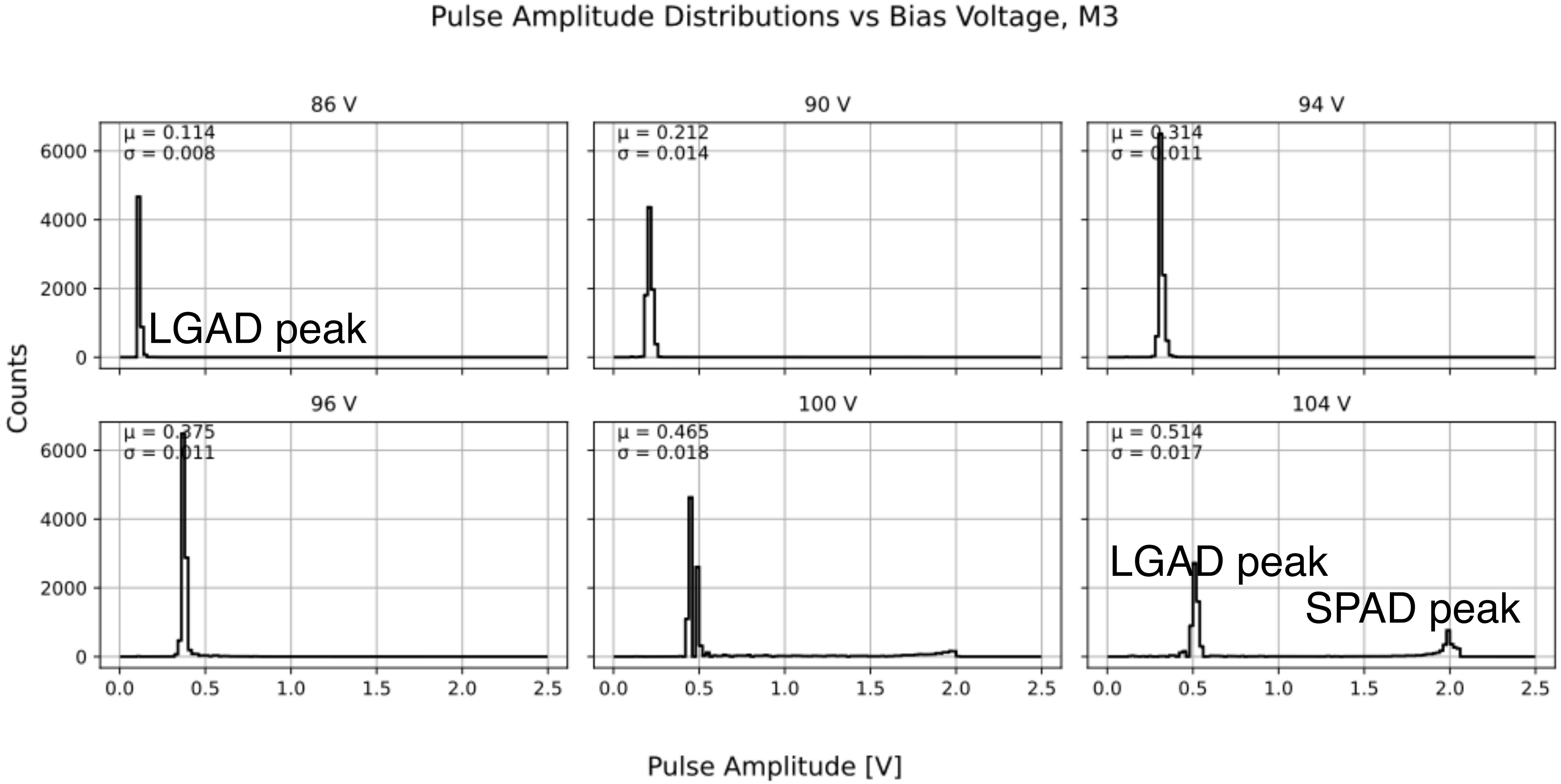
Shallow electrode + p-type GL depth 2



- Observations in I-V of pulsed 1060nm laser:
  - Photo current scales as expected with pulse frequency (flux) and gain layer area
  - In all cases observe LGAD mode and smooth transition to SPAD mode
  - for all combinations of electrode and gain layer implantation the necessary bias voltage to achieve avalanche multiplication can be achieved

Single pulse amplitude distribution (triggered 1060nm laser)

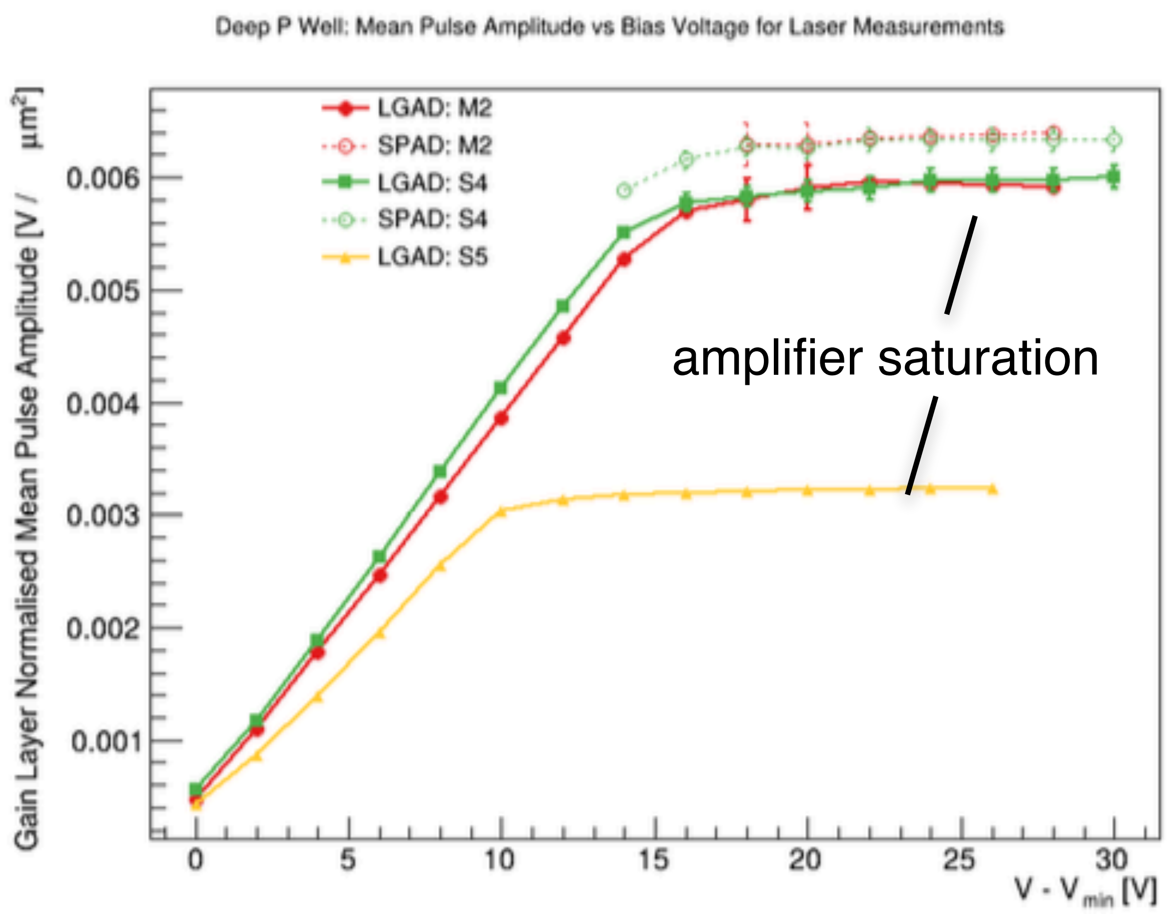
- Single pulse measurements:
  - for each external laser trigger the CASSIA single pulse signal is recorded for the central pixel on amplifier output
  - amplifier gain = 6.7mV/fC
- Analysis:
  - determine amplitude
  - use arrival time to reject any noise



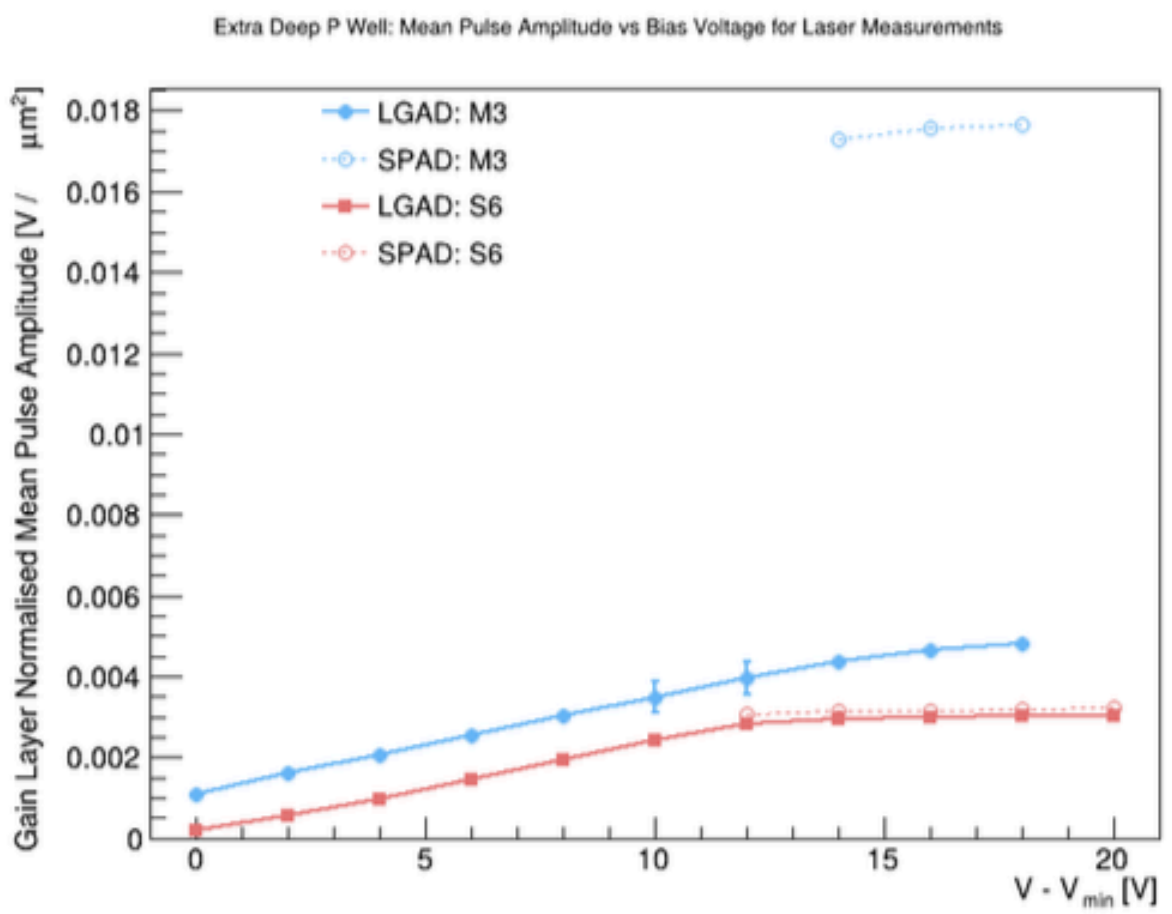
$V>V_{LG}$ =84V : LGAD amplitude increases with applied voltage
@V_{BR} =104V : transition to SPAD mode: second peak occurs
$V>V_{BR}$: detector operates in SPAD mode

Mean single pulse amplitude as function of electrode/gain layer implantation

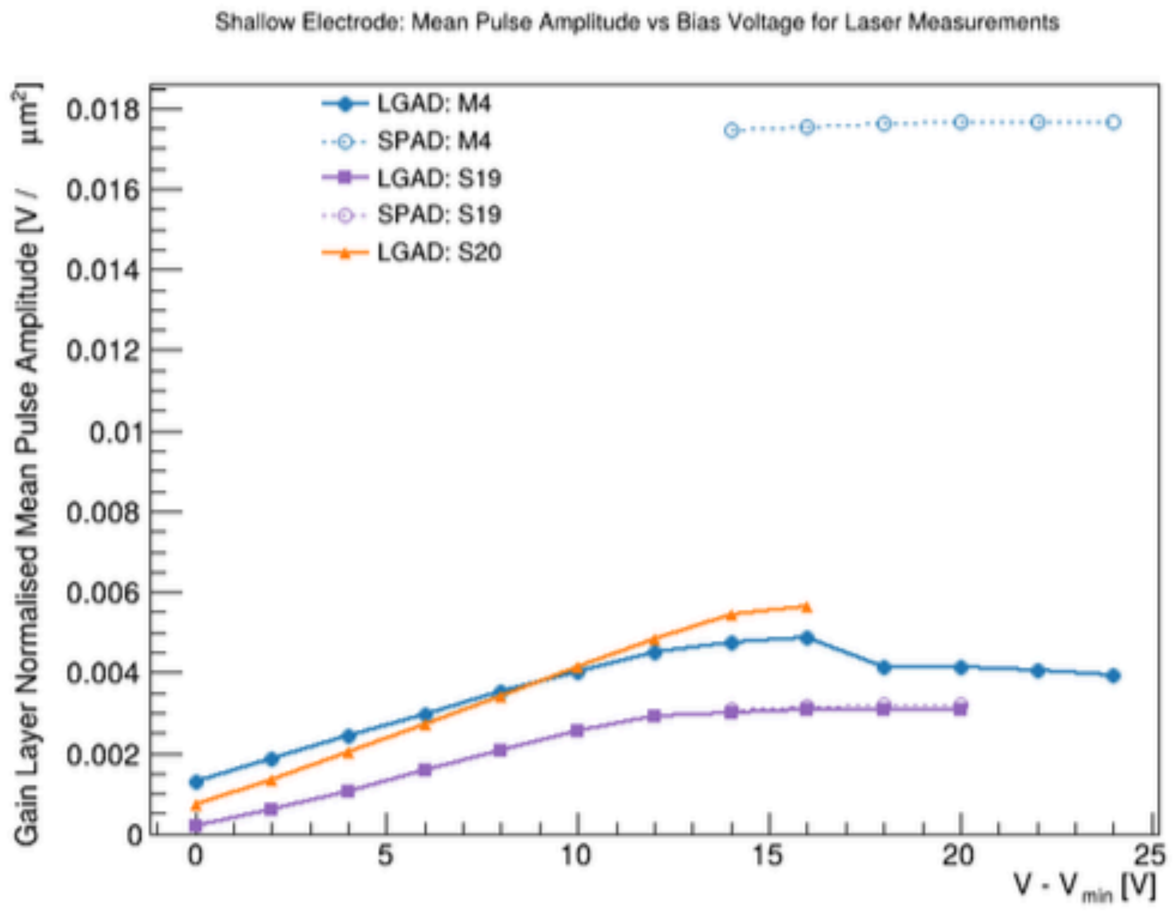
- Mean amplitude depends on:
  - gain layer size , i.e. flux, hence normalize results to gain layer area
- Study single pulse gain as function of:
  - implant configuration of electrode and gain layer
  - bias voltage in LGAD and SPAD mode
- Observations:
  - all structures using GL depth 2 (plots b-d) have ~ same gain in LGAD mode
  - structure with GL depth 1 has x2 larger gain in LGAD mode (shallower gain layer)



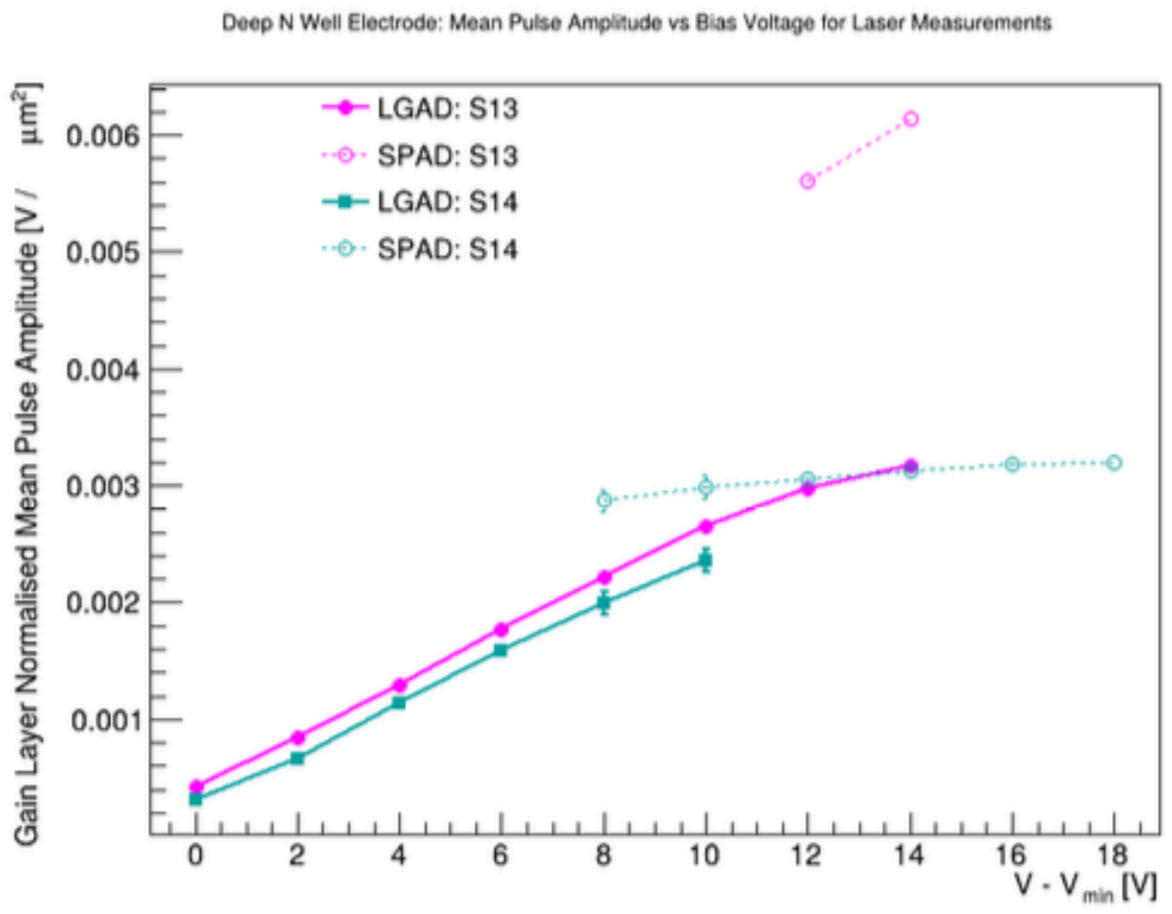
NW electrode + p-type GL depth 1
(a)



NW electrode + p-type GL depth 2
(b)



Shallow electrode + p-type GL depth 2
(c)



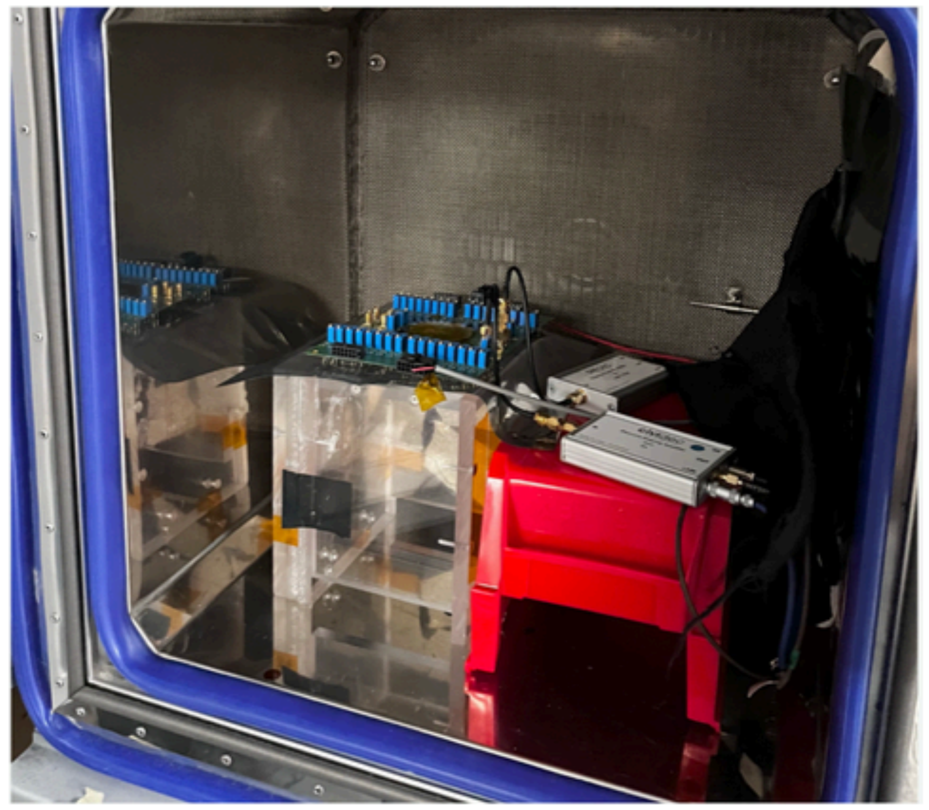
Deep electrode + p-type GL depth 2
(d)

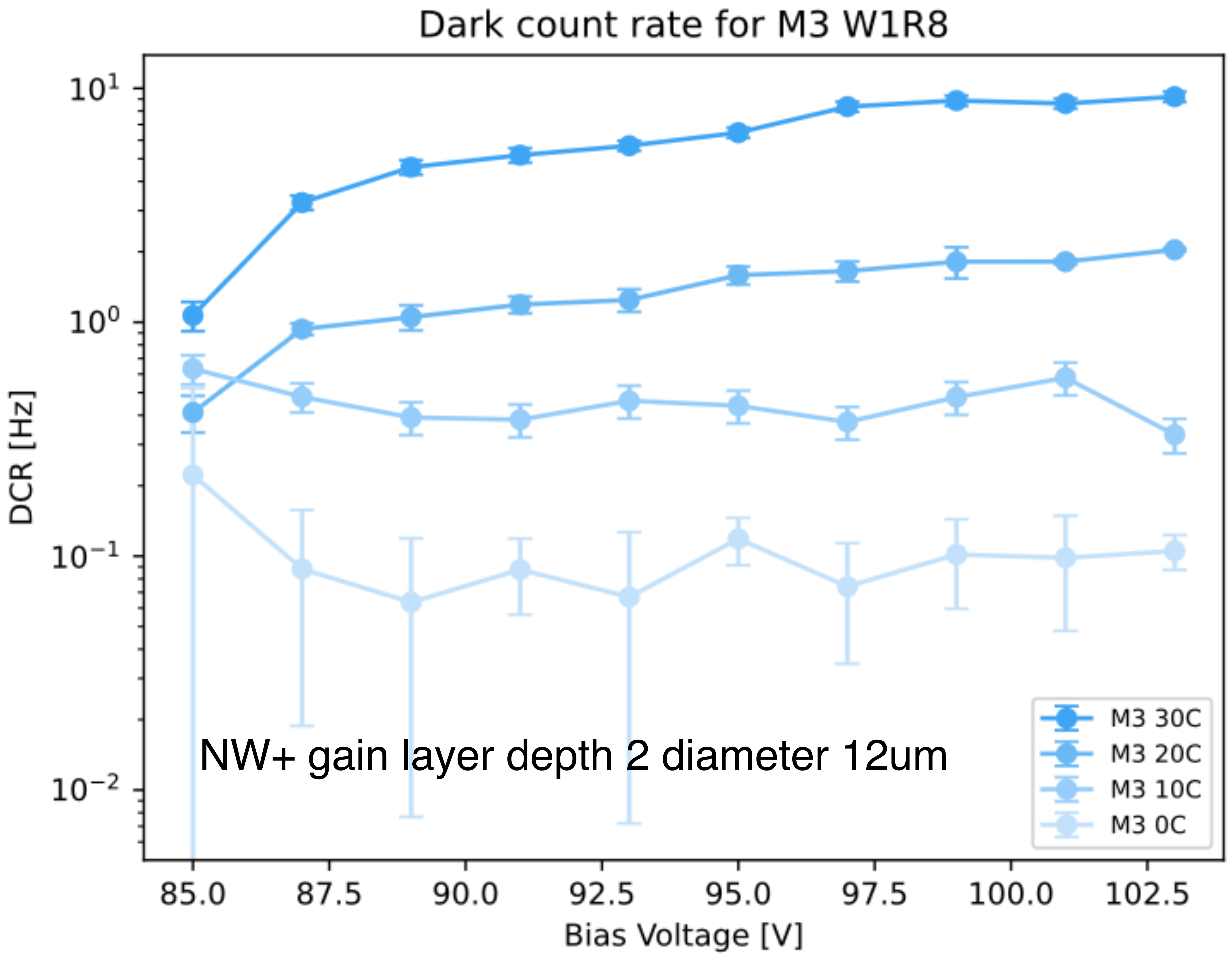
CASSIA Dark count rate for different designs

- Operate CASSIA in climate chamber
  - measure at 0C, 10C, 20C and 30C
  - count pluses at amplifier output (same setup as in triggered laser setup)

Climate chamber

- Controlled temperature and humidity
- Light proof
- Used for dark count and IV measurements



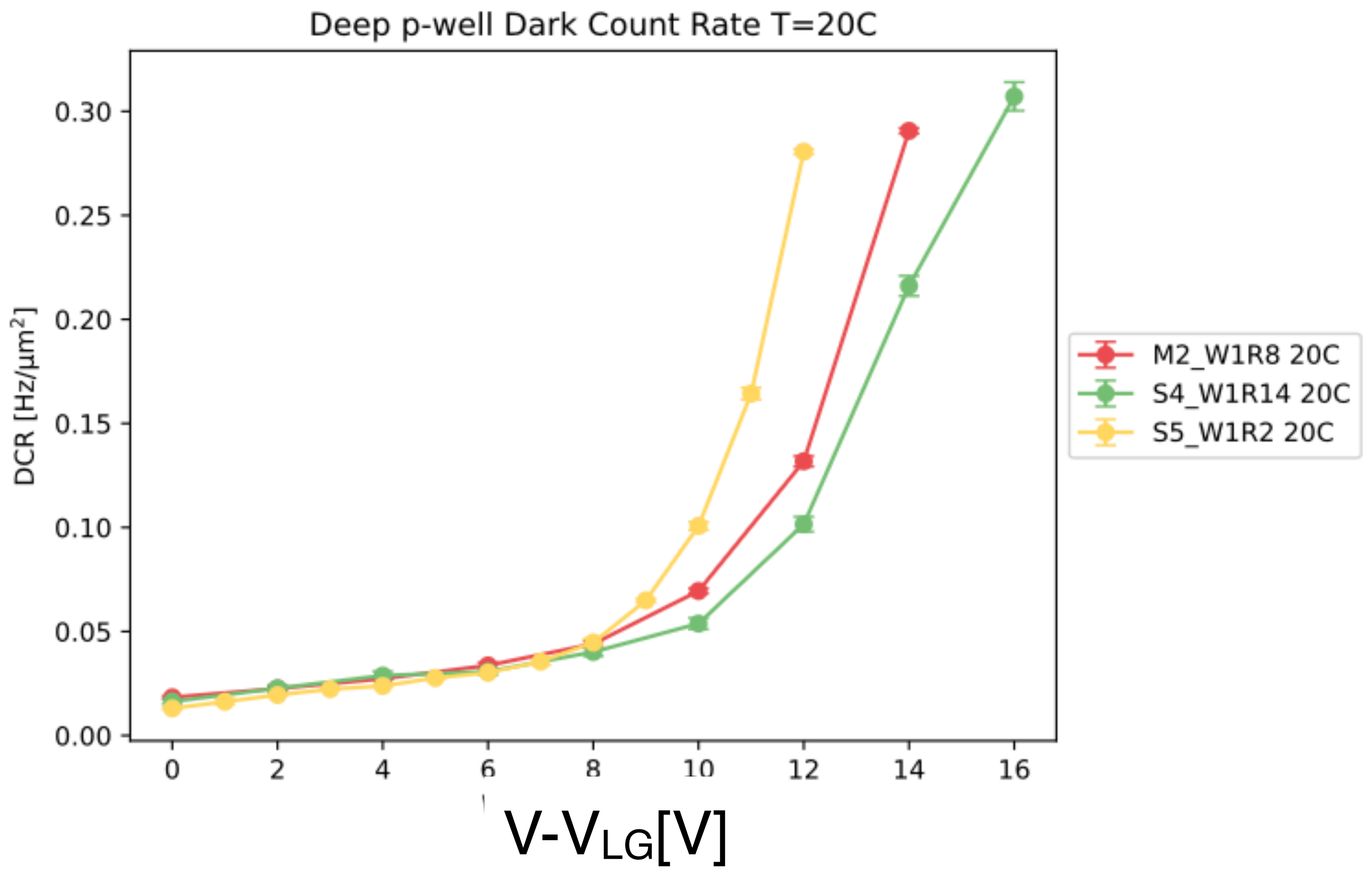


- extremely low dark count rate in voltage range of interest: <0.01 Hz/um2 at RT
- after V_{BR}=100-104V transition to SPAD: with V_{EXCESS}=15V (V_{bias}=120V) DCR ~ 0.1 Hz/um2 at RT
- DCR scales exponentially with temperature (thermally generated noise in active area)

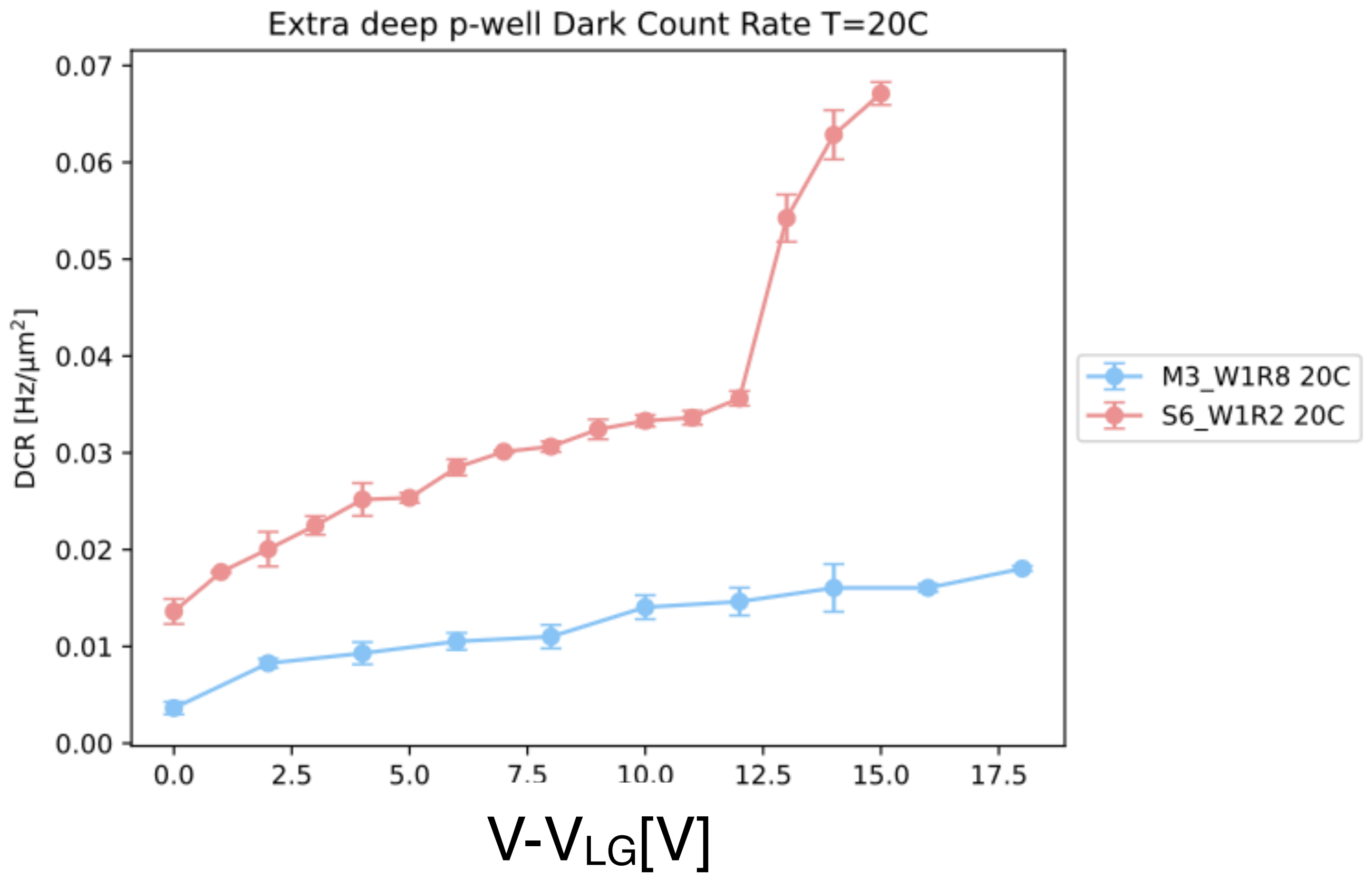
CASSIA Dark count rate for different designs

- DCR normalised to Gain layer area
  - V_{LG} = voltage at start of LGAD amplification
  - Room temperature
- Best results are obtained with gain layer formed by GL depth 2 and either normal or deep electrode contact
- Using only shallow electrode implantation gives significantly worse results (surface defects?)

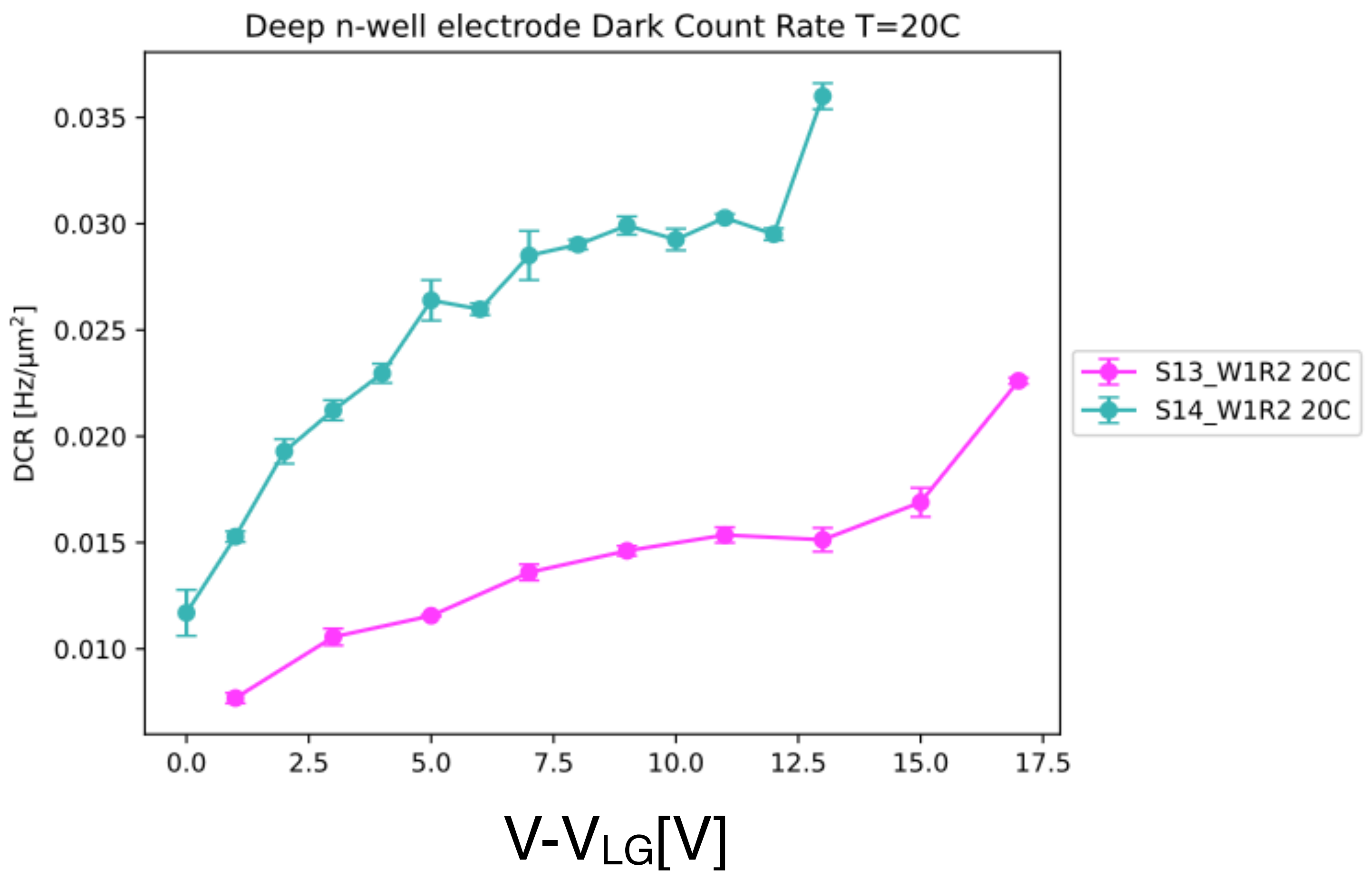
NW electrode + p-type GL depth 1



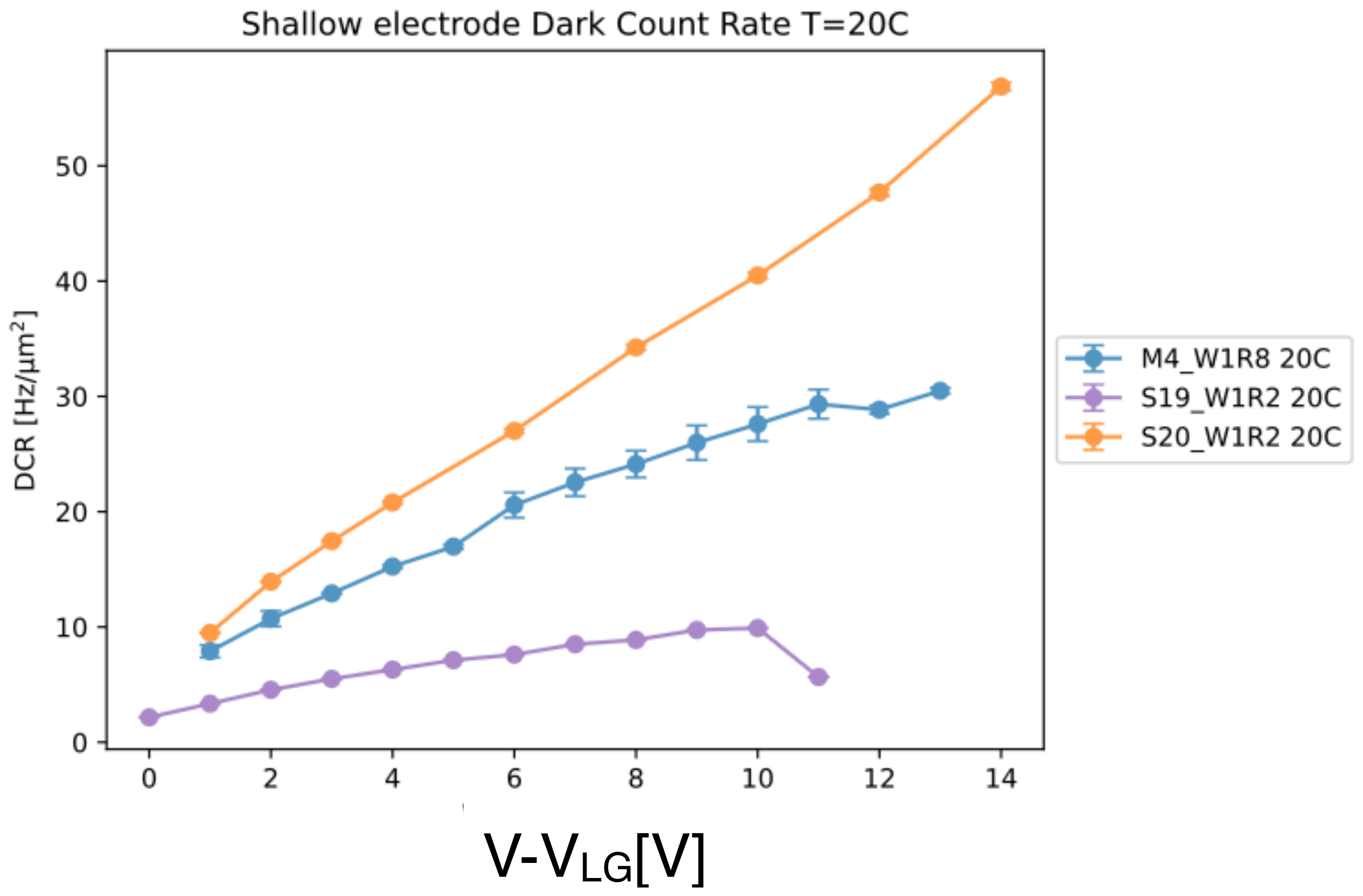
NW electrode + p-type GL depth 2



Deep electrode + p-type GL depth 2

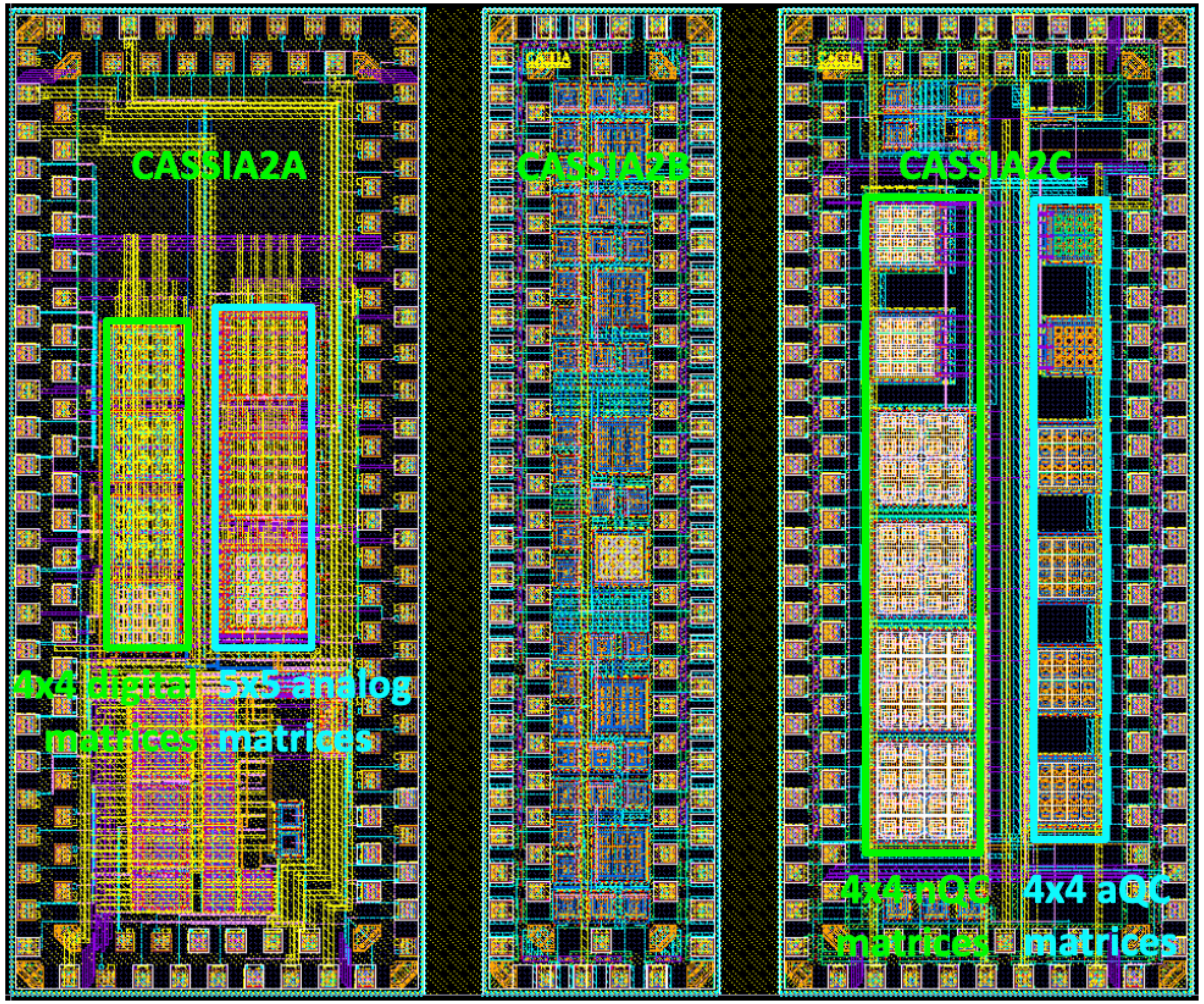


Shallow electrode + p-type GL depth 2



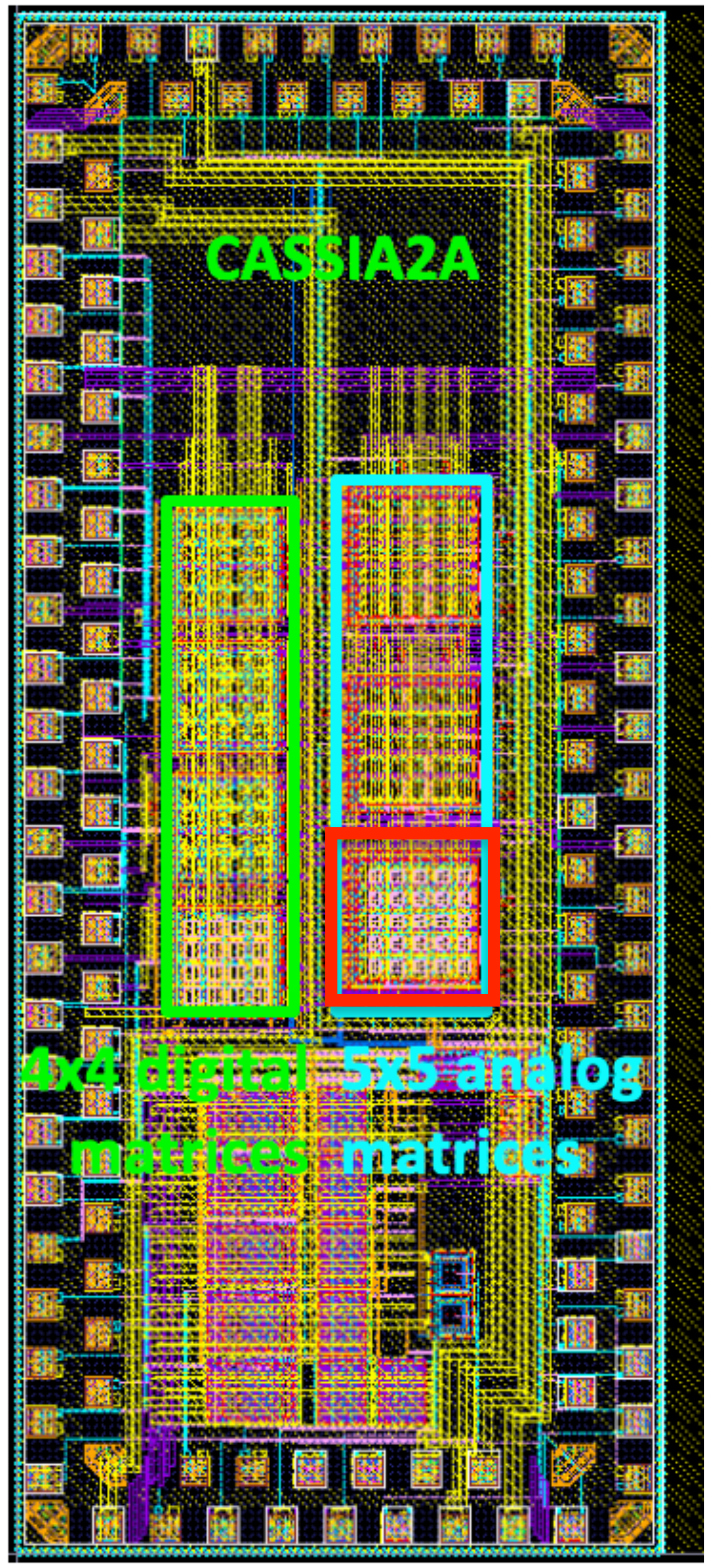
Next developments: CASSIA2 design submitted

- **With next chip CASSIA2 we aim to**
  - enlarge fill factor to achieve gain substantially beyond geometrical GL area (aim at close to 100% efficiency for charged particles)
  - Optimised gain layer doping and design for better charge collection outside GL area (pixel edge)
  - include in-pixel electronics for LGAD and SPAD operation
- **We submitted CASSIA2 to IPHC engineering run QUARTPICS2**
  - focus on small matrixes (4x4,5x5 pixel) suitable for lab and testbeam measurements as well as irradiations
  - designs include in-pixel amplifier and quenching circuits in matrices
  - new designs for GL to achieve full efficiency across the pixel

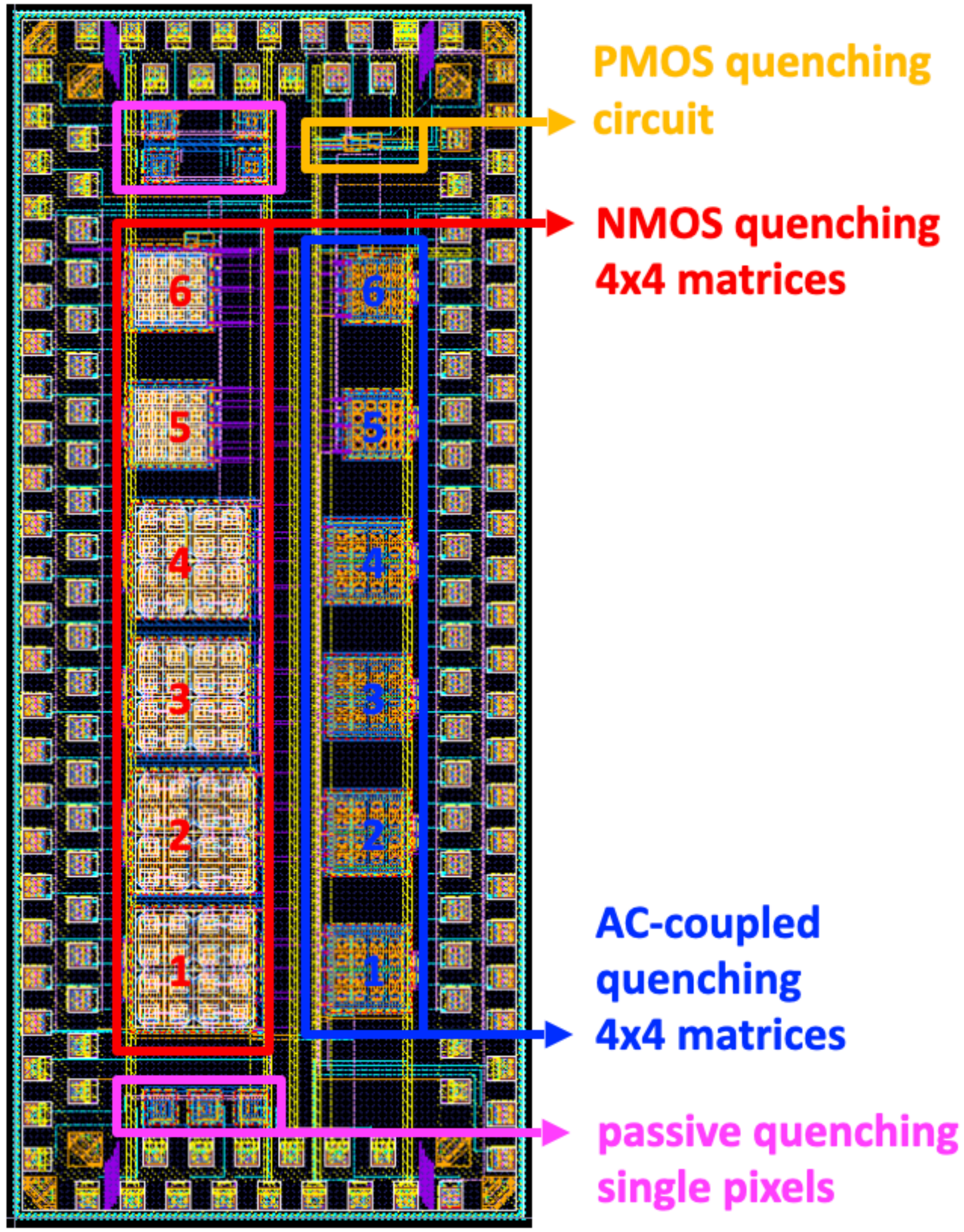


CASSIA2 design 5x5 pixel analog dedicated to LGAD

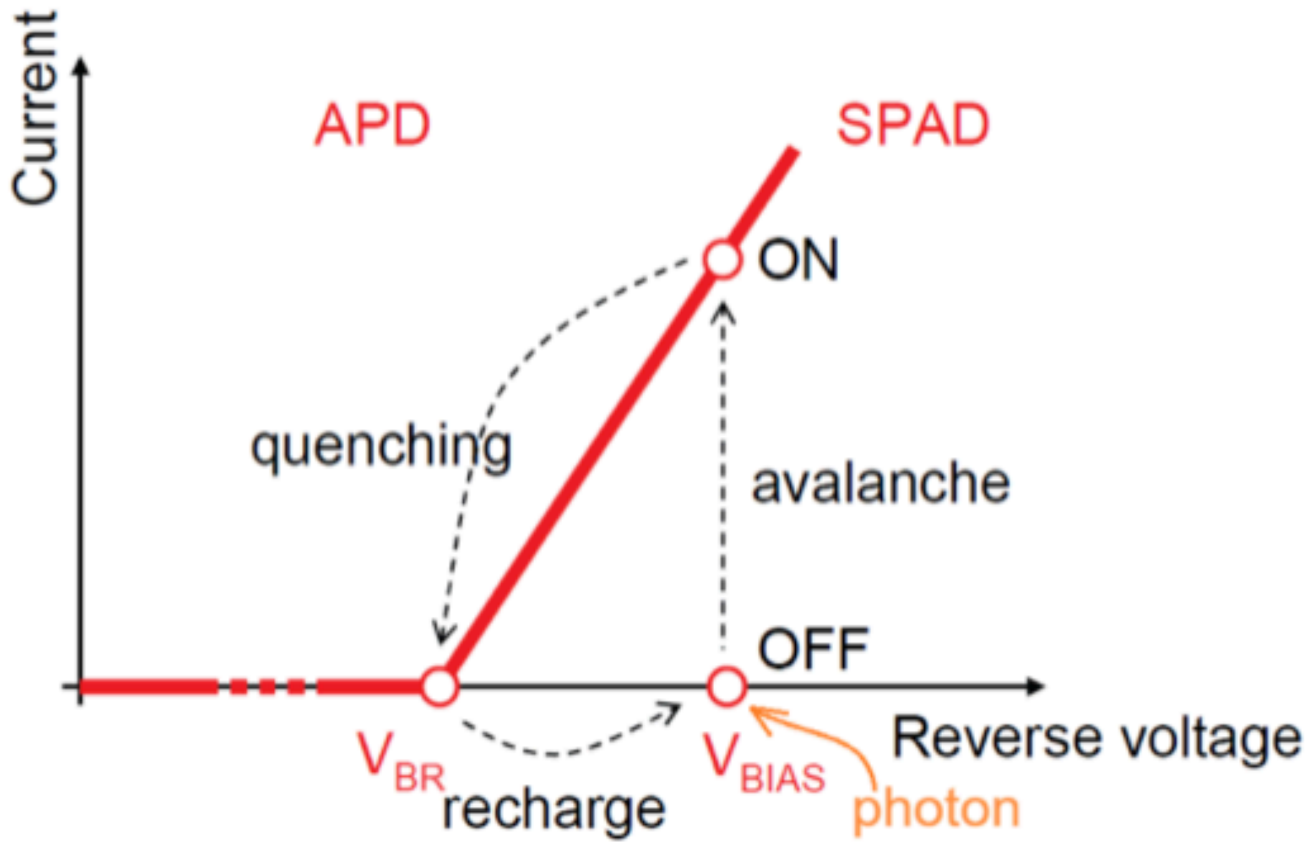
- **5x5 pixel matrix with amplifier for Low Gain mode study**
  - study transition from region without gain to region with gain
  - required sensitivity down to gain=1
  - implement adapted version of MALTA amplifier
  - matrices with analog and digital readout
- **Biasing, AC coupling**
  - PMOS vs diode biasing of NW electrode
  - Integrate pixel AC coupling



CASSIA2 design 4x4 pixel digital dedicated to SPAD



- in SPAD mode, quenching circuit required to stop the avalanche after detection and restore bias voltage to its initial value above breakdown



- 6 4x4 matrices with NMOS-input quenching (i.e. connecting to SPAD anode) and digital readout
- 6 4x4 matrices with AC-coupled quenching (connecting to SPAD cathode, i.e. collection electrode) and digital readout
- 1 PMOS-input quenching circuit (can be bonded to collection electrode of single pixels on other chips)
- several single pixels with passive quenching resistor and other test structures

Summary & Outlook

- With the CASSIA project we propose to develop CMOS sensors with internal amplification to address research topics in DRD3 WG1 Monolithic sensors
  - Develop LGAD and/or SPAD structures in CMOS pixel sensors for high time resolution, higher SNR, possible simplification of circuits & low power circuits
  - Engineer pixel designs in TJ180nm now and enable transfer to 65nm in the future
- The CASSIA project is included in the DRD3 working group on monolithic sensors to address the research program through the design and test of dedicated prototype sensors
- Results of CASSIA 1 have shown that we can operate the CMOS sensor in LGAD and SPAD mode
  - The sensor operates very stable with smooth transition between LGAD and SPAD mode
  - Dark count rate is exceptionally low in voltage range of interest <0.01 Hz/um^2 at RT and operational dark currents are low (1pA/pixel)
  - A first study with different electrode/gain layer implantation designs has been carried out and is basis for next developments
- Design of CASSIA2 is complete with in-pixel electronics towards designs for
  - optimal GL design and implantation for full pixel efficiency for charged particles
  - dedicated in-pixel electronics for LGAD (amplifiers) and SPAD (quenching circuits) operation

Thank you for your attention