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SERIAL POWERING AND ITS IMPLEMENTATION IN THE ATLAS ITK DETECTOR

FLORIAN HINTERKEUSER FOR THE ATLAS COLLABORATION

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OUTLINE

- Introduction to the ITk Pixel Detector
- Implementation of serial powering (SP) in ITk Pixels
  - ITk pixel modules
  - HV distribution in the ATLAS ITk Pixel Detector
  - Data transmission and monitoring
  - Grounding & shielding

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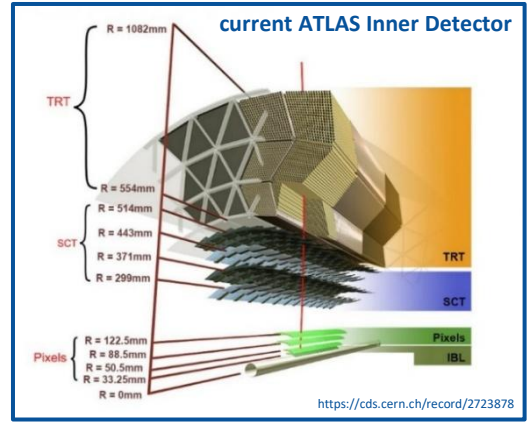
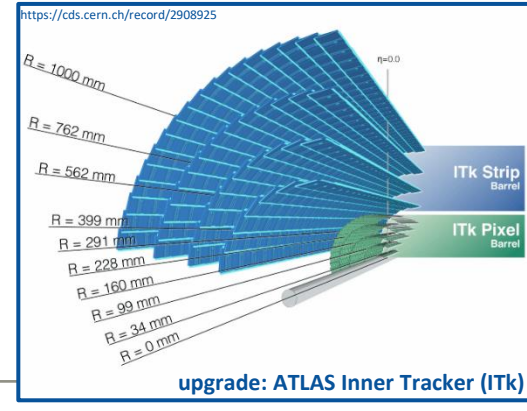
INTRODUCTION TO ITK PIXEL

- ATLAS Inner Detector to be replaced by an **all-silicon tracker (ITk)** for HL-LHC

- **Outermost 4 layers**: silicon strip sensors

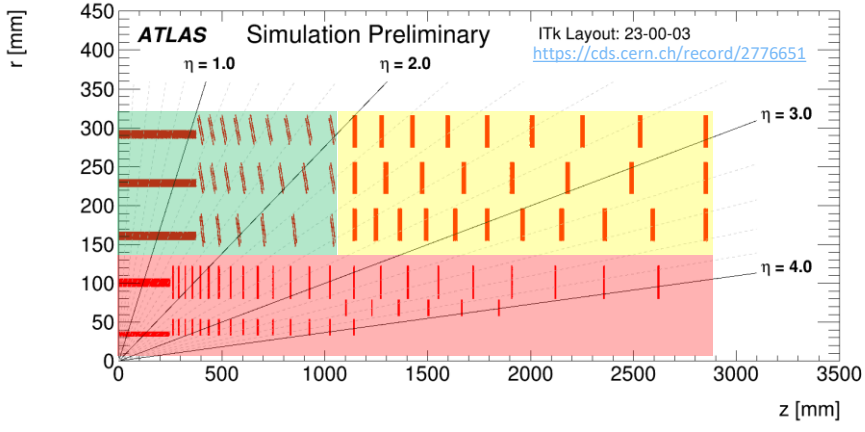
- **Inner 5 layers: Hybrid** pixel modules in
  - **Layer 0**: 3D pixel sensors
  - **Layer 1**: 100µm & 150µm planar pixel sensors
  - **Layer 1-4**: 150µm planer pixel sensors

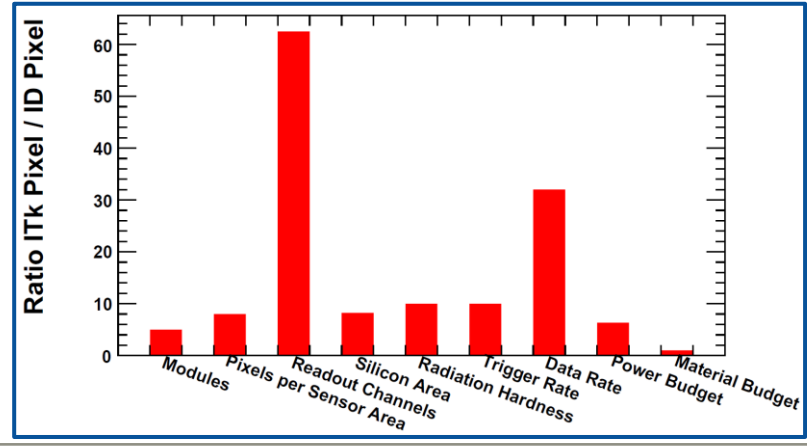




INTRODUCTION TO ITK PIXEL

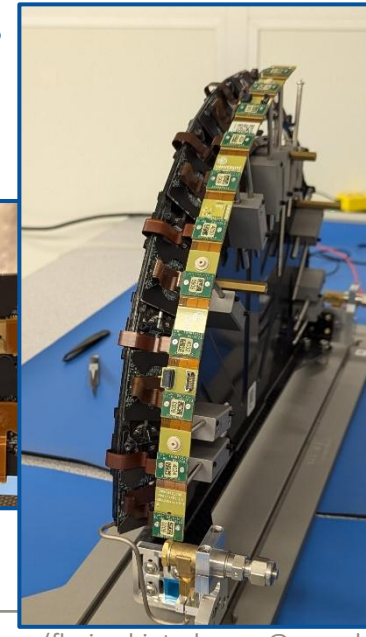
- Approx. **8500 modules** with **~33000 readout ASICs**, each with a 384x400 matrix of **50x50µm²** pixels ➔ **~13 m² of active silicon**
- Roughly **6-10 µW** total power dissipation per pixel
  - > **Total power** budget of **120 kW**, including ASICs, sensors, services

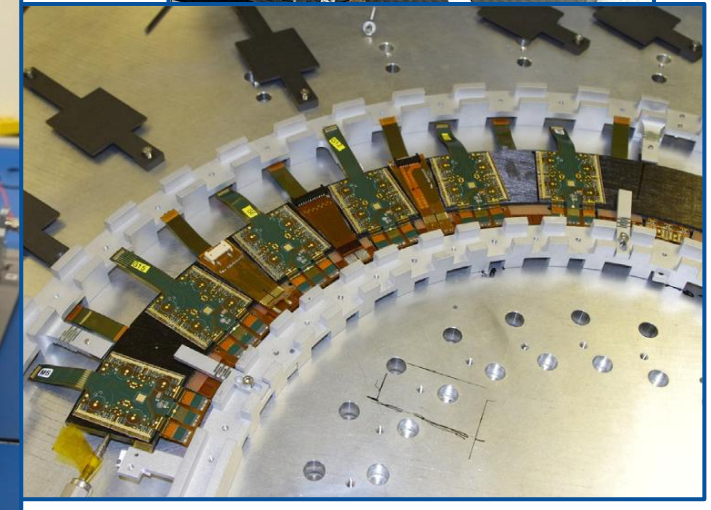




INTRODUCTION TO ITK PIXEL

- Layout determines key design parameters:
  - **2 flavours** of modules: **quads** (2x2 ASICs) and **triplets** (3x1 ASICs)
  - **13 different flavours** of local supports
    - “Smallest” flavour: 8 triplets
    - “Largest” flavour: 36 quads



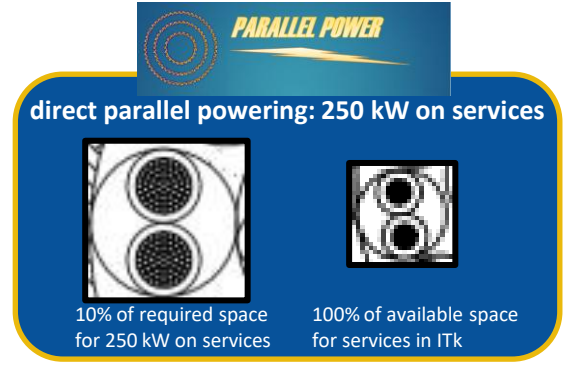


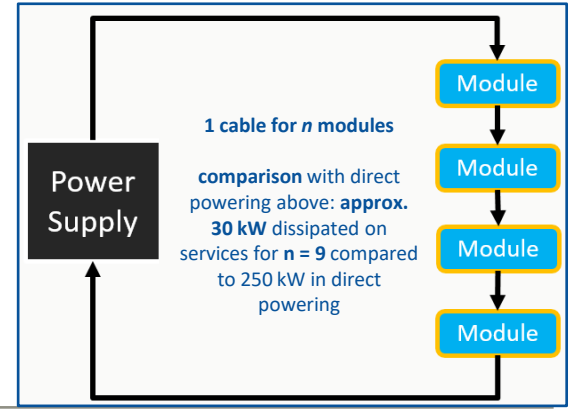
POWERING THE ITK PIXEL DETECTOR

- Upgraded pixel detector for ATLAS (and CMS)
  - **Significantly more modules** than their predecessors
  - **Significantly more pixels** per area than their predecessors
  - **Similar services volume** as their predecessors

- **Currently used parallel powering scheme is not feasible**
  - Assuming 1.25A per readout ASIC and AWG14 cables to supply power: 250 kW on services vs. 70 kW delivered power **(~20% efficiency)**
  - **Incompatible** with **spatial constraints and cooling budget**

- **Use serial powering instead**





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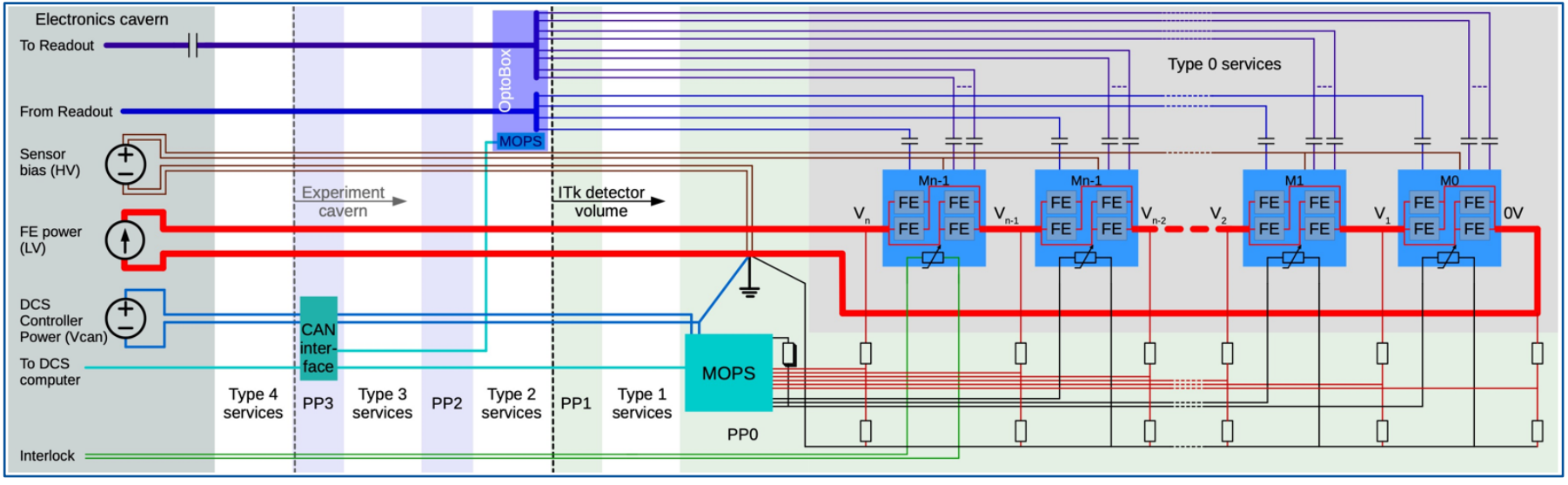
Flavour	Power Unit Type	Length	Number in ITk Pixel Detector
L0 Barrel	Linear Triplet	4	24
L0 Coupled Ring	Triplet	3	60
L0 Intermediate Ring	Triplet	5	24
L1 Barrel	Thin Quad	6	40
L1 Coupled Ring	Thin Quad	10	60
L1 Quad Ring	Thin Quad	10	32
L2 Barrel	Thick Quad	6 12	32 32
L2 Incl. Half-Ring	Thick Quad	8	48
L3 Barrel	Thick Quad	6 12	44 44
L3 Incl. Half-Ring	Thick Quad	11	64
L4 Barrel	Thick Quad	6 12	56 56
L4 Incl. Half-Ring	Thick Quad	14	72
L2 Half-Ring	Thick Quad	8	88
L3 Half-Ring	Thick Quad	11	64
L4 Half-Ring	Thick Quad	13	72
ITk Pixel Detector	-	⌀ 9.2	912

Table 3.7: Inventory of Serial Powering Chains in the ITk Pixel Detector

POWERING THE ITK PIXEL DETECTOR

Example schematic of a typical serial powering chain in ITk Pixel



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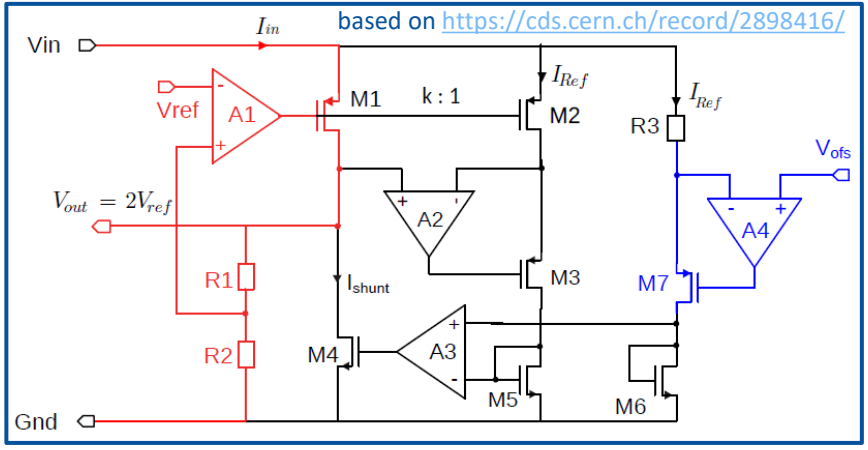
SERIAL POWERING IN ATLAS ITK

SHUNT-LDO AND ITK PIXEL MODULES

SERIAL POWERING ON THE MODULE LEVEL

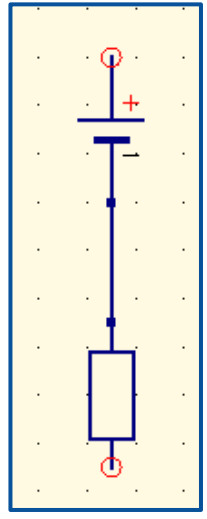


as long as the

≈

SLDO is operational

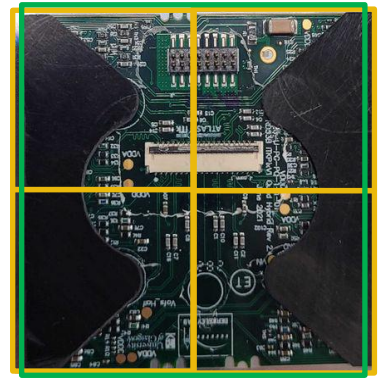
$$\begin{aligned} V_{\text{in}} &= V_{\text{ofs}} + R_{\text{eff}} \cdot I_{\text{in}} \\ &= R_{\text{ofs}} \cdot I_{\text{ofs}} + \frac{R_3}{k+2} \cdot I_{\text{in}} \end{aligned}$$



- **SLDO** regulator converts constant input current into a constant supply voltage for the ASIC
  - Surplus current $\boldsymbol{I_{shunt} \geq 0\ A}$ is drained through M_4
  - Dropout voltage $\boldsymbol{V_{DO}}$ across M_1 → **higher V_{in}** than VDDD/VDDA, **O(0.2 V)**

SERIAL POWERING ON THE MODULE LEVEL

- ITk Pixel modules: **3 / 4 ASICs** on one module
- **DC coupled sensors**
  - → ASICs on module share a common "***Local Module Ground***"
- **2 independent SLDO** regulators integrated **per ASIC**
  - → **6 / 8 parallel SLDOs** on module
  - → **Redundancy** protects SP chain!
- **Common supply line** for module!
  - → Total input current?
    - → **Deal with spikes** in current drain
    - → Counter **current distribution** imbalances



Sensor
Readout ASIC

SERIAL POWERING ON THE MODULE LEVEL

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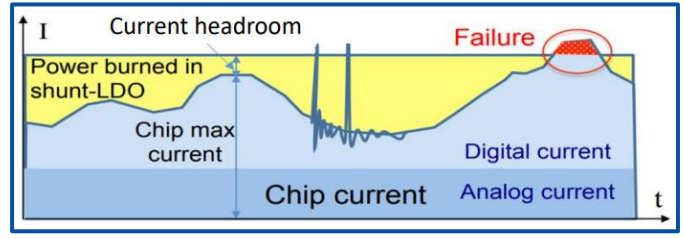
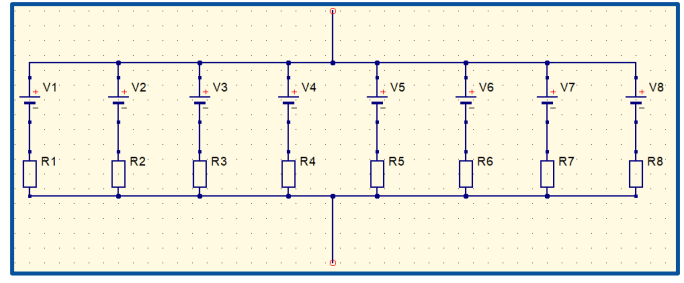
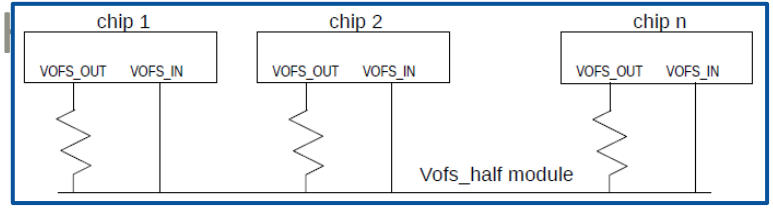
    - → **Deal with spikes** in current drain
    - → Counter **current distribution** imbalances
    - → **Headroom** significantly decreases power efficiency

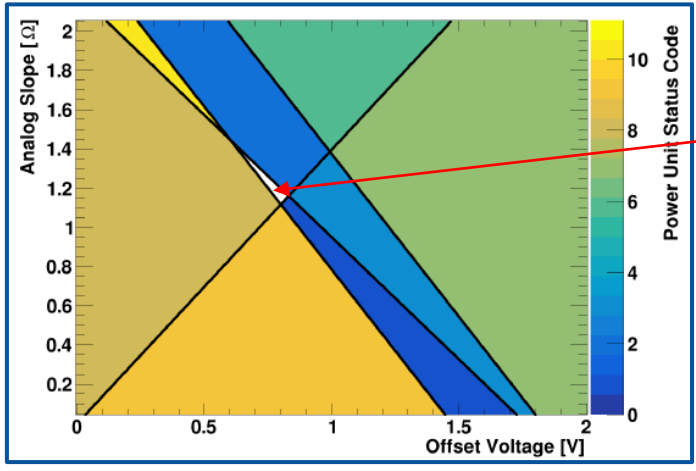




SERIAL POWERING ON TH



- **Offset sharing**
  - Offset voltage generated by draining a small current through large resistor
  - Can share a common offset voltage between ASICs connected in parallel

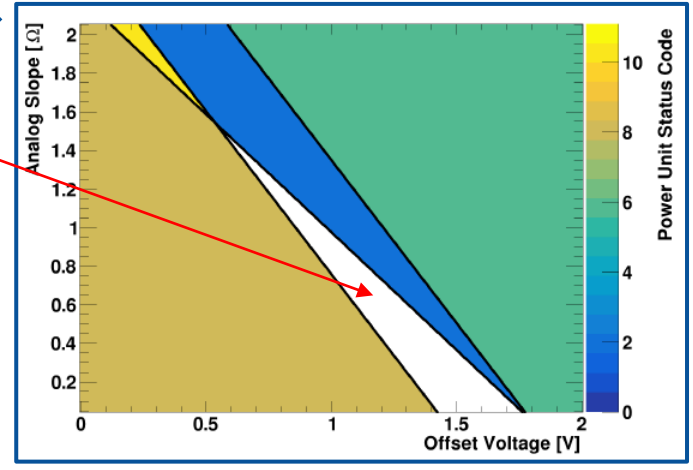


no common offset, 2% variation in V_{ofs}

Offset sharing

Zero Status code:
stable detector operation

Non-Zero Status code:
No stable detector operation



common offset voltage

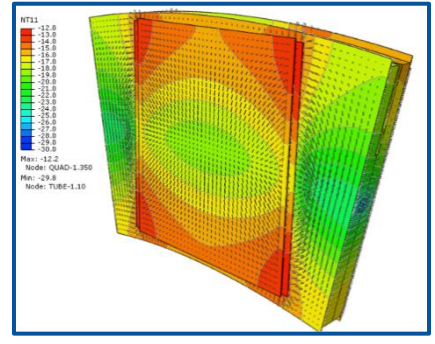
SERIAL POWERING ON THE MODULE LEVEL

- **Local power dissipation**: serial powering not power efficient!
  - **Up to 40%** of the ASIC power **dissipated in periphery** (10% of ASIC area), **depending on configuration state!**
  - **Temperature gradient on module → local current density** varies on sensor, variation in per-pixel leakage current!

$$\begin{aligned} \varepsilon &= \frac{P_{\text{load}}}{P_{\text{total}}} \\ &= \frac{V_{\text{core}} \cdot I_{\text{Load}}}{1.25V_{\text{core}} \cdot 1.2I_{\text{Load}}} \\ &= 67\%. \end{aligned}$$

Table 21: Estimated Power Distribution on the readout chip for the 2021 Power Model with a current overhead of 17%.

		Normal Operation [W/cm2]		No Configuration [W/cm2]		One FE Chip Open [W/cm2]		One FE Chip Open AND no Config [W/cm2]	
Layer	Section	Periphery	Pixel-Matrix	Periphery	Pixel-Matrix	Periphery	Pixel-Matrix	Periphery	Pixel-Matrix
L0	All	0.379	4.161	0.0	8.214	0.379	10.169	0.0	14.222
L1	All	0.335	3.712	0.0	7.294	0.336	7.339	0.0	10.921
L2-L4	All	0.289	3.411	0.0	6.502	0.289	6.648	0.0	9.739



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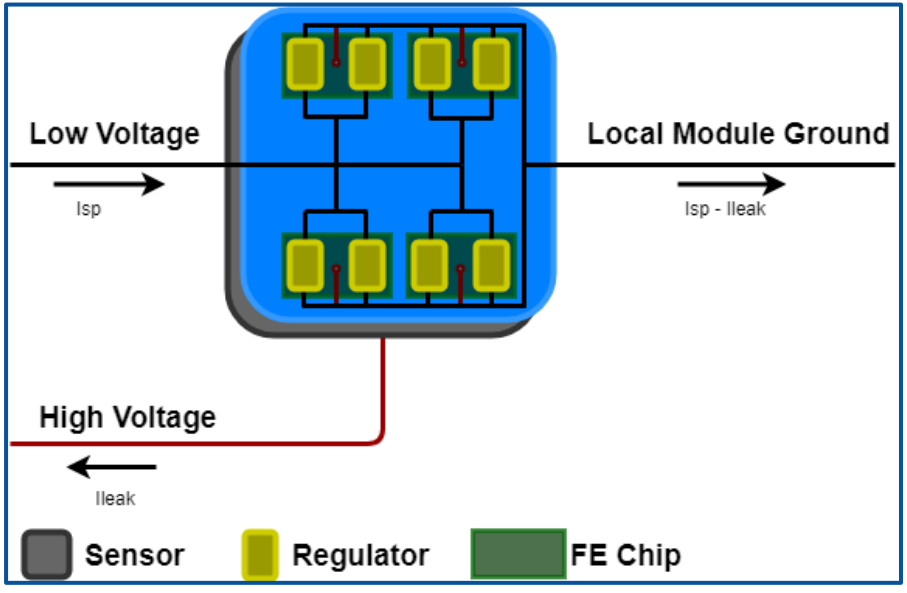
SERIAL POWERING IN ATLAS ITK

HV DISTRIBUTION

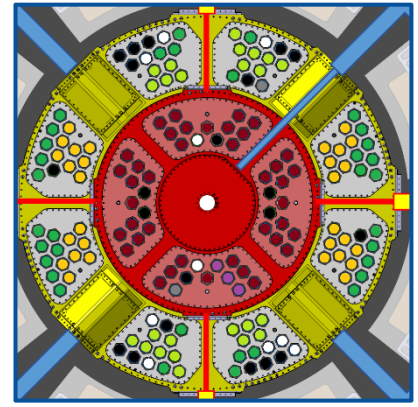
HV DISTRIBUTION

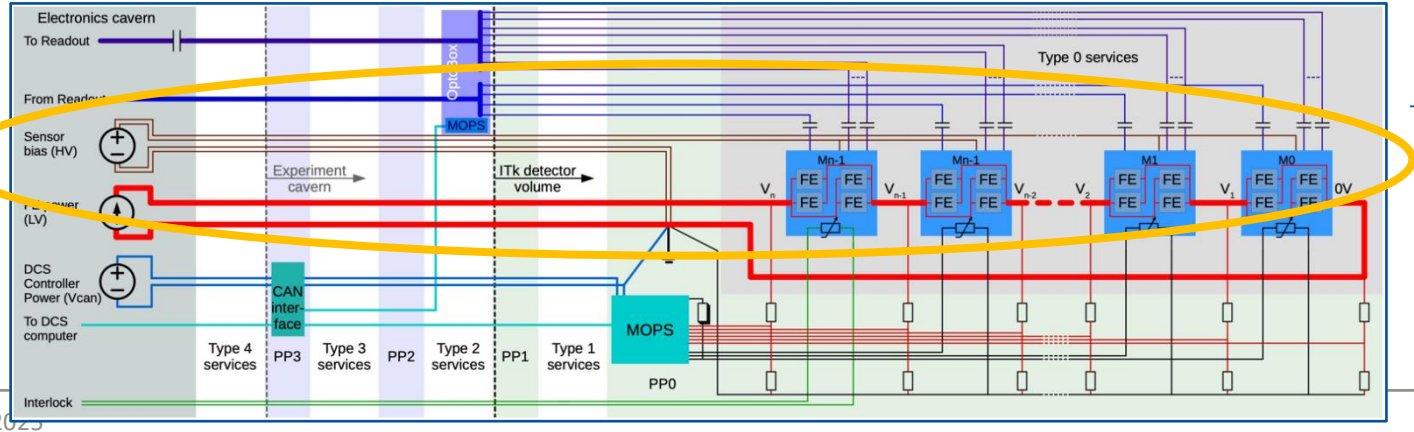


- Sensors are **DC-coupled**
- Majority: planar **n-in-p** sensors
- **Negative depletion voltage** applied to non-structured side of the sensors
- **Return** through readout chip
- Reference potential for HV: **“local module ground”**

HV DISTRIBUTION

- ITk Pixel has **~8500** independent (sets of) sensors = quads or triplets
- Deploying individual HV lines: **~17000** pins required at **Patch Panel 1** (no safety loops considered)
- **Total number** of pins available at PP1: **9048**
- **Need to economize HV lines** → parallel distribution to multiple modules in SP chain
  - **Quad** depletion voltage at start-up: **~50 V**
  - **Quad** depletion voltage at end-of-life: **~600 V**

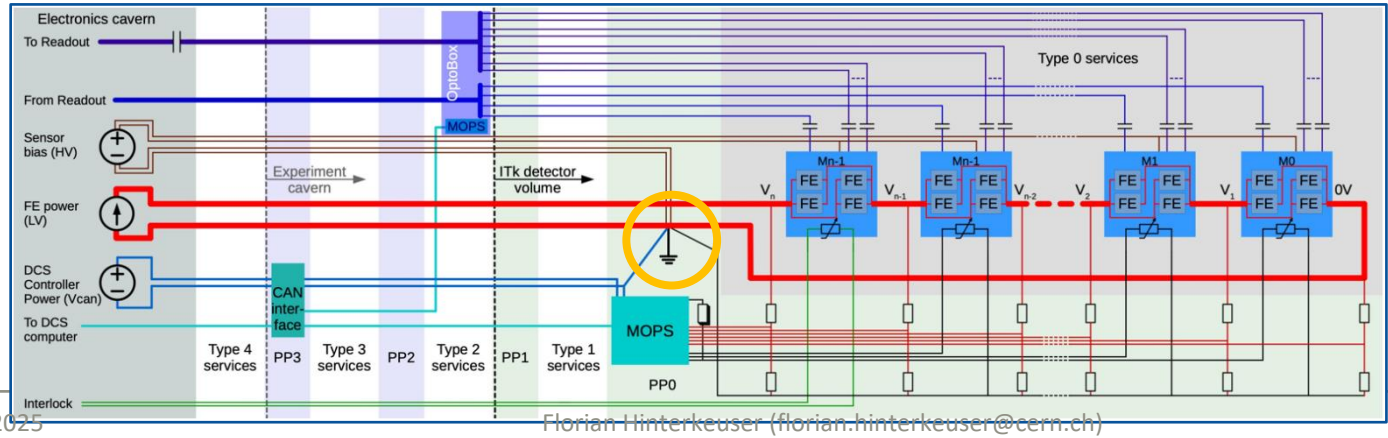




- **All quad SP chains** have **2 HV** lines, **independent** on the **number of modules** in that chain

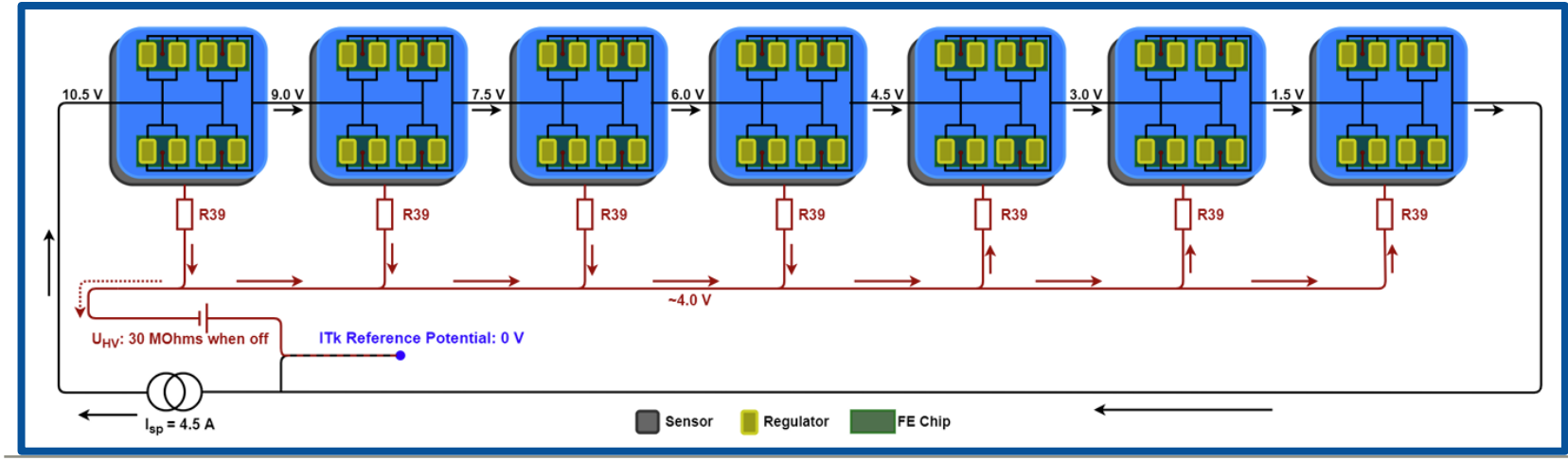
HV DISTRIBUTION

- **Single point of reference** for the serial powering chain: the "**0V-plane**" on the **Patch Panel 0** (on the local support)
- **ATLAS G&S rules**: the return line of every power supply unit **must be referenced to this "0V-plane"**
  - The "0V-plane" is **connected to the ITk reference** potential



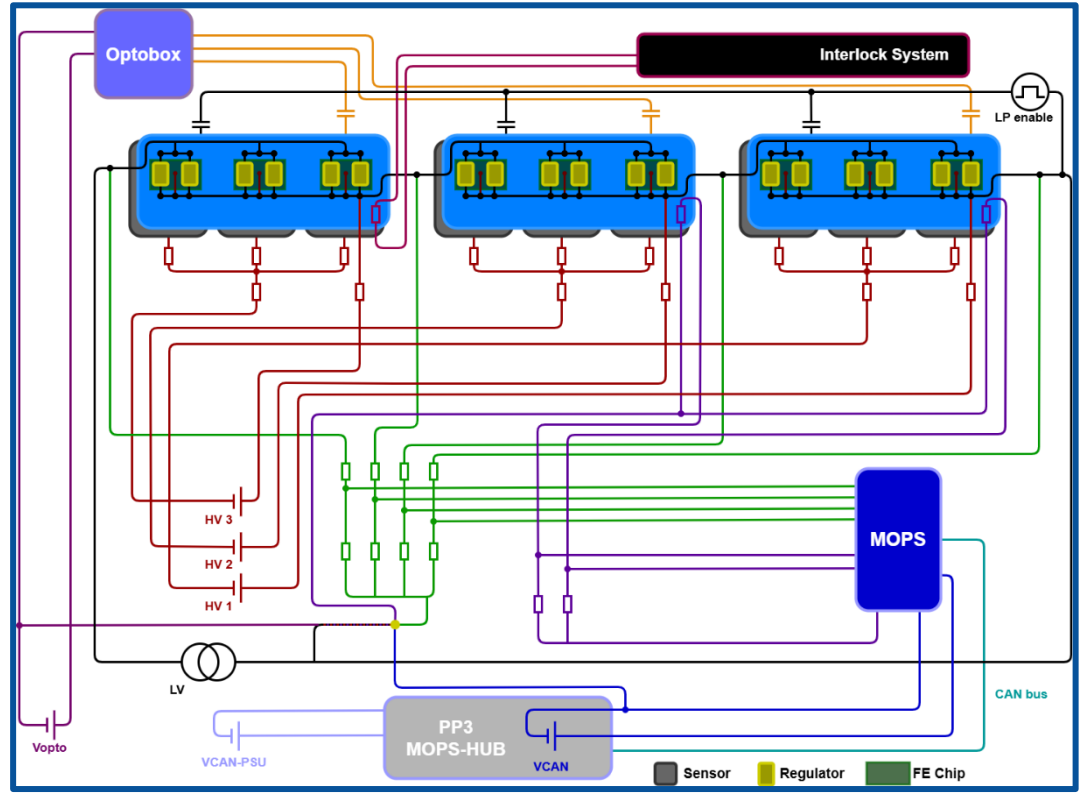
HV DISTRIBUTION

- **Now off-state-behaviour** of the PSU becomes relevant
- Standard issue HV PSU modules used in ID pixels have a **high-impedance/high-resistance off mode**
  - Some sensors at least partially depleted with **LV = on, HV = off** (regular operating condition)
  - Effective forward bias on some sensors with **LV = on, HV = off** (regular operating condition)
- **Further investigations** indicate no serious issue in ATLAS (ATL-ITK-PUB-2022-002)



HV DISTRIBUTION

- **Concern for 3D sensors**: rather low depletion voltage
  - **LV staircase** induced bias voltage might fully deplete sensor before irradiation
  - **ITk Pixels solution**: violation of G&S rules → individual HV lines with dedicated return line and “indirect” referencing



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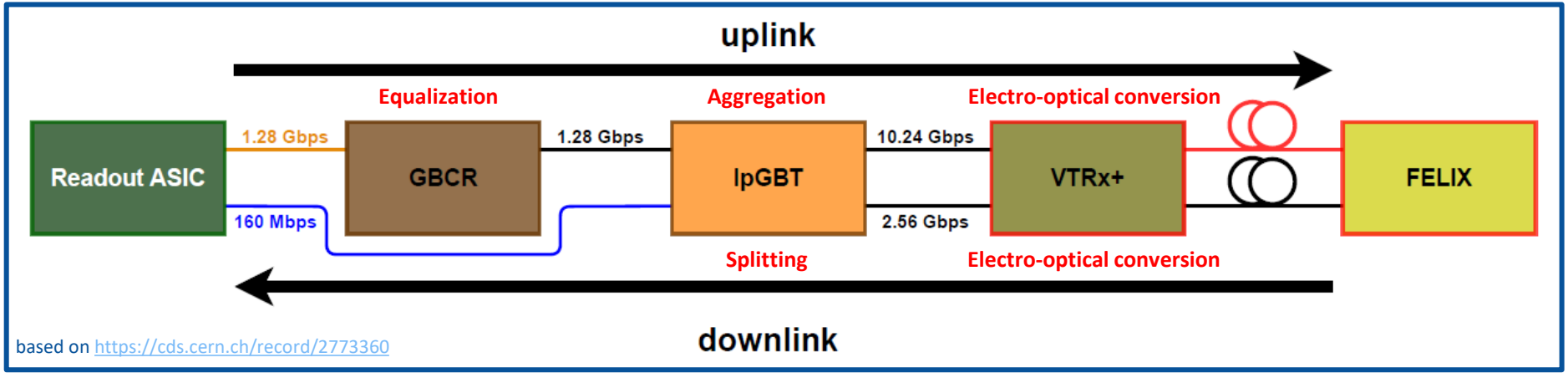
SERIAL POWERING IN ITK PIXEL

DATA-TRANSMISSION AND MONITORING

DATA TRANSMISSION SCHEME

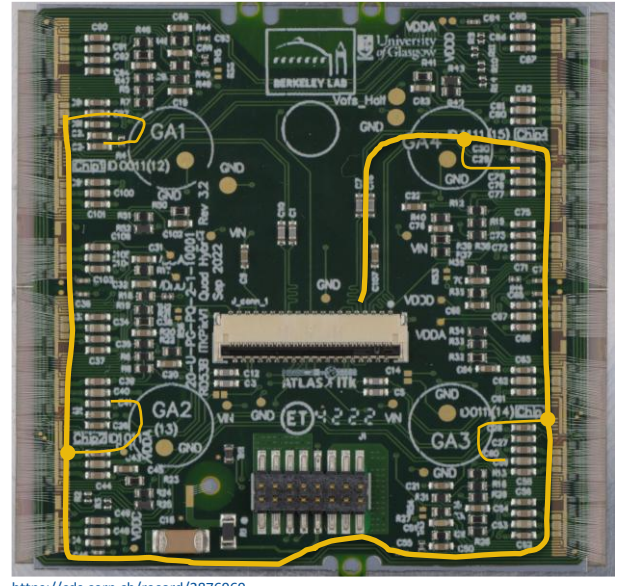


- **Opto-electrical transceivers** outside of the detector package
- **Up to ~6 m electrical transmission**: downlink **160 Mbps**, uplink **1.28 Gbps**
- Pre-emphasis and equalization on uplink
- Aggregation of uplinks in lpGBT, optical transmission to counting rooms

DATA TRANSMISSION SCHEME

- **Downlinks**:
  - **1 downlink per module**, 160 Mbps command stream → CDR on ASIC
  - **Multi-drop**, **AC-coupled** for each readout ASIC **on module flex** (100nF)
  - Distance between first and last drop: ~10 cm

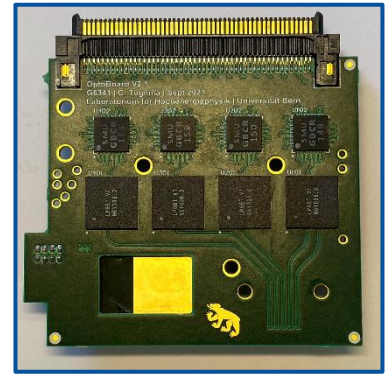
- **Addressing & downlink forwarding**:
  - Each ASIC has **4 address bits**
  - 1 downlink suitable for multiple modules
  - **Considered command forwarding** to reduce material budget
  - Eventually decided against that
    - Risk considerations (availability of detector)



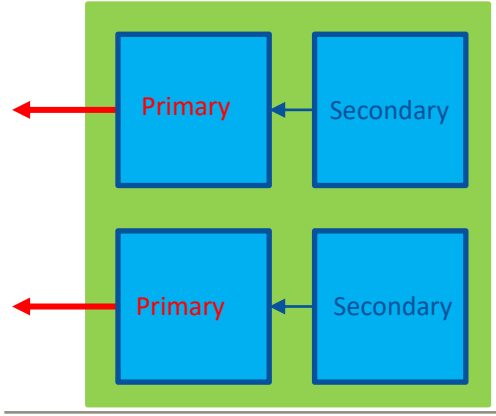
https://cds.cern.ch/record/2876969

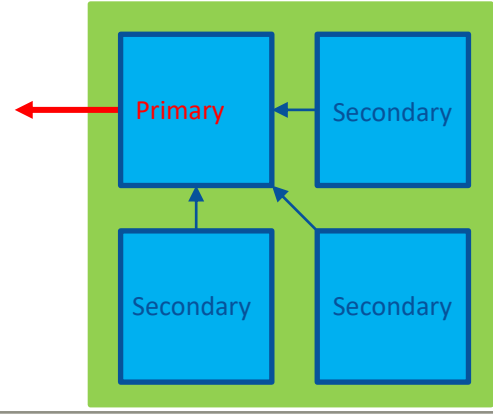
DATA TRANSMISSION SCHEME

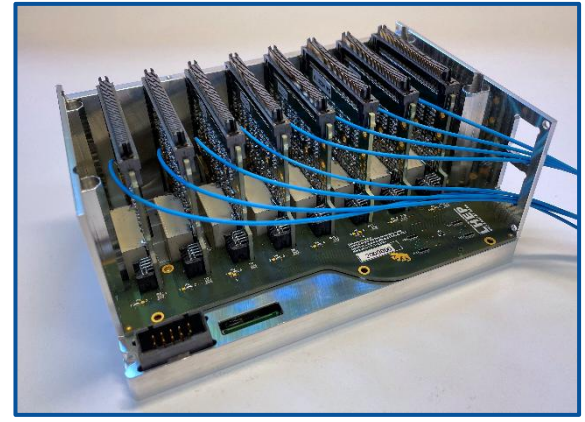
- **Uplinks**
  - Each ASIC capable of transmitting **4x1.28 Gpbs**
  - **AC-coupling** for each ASIC on module flex (8.2 nF)
  - Outermost layers produce significantly less data
    - Reduce material budget through **data merging**



- **Optoboards**
  - 4 GBCR+lpGBT
  - 1 VTRx+
- **Optoboxes**:
  - up to 5 Bpol12
  - up to 8 optoboards







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  - Outermost layers produce significantly less data
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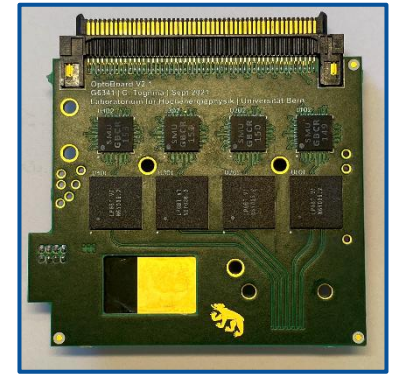
- **Possible complication when LV is on and optoboards not powered**
  - **Floating lpGBT** ports **pulled up** to up to ~20 V through AC-coupling capacitor leakage
  - **As precaution: interlock** of serial power PSU and optobox PSU linked



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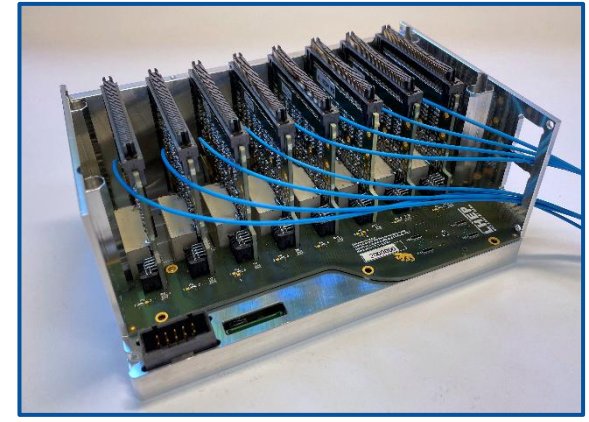
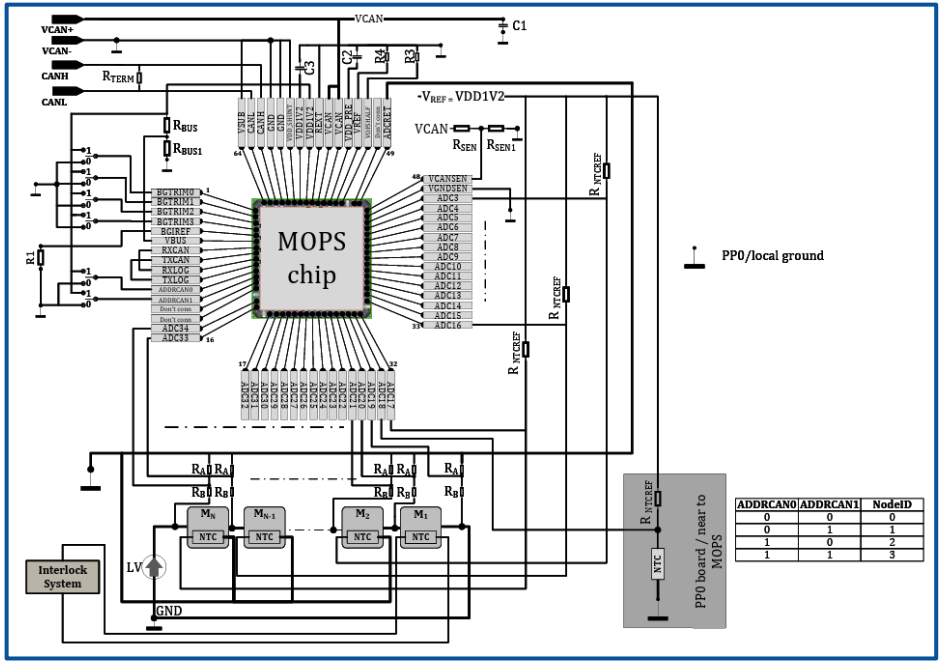


MONITORING

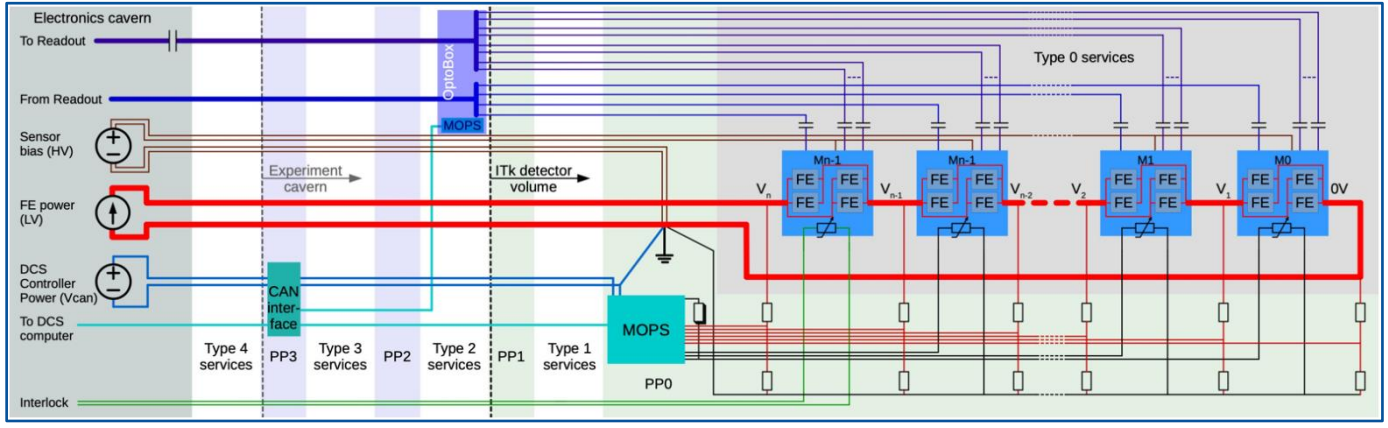
– **Limited monitoring** of the detector through dedicated ASIC – Monitoring of Pixel System (MOPS)



– **Located on PP0** (on the local support)
– Monitoring of
  – **One temperature sensor on each module**
  – **Voltage drop across each module**
– **Electrical communication** to MOPS-HUB through custom 1.2V CAN bus
– **Optical transmission** to the DCS in counting rooms
– Mostly: **one single MOPS per SP chain**
– Additional temperature sensors on the module that are read out through the front-end ASIC, data transmitted through the data uplinks

MONITORING

- **A single NTC per SP chain** is not connected to the MOPS
  - This goes directly to the **interlock system**
  - Always the **last NTC in direction of flow of CO2** → dryout detected earliest at that module
  - Again due to limitation of pins and available space in service gaps



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SERIAL POWERING IN ITK PIXEL

GROUNDING & SHIELDING

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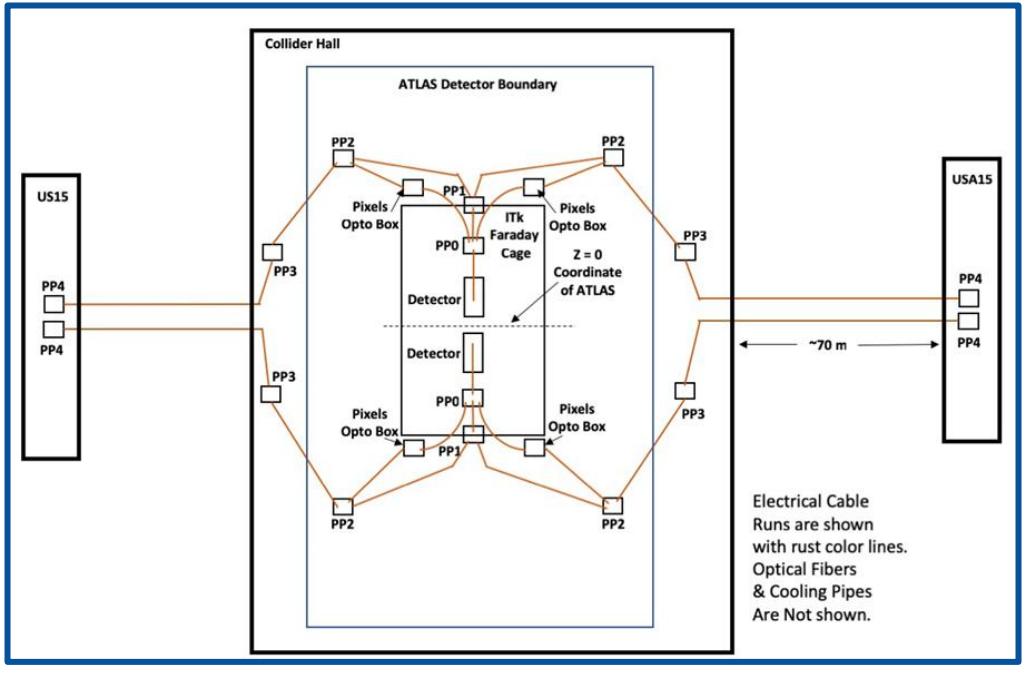
GROUNDING & SHIELDING

- **ATLAS G&S rules apply in general** and were originally conceived without considering SP
- **Design of SP chains** originally based on “local” requirements without considering the ATLAS G&S rules

- **Both had to be adapted** in order to make them compatible!

GROUNDING & SHIELDING

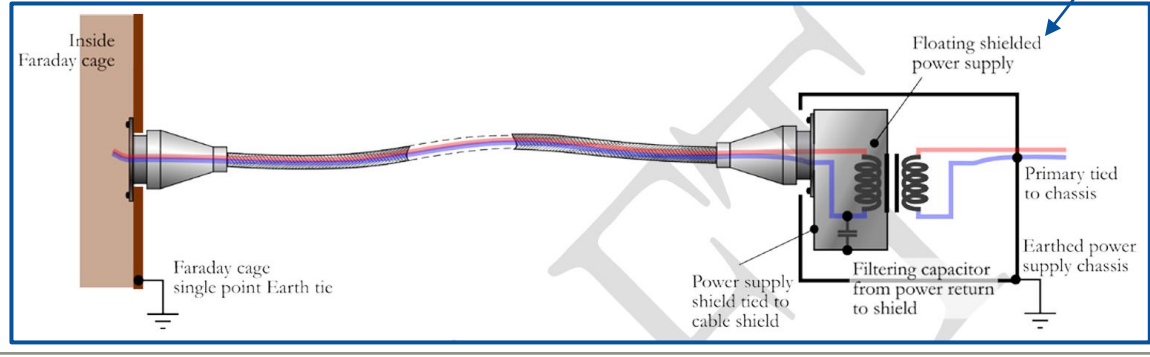


- **STRICT** separation of all components
- **Electrical components** “belong” to one of four sectors:
  - A side powered from USA15
  - A side powered from US15
  - C side powered from USA15
  - C side powered from US15
- **All electrical connections** from a given PP0/EoS run through the same PP1 and are routed to the same service cavern

GROUNDING & SHIELDING

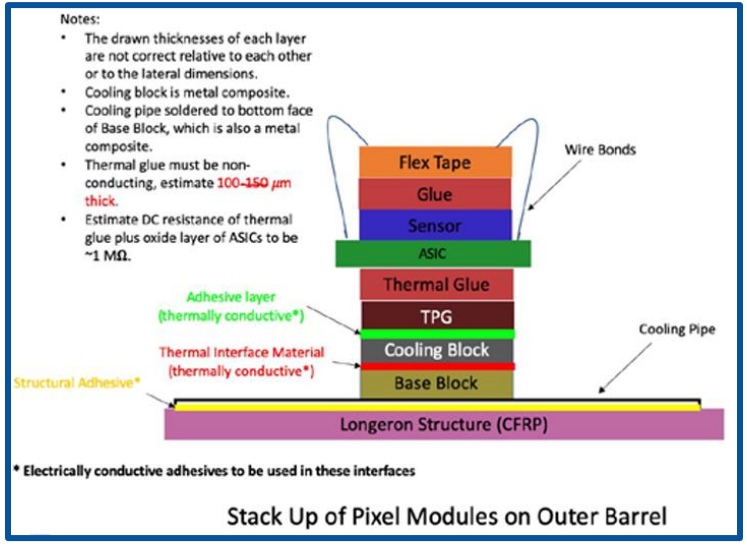
- **ITk reference** potential supplied through the Faraday Cage
  - **Single tie** between the Faraday Cage and the ATLAS ground
  - **Single tie** between the ITk reference potential and the “0V”-plane on each PP0
- **All PSU are floating** and are **locally referenced** to the ITk “0V”-plane/ITk reference potential
- **All SP chains** are **strictly isolated** from each other
- **All cable shields** are tied to the ITk reference voltage at PP1/optobox
- **All cable shields** are left floating at the “far end”

this does not normally exist in commercial PSU



GROUNDING & SHIELDING

- **All conductive structures** must be connected to the ITk reference potential
- By now, the electrical components (SP chain) is **electrically isolated** from the carbon **support structures**



- This was different in the past:
  - Half-rings in endcaps were referenced through a direct connection to “0V”-plane on PP0
  - They were electrically isolated from the global mechanics support structures
    - E-breaks in the cooling pipes!
- In any case: careful not to short circuit the SP chain through the local support!

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GROUNDING & SHIELDING

- **Exceptions from the G&S rules**
  - **HV distribution in L0** → already discussed
  - **Merging of "0V" planes** of several SP chains on PP0 → economization of MOPS
    - very little space close to beam pipe
    - very short SP chains in that area (in particular in barrel region)
    - 1 MOPS sufficient to monitor up to 3 SP chains → direct electrical connection between chains

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SUMMARY

- Hopefully could give a (rushed) overview of **many years of R&D** for ATLAS ITk Pixel
  - That was based on few, partially non-representative setups
- SP is **simple on paper** only, but convoluted system design
  - One needs to **re-think** the **complete system** from the ground up to get SP to work

- We still don’t perfectly understand every detail of SP
  - **System test** with **representative hardware in representative conditions** is crucial
  - **This requires available detector parts OR prototypes**

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MAYBE USEFUL READING

- Some of the links are ATLAS internal
  - ITk public results: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ITkPublicResults
    - PubNote on Layout of the ITk
    - PubNote on HV distribution
  - ITk Pixel Services Specifications (internal)
  - ITk Grounding & Shielding (internal)
  - ITk Pixel Optosystem
  - ITk Pixel Readout ASIC
  - ITk Pixel System Test Overview
  - RD53 Pixel readout ASIC in JINST
  - My PhD thesis

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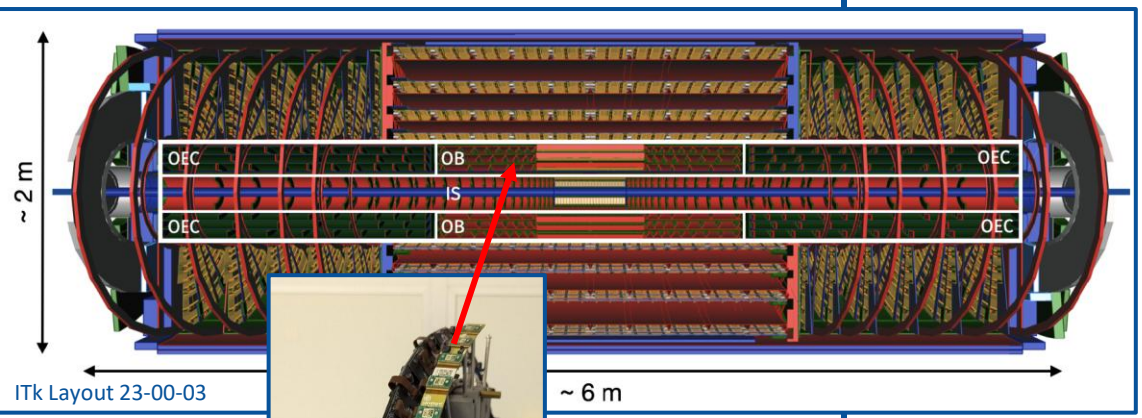
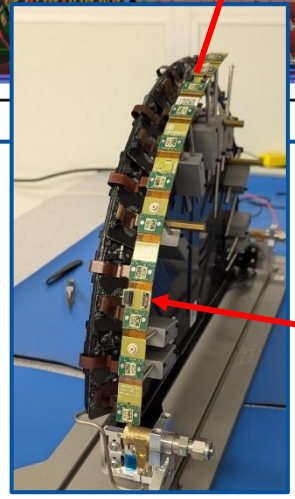
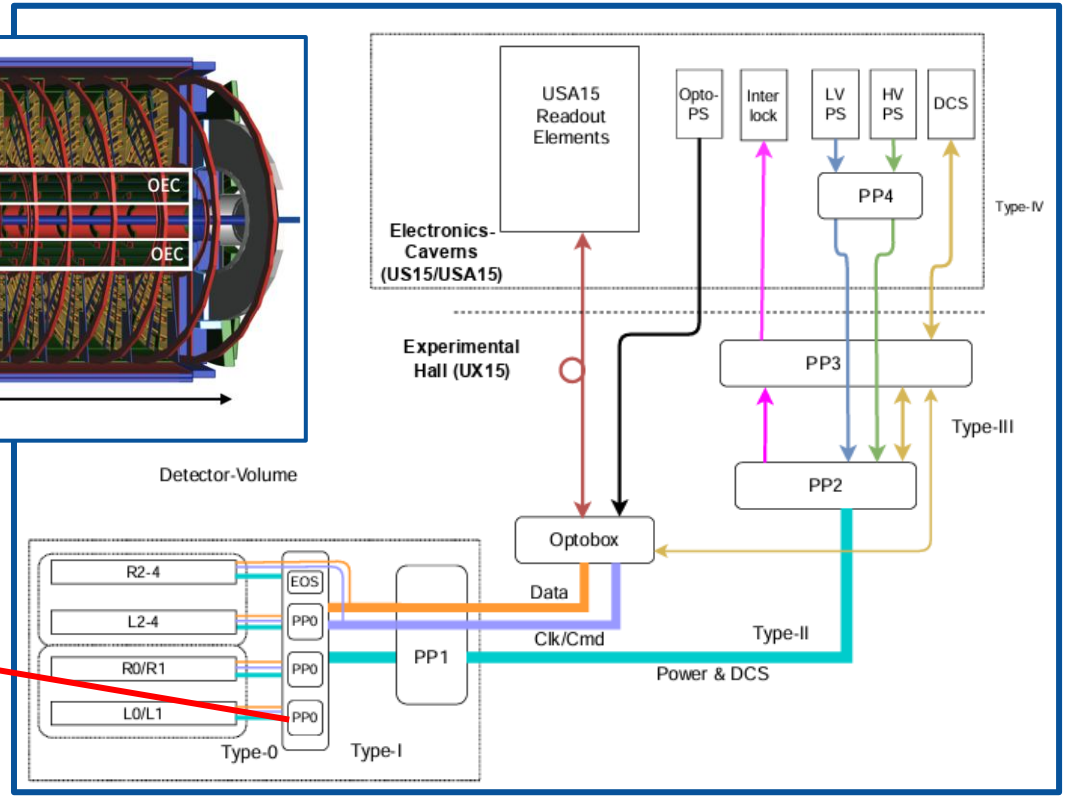
THANK YOU

INTRODUCTION TO ITK PIXEL

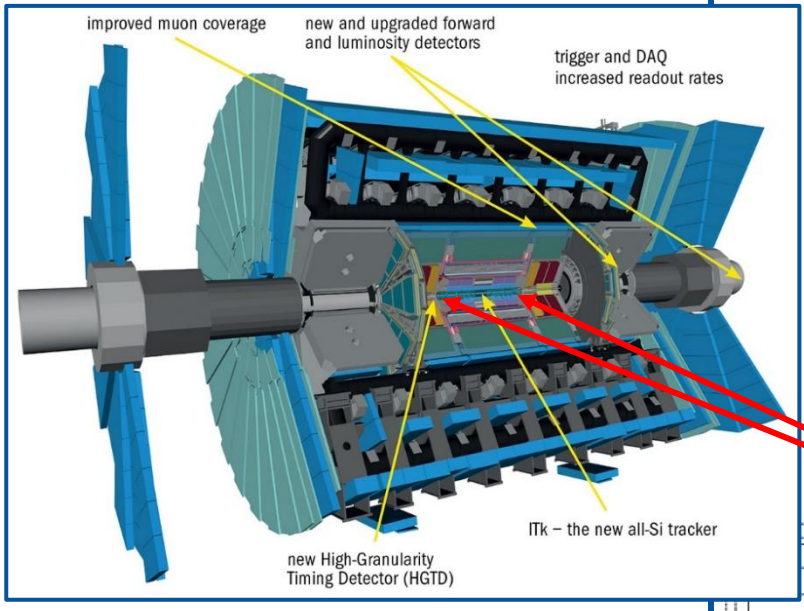


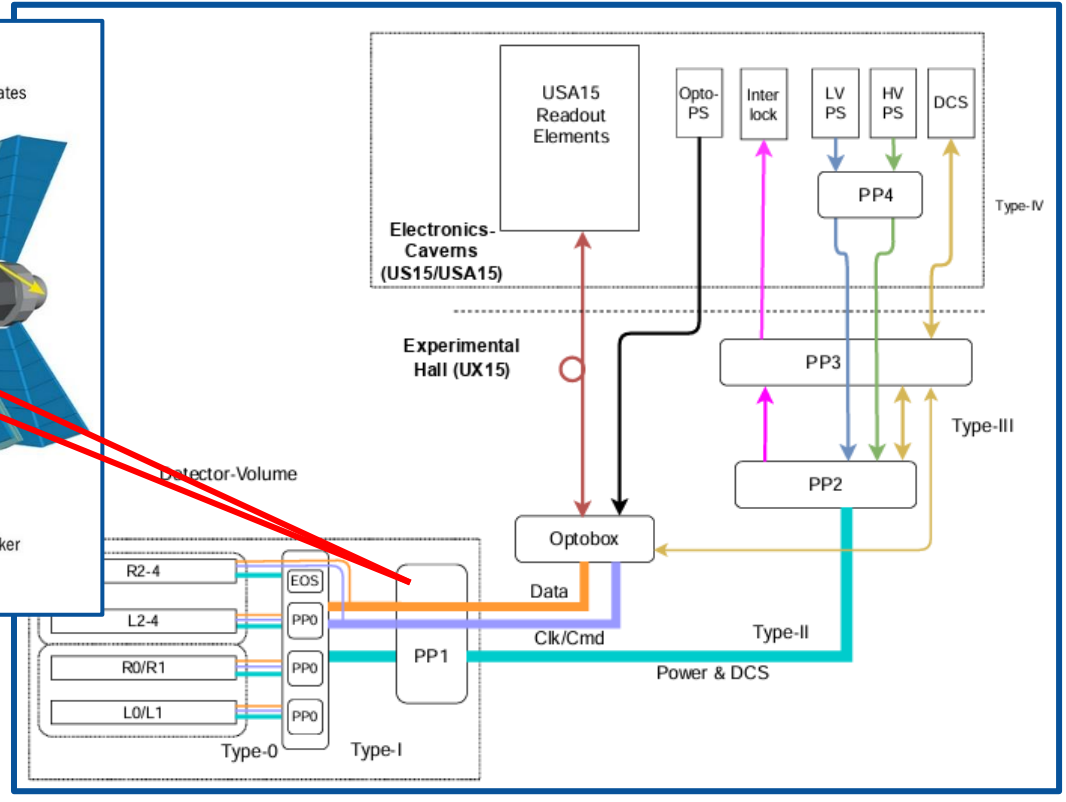
ITk Layout 23-00-03



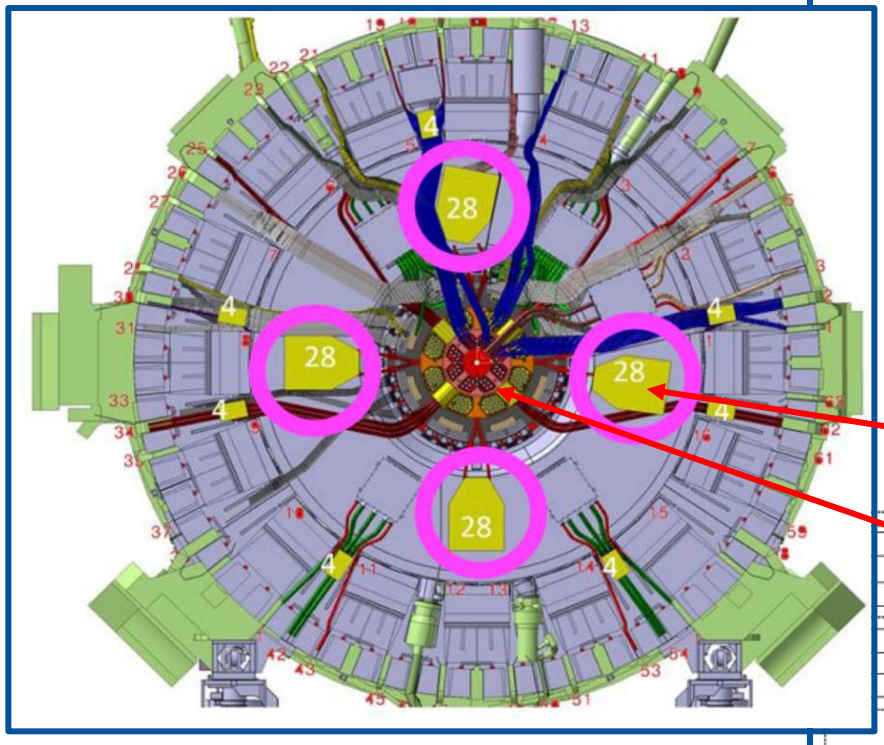


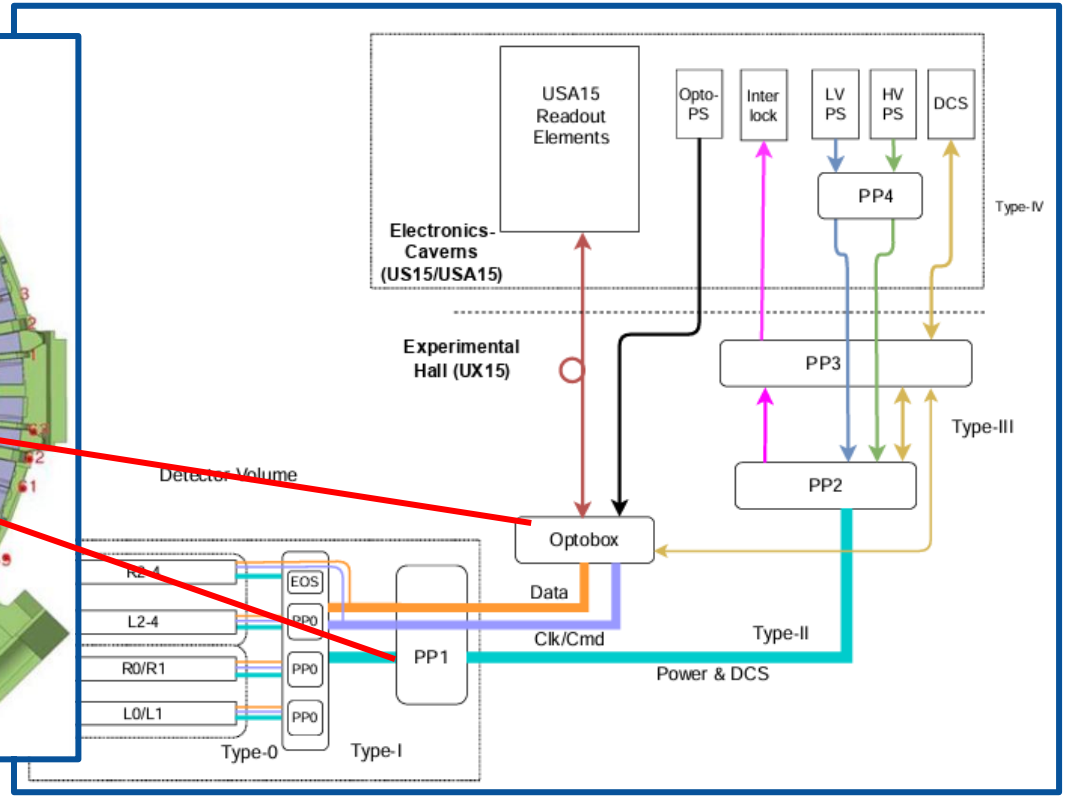
INTRODUCTION TO ITK PIXEL





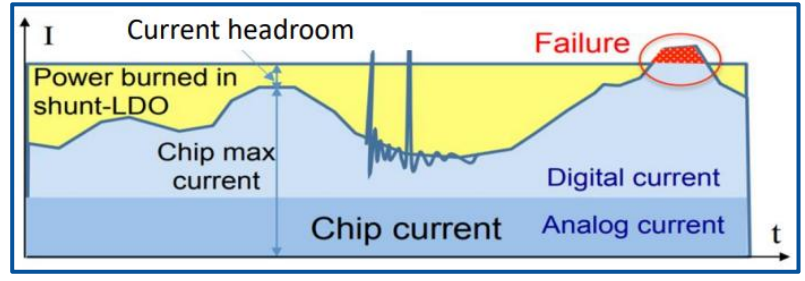
INTRODUCTION TO ITK PIXEL





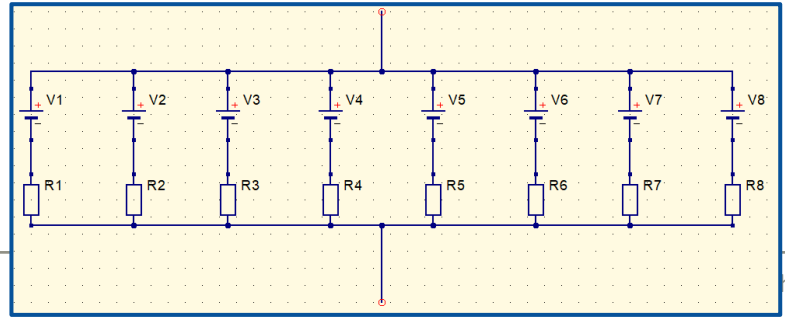
SERIAL POWERING ON THE MODULE LEVEL

- Determine (simulation & measurement) **'nominal'** input current per chip
  - **Add some overhead** for 'unusual events'
- **Current distribution** on module
  - Analyse configuration phase space
  - Tolerances, process variation, manufacturing variability
  - **Add some overhead**



$$I_{\text{in}} = \left(1 + s_{\text{global}}\right) \sum_i I_{\text{Load},i}$$

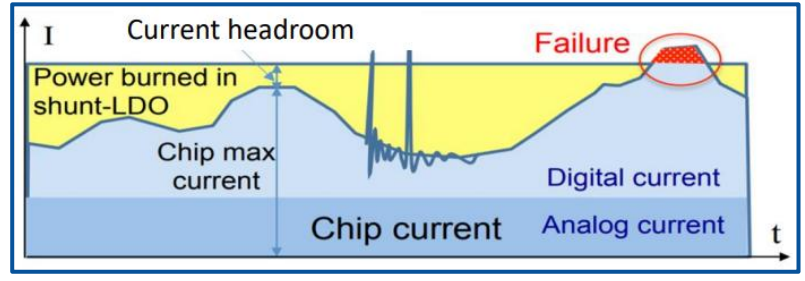
$$I_j = \frac{I_{\text{in}}}{\sum_i \frac{R_j}{R_i}} + \frac{\sum_i \frac{V_i}{R_i}}{\sum_i \frac{R_j}{R_i}} - \frac{V_j}{R_j}$$

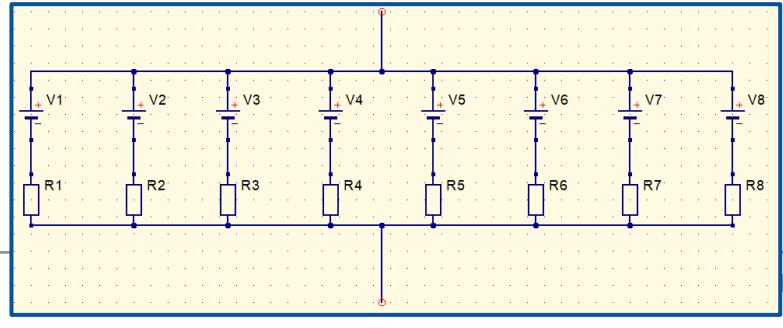


$$I_i \geq I_{\text{Load},i} \cdot \left(1 + s_{\text{min},i}\right)$$

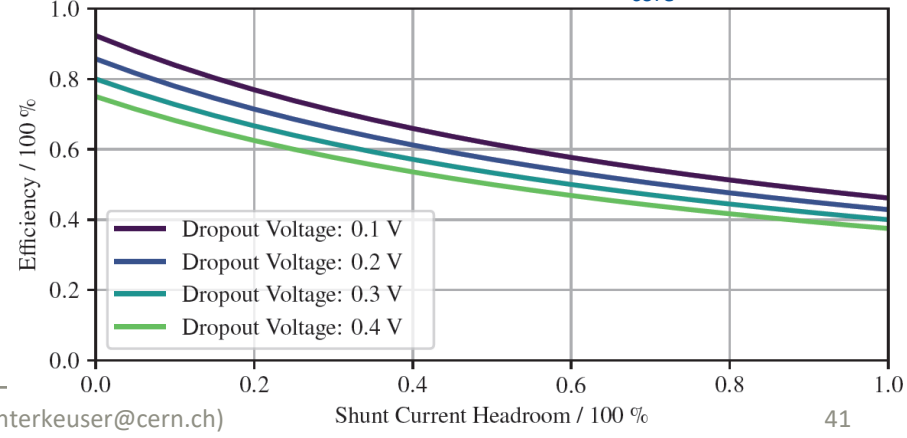
SERIAL POWERING ON THE MODULE LEVEL

- Determine (simulation & measurement) **'nominal'** input current per chip
  - **Add some overhead** for 'unusual events'
- **Current distribution** on module
  - Analyse configuration phase space
  - Tolerances, process variation, manufacturing variability
  - **Add some overhead**
- Headroom decreases **SLDO power efficiency**

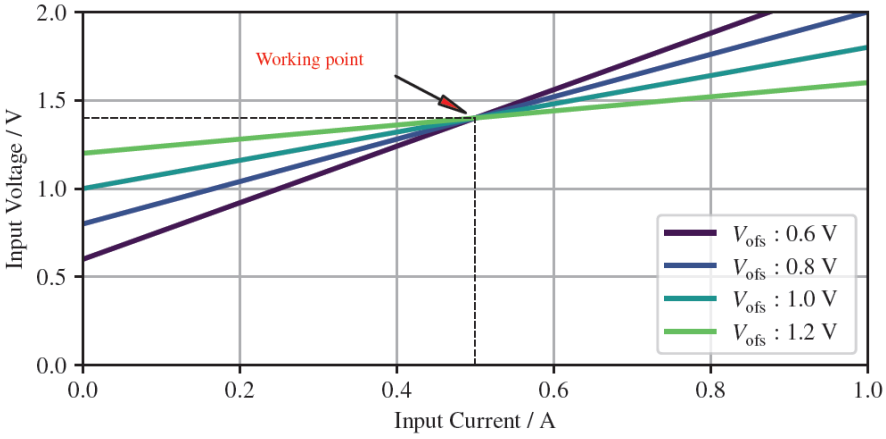




Single-SLDO power efficiency, V_{core} = 1.2 V

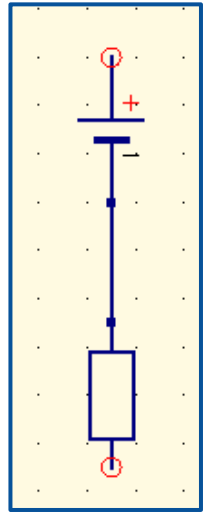


SERIAL POWERING



as long as the ≈ SLDO is operational

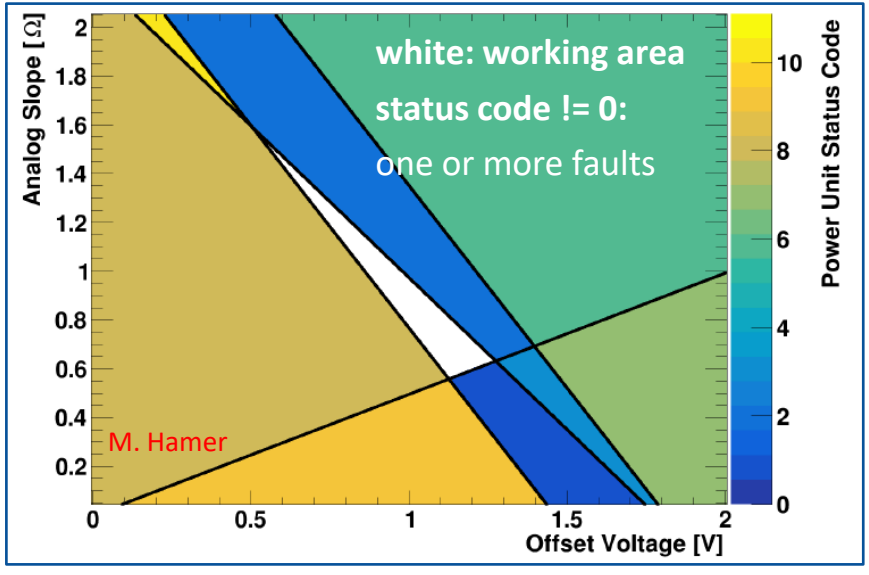
$$V_{in} = V_{ofs} + R_{eff} \cdot I_{in}$$
$$= R_{ofs} \cdot I_{ofs} + \frac{R_3}{k+2} \cdot I_{in}$$



- SLDO regulator converts constant input current into a constant supply voltage for the ASIC
  - Surplus current $I_{shunt} \geq 0$ A is drained through M_4
  - Dropout voltage V_{DO} across M_1 → higher V_{in} than VDDD/VDDA, O(0.2 V)

SERIAL POWERING ON THE MODULE LEVEL

- **Example** for ITk Pixels **Layer 2** modules, highly simplified scenario (well defined, fixed max. deviations)
  - **Numbers to be considered illustrative only**

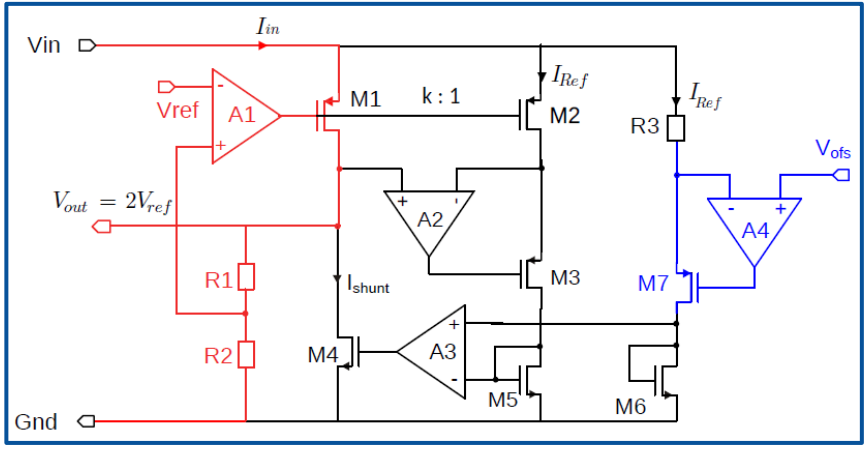


Parameter	μ	σ	max. deviation
$R_{\text{ext,i}}$	see Table 3.21	0.1%	2σ
k_i	1040	1.5%	5σ
$R_{\text{trace,i}}$	see Table 3.21	0.1%	3σ
R_{Vofs}	see Table 3.21	0.0%/0.1%	2σ
I_{ofs}	40 μA	1%/2.5%	3σ

Criterion #	Description	Status Code Bit	Status Code Increment if Failed
1	$U > U_{\text{min}}$	1	+8
2	$U < U_{\text{max}}$	2	+4
3	$U_{\text{high impedance}} < U_{\text{max,H}}$	3	+2
4	$s_i > s_{i,\text{min}}$	4	+1

Table 3.19: Criteria that are used to determine if a given set of SLDO parameters is acceptable or not.

SERIAL POWERING ON THE MODULE LEVEL

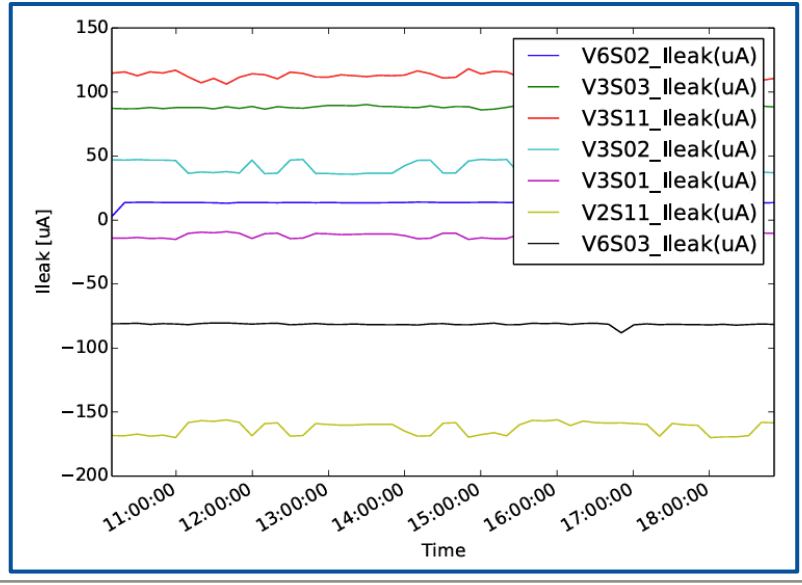


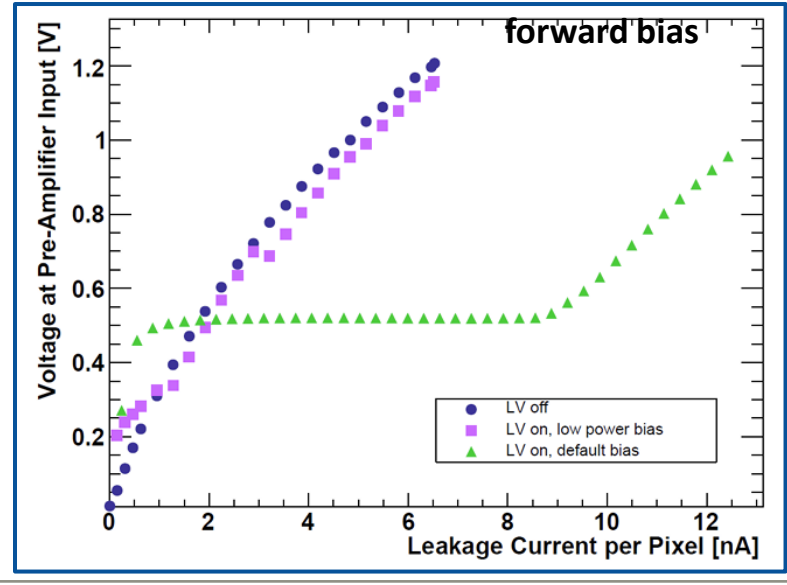
- **Updated SLDO feature set** to improve system reliability
  - Based on system test experience & detector design choices
- SLDO startup in early implementations unreliable -> additional **offset startup**
- **2-stage bandgap** reference scheme
- Input voltage clamp (**OVP**) protects ASIC from voltage transients
- **Undershunt current protection** -> reduces transients from overloaded SLDOs
- Low power mode (**LPM**) for detector testing without cooling

HV DISTRIBUTION

- ITk Pixel ASIC on power up: “low power configuration”, i.e. minimum analog biases and disabled core columns
  - Estimated per-pixel leakage current below critical boundary
  - Alternative: low impedance/low resistance off-mode for HV PSU

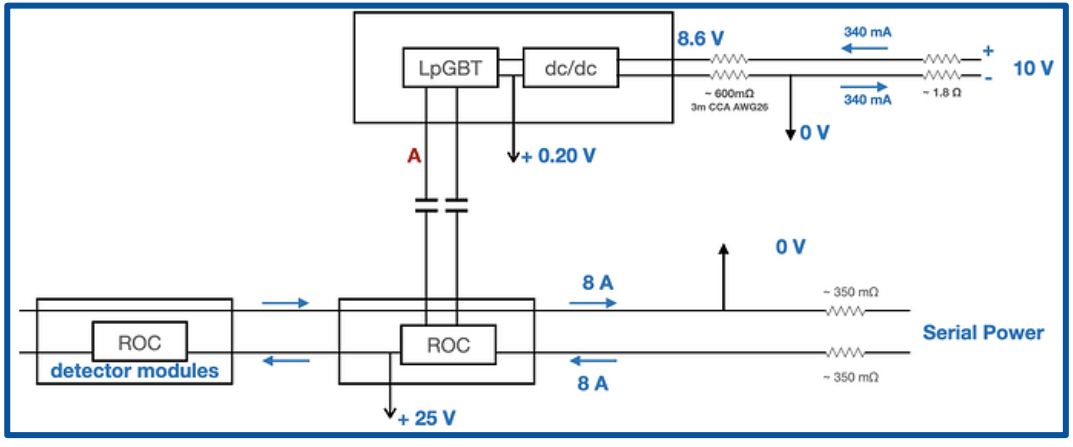
https://cds.cern.ch/record/2808444/files/ATL-ITK-PUB-2022-002.pdf





DATA TRANSMISSION SCHEME

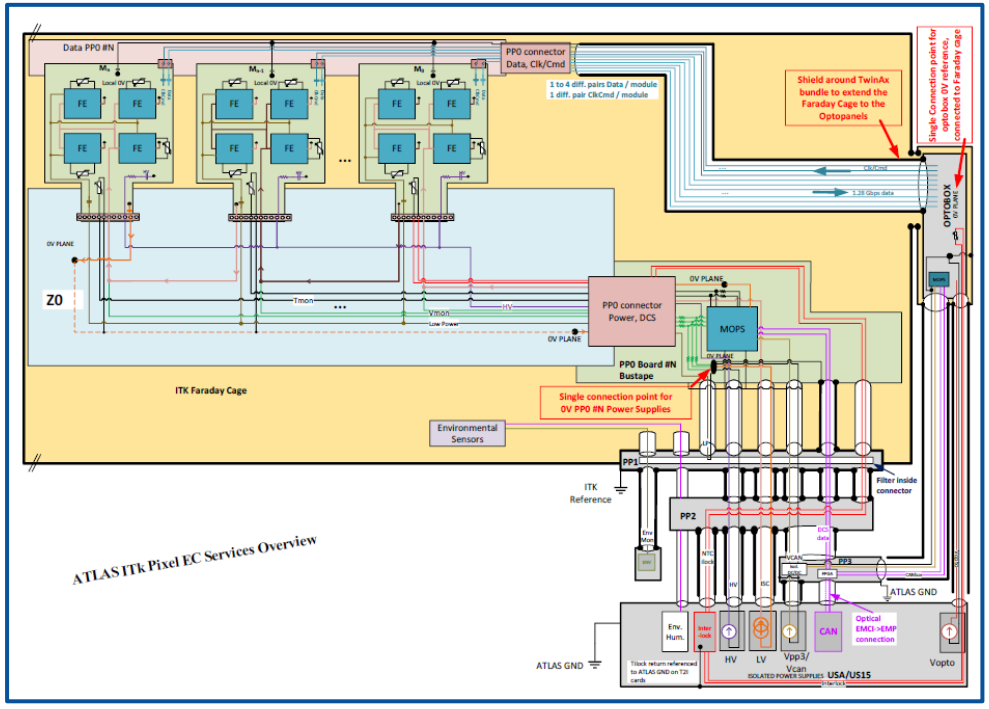
- **Possible complication**:
  - Leakage through parasitic parallel resistance in capacitors
  - For details, see this thread in the lpGBT user forum



- No hardware mechanism to prevent switching on the LV when optoboards are not powered → handled in DCS FSM

- There is a concern that the lpGBTs are damaged if the LV is on ("Serial Power") and Vopto is off
  - ''Floating'' lpGBT e-ports are pulled to module reference voltages (i.e. up to ~20V) through capacitor leakage currents
- The drawing is not entirely accurate for ITk Pixels due to the GBCR in between the module and lpGBT, but the problem is going to be the same (same pads, e-RX on GBCR)
- It is not clear how severe the problem really is → some basic tests we ran indicate it's fine
- Better safe than sorry → interlocking of PSUs for optobox and SP current sources are linked

GROUNDING & SHIELDING



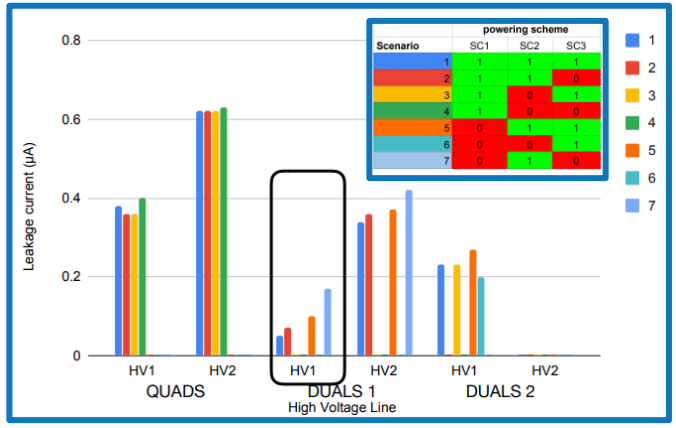
- The **only shielded** Type-1 Cables in ITk Pixels:
  - Data cables
  - CAN bus cables
- Both have **different endpoints**:
  - Optobox
  - PP1
- **“0V”-plane** is referenced through exactly one of both options
  - If the **shields** of either one are connected, the shield of the other flavour of cables is **AC coupled to the “0V”-plane on PP0**

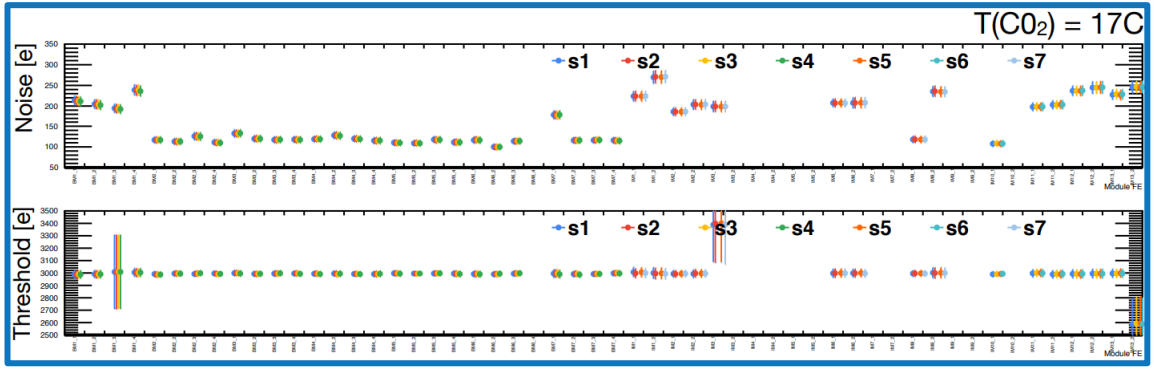
GROUNDING & SHIELDING

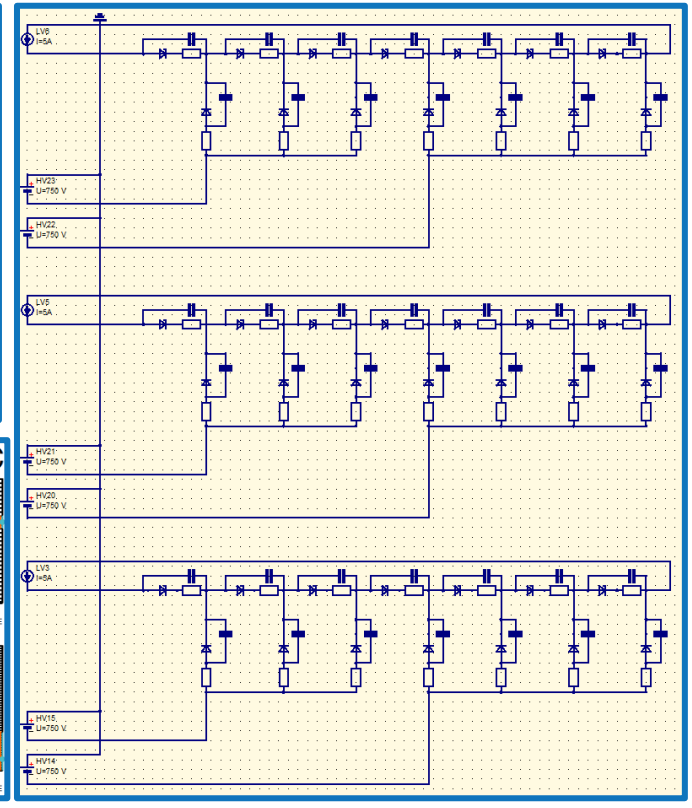
old data from early system test using FE-I4 quad modules!

local merging of SP chains did not show any issues in system test

→ looking into sharing optoboards for coupled SP chains







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SERIAL POWERING IN ITK PIXEL

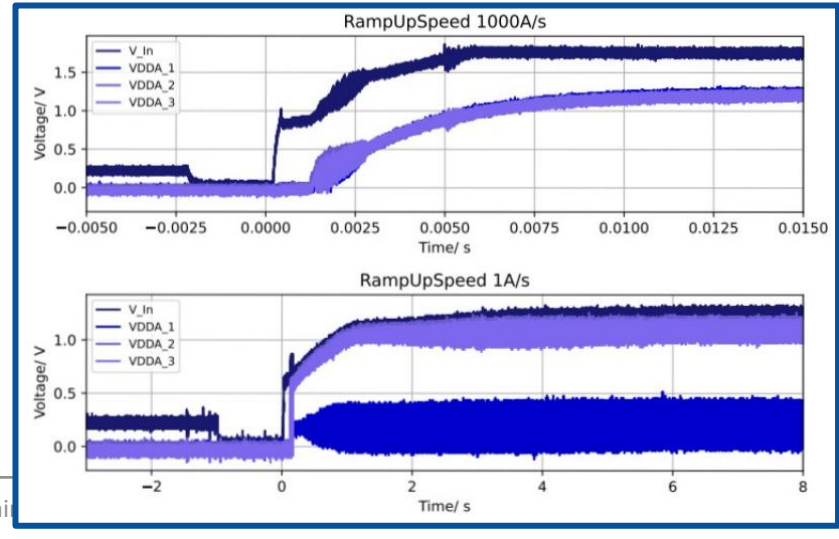
POWER SUPPLIES, START-UP & OPERATIONAL ISSUES

POWER SUPPLIES

- Currently in the process of evaluating pre-production power supply units in system test
- **Current source or voltage source?**
  - For module QC and some system level testing, ATLAS has been using **voltage sources**
  - The detector and the QC of loaded local supports, most institutes will use **'current sources'**
  - Simulations hint at **better stability** of current sources during transients
  - But**: both** seems to work fine!

- Turn-on behaviour?
  - ~Fast ramp-up is required
  - Well specified before, no out-of-the world values required → not an issue

  - Again: off-mode behaviour of PSU can be an issue



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POWER SUPPLIES

- Low voltage PSU to be used for ITk Pixel: PL510 current source

- $I_{LV} \leq 10$ A, $V_{LV} \leq 48$ V
  - Up to 300 W per channel
- Per-channel interlock
- 10 channels / 3U (19”)
  - Up to 3 kW per crate

- Communication via Ethernet (RJ45)

Initial specifications for LV power supply (Ireg)

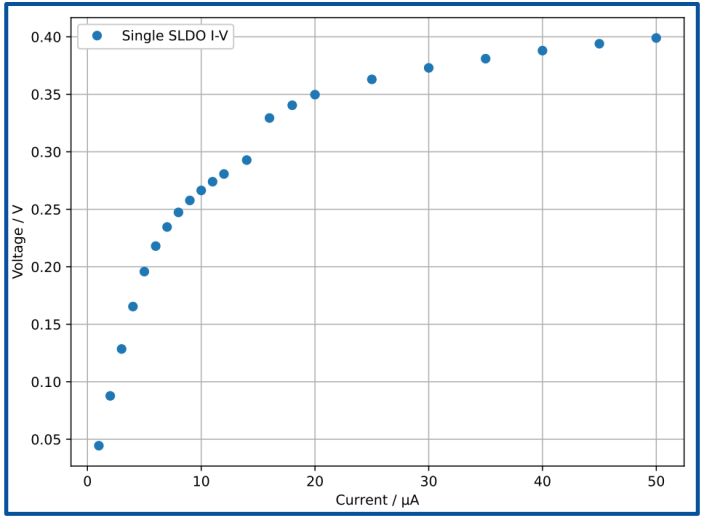
	Min Value	Max Value
Output Current	0.3 A	10.0 A
Delivered Voltage	1.4 V	48 V
Power	0 W	300 W
Floating	|50 V|	|50 V|
Capacitance from floating ground to chassis ground	-	1 uF
Ripple for f <= 20 MHz	-	4 mA pp
Ripple for f > 20 MHz	-	0.15 mA pp
Programmable Ramp (up and down, separately configurable)	1 A/s	10.000 A/s
Set Current Precision/Resolution	0.5% / 8 bits	-
Set Voltage Limit Precision/Resolution	0.5% / 8 bits	-
Measured Current Precision/Resolution HIGH	0.5% / 8 bits	-
Measured Current Precision/Resolution LOW	0.5% / 8 bits	-
Measured Terminal Voltage Precision/Resolution	0.5% / 8 bits	-
Long Term Stability	-	0.2 % / 10 K
Off-Mode	This should be selectable between either High-Ohmic (> 100 kOhms) or Low-Ohmic (< 10 Ohms).	
Maximum Overvoltage for fast Load Change	-	0.3 Ohms / 5 us: 400 mV

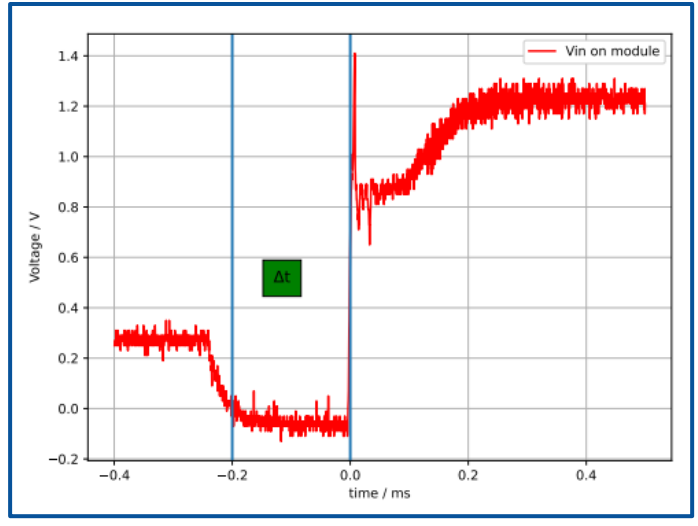
Table 6: Specifications for Low Voltage Power Supplies (Current Sources)

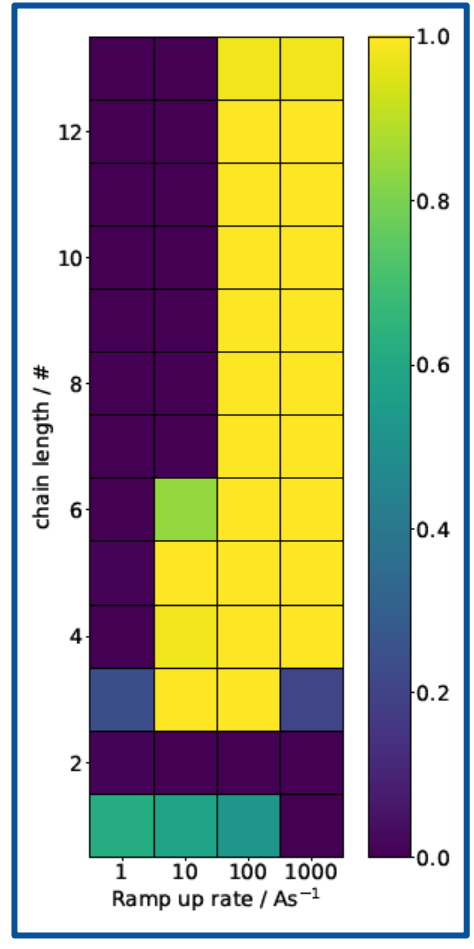
PL510 prototype @ Uni Bonn

START UP

- Did extensive testing with current source prototype
  - Start-up issues observed in “chain length – ramp speed” parameter space
  - Short chains and slow ramp-rates show start-up issues
- For short chains: caused by leakage of PSU in off-mode





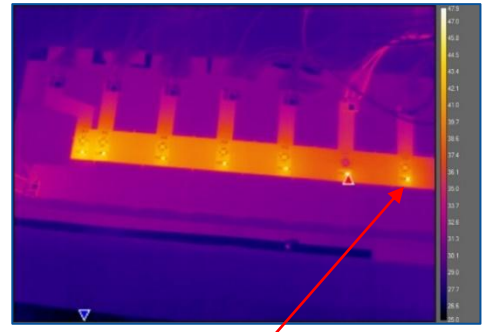


OPERATIONAL ISSUES

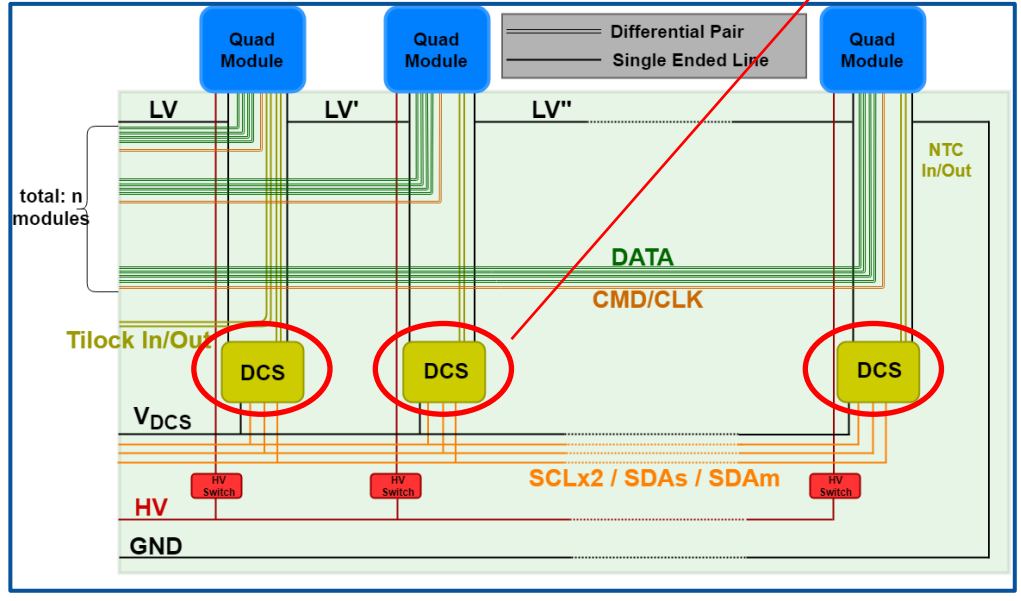
- System testing with production chip modules is still very much ongoing
- **Foreseen turn-on procedure:**
  - Power up MOPS ASIC for monitoring → this is designed to run without cooling
  - Power up optoboards → proper referencing of input pads (requires cooling for optoboxes running)
  - Power up readout ASICs → requires optoboxes to be powered up and CO2 cooling to be running
  - Turn on HV (sensor bias) → proper flow of leakage current
- Interlock interplay:

	action on individual channels or small channel groups			action on all channels		
	HV	LV	Opto-power	HV	LV	Opto-power
SP chain temperature	X	X	TBD			
Optobox temperature	**X**	**X**	X			
BIS				X		
DSS				X	X	X

OPERATIONAL ISSUES



- Things we considered, but that didn't make it into the final design:
  - Individual, switchable bypass for every module (**PSPP ASIC**)
  - **Multiple issues**:
    - Power hungry bias resistors
    - Switchable low resistance path in parallel to the module LV
    - Negative input voltage on modules for standard PSU (LV off)
    - **Fast switching** (power!) triggered chain reaction → **SP chain off**



- Decision to remove the PSPP ultimately **driven by risk analysis**

OPERATIONAL ISSUES

- Things we considered, but that didn't make it into the final design:

  - Individual, switchable bypass for every module (**PSPP ASIC**)
  - **HV switches** for each module
    - Require negative bias voltages up to -650 V
    - All components must be rated for twice that number
    - No signal available that can switch such high voltages
  - Fuses were studied instead
    - Expect up to 6.6mA per quad in nominal operation
    - **No suitable fuses identified**