HV-CMOS Multi-chip and Serial Powering Prototyping

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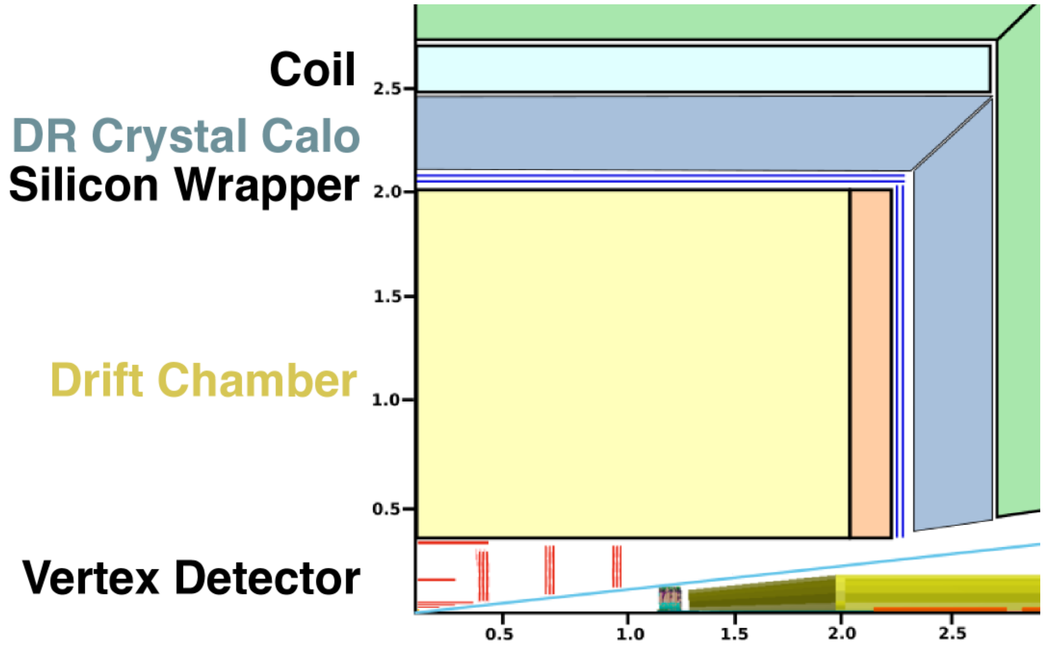
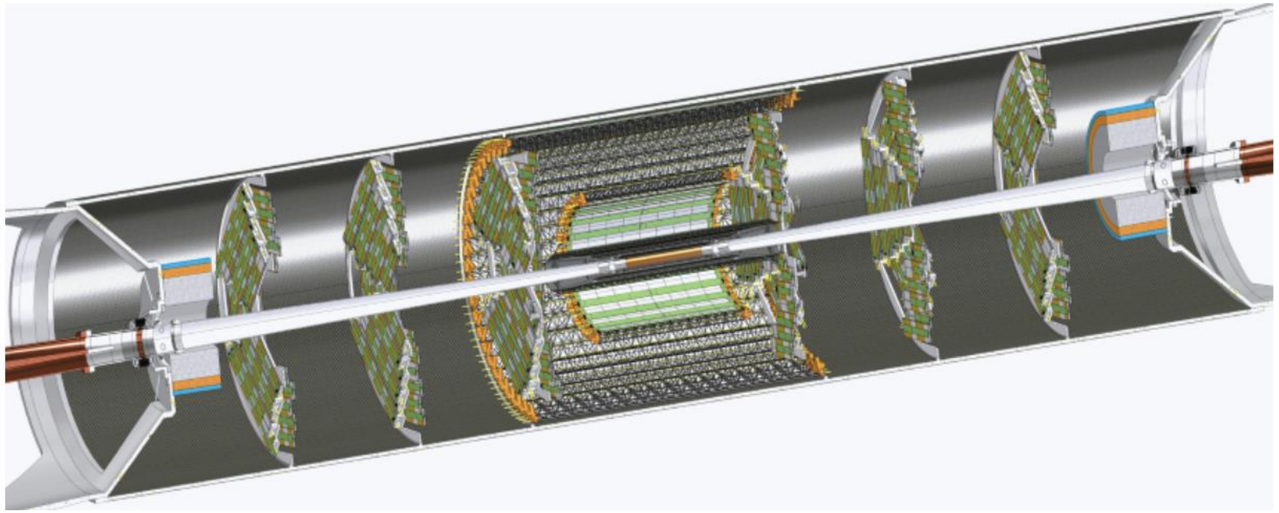
Guangzhou, 6-10 November 2025

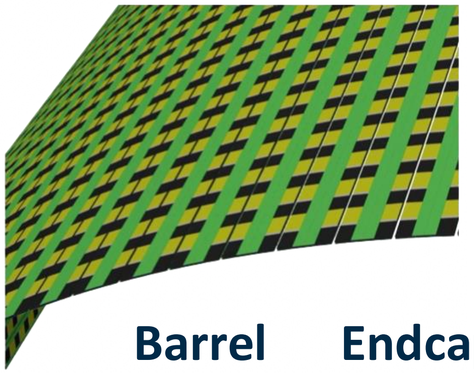
General Objective

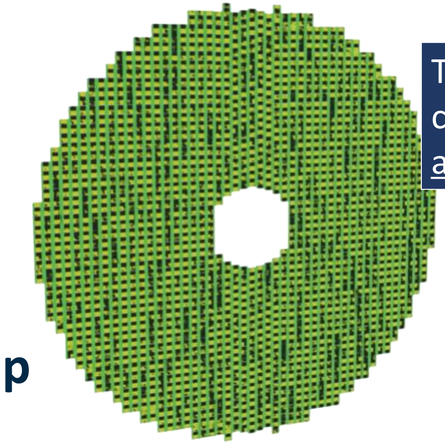
- Develop large-area HV-CMOS pixel detector for future Higgs factories.
- Use multi-chip modules with **data aggregation** and **serial powering**.
  - Reduce number of **data and power connections**.
  - Employ on-chip **shunt-LDO regulators** for serial powering.
- Integrate modules on **low-mass multilayer flex PCBs** into staves.
- Explore **low-mass aluminium flex**, **single-point TAB bonding**, **lightweight supports**, and **efficient cooling** for optimised power and material budget.

Higgs Factory (IDEA Concept)









Barrel Endcap

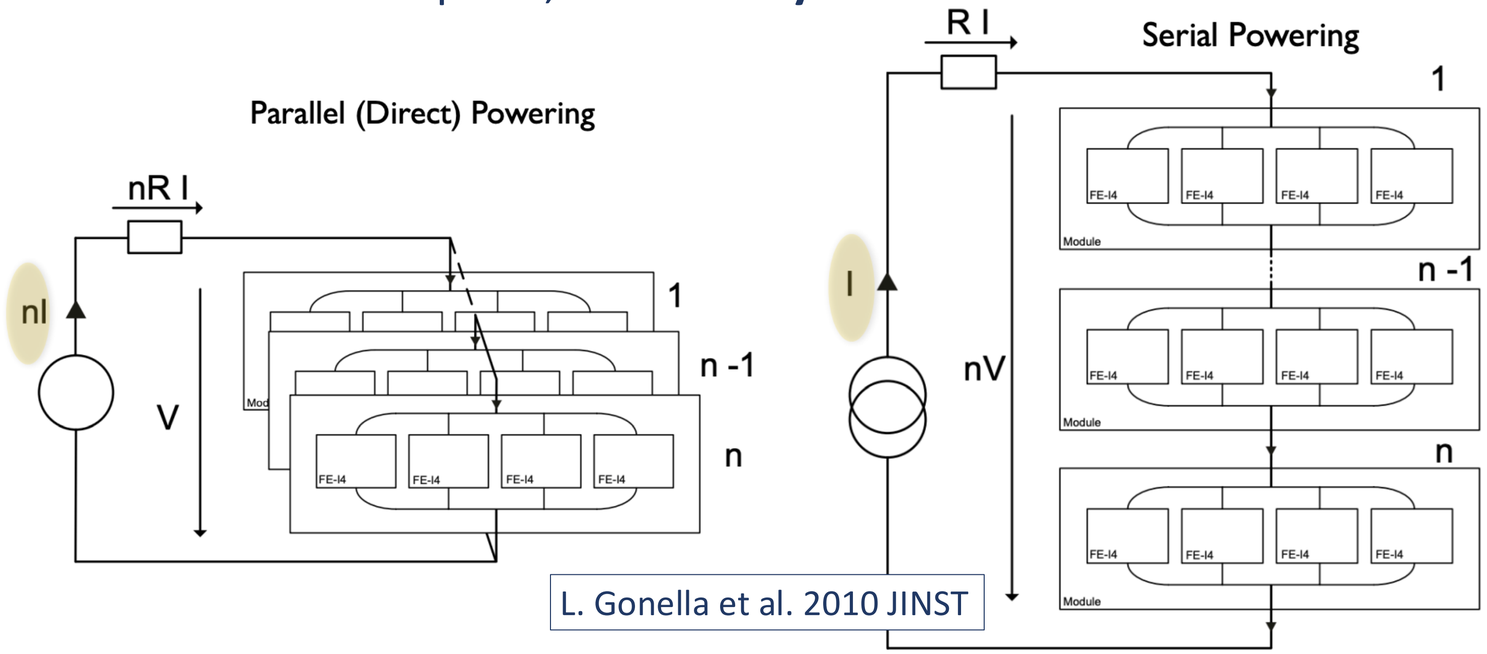
The IDEA detector concept for FCC-ee arXiv:2502.21223

- **Silicon tracking in different regions for IDEA concept.**
- Inner Vertex Detector (R = 1.4–3.3 cm)
- **Outer Vertex Detector (R = 13–31 cm)**
  - HV-CMOS monolithic pixel sensors proposed **as the elementary unit.**
- Silicon Wrapper / TOF (R/z = 200 cm)

CEPC Technical Design Report arXiv:2510.05260

Motivation: Serial Powering

- **Serial Powering (SP) Concept:**
  - **Modules are powered in series** using a **constant current** source.
    - Power: the readout electronics powering (Low Voltages) **~1.8-2.2V**
  - Voltage is locally regulated on each module with **on-chip shunt-LDO regulators (are powered parallel in quad modules).**
- **Advantages:**
  - High power efficiency, cable power consumption scales down **by a factor of n^2.**
  - Current consumption, reduced **by a factor of n** and less services and material requirements.



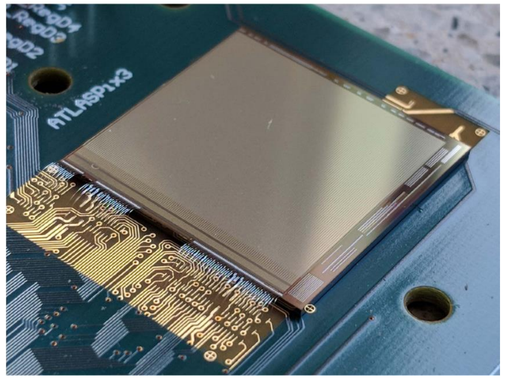
L. Gonella et al. 2010 JINST

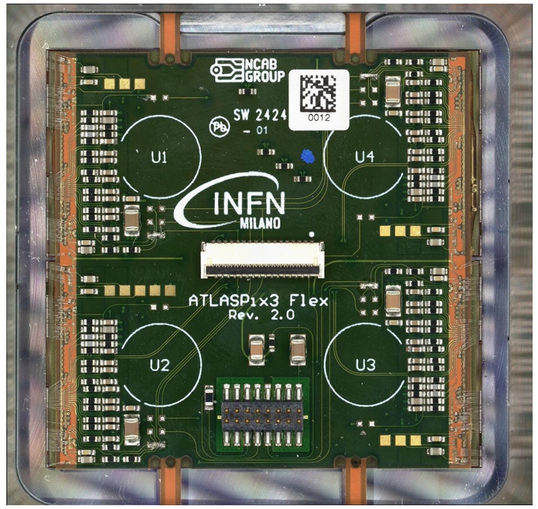
Scaling the large area pixel applications.

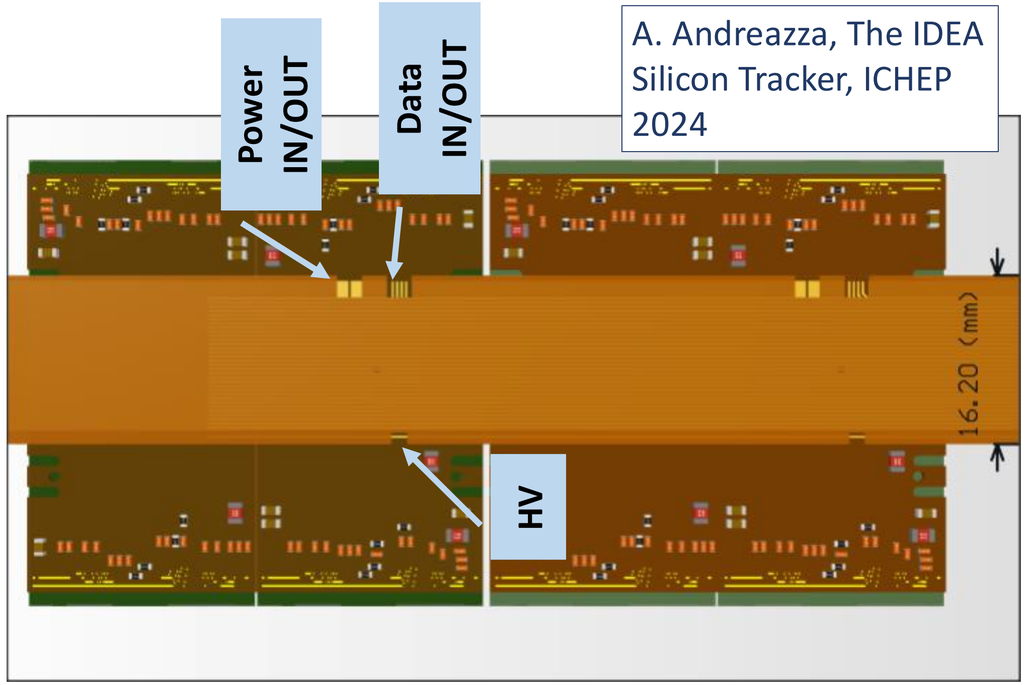
CCF approved!

Serial Powering: CCF DRD3 Project

Quad Flex designed by University of Milano

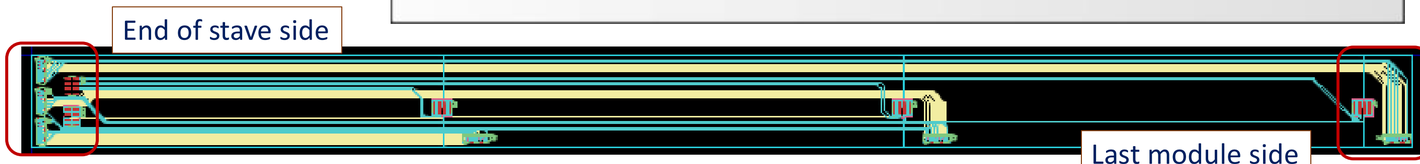


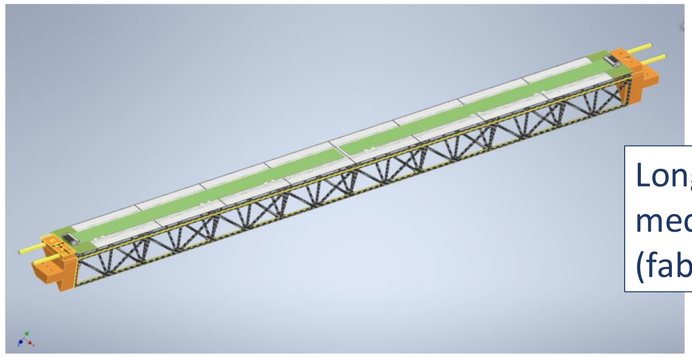




A. Andreazza, The IDEA Silicon Tracker, ICHEP 2024

- Optimized **power and data signal routing** along the stave
- **Readout Unit Design**
  - **Multi-chip modules** (e.g., 2×2 quad modules)
  - **Serial Powering Architecture**:
    - 1 LV and HV line per stave
  - **Chip-to-chip data transfer** for local aggregation
  - LVDS module configuration with **CDR**.

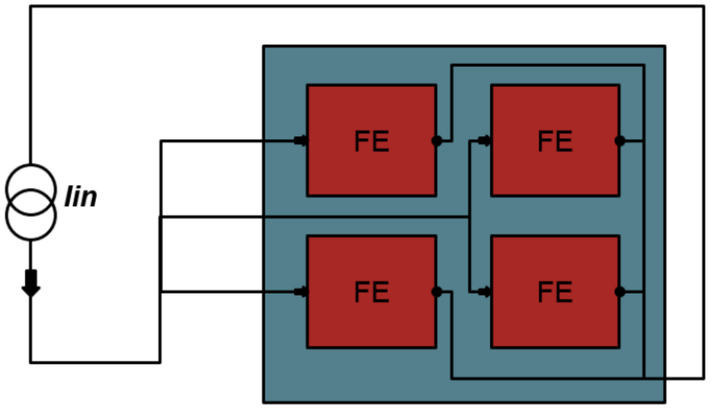


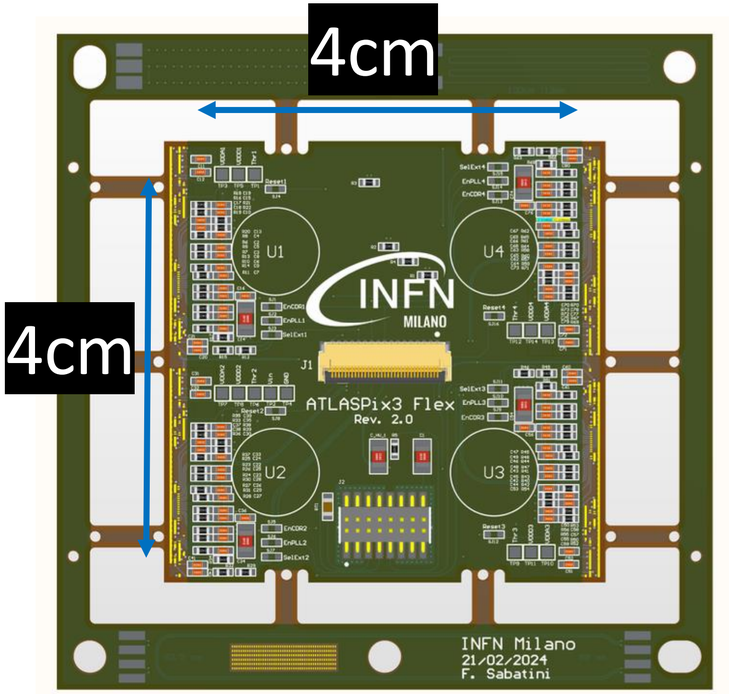


Long stave **(~1.3m)** mechanical structure (fabricated **in Pisa)**

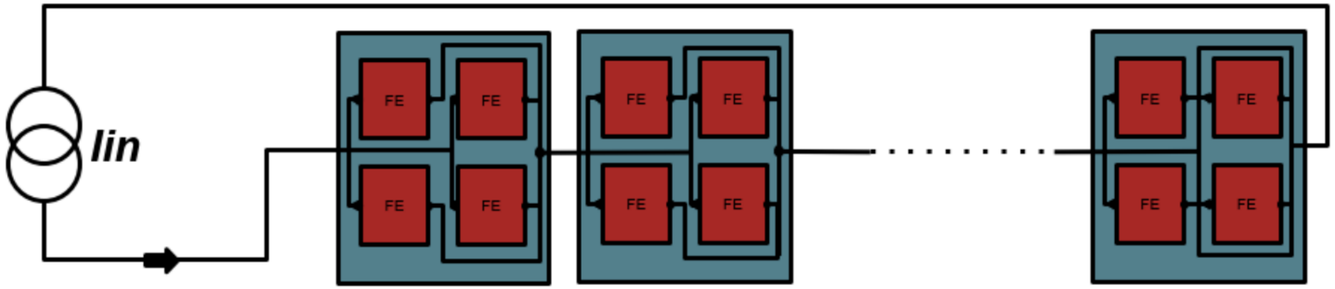
Serial Powering on ATLASPix3.1 Quad Module

- **ATLASPix3.1 sensors**:
  - TSI 180nm CMOS
  - 2x2 cm^2 (pixel pitch 50x150 um^2)
  - ~600mW/chip
- Multi-chip **(Quad module)** approach:
  - 4 FE regulators in **parallel**
  - Single LV (via **shunt-LDO**) and HV bias
  - **Molex data** & **FTM-108** power connectors
  - Common command lines
  - Each chip has its own dedicated data-out line.
  - **AC coupling**





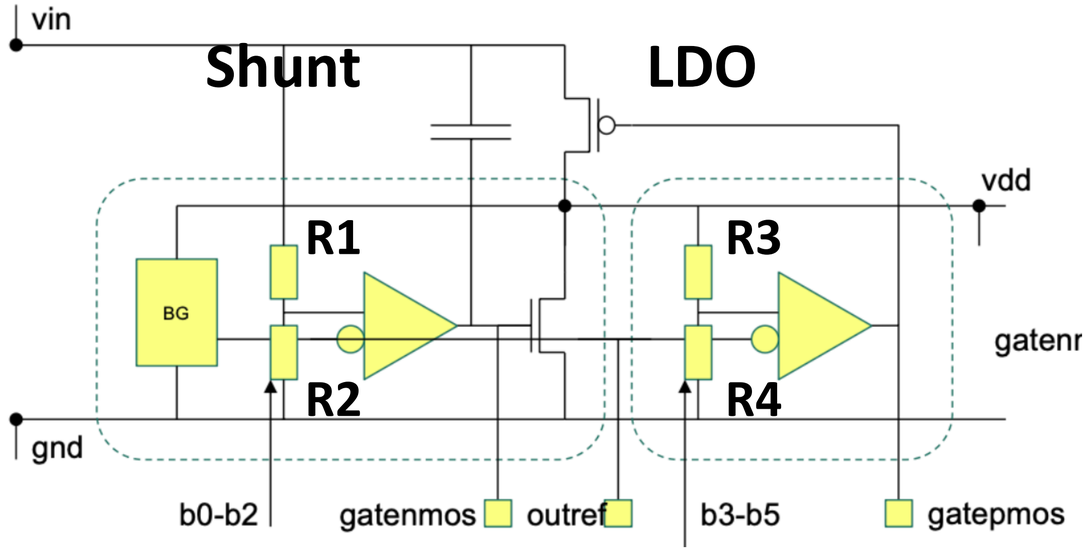
- The quad module, **serial powering integration make it ideal for large-scale applications**.

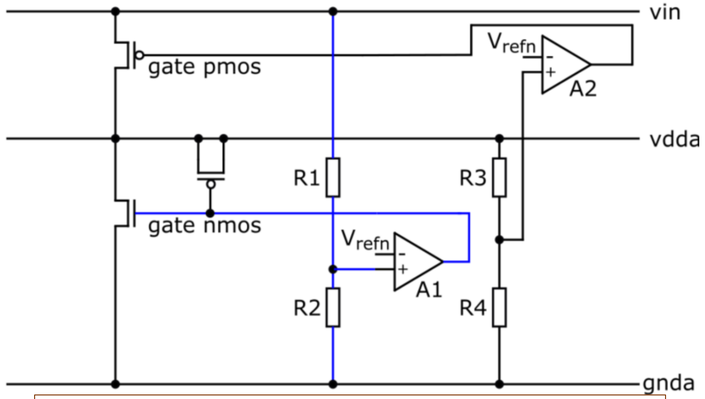


A. Andreazza & Y. Gao, HV-CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections, 2025

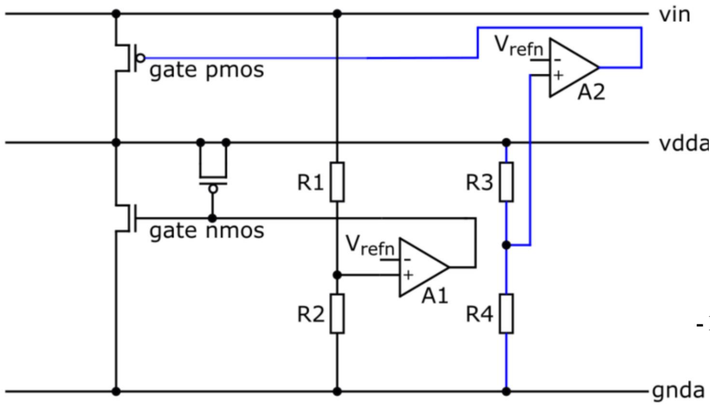
Shunt-LDO Regulators on the Chip

- ATLASPix3.1 can be powered via a **single constant current** with two shunt-low dropout regulators.
  - **Digital &Analog (VDDD/A)**
  - 3-bits (b0-b2) to **tune threshold** of the shunt regulator
  - 3-bits (b3-b5) to **tune VDDs**
- **Vin** is created from constant current via regulators.
- **VDDD/A** presents the **regulated voltage** (output of the shunt-LDOs) to use the chip for operation.





Shunt: allows for the constant current operation, **extra current protection**



LDO: regulates **VDDD/A**

ATLASPix3.1 Quad Module Assembly Process

1) Flex verifications before assembly: Electrical characterisations and signal integrity tests on 5 differential lines

2) Bare Chip Probing using probe needles in probe stations (no probe card)

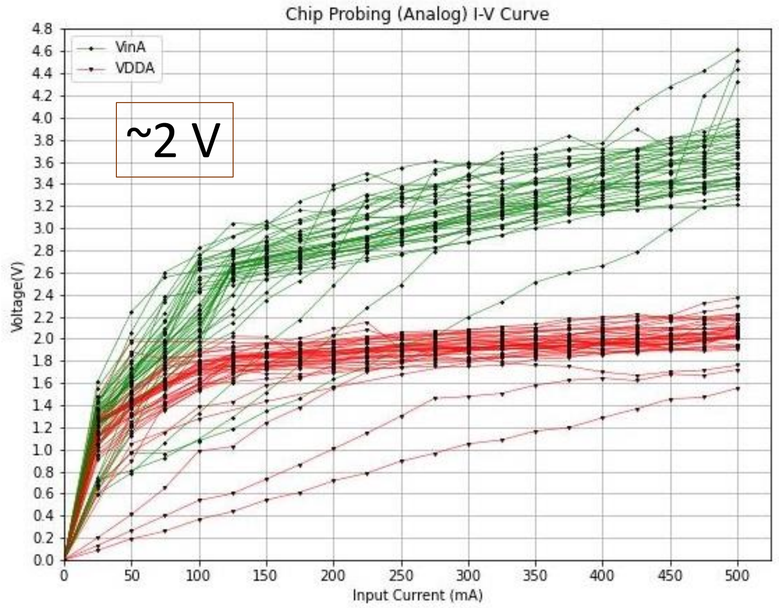
3) Chip to flex assembly:

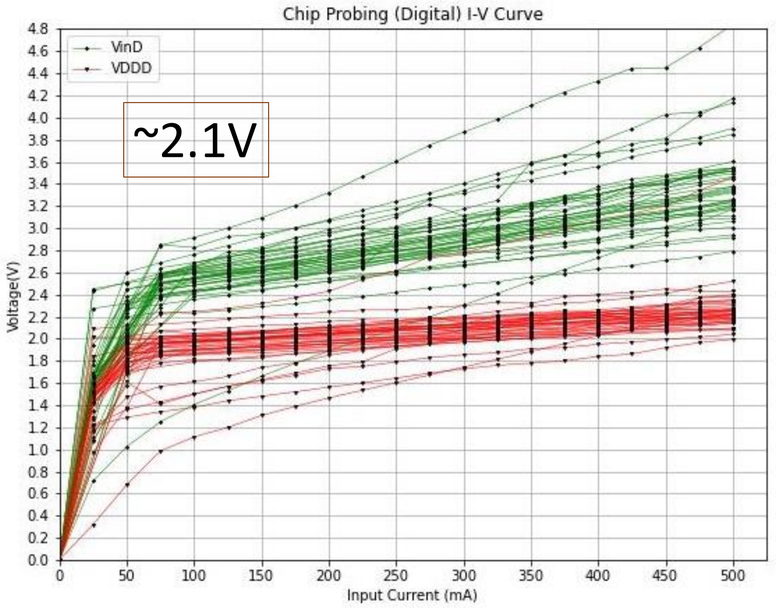
- Chip to flex gluing via customised assembly jig
- Basic visual inspection and metrology measurements
- Wirebonding the chip

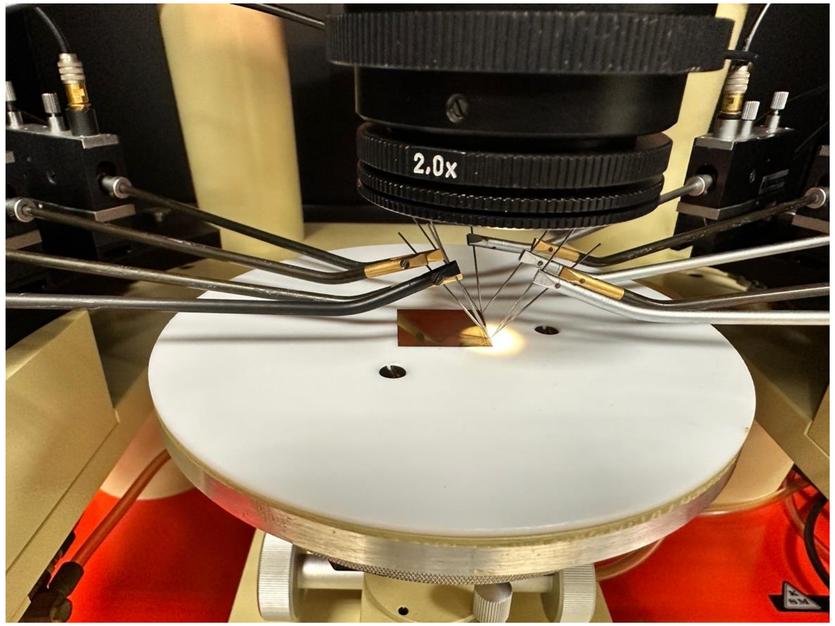
4) IV tests and SLDO verification on the assembled module

https://indico.cern.ch/event/1529127/contributions/6433200/attachments/3036376/5362420/ATLASPix3.1_Quad_Flex_SLDO_Characterisation.pdf

Chip Probing Summary

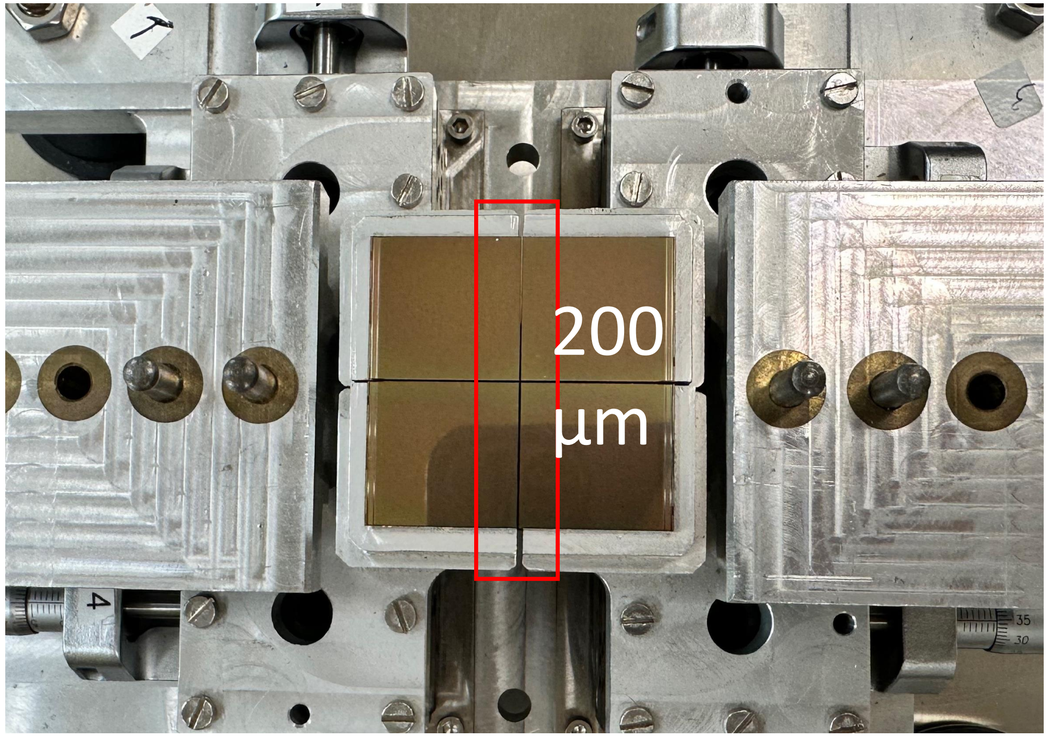


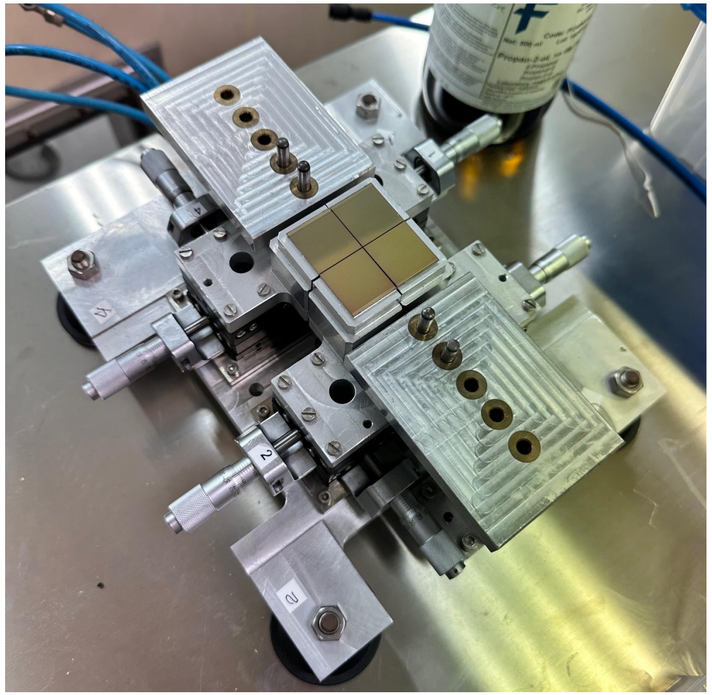


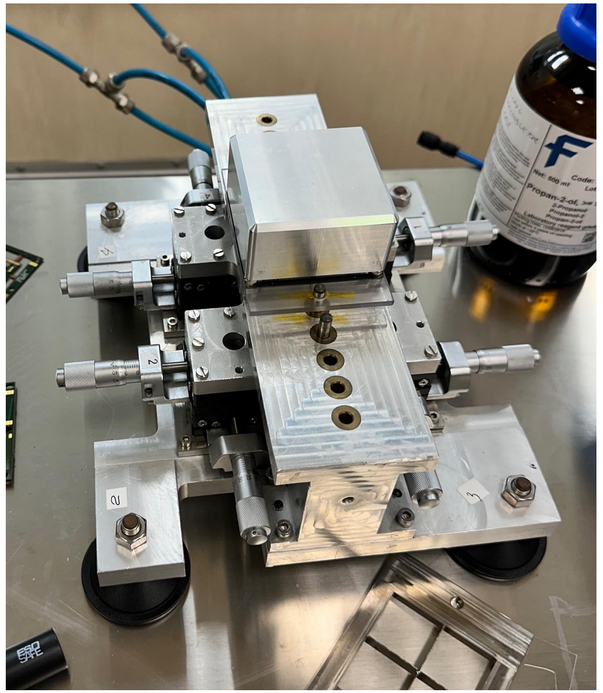


- In total, **48 chips** were probe tested: **38** of them have functional IV/SLDO **(74% pass rate)**
  - **2 chips**, Vin is too high up to 4.5V. The power consumption is high.
  - **8 chips have issues with SLDO performances**
    - **3 chips**, VDDD is not regulated, keeps on rising as currents goes up
    - **3 chips** , both VDDD/A are not regulated, and increasing trend has been seen
    - **2 chips**, VDDD/A are regulated at low level, around **1.6-1.7V**
- The test time for a single chip is approximately **20 mins.**

Gluing the Chip to Quad Flex

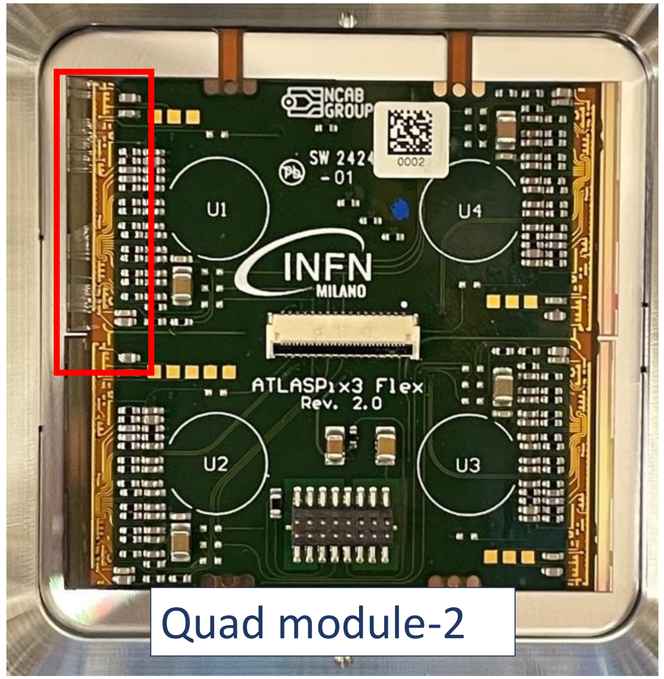




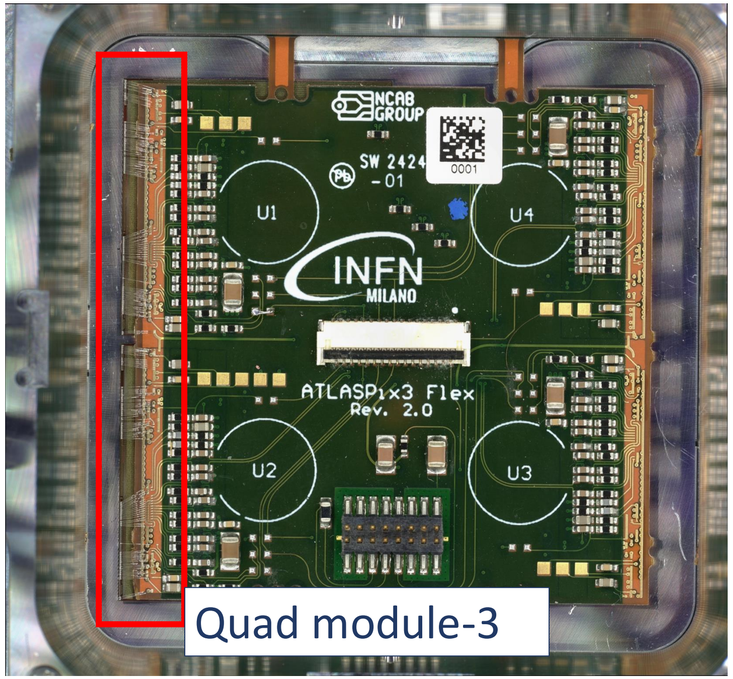


- The **assembly tool** is used to mount the chips onto the quad flex.
- This tool ensures **precise alignment and positioning** of the chips onto the quad flex.
- The inter-chip spacing at the **center** is maintained at **200 µm**.
- After gluing, a weight (300g) is applied to the module for at **least 5 hours.**

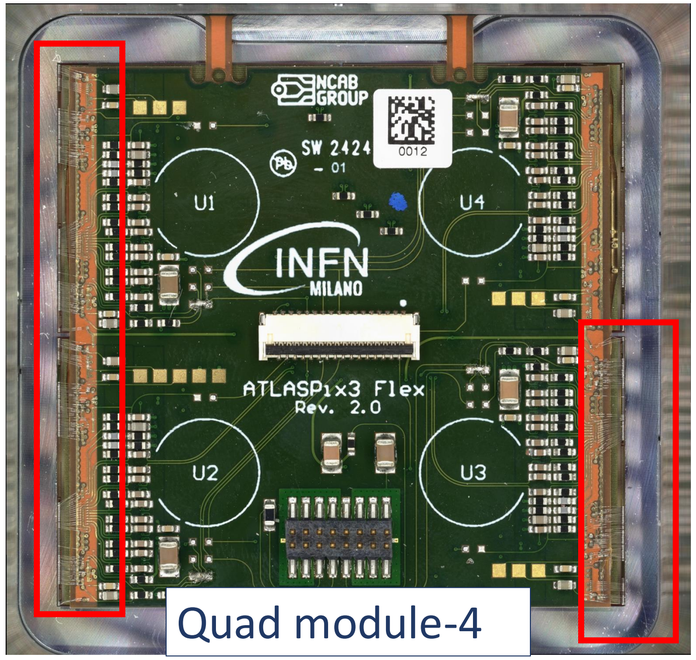
Assembled “Quad” Modules



Quad module-2



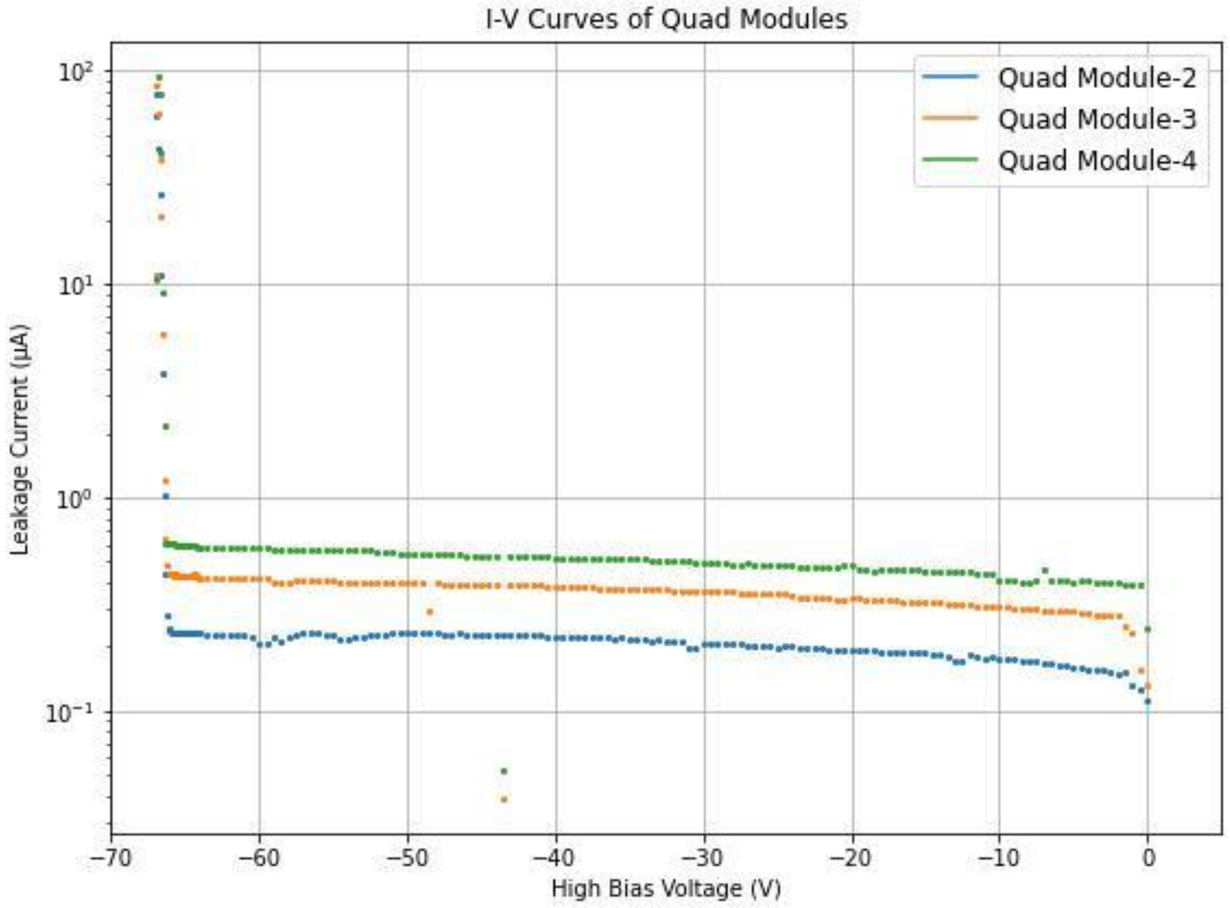
Quad module-3



Quad module-4

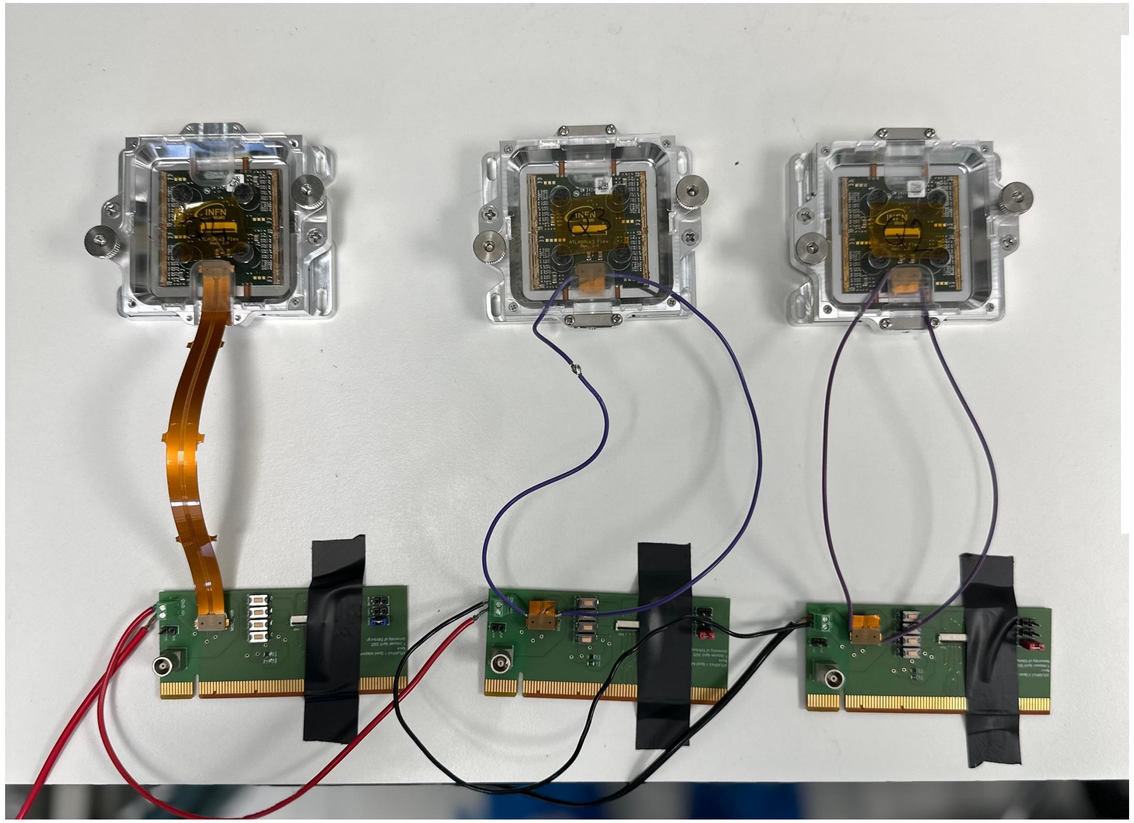
Module	Location	Assembled Chips				Bonded Chips				Power On		Test Configuration				Test Readout			
		1	2	3	4	1	2	3	4	Current (mA)	Voltage (V)	1	2	3	4	1	2	3	4
Q1	Milano	✓	×	×	×	✓	×	×	×	400	2.42	✓	×	×	×	✓	×	×	×
Q2	Edinburgh	✓	×	×	×	✓	×	×	×	400	2.324	✓	×	×	×	✓	×	×	×
Q4	Edinburgh	✓	✓	×	×	✓	✓	×	×	800	2.437	✓	✓	×	×	✓	✓	×	×
Q4	Edinburgh	✓	✓	✓	✓	✓	✓	✓	×	1200	2.435	✓	✓	✓	×	Noisy	✓	✓	×
Q5	Milano	✓	✓	✓	✓	✓	✓	✓	✓	2200	2.52	✓	✓	×	✓	✓	✓	×	✓

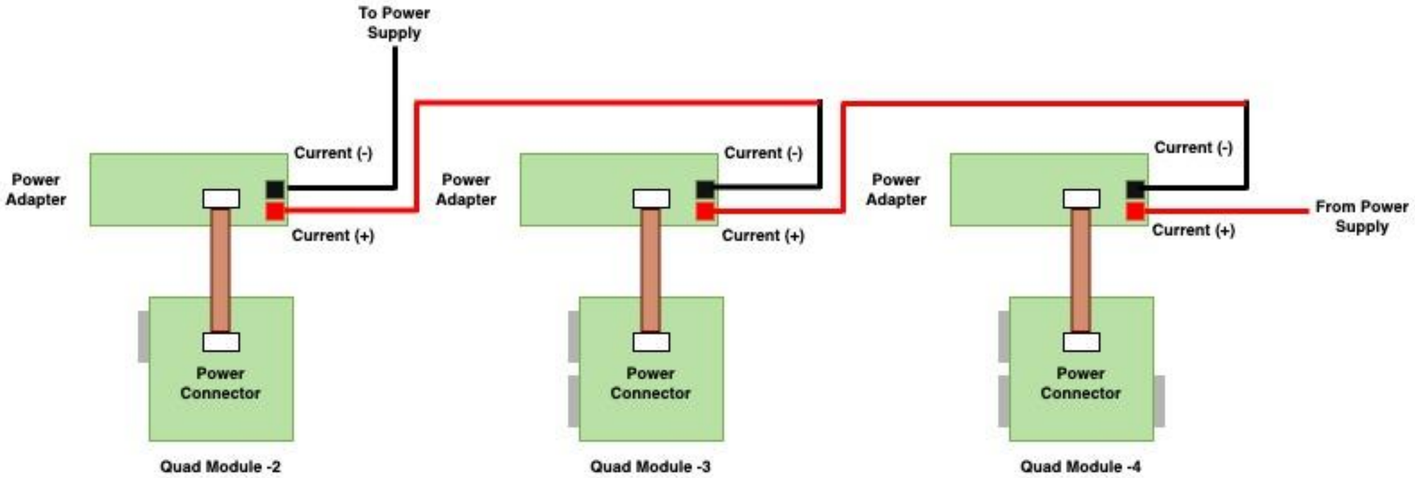
High Voltage (HV) Bias-Leakage Current



- The breakdown voltage of each module is **about -65.38 V**.
- The leakage current has a linear trend with increasing chip in the quad module.
  - Quad Module-2: **varies -112 & -225 nA**
  - Quad Module-3: **varies -253 & -415 nA**
  - Quad Module-4: **varies -440 & -586 nA**

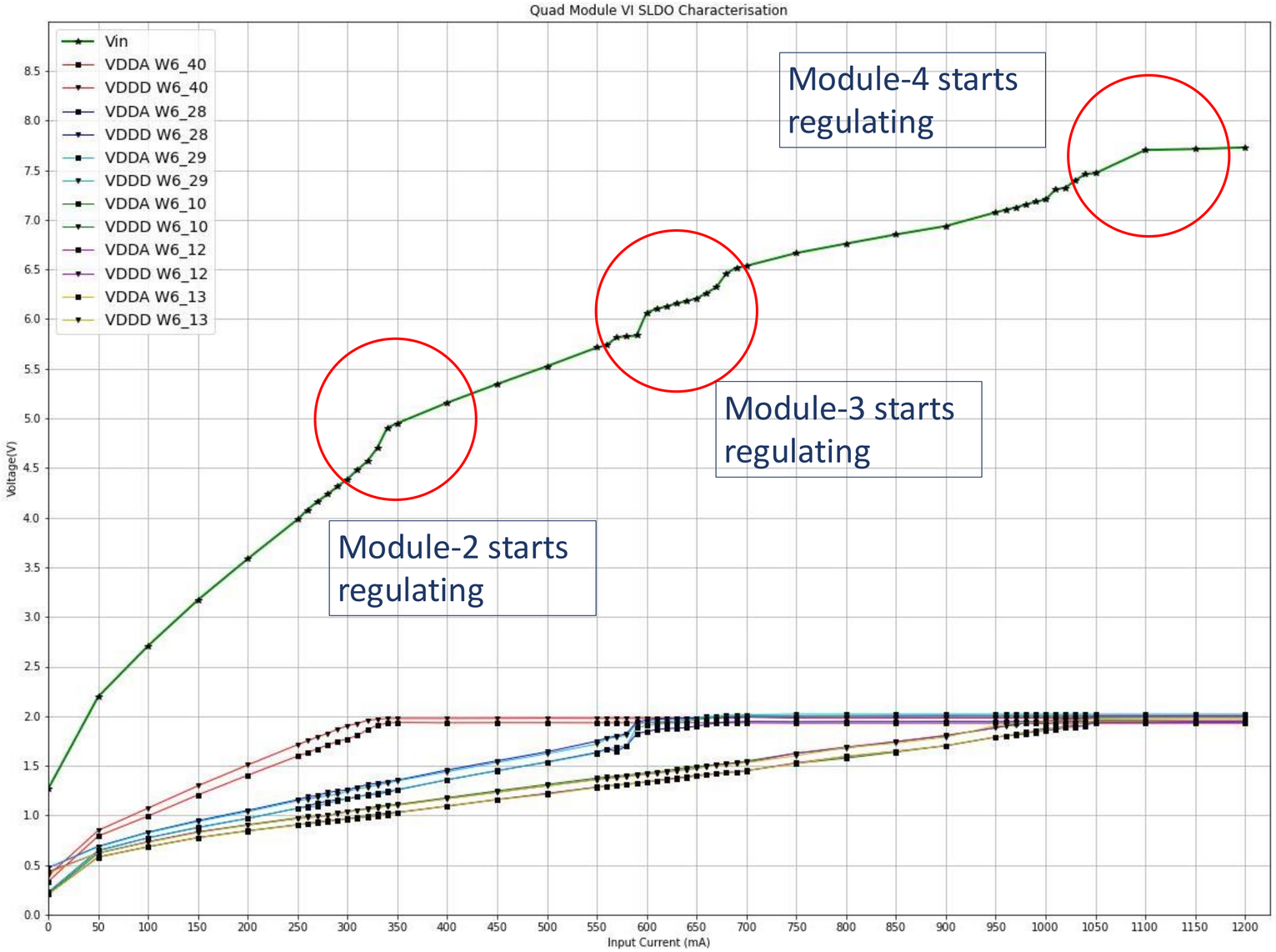
Serial Powering Chain with 3 Quad Modules





- Three quad modules are powered **serial**, with max current of **1.2 A**

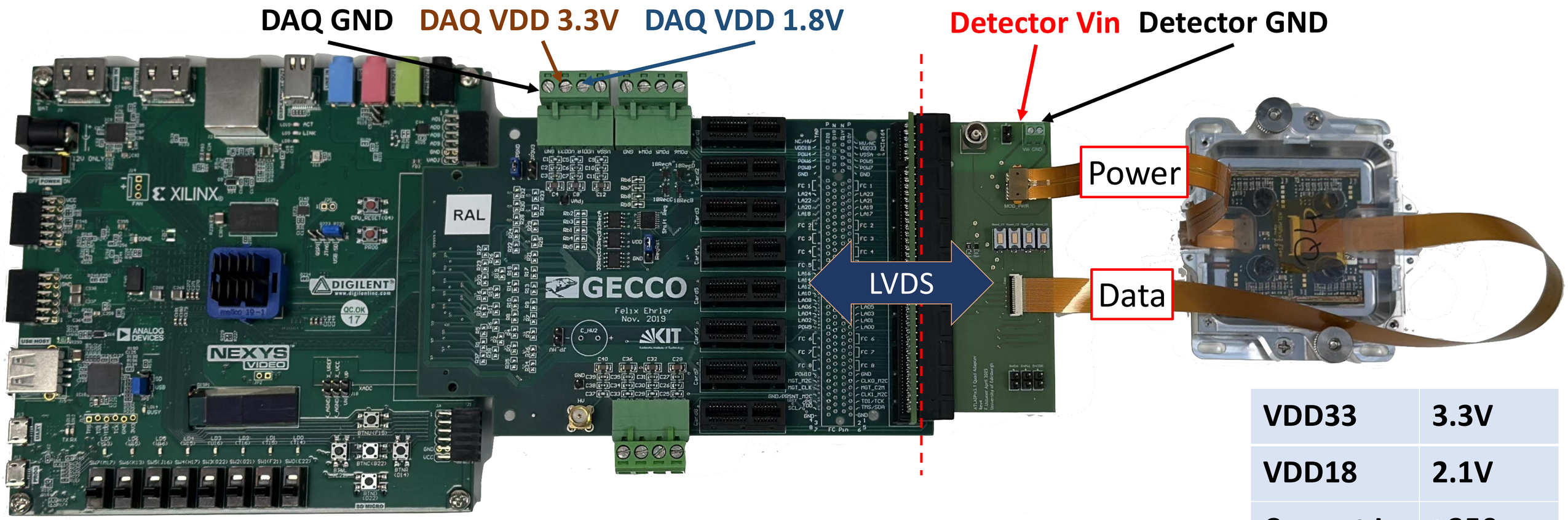
3-Module SP (total 6 chips) LV-IV Characterisation



- Three distinct regulation current
  - All VDDD and VDDA are regulated above **~1A**
  - Vin: 7.6 V
    - **~20% higher** than the sum of VDDD or VDDA in the 3-chip

	Chip Name	Current	VDDD	VDDA
Q-2	W6-40	350 mA	1.98 V	1.93 V
Q-3	W6-28	703 mA	2 V	1.946 V
	W6-29	699 mA	2.01 V	1.99V
Q-4	W6-10	1040 mA	2.02 V	1.97 V
	W6-12	1048 mA	2 V	1.937 V
	W6-13	1052 mA	1.981 V	1.96 V

ATLASPix3.1 Quad Module GECCO Readout DAQ

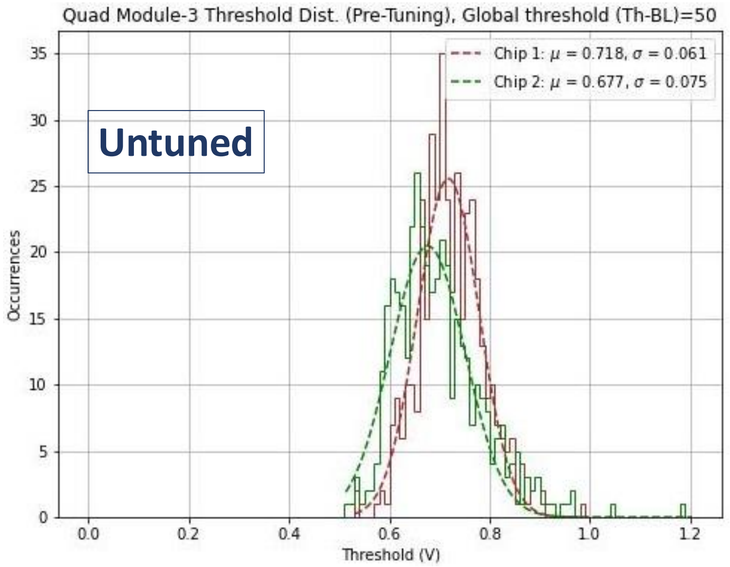


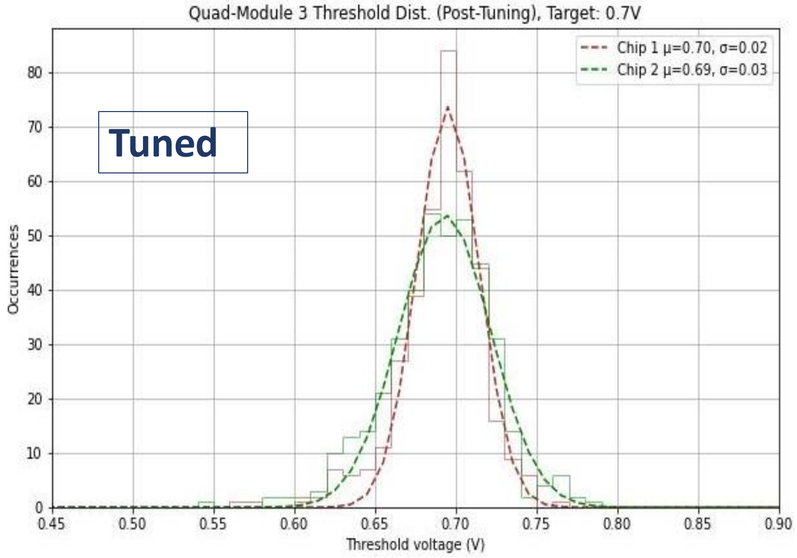
VDD33	**3.3V**
VDD18	**2.1V**
Current In for single chip	**~350-400mA**

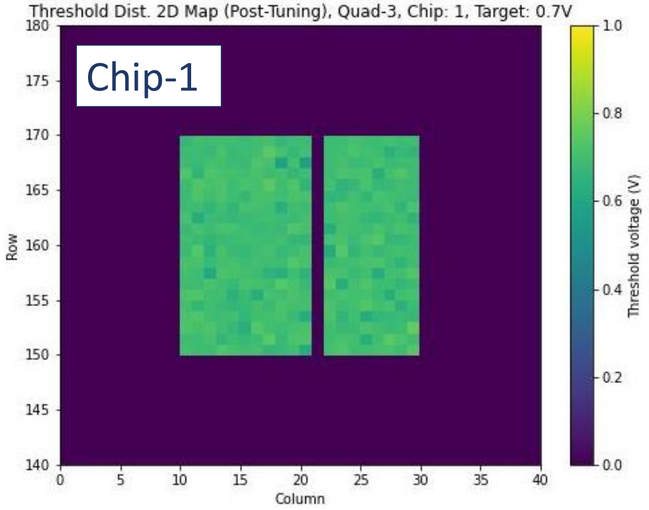
- **GECCO**, flexible readout system developed by **KIT**
- **Power adapter** is splitting the power domains.
- LVDSs (5x) are **decoupled** on flex.

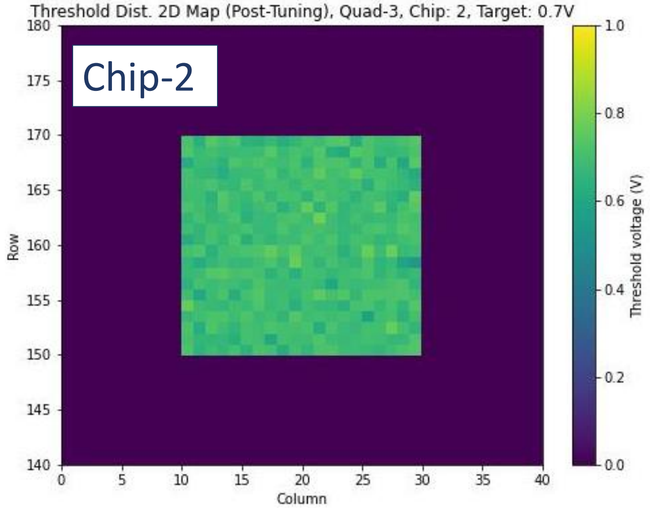
- **Firmware and software adapted for quad module operation**
- **CMD configuration** mode is used **at 160 MHz**.

Quad Module-3 Threshold Scan



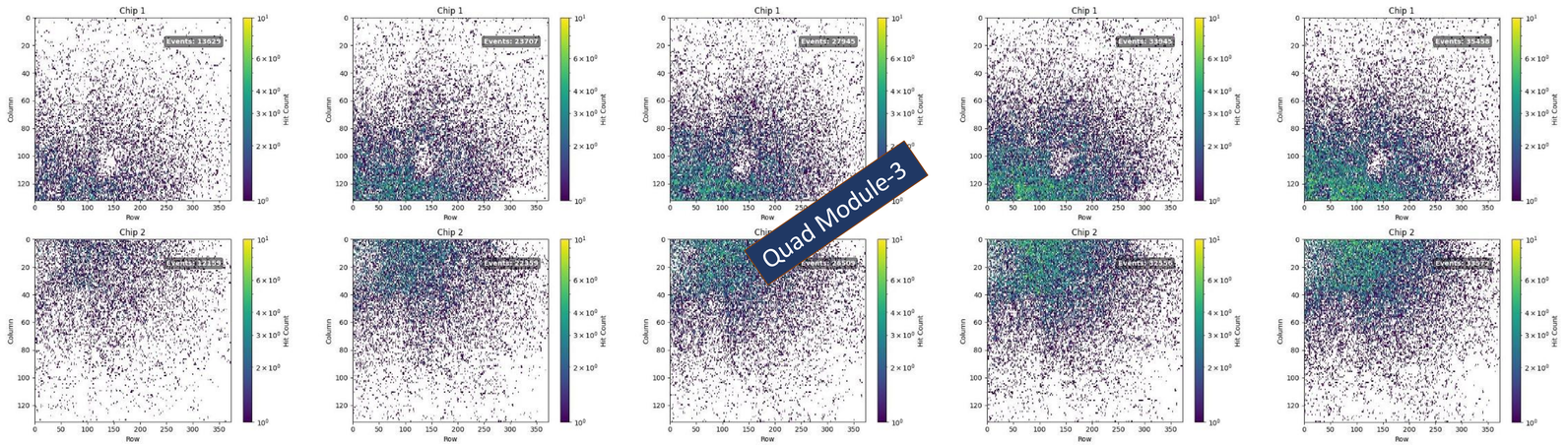


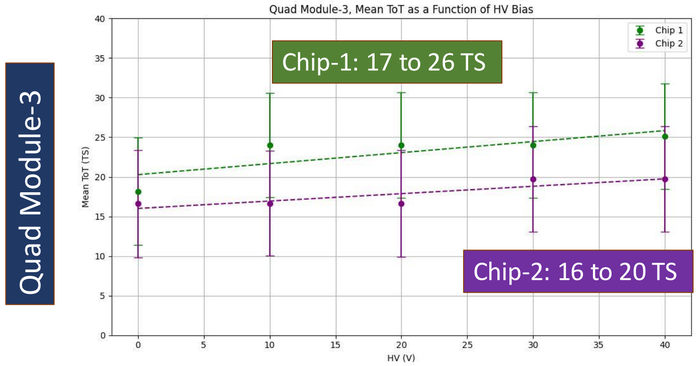


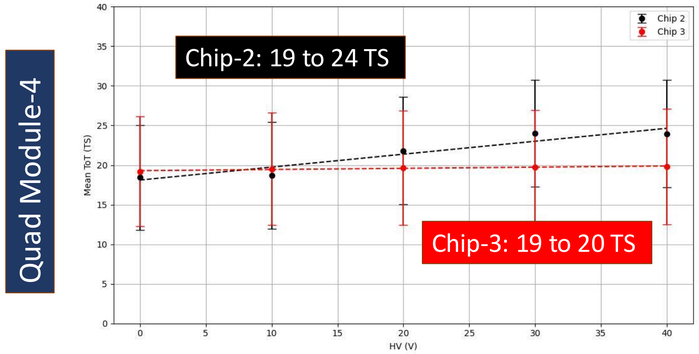


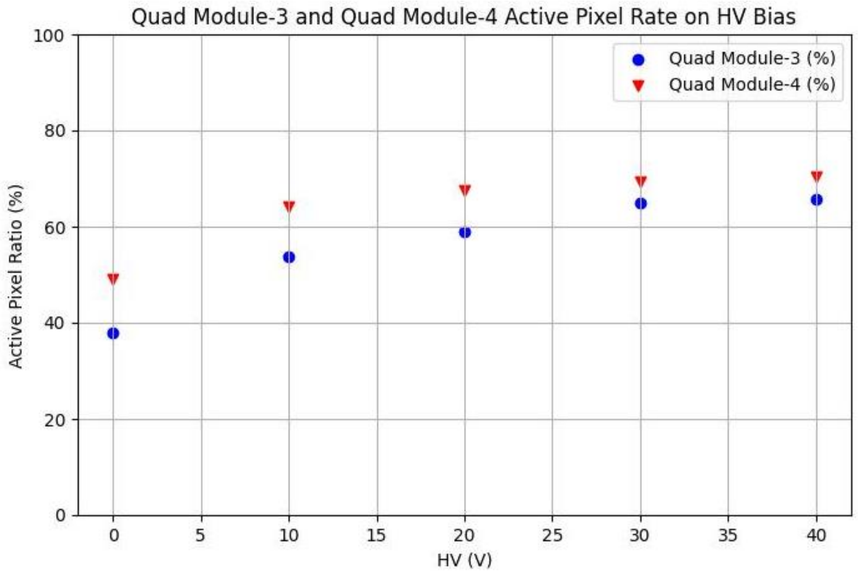
- **400** pixels are used. (10-29 / 150-169).
- **HV** is not applied.
- **TDAC=4**, and global threshold DAC is **175, for untuned scan**.
- Mean thresholds are **0.718V and 0.677V** for chip1 and 2, respectively.
- Same global threshold, different chip responses.
- Target threshold is **0.7 V for tuning**.

Quad Module-3 & 4 ^{90}Sr Measurement by HV



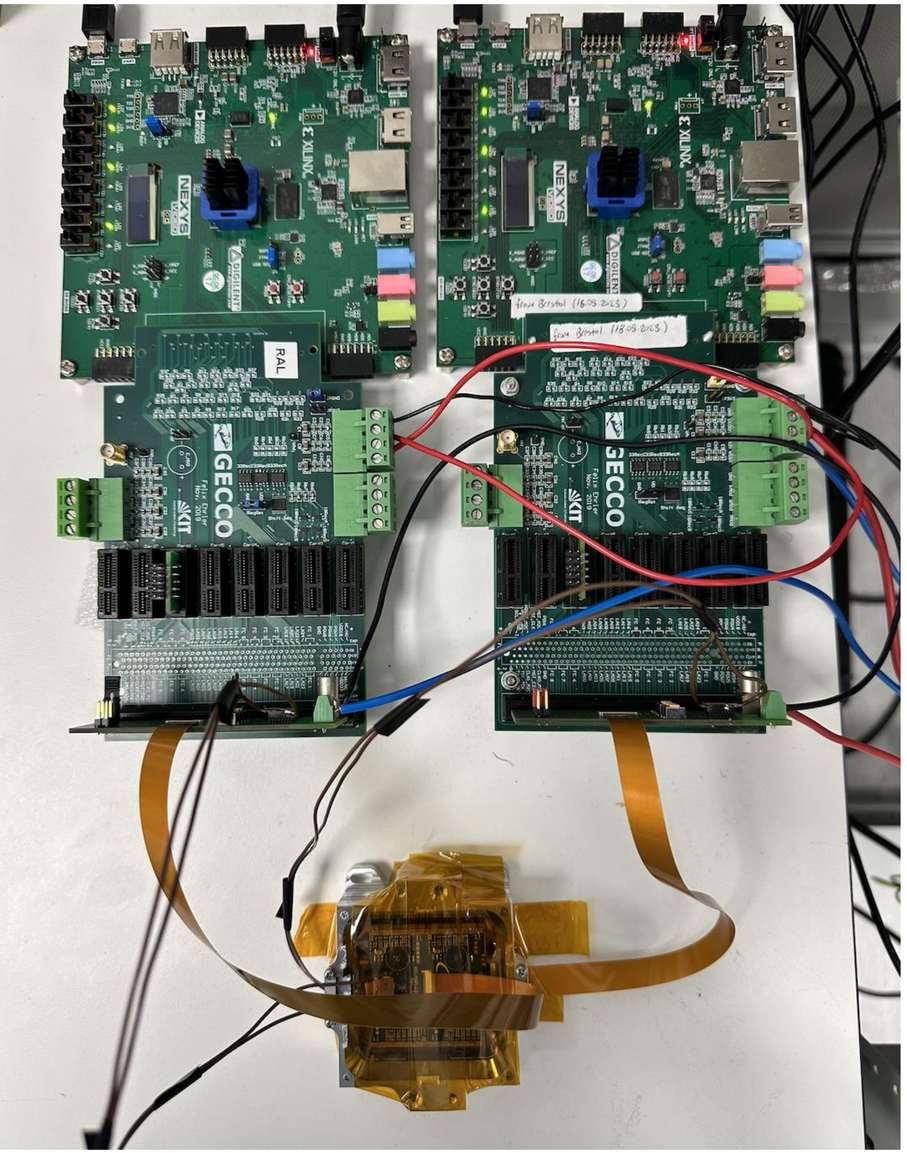


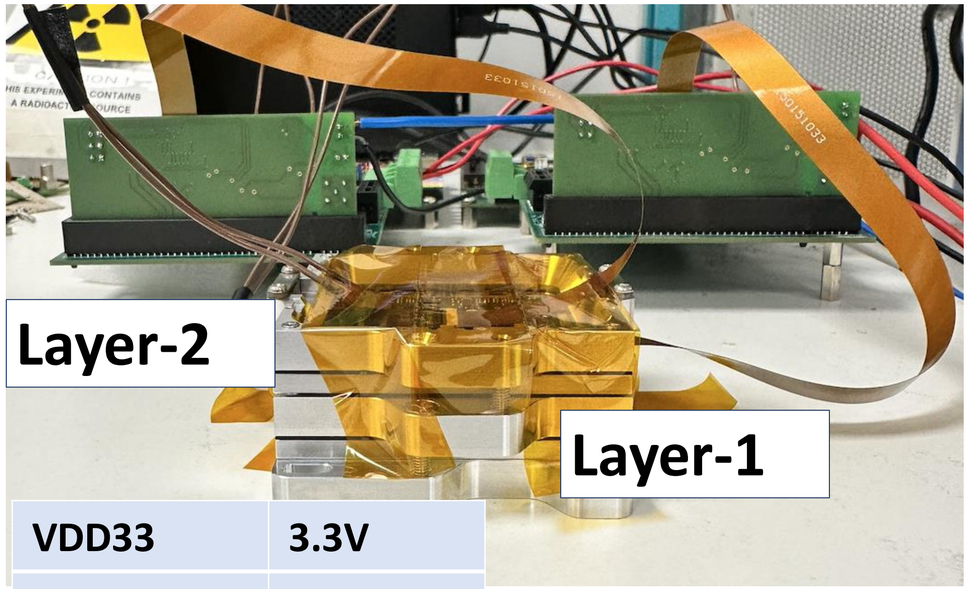




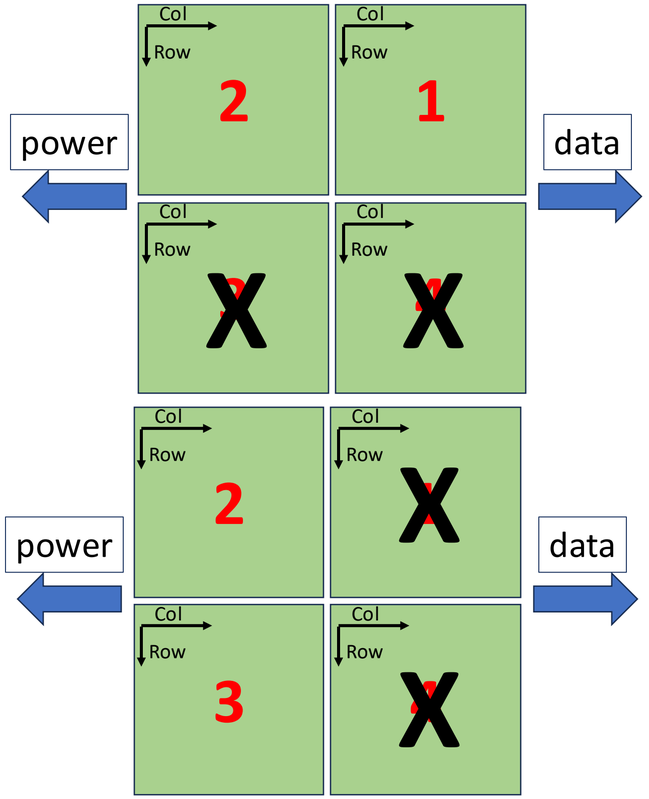
- Beta particles from ^{90}Sr.
- Global threshold is **175 DAC**.
- **TDAC is set 4** for all pixels.
- Increasing HV bias from **0V to -40V**.
- Increasing ToT by HV for both modules **(TS=25ns)**.
  - Quad Module-4 -> Chip3, does not show similar trend! (broken **SubsratePixel)**
- The total active pixel rate rises to just above **60% (Q3) & ~70% (Q4) at –20 V HV bias** and remains steady thereafter.

Readout of a SP chain (2 "Quad" Modules)





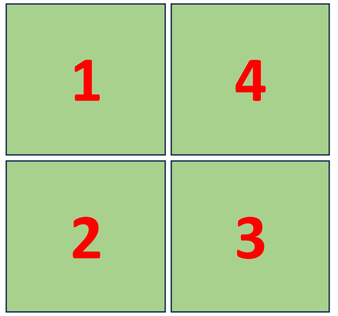
VDD33	3.3V
VDD18	2.1V
Current In	1.2A
Voltage	2.486V

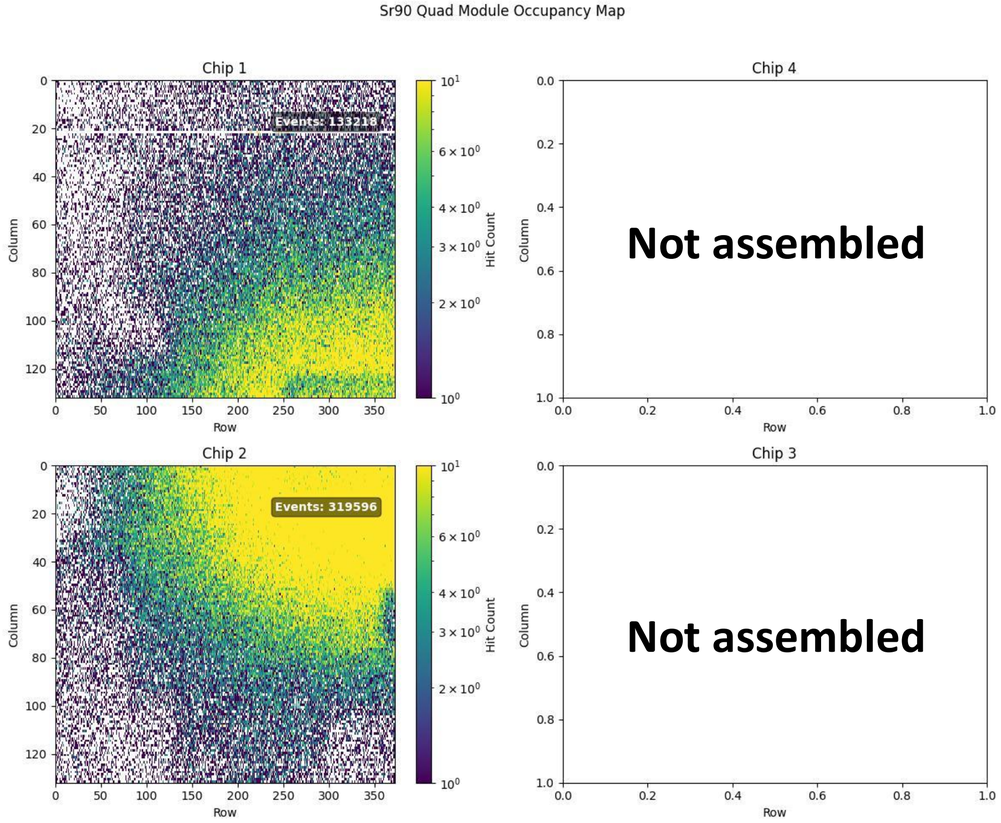


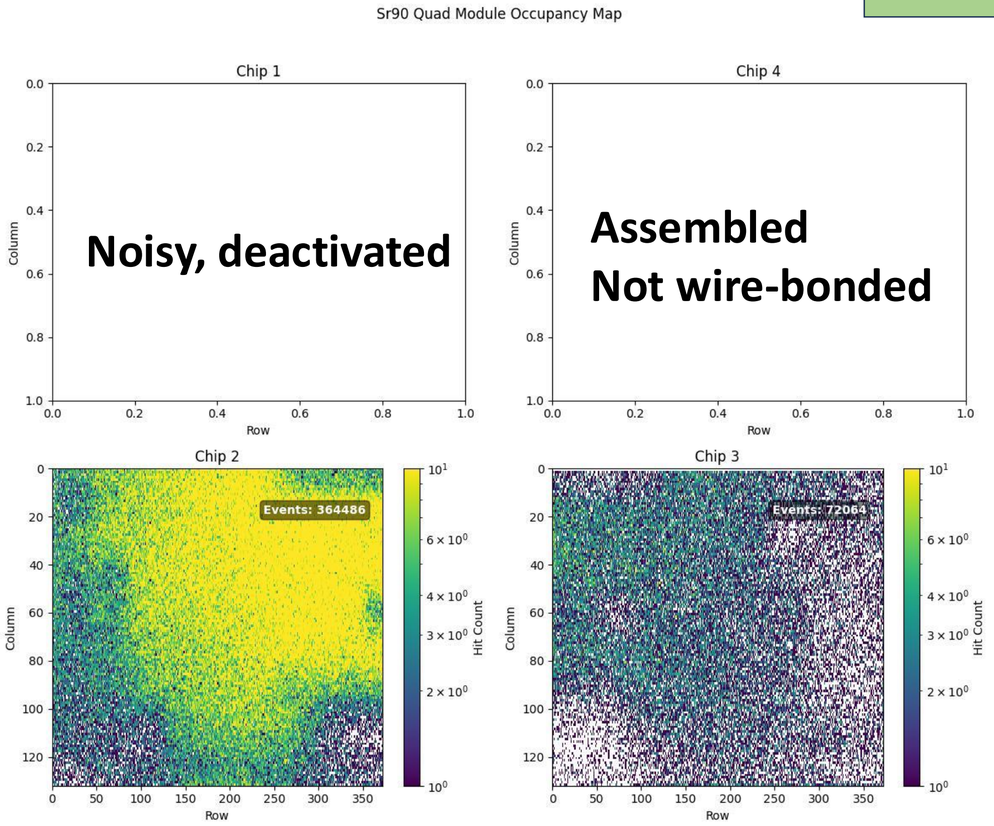
- **Two separate** GECCO DAQ, one for each quad, connected to 1 PC
- Modules are powered **serial** via power adapters.
- **Quad Module-4 (layer-1) and 3 (layer-2) are used**, chip-1 in Q4 is noisy and chip is masked.
- Two GUIs are run **simultaneously**
- **No synch** between the two

Simultaneous Source Scan (Quad 3 and 4)

- The simultaneous ^{90}Sr source scan both quad modules.
- The source located on the center of the Layer-2.
- The **HV=-20V** was applied. (**Layer-1, chip-3** has broken wire bond pad on **SubsratePixel**)
- Correlated occupancy map.







Layer-2

Layer-1

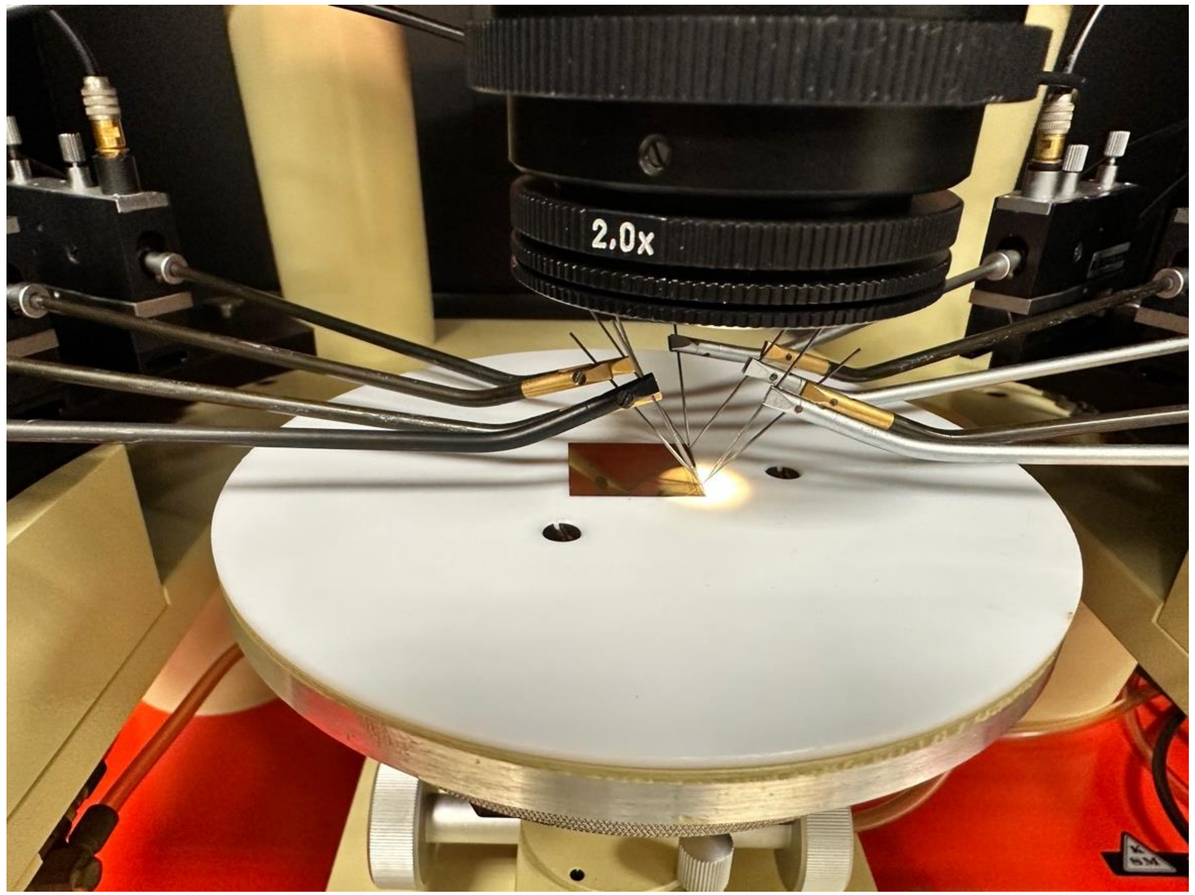
Conclusion and Next Steps

- Quad module assembly summary
  - 48 chips probed, 38 have functional IV/SLDO -> **74% "yield"**
  - 5 multi-chip modules are assembled in **Milan**
    - 3 are used in dedicated readout studies in Edinburgh
- Individual **HV bias and leakage current** tests. (breakdown voltage: **~-65 V**)
- The shunt-LDO regulator IV performances are tested and verified in three different configurations:
  - **Bare chip level using probe stations**
  - **Multi-chip module level** (not included in this talk)
  - **In the multi-module serial powering chain (with three modules).**
- Commissioned a working GECCO based setup to simultaneous readout a SP chain of two modules
  - **Threshold and noise scans, source measurements (occupancy, ToT)**
- Designed a power bus to test a multi-module serial power chain.
- **Plans:**
  - **Expand SP setup to include more chips/modules** to test shunt-LDO performance.
  - Multiple readout with up to **three modules** by **current GECCO setup.**
  - Production of multi-chip power bus and its SP tests.

Backup

Chip Probe Testing

- Probe testing, at the individual chip level, is a key step in semiconductor manufacturing.
- Evaluates functionality and quality of individual ICs while still on the wafer.
- **Temporary electrical contact is made with test pads or contact points on each chip.**
- Electrical signals are sent through the probes.
- Aims:
  - Test electrical behaviour of **regulators**
  - Identify **potential defects and contaminations**



Probe Testing Setup at Milan

VDDA2 in, Pad-104

GNDD, Pad-116

VDDA2 out, Pad-106

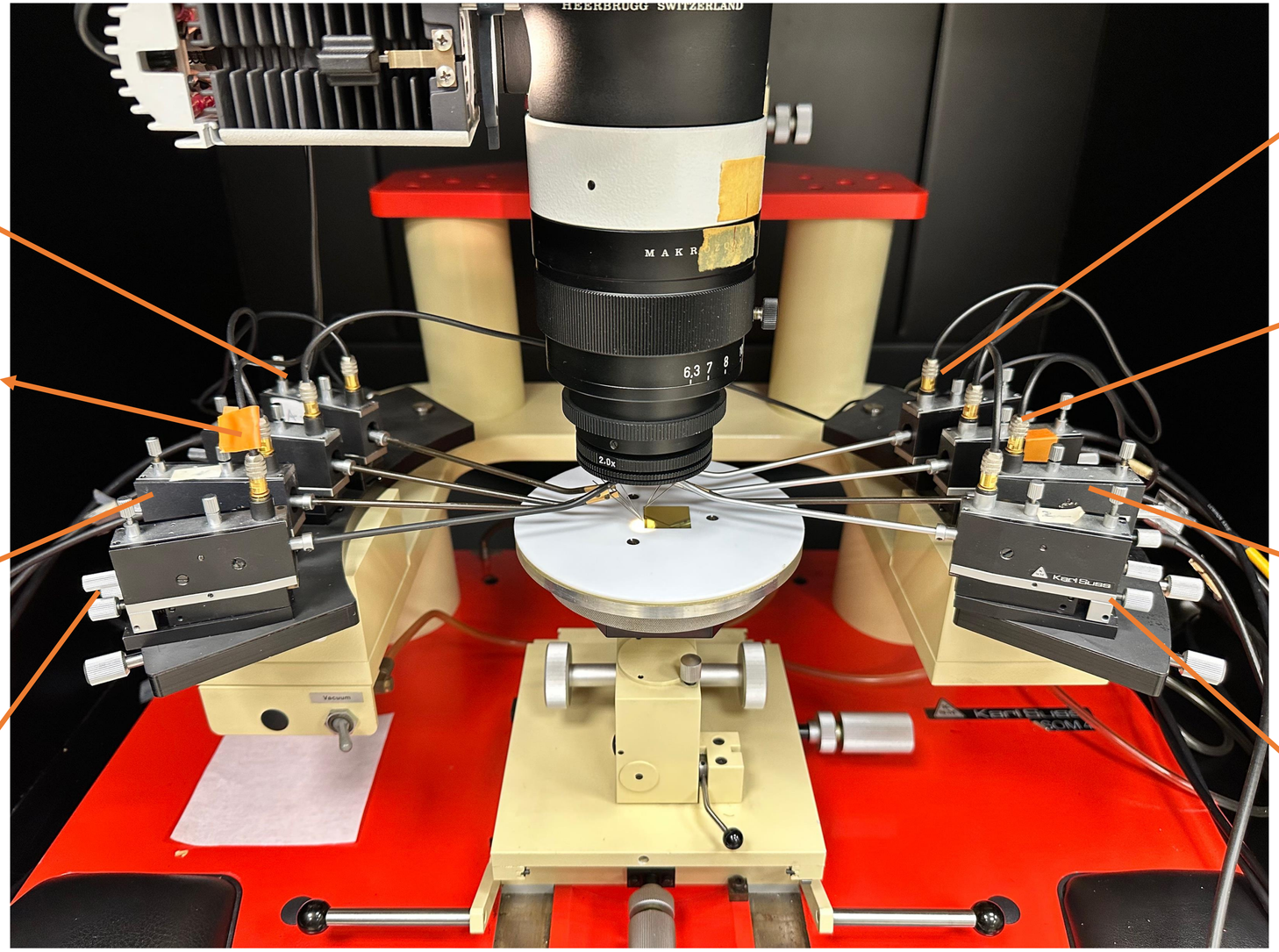
VDDD2 in, Pad-117

Vina2, Pad-108

VDDD2 out, Pad-118

GNDA, Pad-110

Vind2, Pad-119



VDDA1 in, Pad-24

GNDD, Pad-39

VDDA1 out, Pad-26

VDDD2 in, Pad-40

Vina1, Pad-28

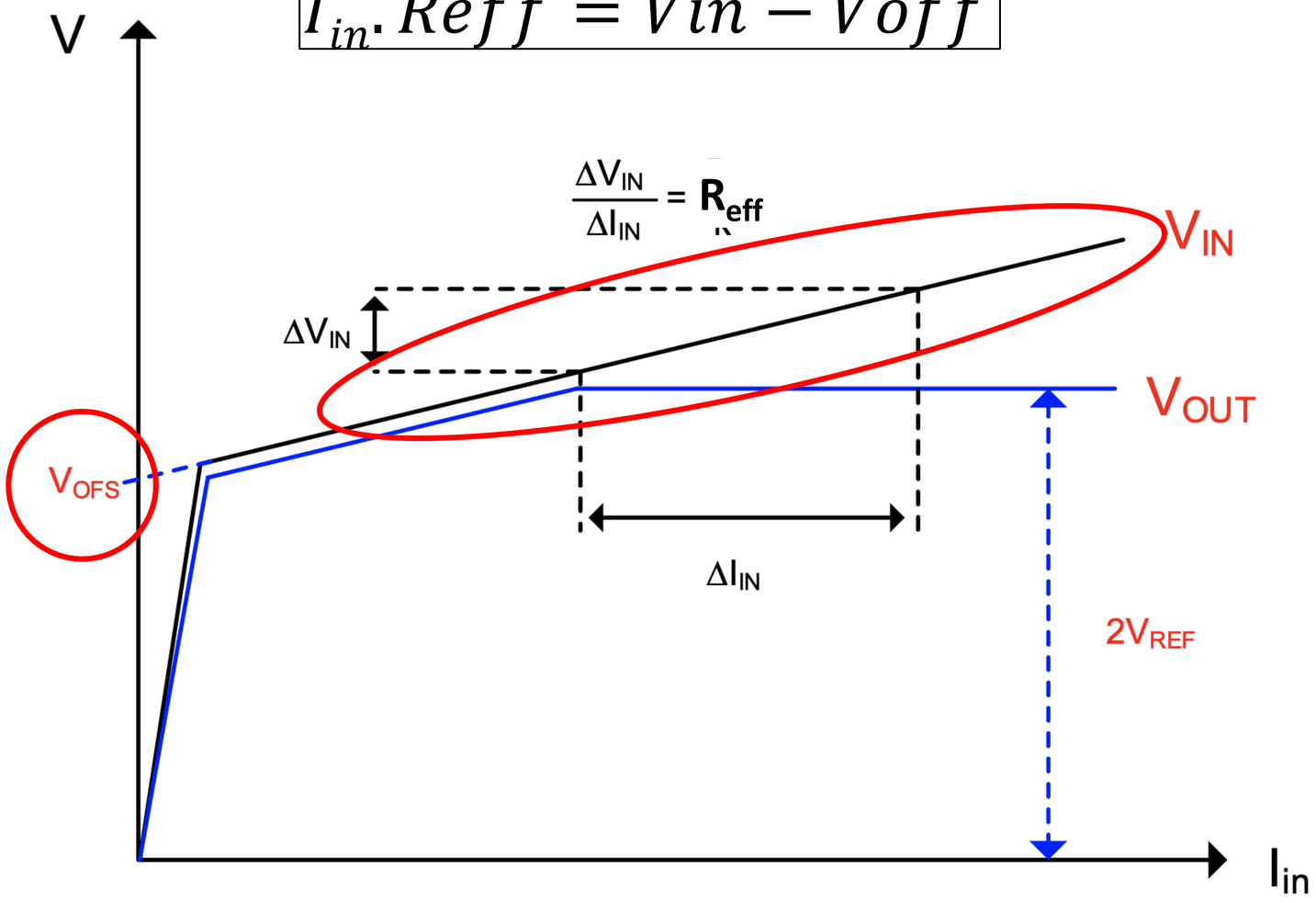
VDDD2 out, Pad-41

GNDA, Pad-30

Vind2, Pad-42

Shunt-LDO Characterisation

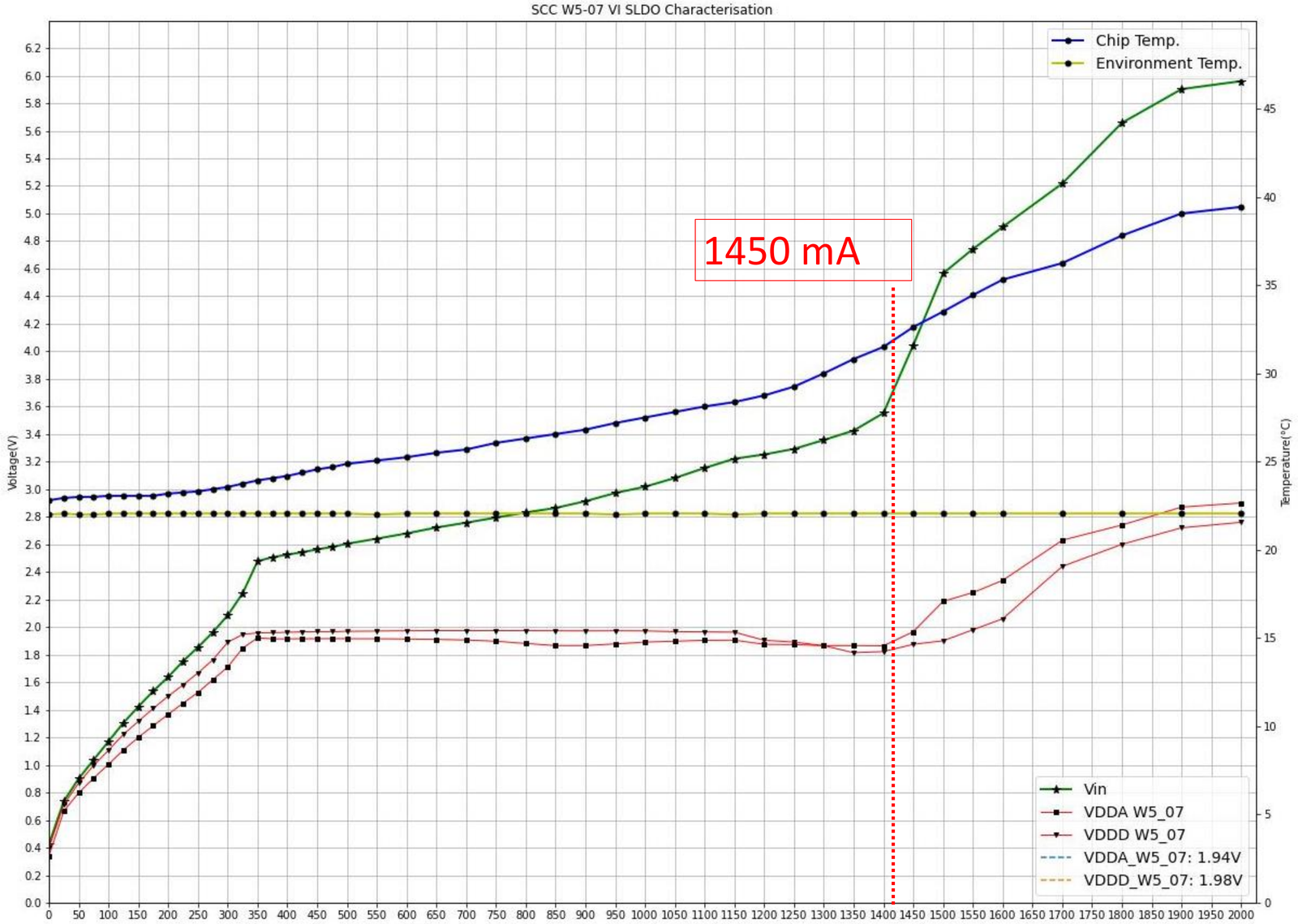
$$I_{in}.Reff = Vin - Voff$$



- The slope of the V_{in} gives the effective resistance value.
- **R_{eff}**: a small-signal parameter represents the dynamic behaviour of the shunt regulator. Also called, **parasitic resistance, and input impedance of the regulators.**
  (https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8950368, Characterization and verification of the Shunt-LDO regulator and its protection circuits for serial powering of the ATLAS and CMS pixel detectors)
- Impacts load regulation, which is the regulator's ability to maintain a constant output voltage. Lower R_{eff}, better load regulation.
- **V_{OFS}**: defines the minimum input voltage at which the regulator begins to operate correctly.

https://indico.cern.ch/event/72160/attachments/1036621/1477145/Shunt-LDO_Regulator.pdf

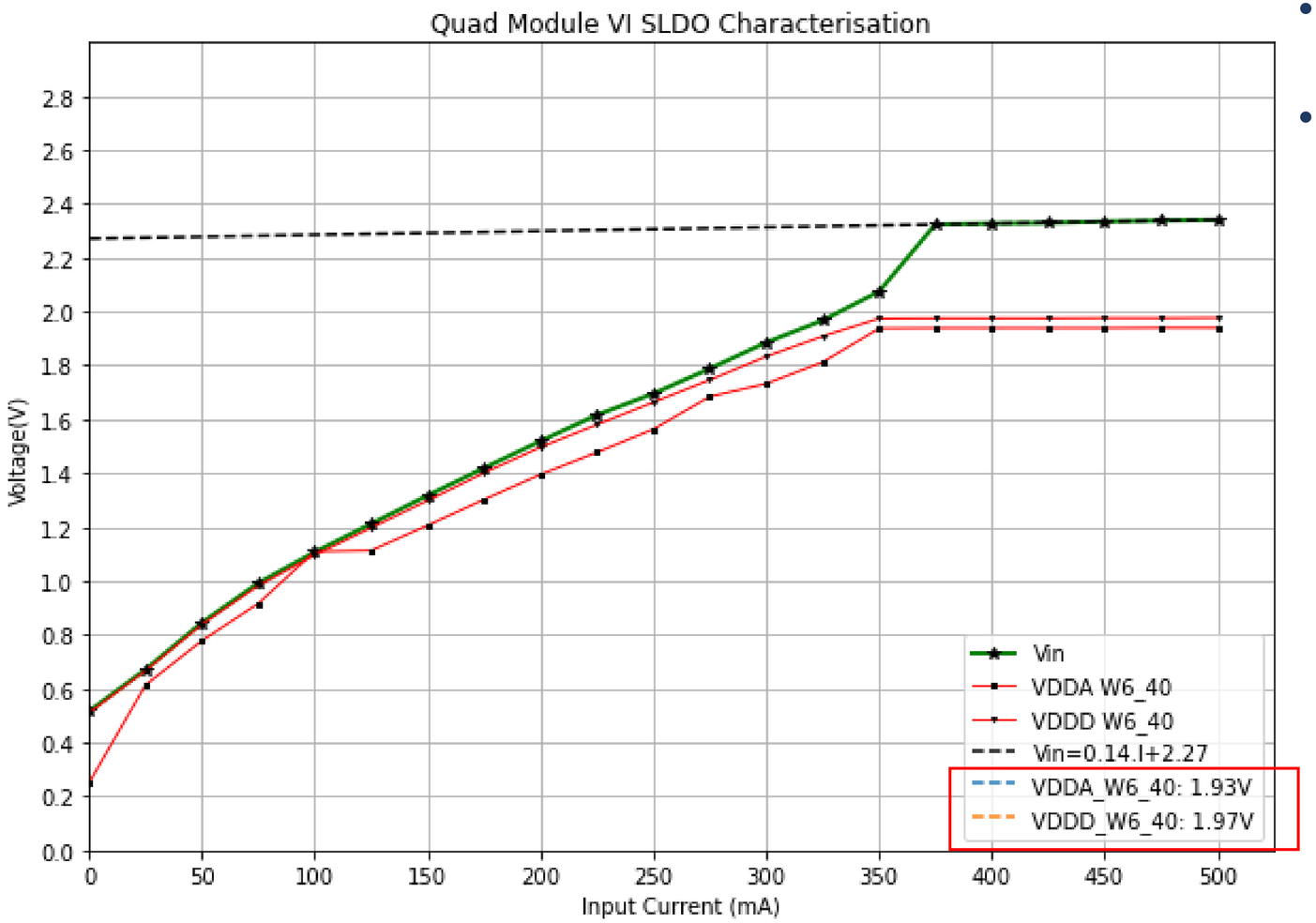
Single-Chip SLDO IV Stress Test



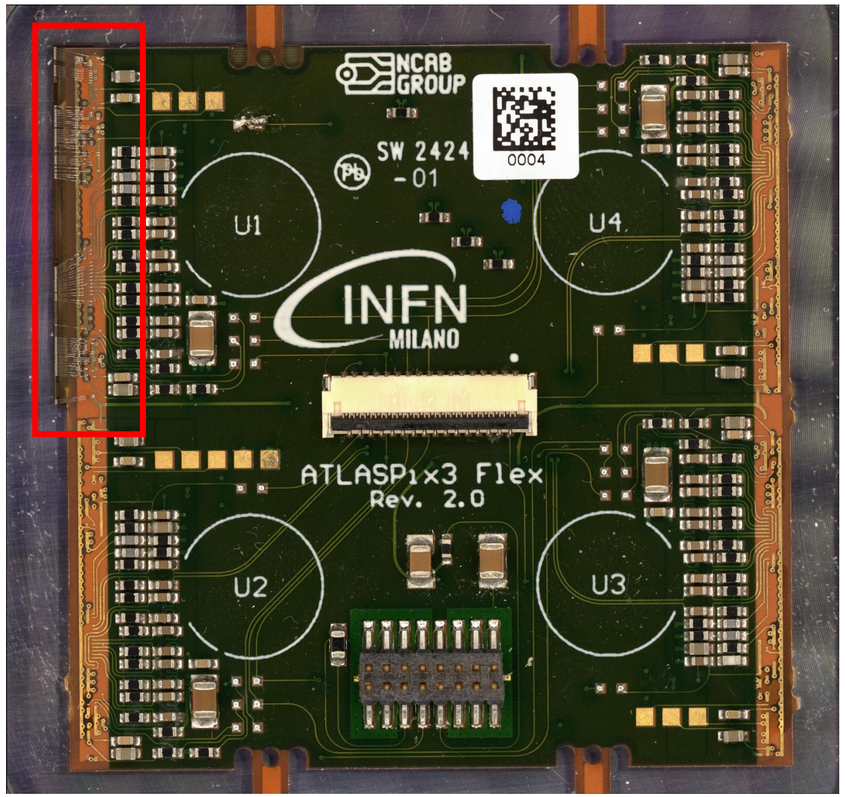
- Single chip operation current is **~350mA-400mA**
- Stress test SLDO to **2A** (expected value of a **5-chips.**)
- Stable regulated output
  - VDDD: 1.98V
  - VDDA: 1.94V
- Both VDDD/A SLDO breaks down at **~1450mA**
  - **(~4 times single chip op. point)**
- Linear increase in the chip temperature (measured on the plastic cover)

Quad Module-2

- The quad module-1 includes one wirebonded chip. The chip **is W6-40**, does not have a probing test results.
- The input current is **349 mA** as the regulation starts.

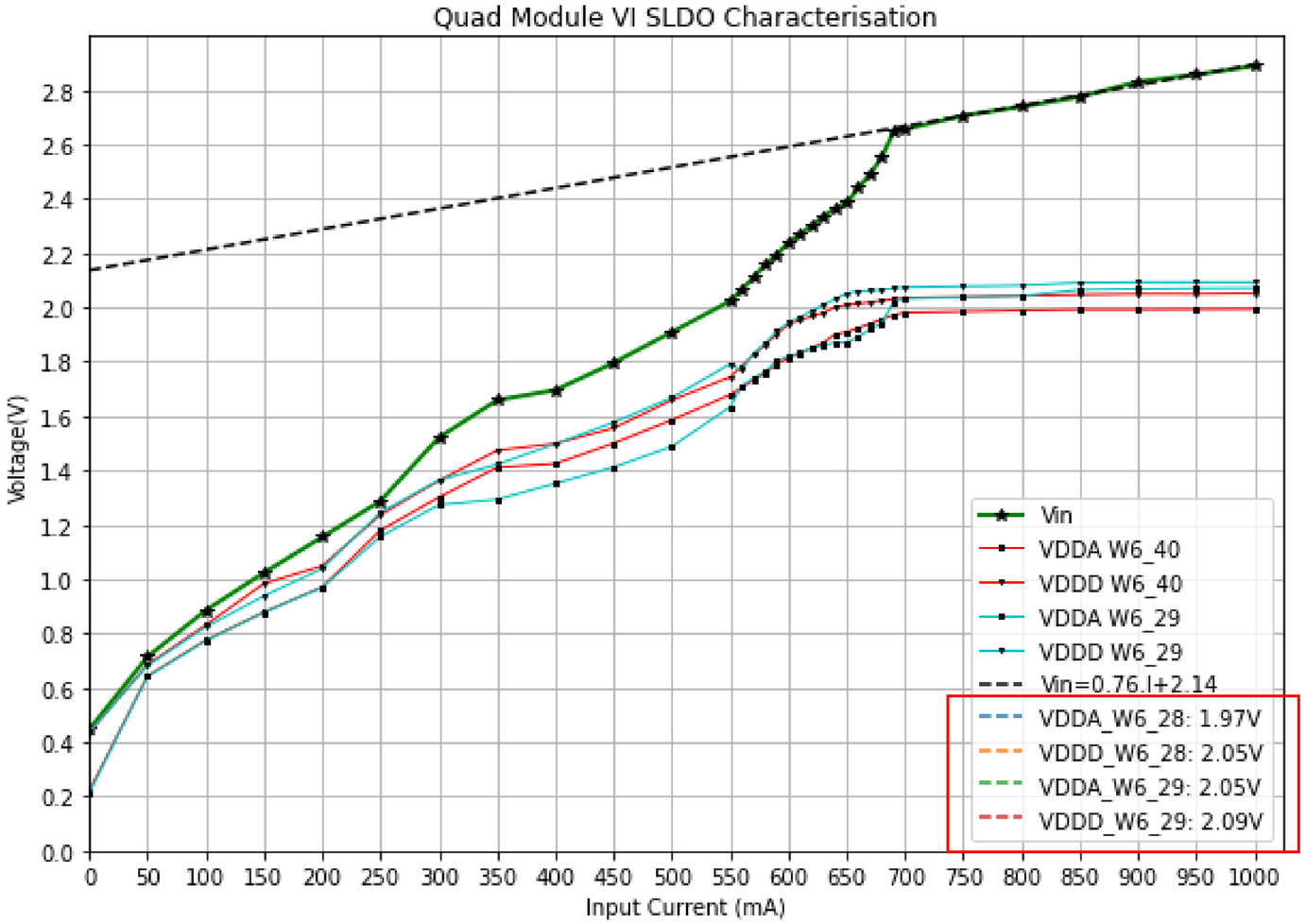


- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) **2.27 V.**
- **Parasitic** resistance is **0.14 Ohm**.

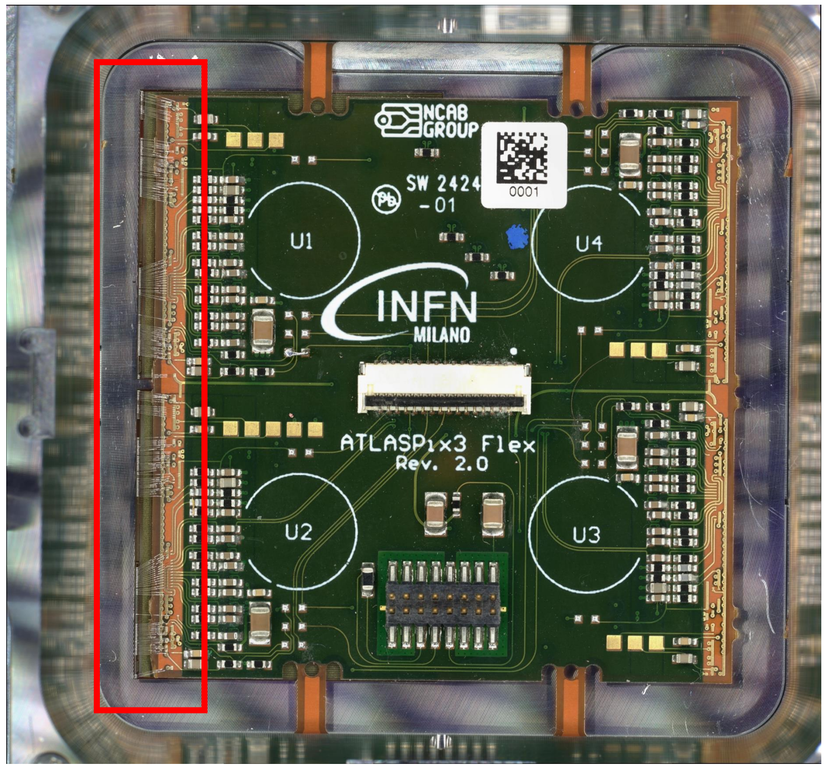


Quad Module-3

- The quad module-2 includes two wirebonded chip. The chips are **W6-28 and W6-29.**
- The input currents change between **640.75 mA and 703.96mA** as the regulation starts for each regulators on the chips.

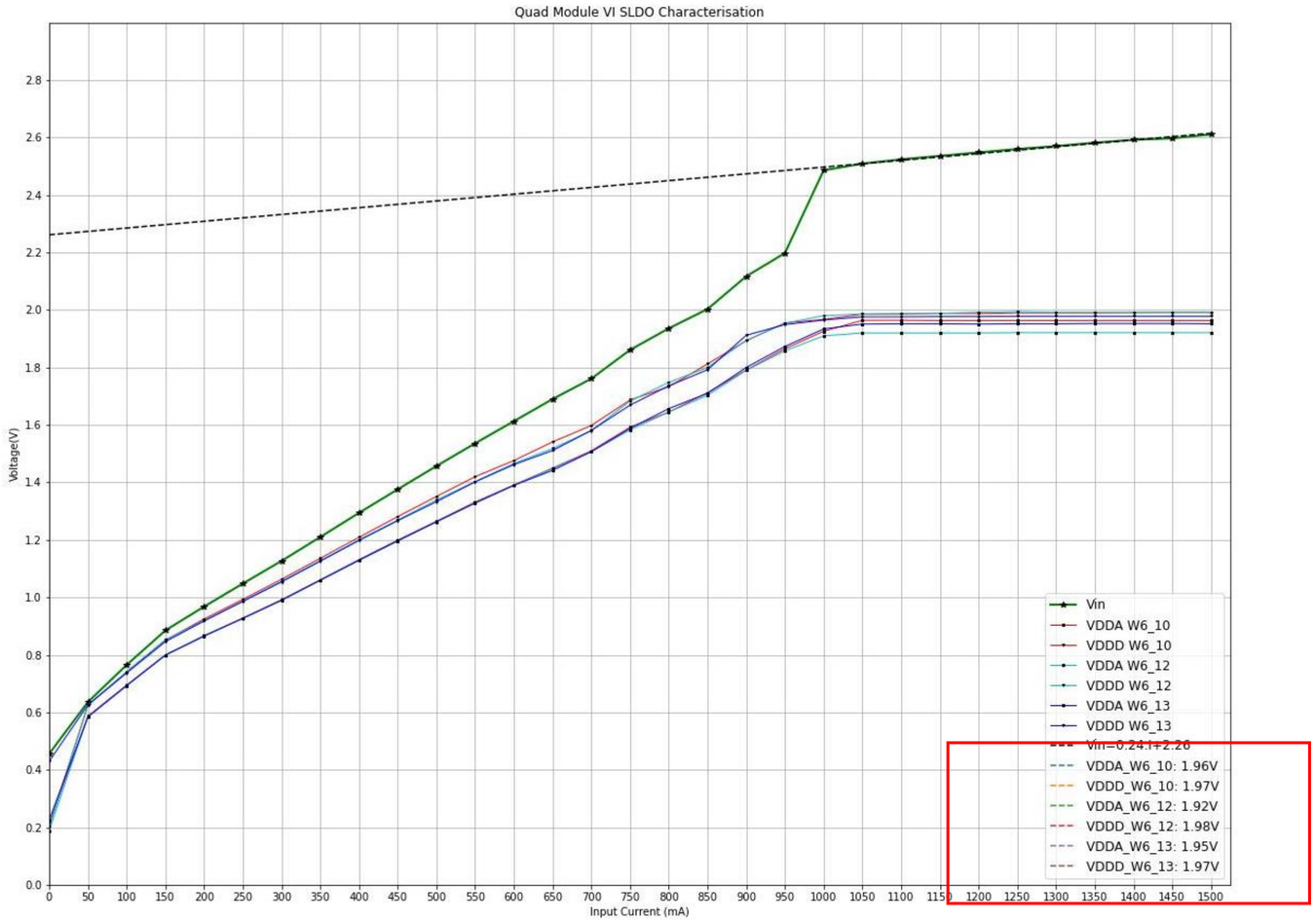


- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) is **2.14V.**
- **Parasitic** resistance is **0.76 Ohm**.

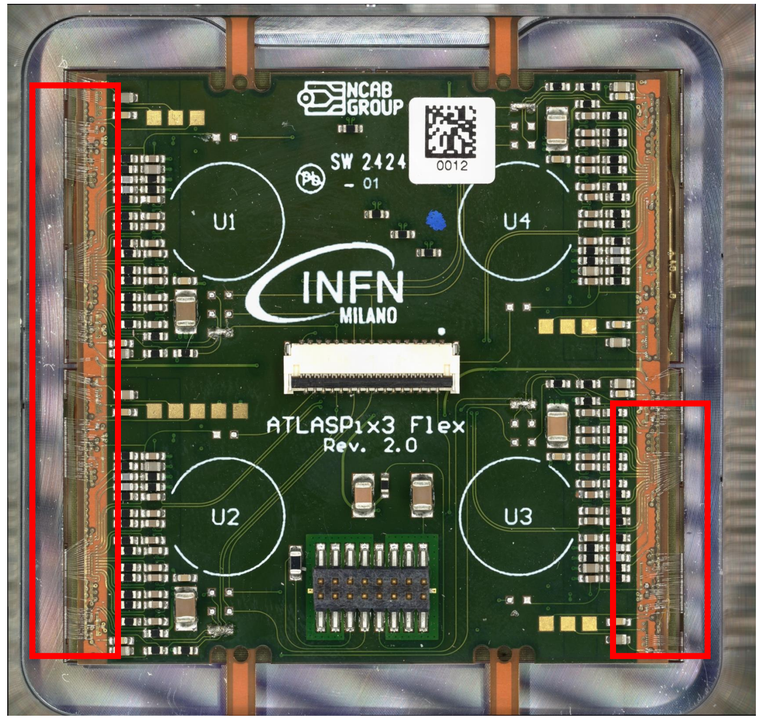


Quad Module-4

- The quad module-4 includes three wirebonded chip. The chips are **W6-10, W6-12 and W6-13.**
- The input currents change between **1 A and 1.2 A** as the regulation starts for each regulators on the chips.



- Ohmic behaviour is seen after regulation starts.
- V_{offset} (the minimum required voltage to run the regulators) is **2.26 V.**
- **Parasitic** resistance is **0.24 Ohm**.



ATLASPix3.1 Quad Module Readout