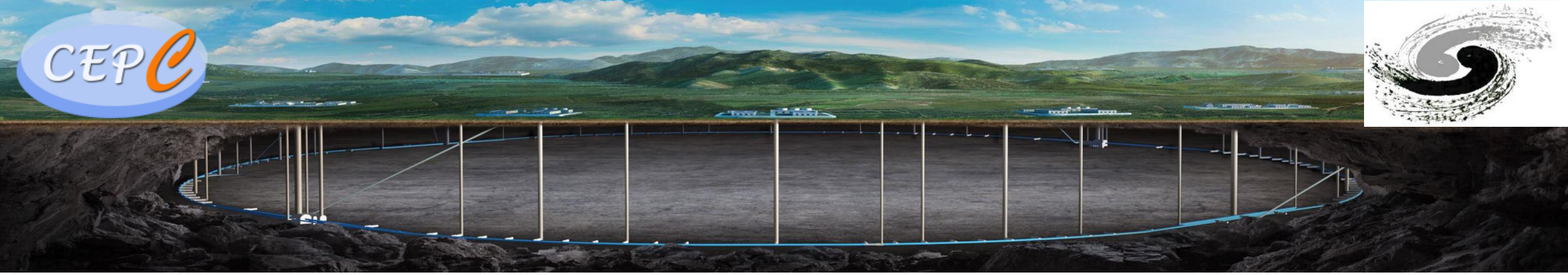


L1 trigger design progress on CEPC ref-Detector TDR

Jingzhou ZHAO

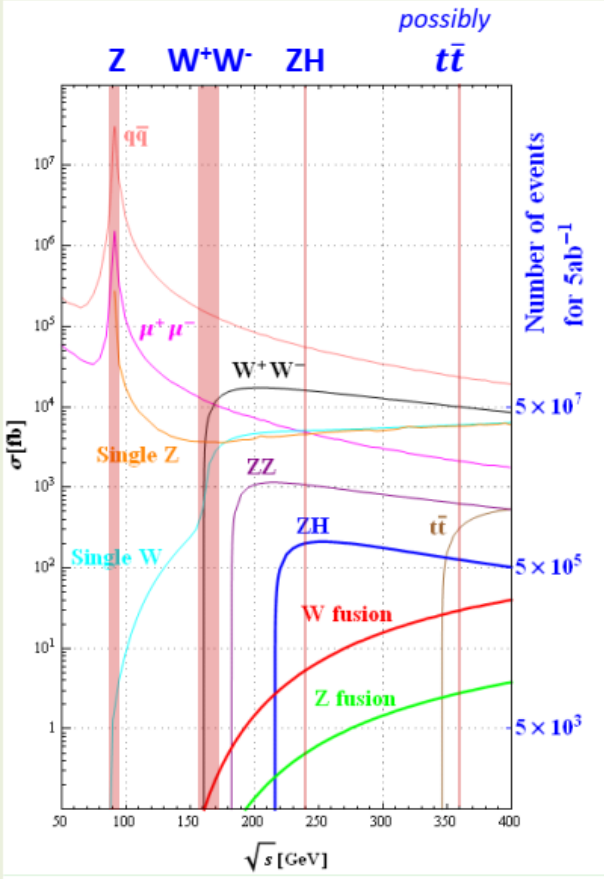
IHEP, Beijing
On behalf of CEPC TDAQ Group

Content

- Introduction
- Requirements
- TDAQ structure
- L1 trigger design
- R&D progress on Trigger board
- Summary

Introduction

- The CEPC is designed to operate at center of mass energies that scale from the Z-pole at 91 GeV to WW at 160 GeV, ZH at 240 GeV, and up to $t\bar{t}$ at 360 GeV.
- The project employs a two phase operational strategy – baseline and upgraded – to accelerate its readiness and maximize its scientific output.



Baseline operation plan

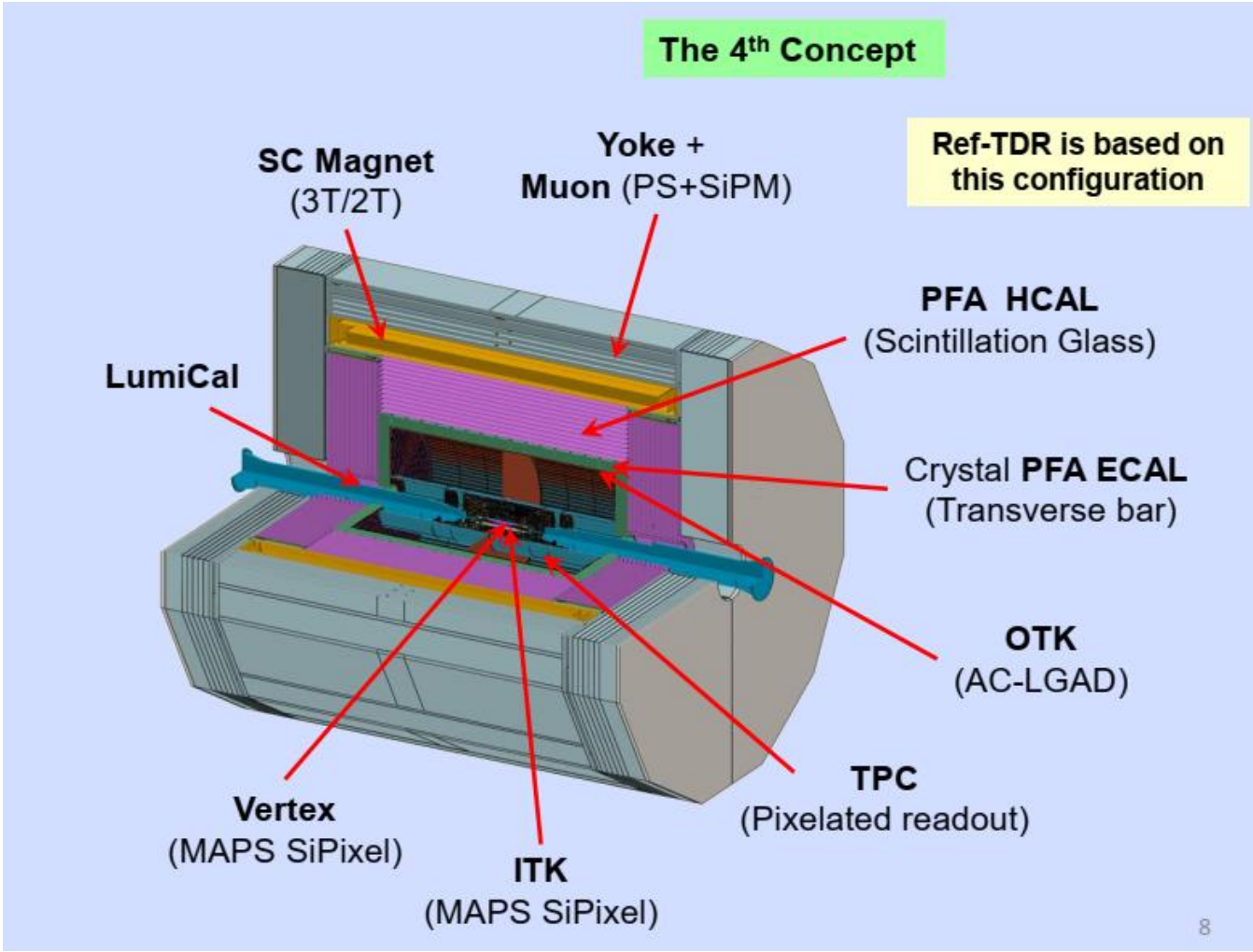
Operation mode	$\sqrt{s}$ (GeV)	SR power (MW)	$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	$\int \mathcal{L}$/year (ab^{-1})	Years	Total $\int \mathcal{L}$ (ab^{-1})	Event yields
H	240	30	5	0.65	15	10	2.0×10^6
Z	91	12.1	26(*)	3.2	4	13	5.6×10^{11}
W^+W^-	155-170	30	16	1.2	1	1.2	1.0×10^7(†)

Upgrade operation plan

Operation mode	$\sqrt{s}$ (GeV)	SR power (MW)	$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	$\int \mathcal{L}$/year (ab^{-1}, 2 IPs)	Years	Total $\int \mathcal{L}$ (ab^{-1}, 2 IPs)	Event yields
H	240	50	8.3	2.2	10	21.6	4.3×10^6
Z	91	50	192(*)	50	2	100	4.1×10^{12}
W^+W^-	155-170	50	26.7	6.9	1	6.9	5.5×10^7
$t\bar{t}$	360	50	0.8	0.2	5	1.0	0.6×10^6

Detector introduction

- From innermost to outer (ref-TDR baseline option)
  - Vertex
    - 4 single side layers + 1 double sides layer
  - ITK
    - ITKB 3 layers; ITKE 4 layers
  - TPC
    - Maximum drift time: 34us
  - OTK
    - 50 ps for TOF
  - ECAL
    - Barrel:480 modules,
    - Endcap: 224 modules
  - HCAL
    - Barrel/Endcap:16 sectors,48 layers,
  - Muon
    - 6 super layers



Physical Event Rate

- Physical Event Rate
  - ~500Hz @ Higgs (50MW)
  - ~10 kHz @ Low lumi Z (12.1MW)
  - ~77KHz @ High lumi Z(50 MW)
- Trigger aim is to keep physical events as more as possible
  - By a rough selection of the relevant objects (jet, e, muon, tau,v, ...) and their combinations.
  - Based on particle features: energy, cluster, track and time relation

Table 12.1: Expected Standard Model processes event rate at the Higgs mode for 50 MW.

Higgs mode processes	Cross section (fb)	Event rate (Hz)
Physical events (top priority)		
Higgs production	203.7	0.017
Two Fermions processes (exclude Bhabha)	6.4×10^4	5.3
Four Fermions processes	1.9×10^4	1.6
Bhabha	1.0×10^6	80
Diphoton process (low priority)		
$\gamma\gamma \to b\bar{b}$	1.6×10^6	136
$\gamma\gamma \to c\bar{c}$	2.1×10^6	173
$\gamma\gamma \to q\bar{q}$	6.0×10^7	4963
$\gamma\gamma \to \mu^+\mu^-$	2.1×10^8	17210
$\gamma\gamma \to \tau^+\tau^-$	2.3×10^6	193

Table 12.2: Expected Standard Model processes event rate at the Z mode for 12.1 MW.

Z mode processes	Cross section (fb)	Event rate (Hz)
Physical events (top priority)		
$q\bar{q}$	3.1×10^7	7970
$\mu^+\mu^-$	1.5×10^6	400
$\tau^+\tau^-$	1.5×10^6	396
Bhabha	6.6×10^6	1714
Diphoton process (low priority)		
$\gamma\gamma \to b\bar{b}$	2.7×10^5	71
$\gamma\gamma \to c\bar{c}$	5.1×10^5	132
$\gamma\gamma \to q\bar{q}$	3.5×10^7	9014
$\gamma\gamma \to \mu^+\mu^-$	1.3×10^8	33696
$\gamma\gamma \to \tau^+\tau^-$	6.3×10^5	163

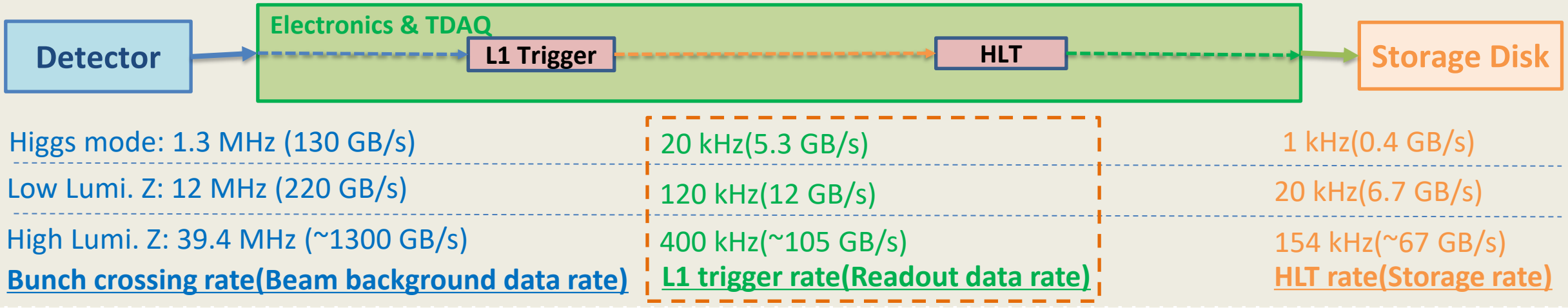
Raw Data Rate and Event Size

- Raw data rate and event size with better beam BG control (noise not considered yet)
  - Readout time windows
    - TPC 34 us , Hcal 1 us
    - Other detectors: 69 ns
  - Raw event size
    - 405/333/1824 Kbytes
    - TPC portion: 76%/92%/91%
  - Full raw data rate 130~1300 GB/s
    - 130 GB/s(1040Gbps)@Higgs
    - 220GB/s(1771Gbps)@low lumi. Z
    - ~1300GB/s@High lumi. Z

	VTX	ITK	OTK	TPC	ECAL	HCAL	Muon	Total
Time windows (ns)	69	69	69	34000	69	1000	69	
50 MW Higgs mode Full Data (Gbps)	130	21.2	82.7	26.4	752	26.6	<1	1040
Data size / bunch (kB)	12.1	1.98	7.71	2.46	70.1	2.48	<0.1	96.9
Data size / event (kB)	12.1	1.98	7.71	303	70.1	9.92	<0.1	405
12.1 MW Z mode Full Data (Gbps)	307	37.8	139	57.1	1202	27.2	<1	1771
Data size / bunch (kB)	3.20	0.394	1.45	0.595	12.5	0.283	<0.1	18.4
Data size / event (kB)	6.40	0.788	2.90	293	25.0	4.53	<0.1	333

Table 12.3 in TDR

Estimation of Trigger and Data Rate



- L1 trigger rate
  - Expect to reduce beam BG to <1% of BX rate
- HLT rate
  - Expect to reduce beam BG to <0.1%
  - Expect to reduce event size by ROI
- DAQ data storage volume(two weeks)
  - 0.48 PB@ Higgs, 8 PB@ Low L. Z

Running mode SR power	Higgs 50 MW	Z 12.1 MW
Non-empty bunch crossing rate(MHz)	1.34	12
Luminosity ($10^{34}/cm^2/s$)	8.3	26
Physical event rate (kHz)	0.5	10
L1 triger rate (kHz)	20	120
DAQ readout rate (Gbyte/s)	5.34	11.9
HLT rate (kHz)	1	20
Raw event size (kbyte)	405	333
DAQ storage rate (Gbyte/s)	0.405	6.66

Table 12.4 in TDR

TDAQ structure

- Electronics framework schema
  - Transmit full raw data from Front-End Elec. to Back-End Elec.(BEE)
  - Trigger connect with Back-End Elec.
- Trigger solutions
  - Hardware trigger(L1) + high level trigger(HLT)
    - A single type of common hardware trigger board
      - Collect trigger primitives from BEE common boards
      - Send back trigger accept signal to BEE
    - Provide fast and normal trigger menu
    - Network readout

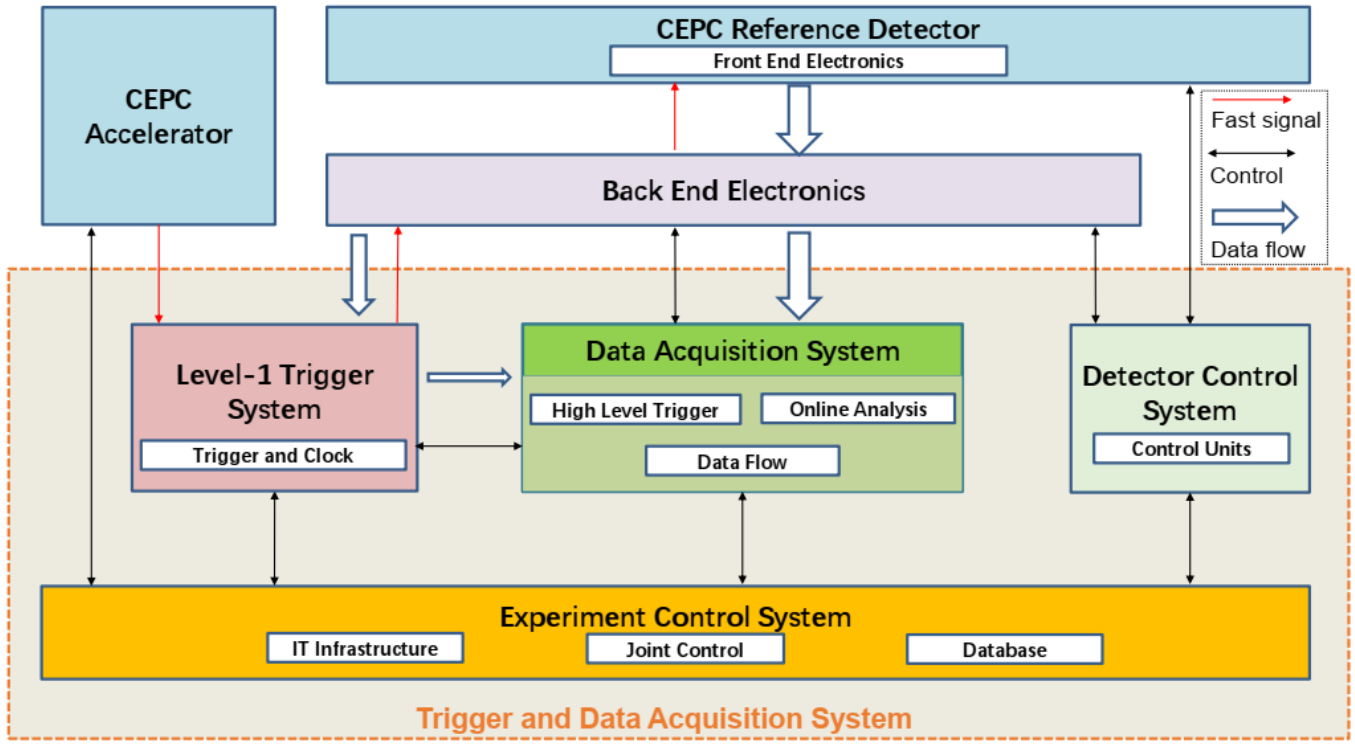


Figure 12.1: Overall structure of TDAQ and Online system for Reference Detector

Hardware Trigger Structure

- Ecal+Hcal+Muon is baseline for L1 trigger
- VTX, ITK, TPC, OTK and LumiCal are optionals for L1 trigger depends on requirement
- Trigger primitive(TP)
  - Extracted by BEE
- Local detector trigger
  - Sub energy and tracking…
- Global trigger
  - E-sum and tracking
  - Fast trigger(FT) and L1A generation on demand
- TCDS (Trigger Clock Distribution System)
  - Distribute clock and fast control signals to BEE

Trigger Simulation please see Boping Chen's report

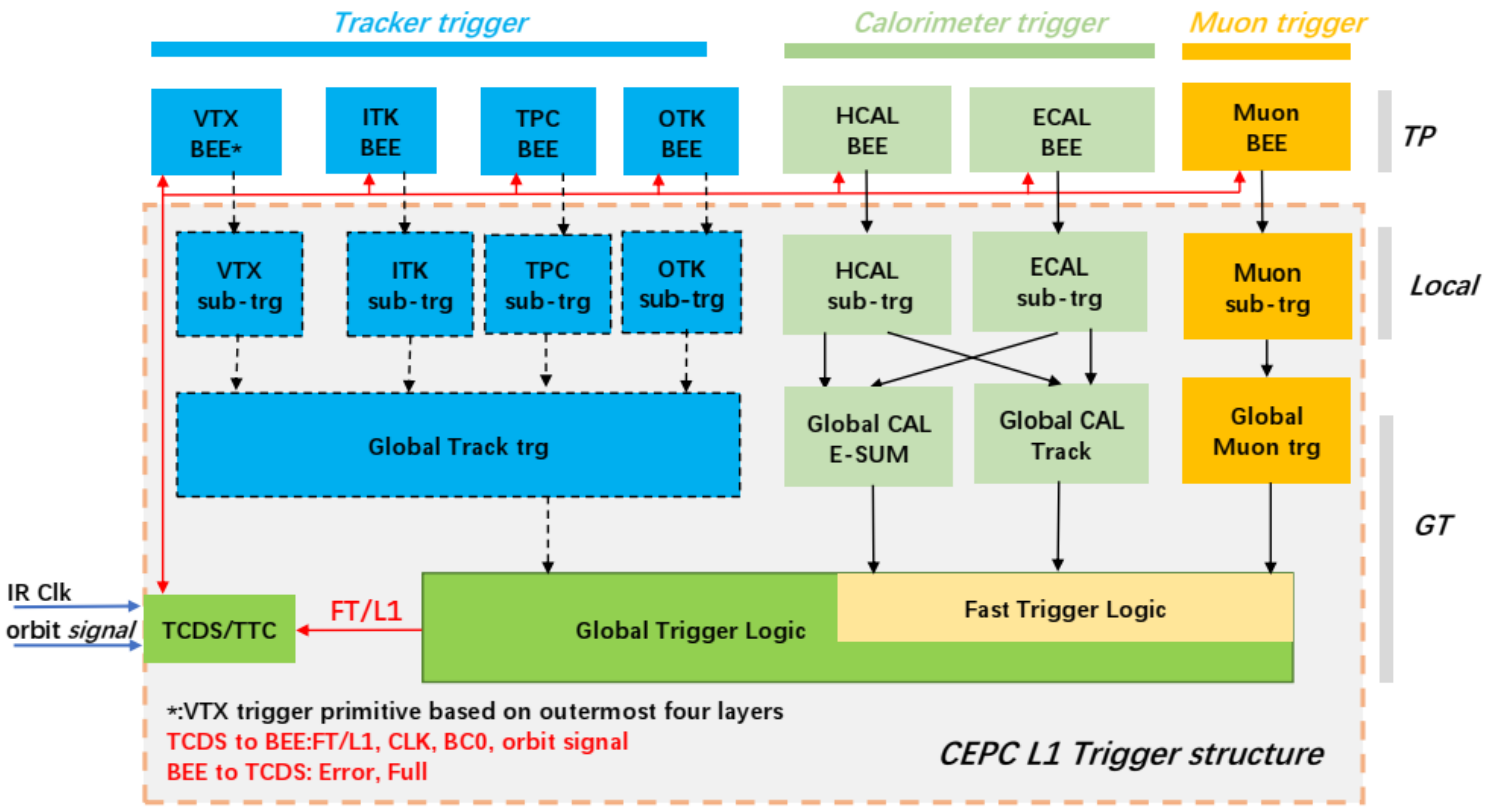


Figure 12.2: Trigger architecture diagram

Design of TCDS and Readout

- TCDS/TTC
  - Clock, BC0, Trigger, orbit start signal distribution
  - Full, ERR signal feed back to TCDS/TTC and mask or stop L1A
- Data readout from BEE
  - Read out directly or concentrated by DCTD/TTCD board
  - Depending on the size of the data volume

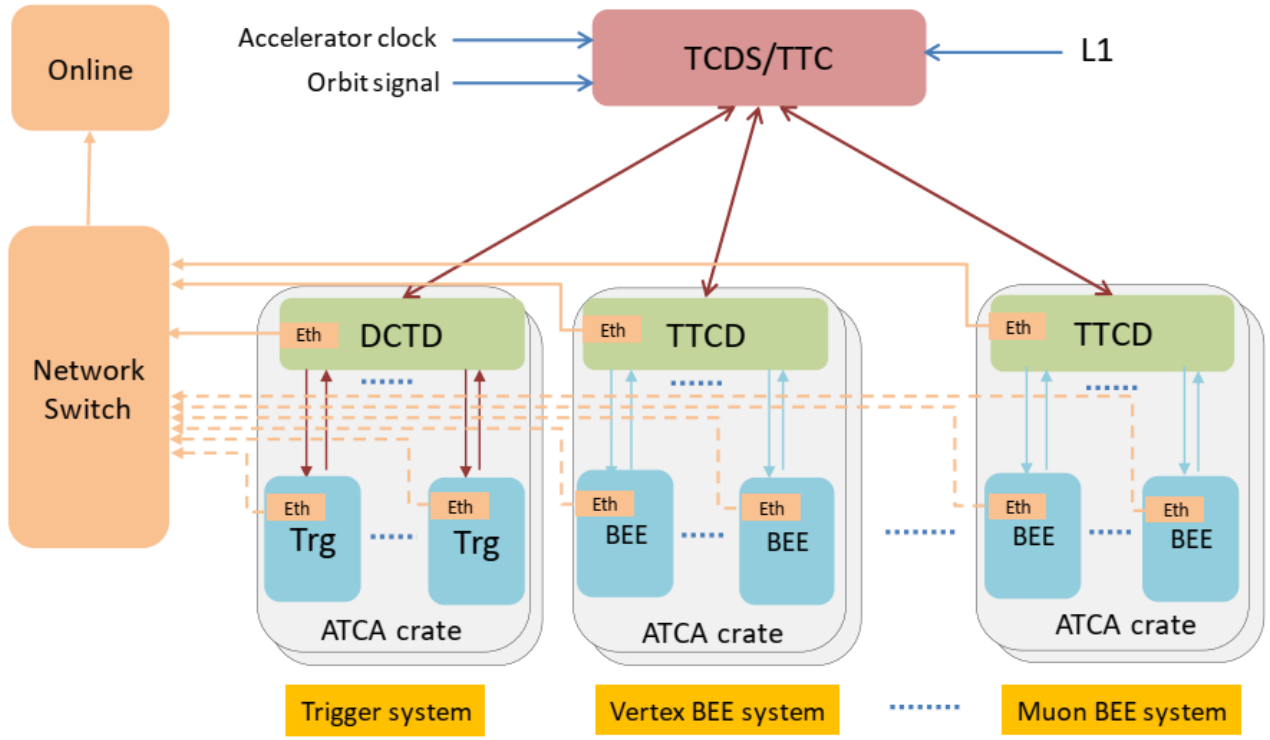


Figure 12.4: TCDS/TTC proposed structure.

- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- DCTD- Data Concentrator and Timing Distribution
- BEE-BackEnd Electronic

TCDS/TTC

- Function list of TCDS/TTC -preliminary
  - system clock generation based on accelerator clock or local high-precision clock for test.
  - orbit signal receive from accelerator and generate orbit number and Bunch Crossing Zero(BC0) signal for Bunch counting.
  - BEE system status receive from feedback link.
  - L1A(FT) received from trigger system, fanout trigger signal or mask trigger signal to all BEE system according to each sub-system's status.
  - Downlink signal to BEE(fan out to all BEE and trigger system)
    - Clock, L1T(FT), L1T(FT)_chk, BC0, orbit number,……
  - Uplink signal information(Feedback to TCDS):
    - Busy, Fiber ERR, and some other system status

DCTD

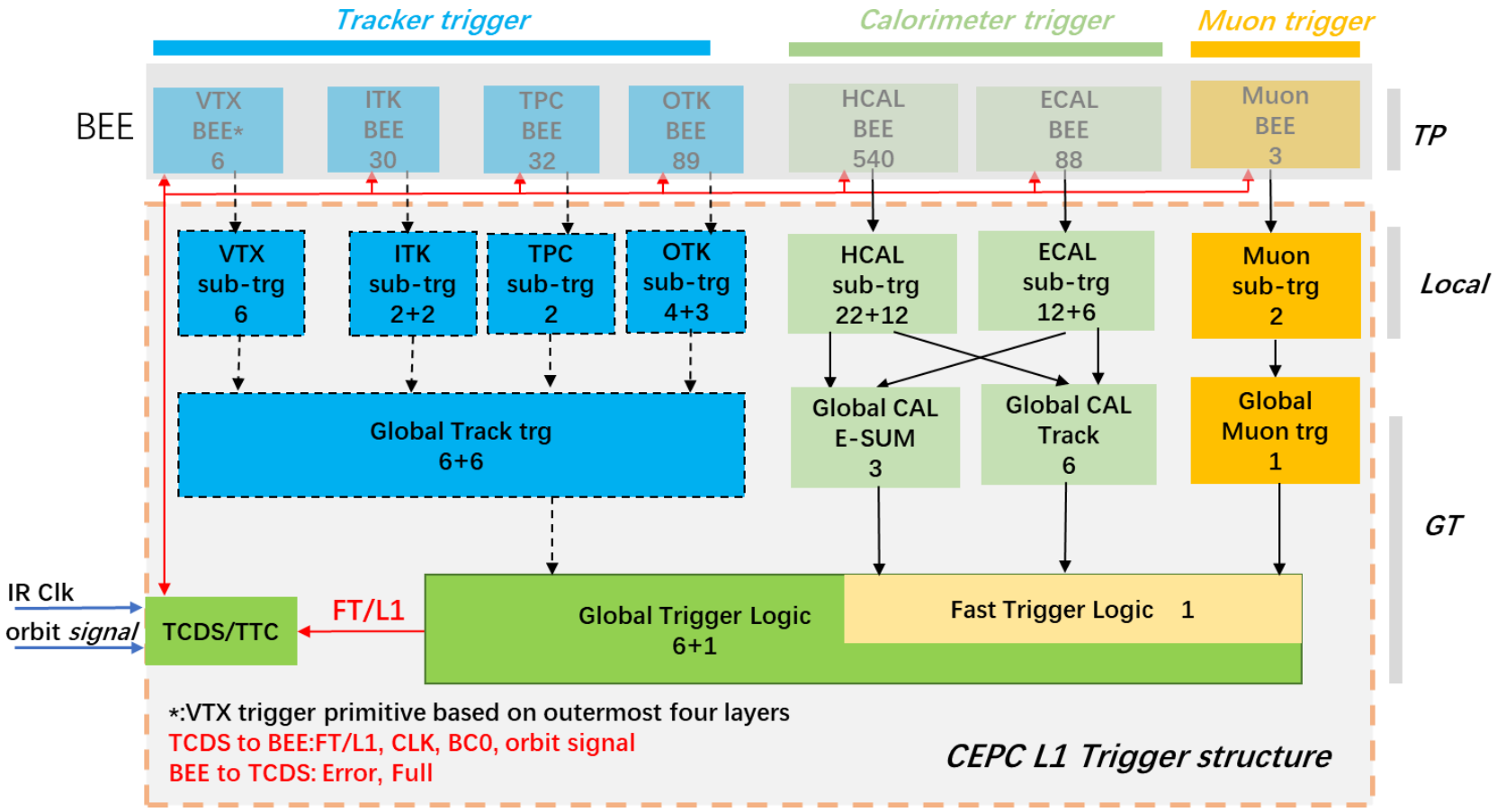
- DCTD is the xTCA based Data Concentrate and Timing Distribution for trigger system.
- Data concentrate
  - receive data from each ATCA trigger board
  - package the ATCA crate data based on trigger number
  - packaged data send to online via TCP or RDMA
- Timing Trigger Distribution
  - Receive system clock/Fast control signals from TCDS or generate locally for test
  - system clock fan-out to ATCA trigger board within ATCA crate
  - Fast control signals fan-out(FT/L1A, BC0, orbit number,...)
  - Collect trigger ATCA boards' status information and send back to TCDS

Low latency data transmission link

- uniform data transmission link between BEE to trigger and within trigger system
  - 10Gbps/ch or 16Gbps/ch
  - low latency for time alignment between different channels
  - uniform data frame format with BX number, delay number, trigger primitive(such as cluster, energy, track, hit) information

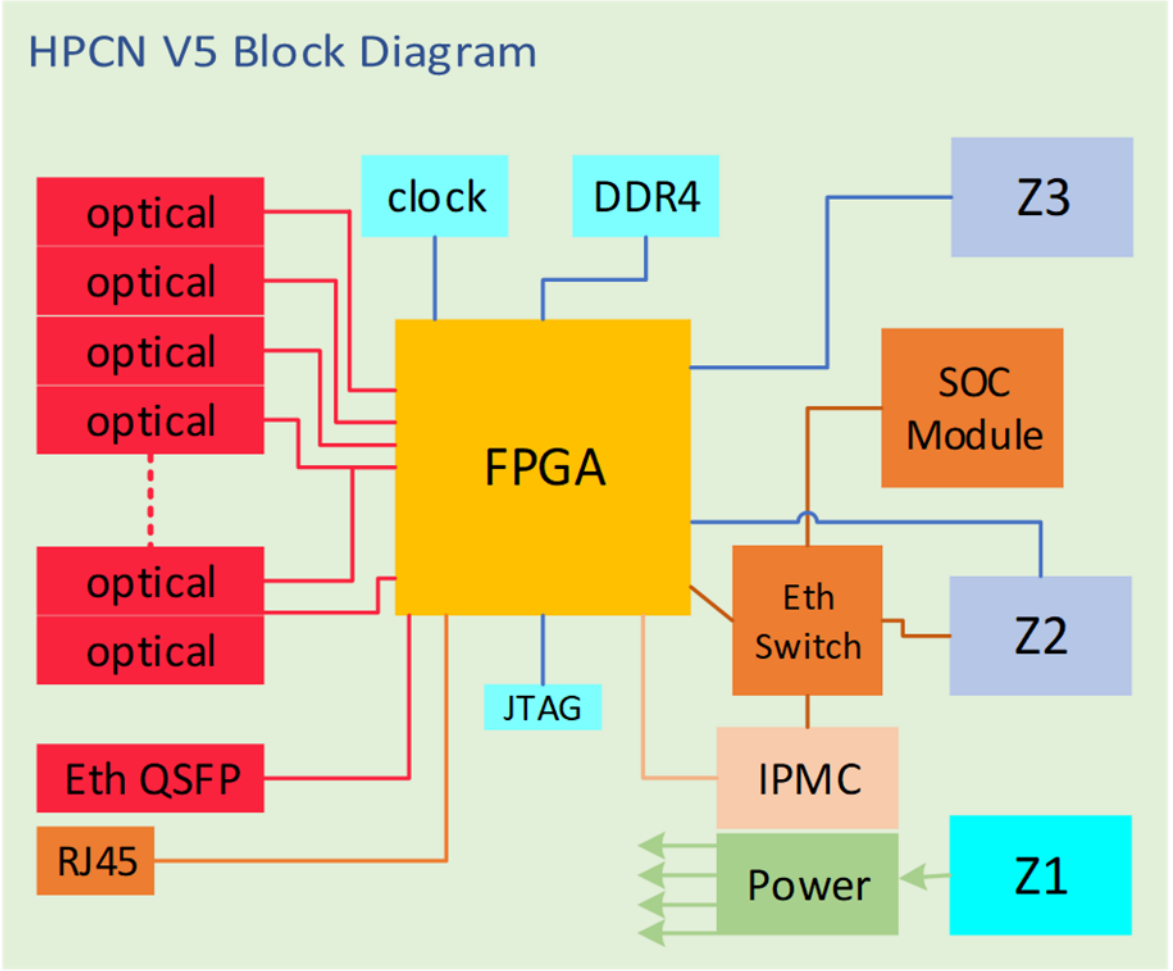
Estimation of trigger system scale

- Scale of L1 trigger system(including Tracker)
  - ~105 Trigger boards
  - 17 DCTD boards
  - 17 ATCA crates

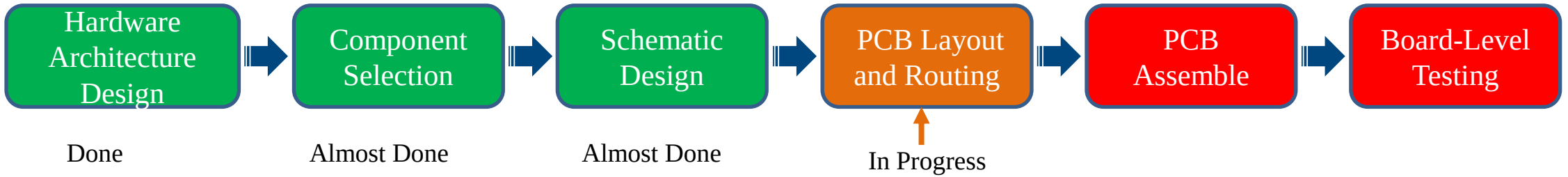


Structure of the common Trigger Board

- Common Trigger board function list
  - ATCA standard
  - Xilinx Virtex Ultrascale Plus FPGA
  - Optical channel: 10-25 Gbps/ch
  - Channel number:44 channels
    - 40 for data link
    - 4 for Optical Ethernet port: 40-100GbE
  - DDR4 for mass data buffering
  - SoC module for board management
  - Ethernet Switch for on board and Ethernet Interface connection
  - IPMC module for Power management



Progress on Trigger board R&D



- Main Components Selection done
  - FPGA,DDR4,QSFP,Clock fan out ,PHY , Eth switch , Power have been selected and validated against design requirements.
  - some components for test (e.g., Socket, Conversion chip) require further specification alignment.
- Schematic Design almost completed
  - The main section of the schematic has been designed, and it is currently undergoing a synchronization verification.
- PCB Layout and Routing is in progress
  - Layout of key components has been completed, with the routing of high-speed signal lines and clock lines preliminarily finalized.
- Next Phase: PCB Fabrication
  - PCB Fabrication shall commence following Layout and Routing sign-off.

Key components Selection

- FPGA: AMD/XILINX
  - Footprint: B2104, pin compatible withVU5P,VU7P,U9P, VU11P and VU13P for FPGA resource upgrade
  - Pin2pin compatible with Fudan Micro chip

Virtex UltraScale+ FPGA Feature Summary

Table 9: **Virtex UltraScale+ FPGA Feature Summary**

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P
System Logic Cells	862,050	1,313,763	1,724,100	2,586,150	2,835,000	3,780,000
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,592,000	3,456,000
CLB LUTs	394,080	600,577	788,160	1,182,240	1,296,000	1,728,000
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3
Block RAM Blocks	720	1,024	1,440	2,160	2,016	2,688
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5
UltraRAM Blocks	320	470	640	960	960	1,280
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0
HBM DRAM (GB)	–	–	–	–	–	–
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16
Max. HP I/O(1)	520	832	832	832	624	832
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288
System Monitor	1	2	2	3	3	4
GTY Transceivers 32.75Gb/s(2)	40	80	80	120	96	128
GTM Transceivers 58.0Gb/s(2)	–	–	–	–	–	–
100G / 50G KP4 FEC	–	–	–	–	–	–
Transceiver Fractional PLLs	20	40	40	60	48	64
PCIe Gen3 x16 and Gen4 x8	2	4	4	6	3	4
CCIX Ports(3)	–	–	–	–	–	–
150G Interlaken	3	4	6	9	6	8
100G Ethernet w/RS-FEC	3	4	6	9	9	12

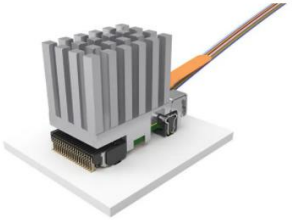
Table 12: **Virtex UltraScale+ Device-Package Combinations and Maximum I/Os**

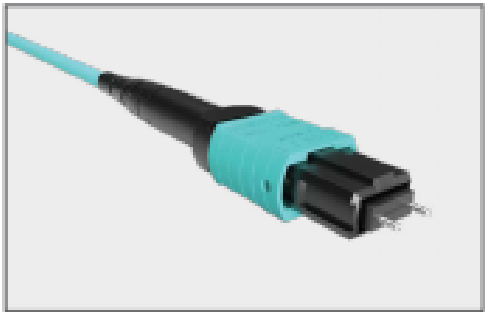
Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY
VSVA1365	35x35						
FFVC1517	40x40	520, 40					
FSVJ1760	42.5x42.5						
FLGF1924(5)	45x45					624, 64	
FLVA2104	47.5x47.5		832, 52	832, 52			
FLGA2104	47.5x47.5				832, 52		
FHGA2104	52.5x52.5(6)						832, 52
FLVB2104	47.5x47.5		702, 76	702, 76			
FLGB2104	47.5x47.5				702, 76	572, 76	
FHGB2104	52.5x52.5(6)						702, 76
FLVC2104	47.5x47.5		416, 80	416, 80			
FLGC2104	47.5x47.5				416, 104	416, 96	
FHGC2104	52.5x52.5(6)						416, 104
FSGD2104	47.5x47.5				676, 76	572, 76	
FIGD2104	52.5x52.5(6)						676, 76
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128
FSGA2577	52.5x52.5						448, 128
FSVA3824	65x65						
FSVB3824	65x65						

Key components Selection

- QSFP
  - 4ch TX/RX /module
  - MPO optics fiber port
  - 25Gbps/ch

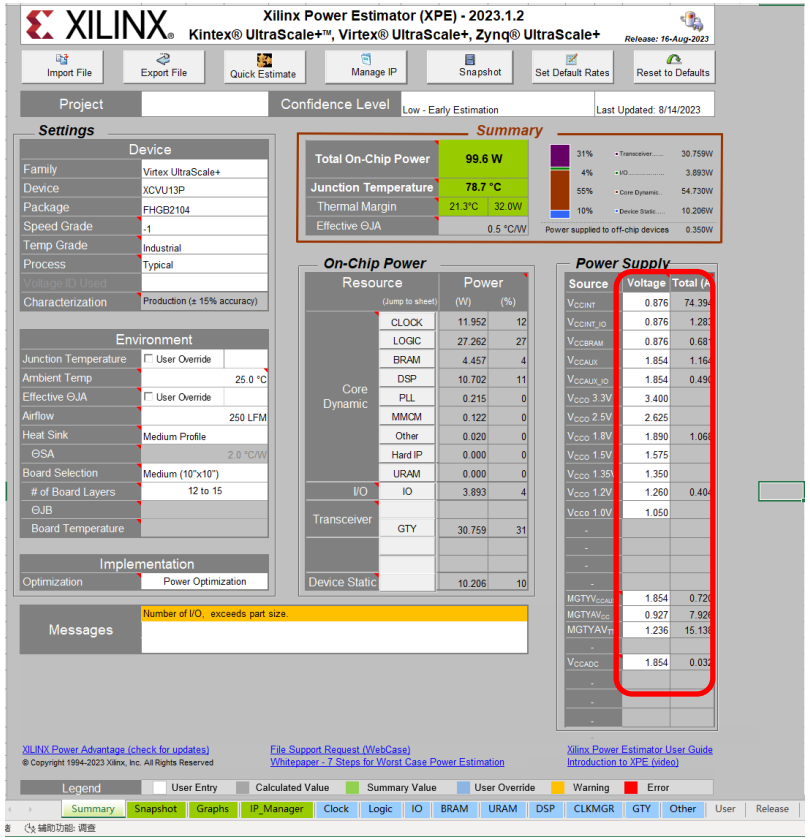
- Samtec Firefly
  - High desity
  - 12ch TX/RX /module
  - MPO optics fiber port
  - 25Gbps/ch

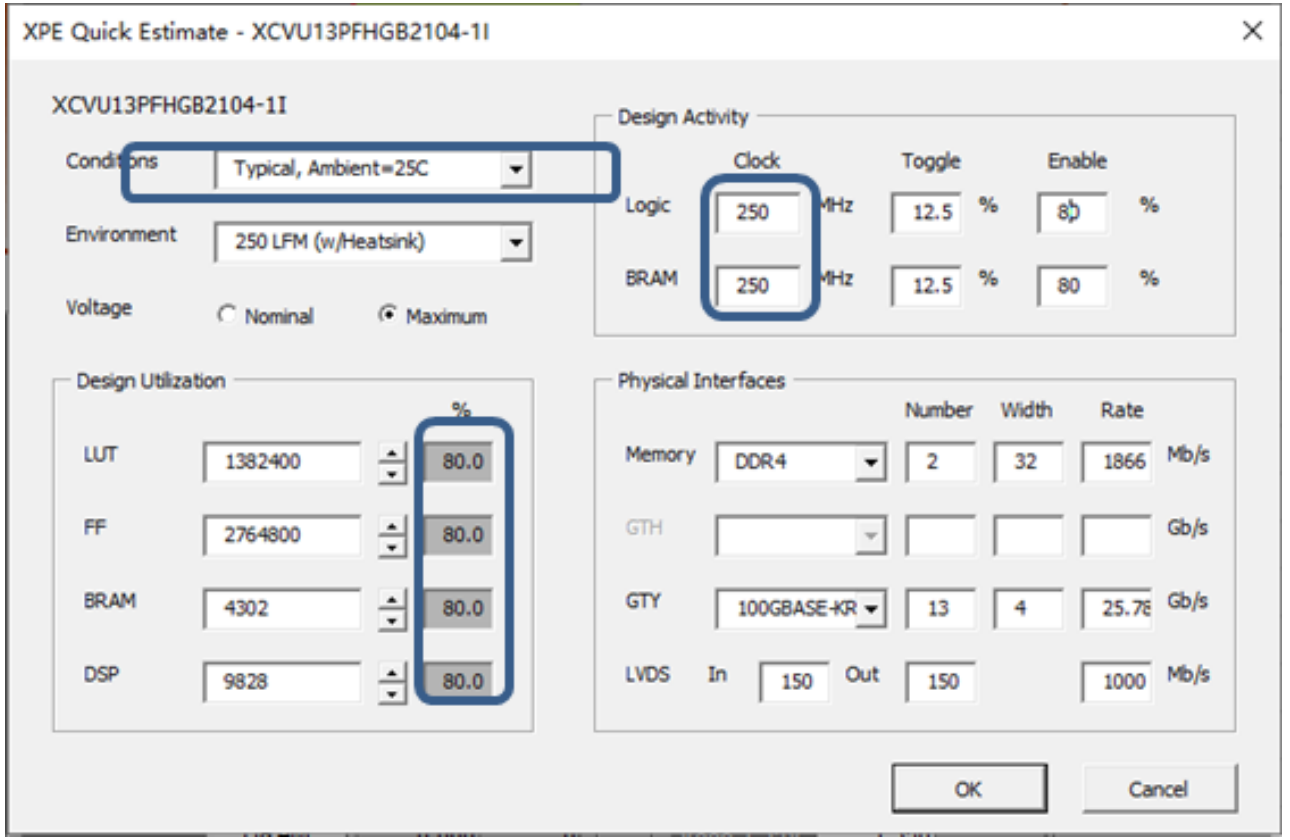




Power consumption estimation

- Power consumption estimation using XPE
  - FPGA： XCVU9P or XCVU13P(Compatible with domestic chips)
  - Evaluate the power consumption of the Xilinx XCVU13P FPGA under specified operating conditions to guide optimal power supply design.





Power consumption estimation

- QSFP power consumption
  - Optical transceiver :36-48 channels
  - Recommand :QSFP*10 (40 channels)
  - 3.3V Power Rail Current Estimation 1.2*10 = 12A

- Clock and Ethernet switch power consumption
  - ETH switch :
    - 6 or more ports
    - Recommend : KSZ9897R(7 ports) Estimation 2A
  - Clock fan out : QSFP*10 ,FPGA.....
    - Recommend : ZL30274 *2 (8*2) Estimation 1A

Performance	
SFP transceiver type *	Fiber optic
Maximum data transfer rate *	100000 Mbit/s
Interface type *	QSFP28
Single-mode fiber (SMF) supported	✗
Multi-mode fiber (MMF) supported	✓
Fiber optic connector	MPO-12
SFP transceiver standard	SR4
Maximum transfer distance	100 m
Wavelength	850 nm
Ethernet LAN	✓
Ethernet interface type	100 Gigabit Ethernet
Fiber ethernet cabling technology	100GBASE
Digital Diagnostics Monitoring (DDM)	✓
Features	
Product colour	Silver
Housing material	Metal
Plug and Play	✓
Hot-Plug support	✓
Hot-swap	✓
Easy to install	✓
Brand compatibility	Arista Networks
Power	
Input voltage	3.3 V
Maximum voltage	3.5 V

Power	
Power consumption (typical)	4 W
Certificates	
Compliance certificates	TÜV mark, UKCA, UL, US FDA, REACH, Federal Communications Commission (FCC), RoHS, CE
Certification	CE, FCC, RoHS, REACH
Sustainability	
Sustainability compliance	✓
Doesn't contain	Lead
Operational conditions	
Minimum operating temperature	0 °C
Maximum operating temperature	70 °C
Operating temperature (T-T)	0 - 70 °C
Storage temperature (T-T)	-40 - 85 °C
Operating relative humidity (H-H)	0 - 95%
Storage relative humidity (H-H)	0 - 95%
Weight & dimensions	
Width	13.5 mm
Depth	72.4 mm
Height	18.4 mm
Weight	100 g
Packaging content	
Quantity per pack	1 pc(s)
Packaging data	
Package type	Box
Logistics data	
Country of origin	United Kingdom

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current - Full 1000 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**VDDIO** @ 3.3V Ports 1-5 in 1000BASE-T Ports 6 & 7 in RGMII (1000 Mbps) All ports 100% utilization		330		mA
I_{DD_IO}	**VDDIO** supply current			80		mA
I_{DD_CA}	**AVDDL** supply current			460		mA
I_{DD_CD}	**DVDDL** supply current			750		mA

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled	P_{DISS}	—	0.8	—	W
Total current, 3.3V supply (VDD33+VDDOx pins)	I_{DD33}	—	160	322	mA
Total current, 1.8V supply (VDD18 pins)	I_{DD18}	—	207	519	mA

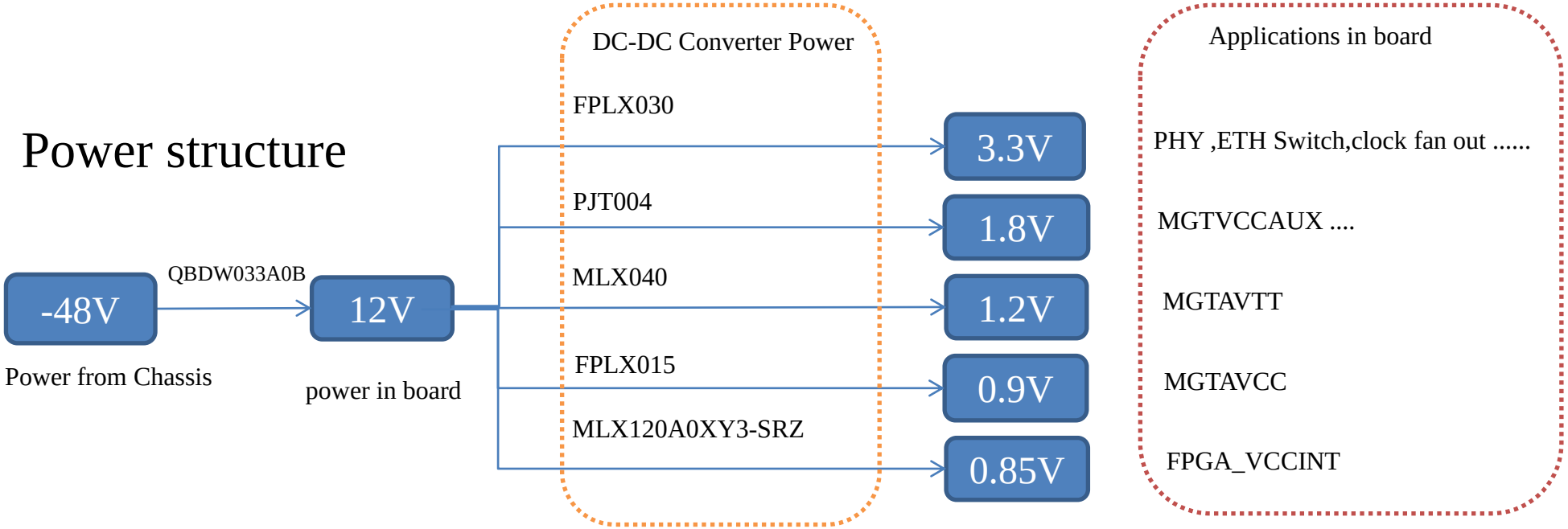
Power Design

- Estimated Power Consumption: ~170W
- Designed Power Consumption:~280W

Power Consumption Evaluation Summary

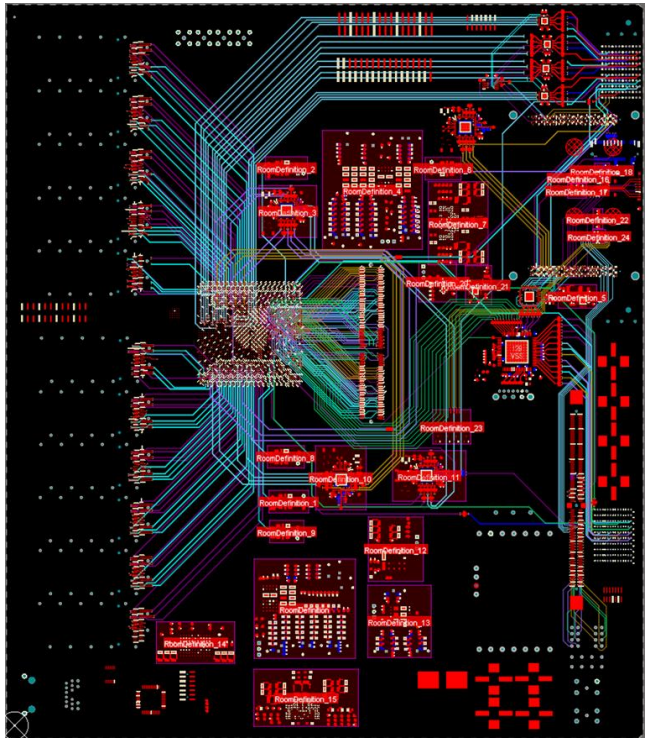
Voltage (V)	3.3	1.8	1.2	0.9	0.85
Estimated Current (A)	20	4	16	8	80
Design Maximum Current (A)	30	8	40	15	120

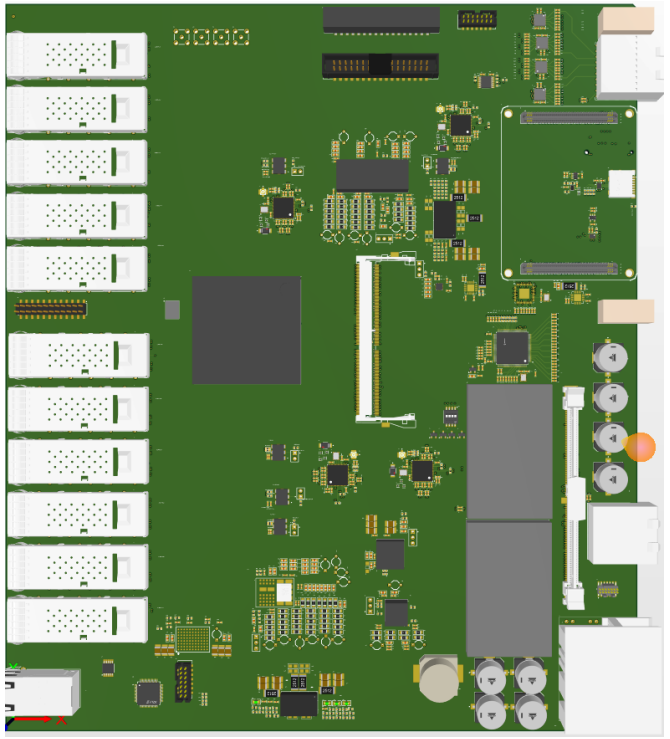
Power structure



PCB layout

- PCB layout
  - FPGA Positioning（Centralized placement）
  - High-Speed Interface Arrangement
    - QSFP connector
    - DDR4 connector
    - ETH Switch
  - Power
    - -48V-12V Converter Power
    - FPGA VCCINT
    - MGT Power
  - IO
    - Backplane connectors
    - RJ45,QSFP,USB





Summary

- L1 Trigger is a key system for CEPC ref-detector.
- Trigger strategy : Hardware trigger(L1) + high level trigger(HLT)
- Baseline L1 trigger strategy: Ecal+Hcal+Muon
- L1 trigger system structure is designed. Common trigger board will be used for trigger algorithm.
- R&D on trigger board is ongoing. PCB layout is in progress.
- Collaborations are welcome.

Thank you.