Contribution ID: **269** Type: **Talk**

L1 trigger design progress on CEPC ref-Detector TDR

Sunday, 9 November 2025 09:30 (20 minutes)

CEPC ref-Detector TDR is finished and submmitted for publish.CEPC plans to run at a non-empty bunch crossing rate of 1.34–40 MHz.Background data throughput will be from 100 GB/s (Higgs mode) to 1 TB/s (Z-boson pole). Simulations show the trigger system can reduce rates to the range of few to tens of GB/s efficiently and event rate to 30 kHz (Higgs) and 120 kHz (low lumi-Z). The L1 trigger employs a three-stage hardware system: the first stage generates module-level triggers from backend electronics; subsequent stages integrate sub-detector triggers and execute global selection.The L1 signals are sent to Backend Electronic of each detector for data readout via the TCDS(Trigger and Clock Distribution System).This report will show more detials of L1 trigger system design and progress on the R&D.

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Session Classification: TDAQ

Track Classification: Detector and System: 17: TDAQ & Online