CENTRAL CHINA NORMAL UNIVERSITY

Pixel Laboratory at CCNU
PLAC

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

R&D of Topmetal Pixel Readout Chips

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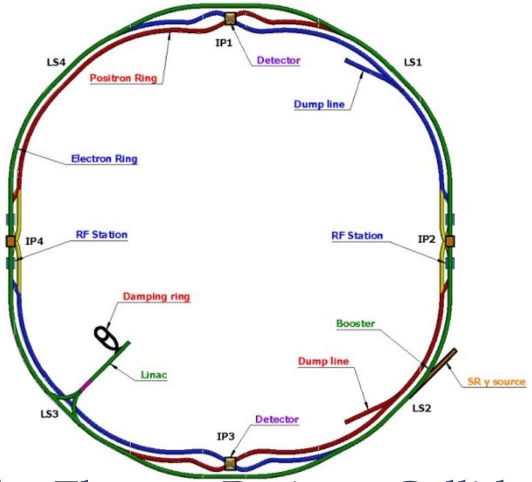
On behalf of Prof. Xiangming Sun's Research Group

The 2025 international workshop on the high energy CEPC, Guangzhou

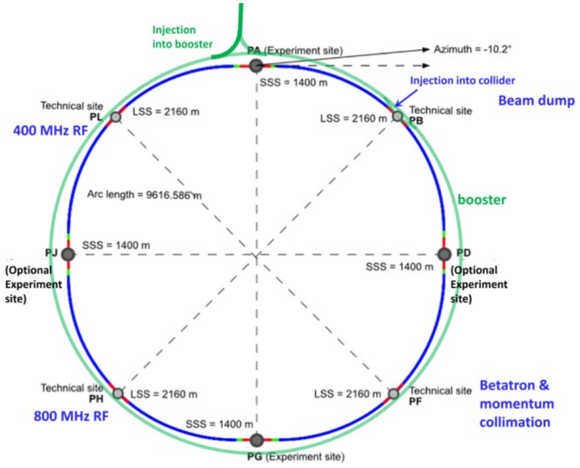
CONTENTS

Detector Demands in High-Energy Physics

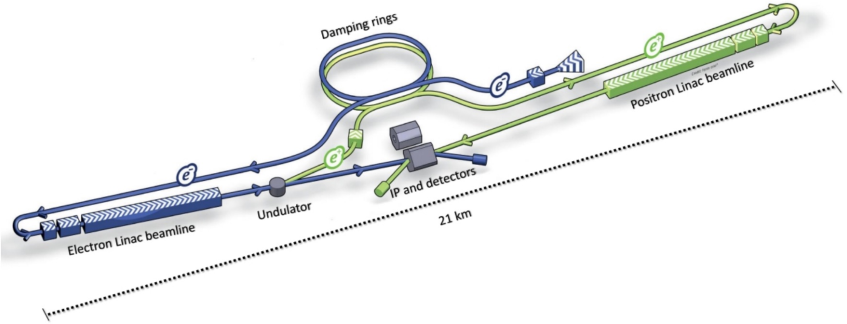
- Extreme Experimental Environments (e.g. CEPC, ILC, ALICE) require sensors with high spatial granularity, fast readout
- High-granularity pixel readout now adopted not only in vertex detectors but also in TPC systems for precise 3-D tracking
- Massive data throughput → fast readout electronics
- Minimal material budget → ultra-thin detectors
- Integration of sensor + readout + DAQ in compact form



Circular Electron Positron Collider CEPC



Future Circular Collider （FCC-ee）

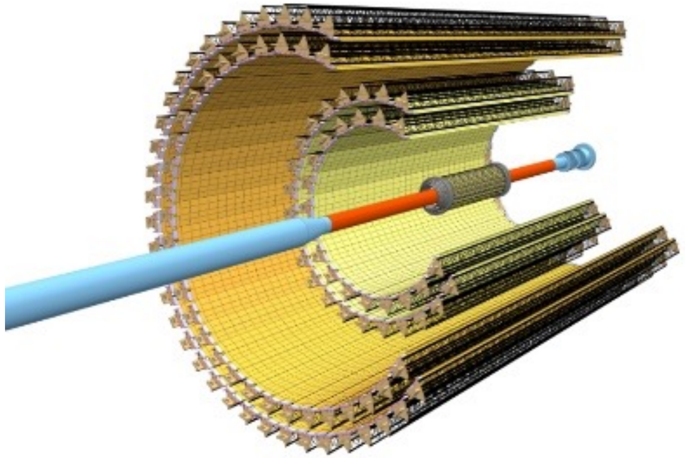


International Linear Collider(ILC)

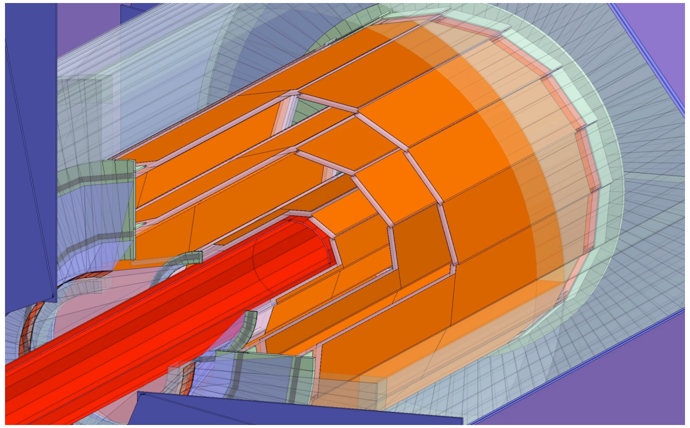
From Detector Needs to Chip Requirements

- Low Noise – essential for thin silicon or TPC sensors
- Low Power (< 100 mW/cm² for CEPC TPC & < 40 mW/cm² for CEPC Vertex)

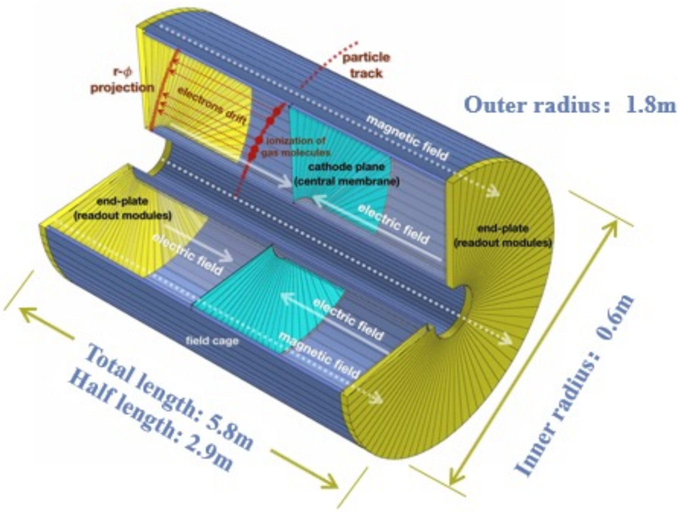
  – lightweight cooling, reduced X_0
- High Resolution (~5 μm for CEPC Vertex & ~100 μm for CEPC TPC)
- Fast Readout for high-rate beams
- Radiation tolerance & scalability for large-area detector systems.



ALICE ITS2



CEPC Vertex



CEPC TPC

Overview of the PLAC Laboratory

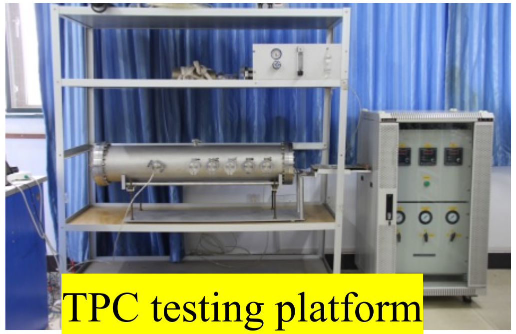
- Quark and Lepton Physics Education Ministry Key Lab
- CCNU–Silicon Pixel Lab, Hubei Engineering Center
- Cooperation with CERN, IHEP, etc.
- Over 50 staff members, 23 senior researchers.

Pixel Laboratory at CCNU
PLAC

Overview of the PLAC Laboratory

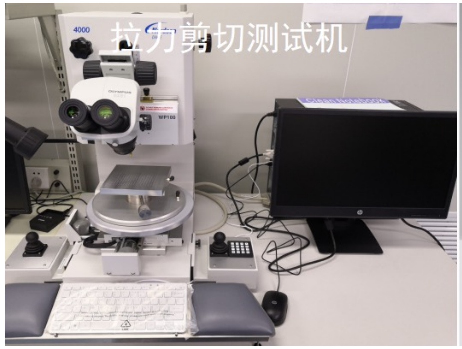
- IC design and testing platform (2000 m² lab)
- Includes detector test stands, readout systems, FPGA DAQ, and cleanroom
- Supports full chain of pixel R&D

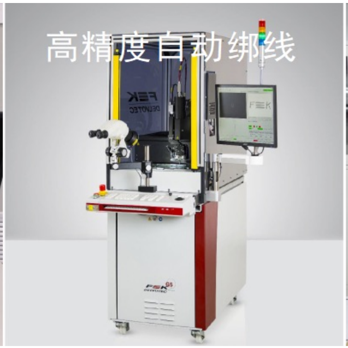
MRPC Detector testing platform

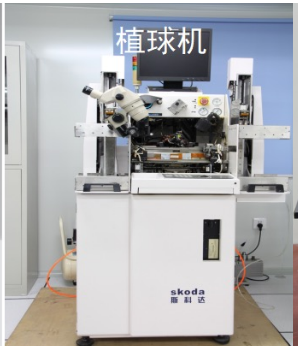


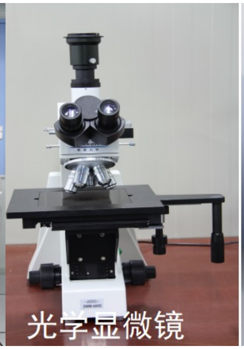
TPC testing platform

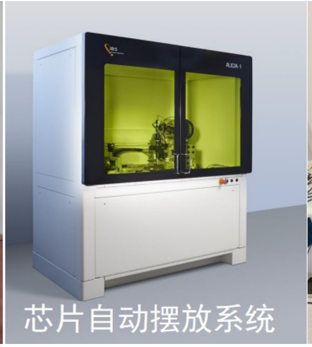
FPGA DAQ setups







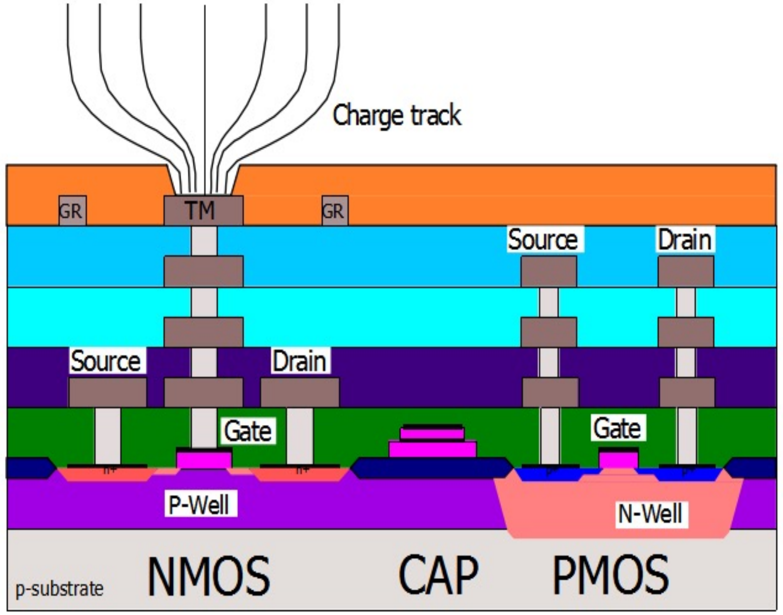




PLAC Laboratory: Pixel Chip Series

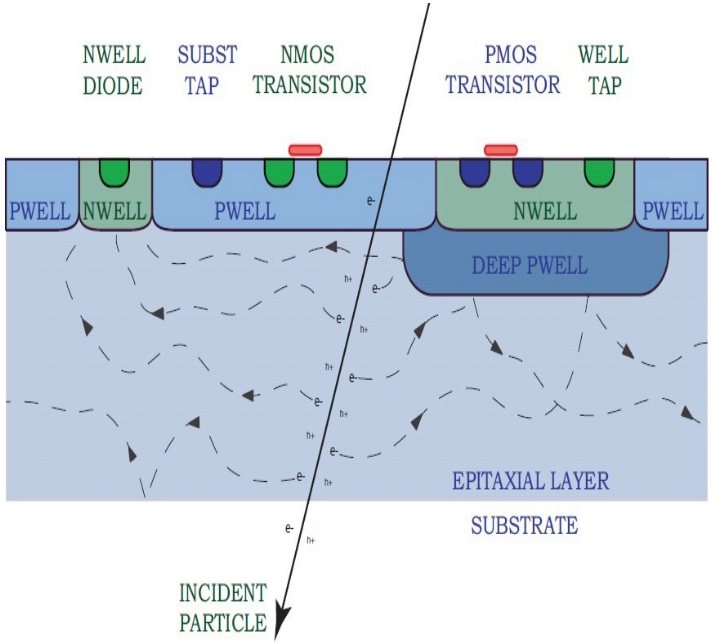
Topmetal

- CMOS process with top metal node for direct charge collection.
- Designed to directly sense ionization charge in gas or solid media.
- Widely applied in X-ray polarimetry, TPC readout, and neutrino detection.



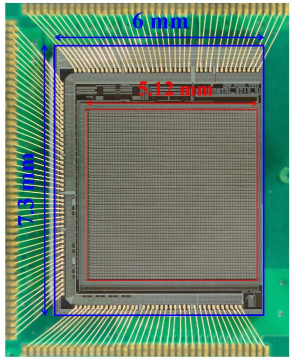
MIC

- Based on advanced MAPS technology.
- Developed by PLAC Lab for vertex and tracking detectors in HEP.
- Features deep P-well isolation and in-pixel amplification for low noise & high speed.

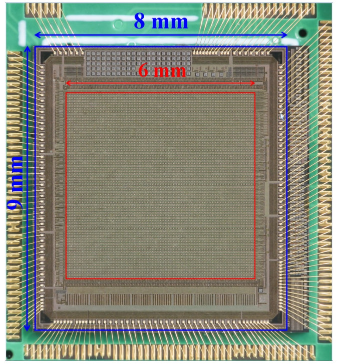


Evolution of Topmetal Series

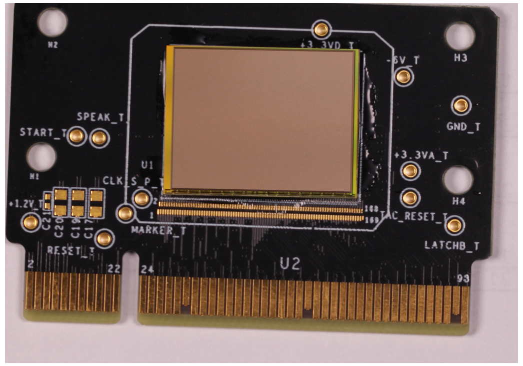
- Topmetal-I → II → M → M2 → L → S
  - Based on CMOS IC process, direct charge-collection using top metal layer.
  - Low noise (~20 e^- ENC), moderate pixel pitch (45–80 μm).



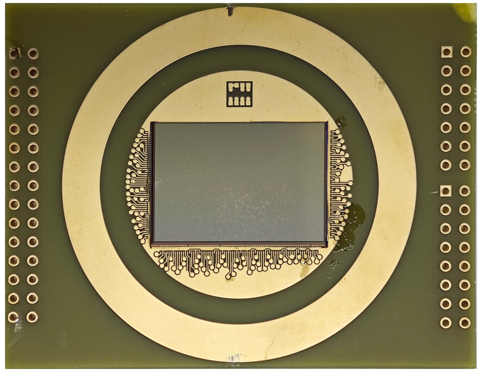
Topmetal-I



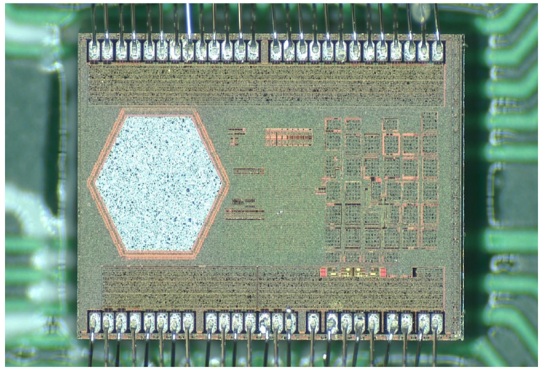
Topmetal-II



Topmetal-M

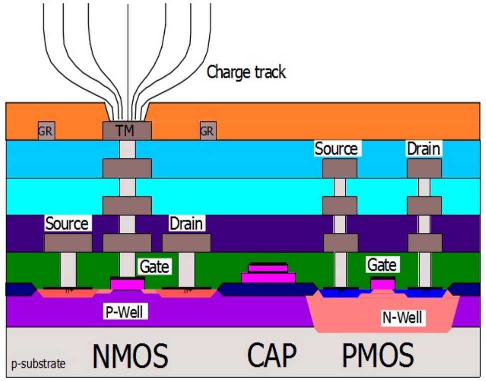


Topmetal-L



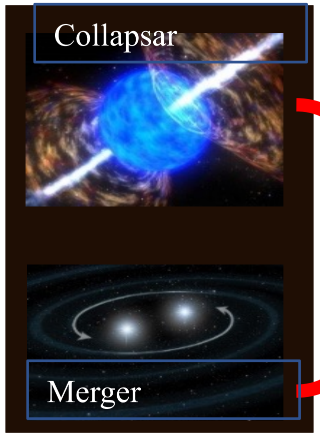
Topmetal-S

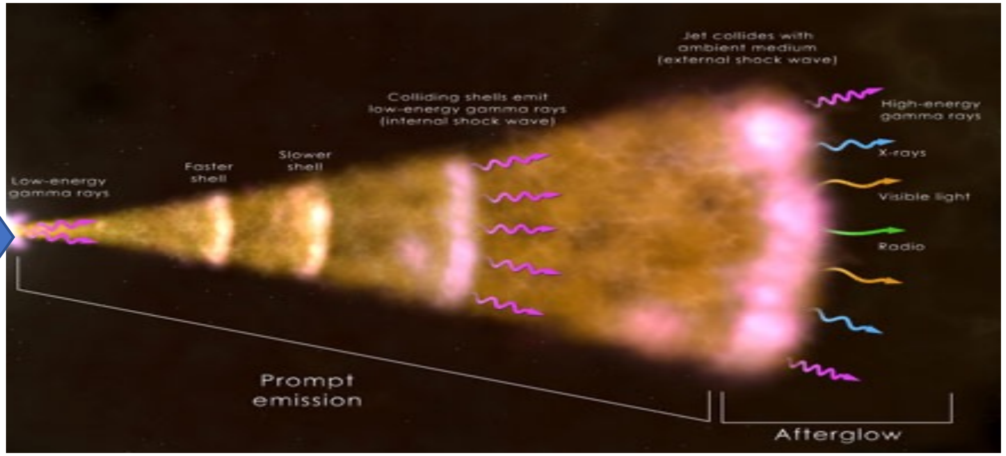
- Design Concept
  - Direct charge collection via exposed top metal node.
  - Avoid avalanche multiplication → better energy resolution.
  - High integration, low leakage, scalable pixel matrix.

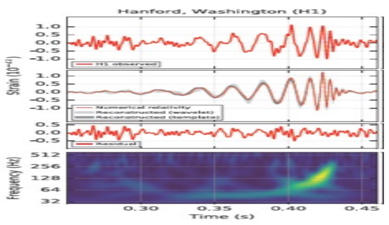


Application I — Space X-ray Polarization Detector

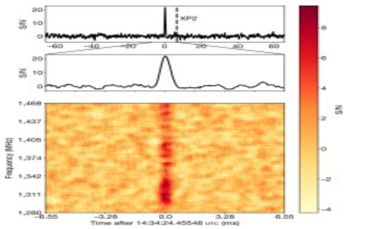
- **Topmetal for POLAR-2—joint effort with the payload team**
  - **Developed by CCNU, evolving from Topmetal-II to Topmetal-M, and finally to Topmetal-L optimized for the LPD detector.**
  - **512×356 array, 45 μm pitch, ENC ~20 e⁻**
  - **Successfully launched in 2023 on Low-Earth orbit CubeSat.**



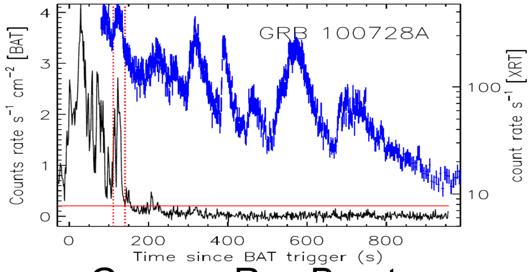




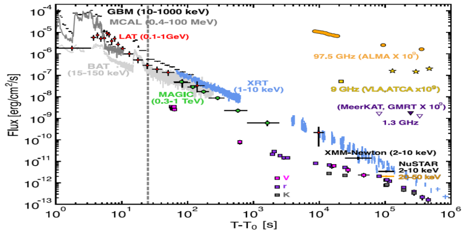
Gravitational Wave



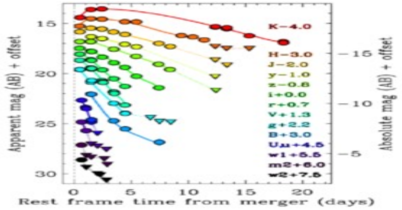
Fast Radio Burst (FRB)



Gamma-Ray Burst



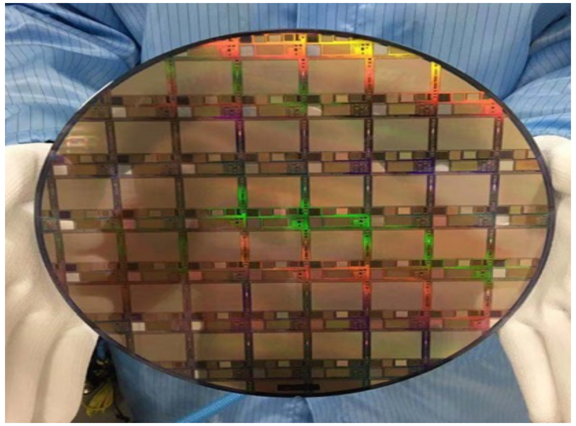
Multi-band Afterglow

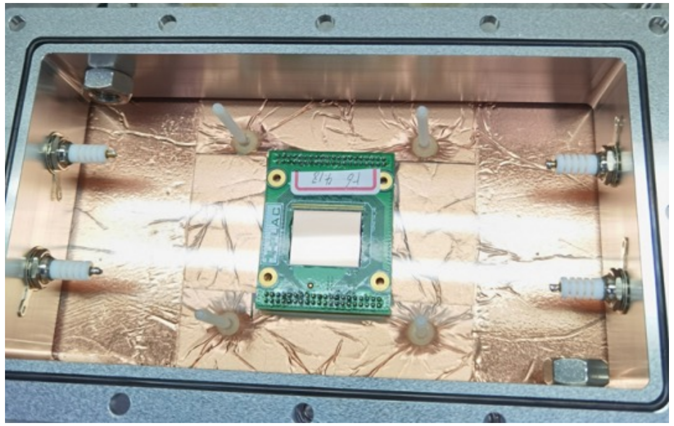


Supernova and Kilonova

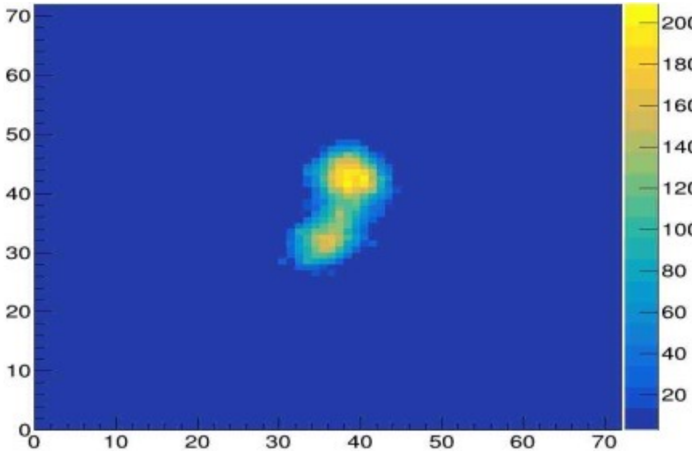
Topmetal-M coupled with gas detector

- **Topmetal-M parameters**
- 400 × 512 pixels, 45 μm pitch;
- ~20 e^- ENC noise, 0.73 W @ 1.5 V.
- **Gas Detector Integration**
- He + 70% DME @ 1 atm with GMCP gain;
- **Experimental Results**
- Energy resolution: 22.9 % @ ^{55}Fe;
- Clear modulation for polarized (5.4 keV) and unpolarized (5.9 keV) X-rays.

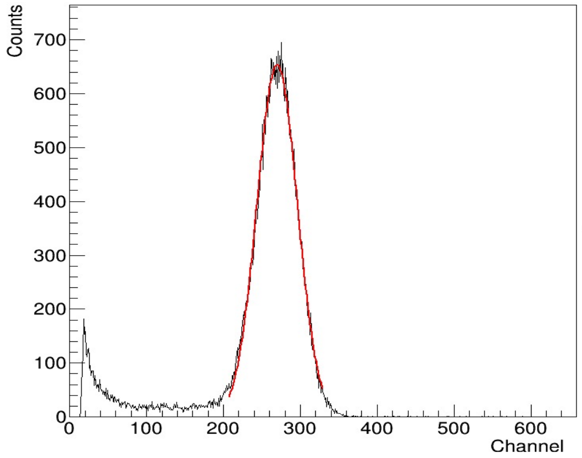




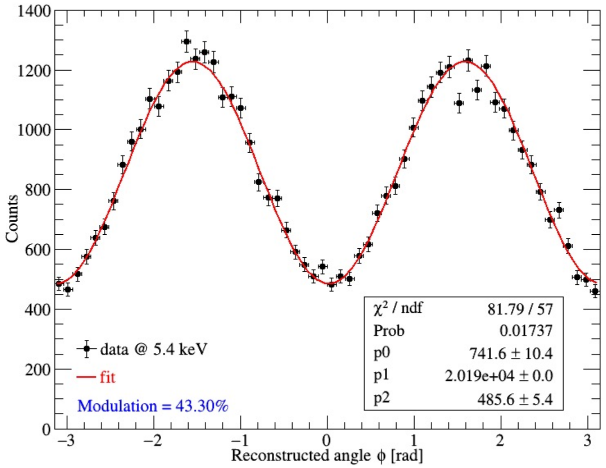
Demonstrates the potential of Topmetal sensors in soft X-ray polarization measurements



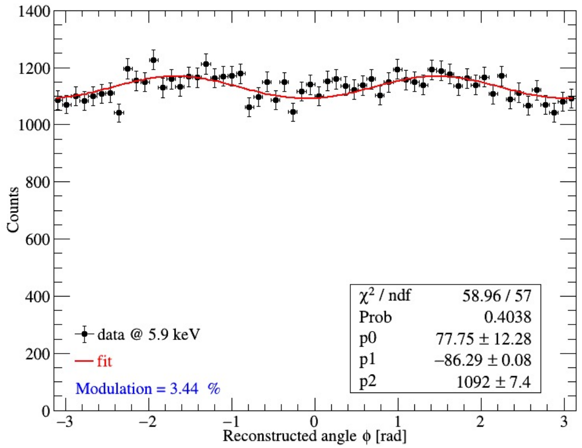
Track of 5.9 keV soft X-ray photoelectrons measured with Topmetal-M2



Energy spectrum of ^{55}Fe
Energy resolution: 22.88 %



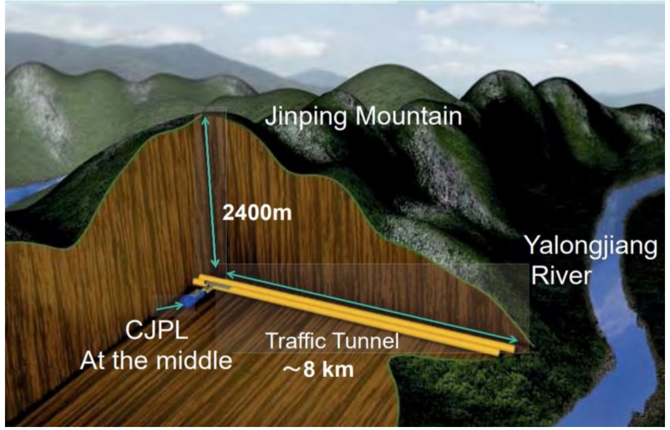
Full-polarized X-ray modulation curve (5.4 keV)

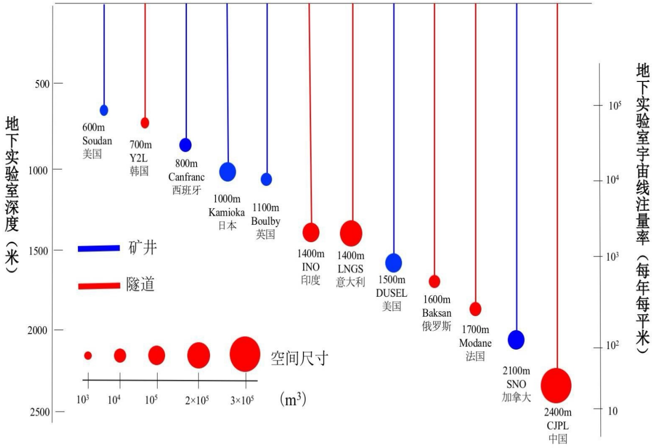


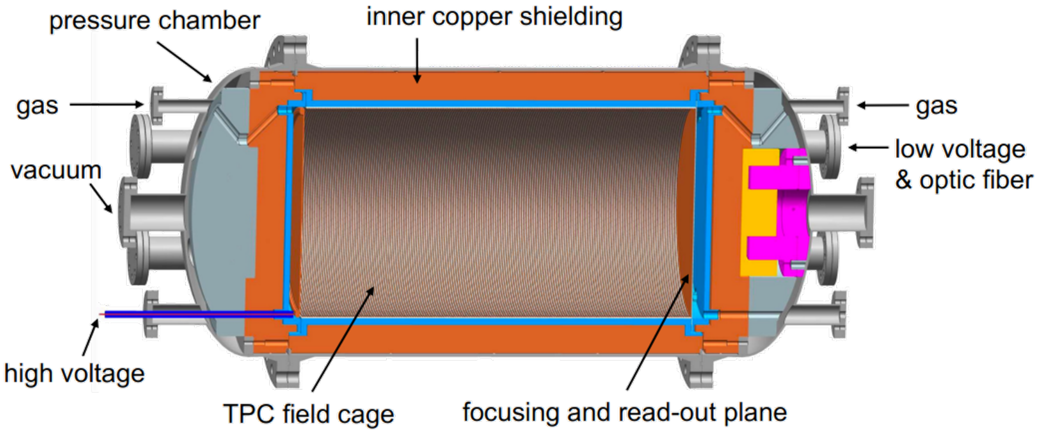
Unpolarized X-ray modulation curve (5.9 keV)

Application II — NvDEx

- ■ Scientific goal: probe Majorana nature and absolute neutrino mass
- ■ Readout concept: direct ion charge collection in TPC
  - 100 kg SeF_6 gas @10 atm.
  - TPC length 160 cm, diameter 120 cm.
  - Gas tightness and temperature stability verified.

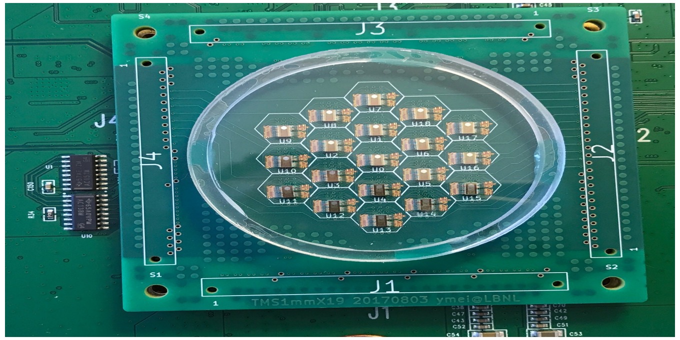


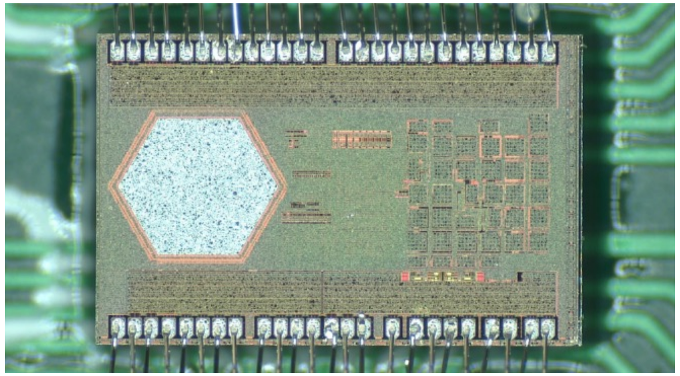


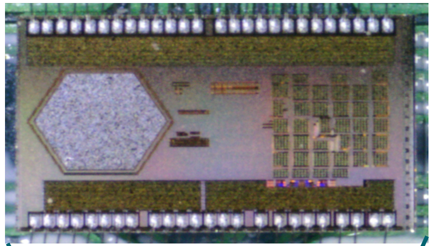


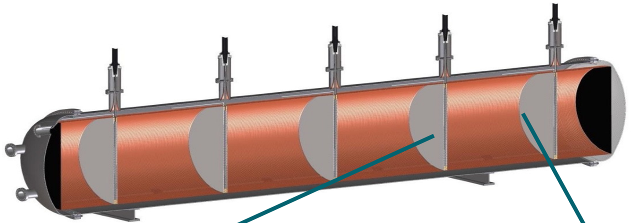
Key Feature of Topmetal-S Readout — NνDEx

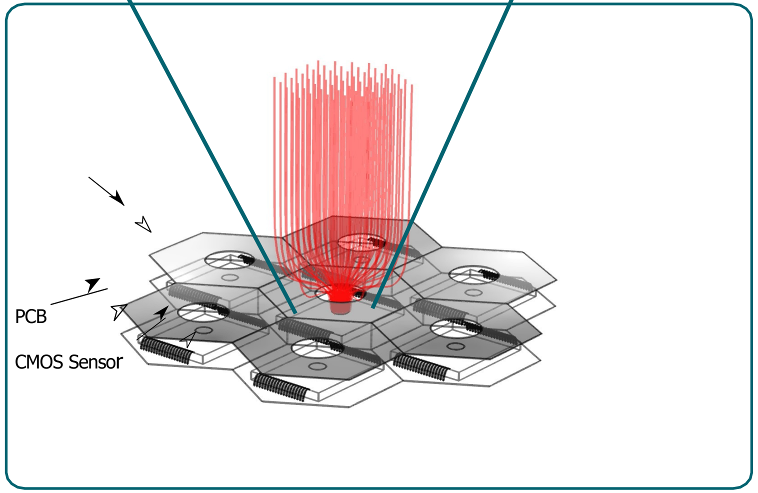
- Topmetal-S directly collects ionization charges without amplification, avoiding avalanche fluctuations and achieving improved energy resolution (~1.5%).
- Demonstrated ultra-low noise performance (<130 e^- ENC, target: 45 e^-).



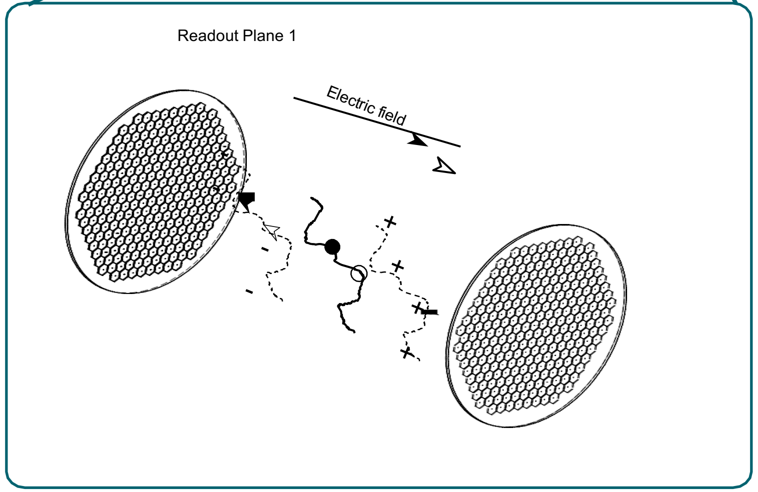








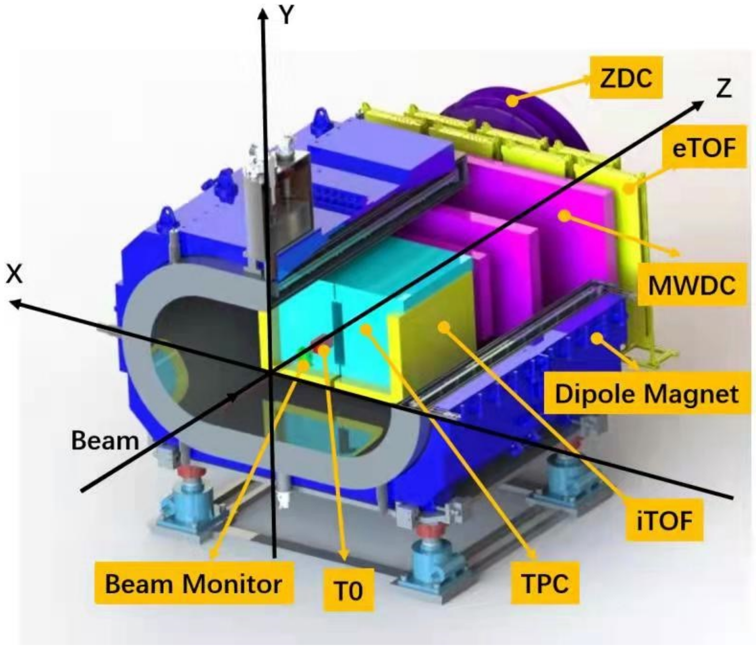
Topmetal CMOS Array



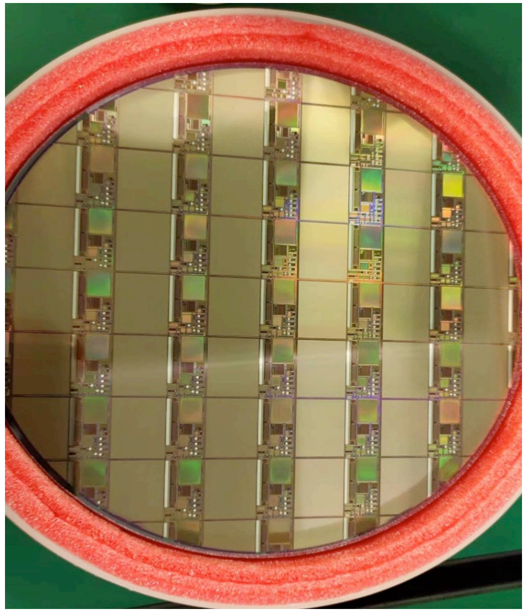
Topmetal Read-out Plane

Application III — CEE

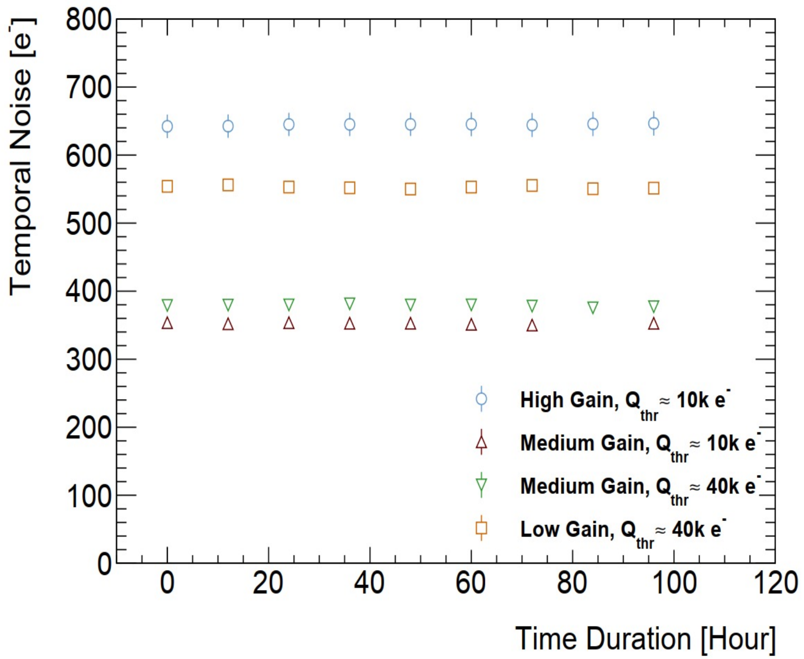
- Purpose: Non-destructive measurement of beam particle positions to determine the reaction point in the CEE
- System composition: gas chamber and field cage, front-end and back-end readout electronics.
- Pixel technology: Topmetal chip provides high spatial resolution (≤50 μm) and ultra-low noise charge sensing.
- Performance: Long-term tests show <1 % noise variation and <3 % threshold drift.



CEE spectrometer schematic



Topmetal-CEE

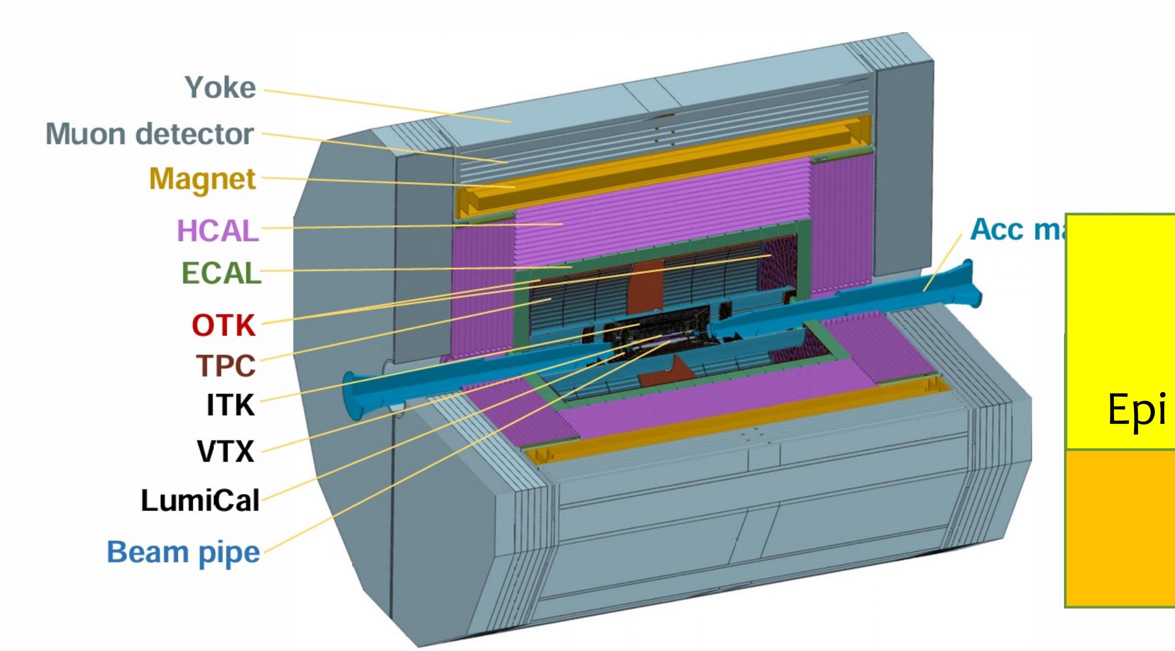


Noise stability plots

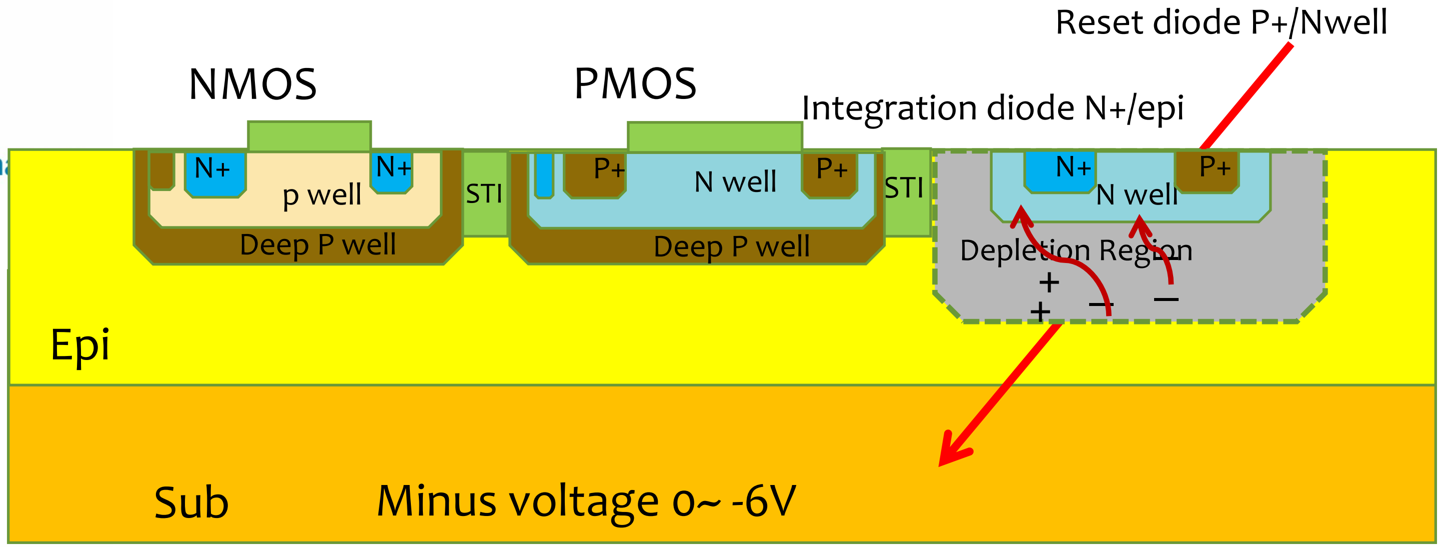
MIC Chip for CEPC Vertex Detector

■ MIC Series – CMOS MAPS for the CEPC Vertex and Tracking Detectors

- **Aims to provide high spatial resolution, low power, and fast readout for vertex tracking.**
- **Based on TowerJazz 0.18 μm CIS process with high-resistivity (≥1 kΩ·cm) epitaxial layer.**
- **Employs deep P-well isolation and thin oxide (< 4 nm) for strong radiation tolerance.**
- **Forms the foundation of a domestic MAPS technology chain for future HEP experiments.**

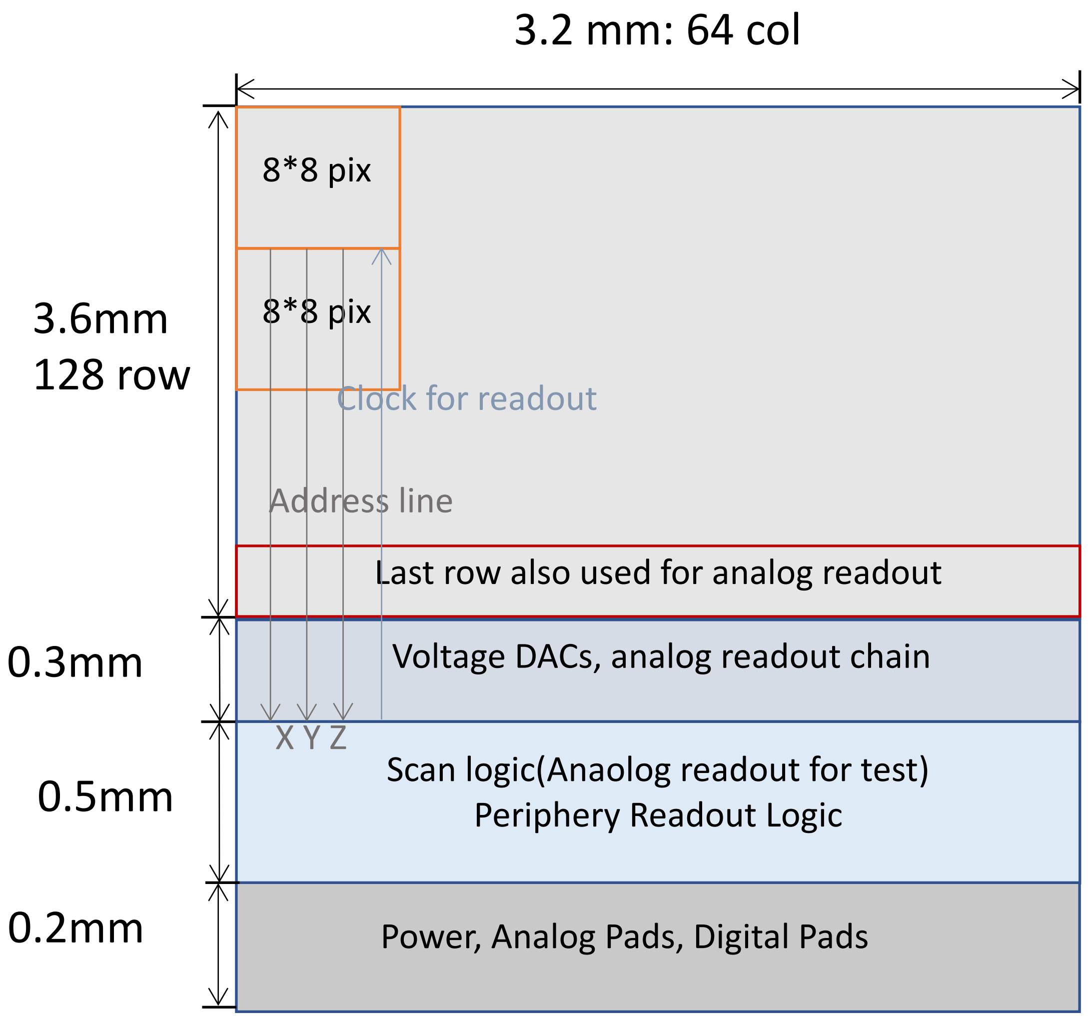


CEPC detector layout



TowerJazz CIS cross-section diagram

MIC Chip Architecture and Design Features



Readout architecture diagram

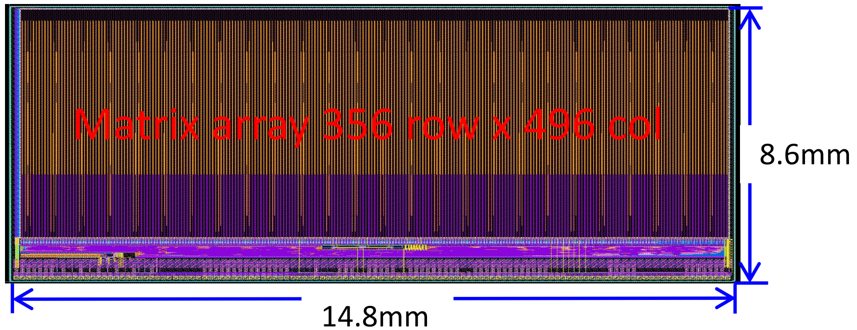
MIC4 Chip: 3.2 × 3.7 mm², 128 × 64 pixels, integration time < 5 μs, 40 MHz/pixel, power < 80 mW/cm².

Pixel pitch: 20 × 29 μm² → single-point precision ≈ 3–5 μm.

Readout modes: triggered or continuous; non-zero suppression for fast data reduction.

Multi-metal (6-layer) layout for signal integrity

MIC5 prototype under testing with improved timing and readout stability.



MIC5 layout

Summary & Future Prospects

Summary

- Topmetal series provides a flexible, low-noise, scalable pixel readout solution
- Demonstrated applications in space, collider, and neutrino experiments
- Continuous R&D will support future HEP detector upgrades and China's CEPC program

Future Prospects

- Higher time resolution & radiation hardness
- MAPS process localization (domestic CMOS line)
- Expansion to medical imaging, space exploration, neutrino physics, and CEPC detector subsystems