Fully digital SiPM for fast amplitude and timing measurements

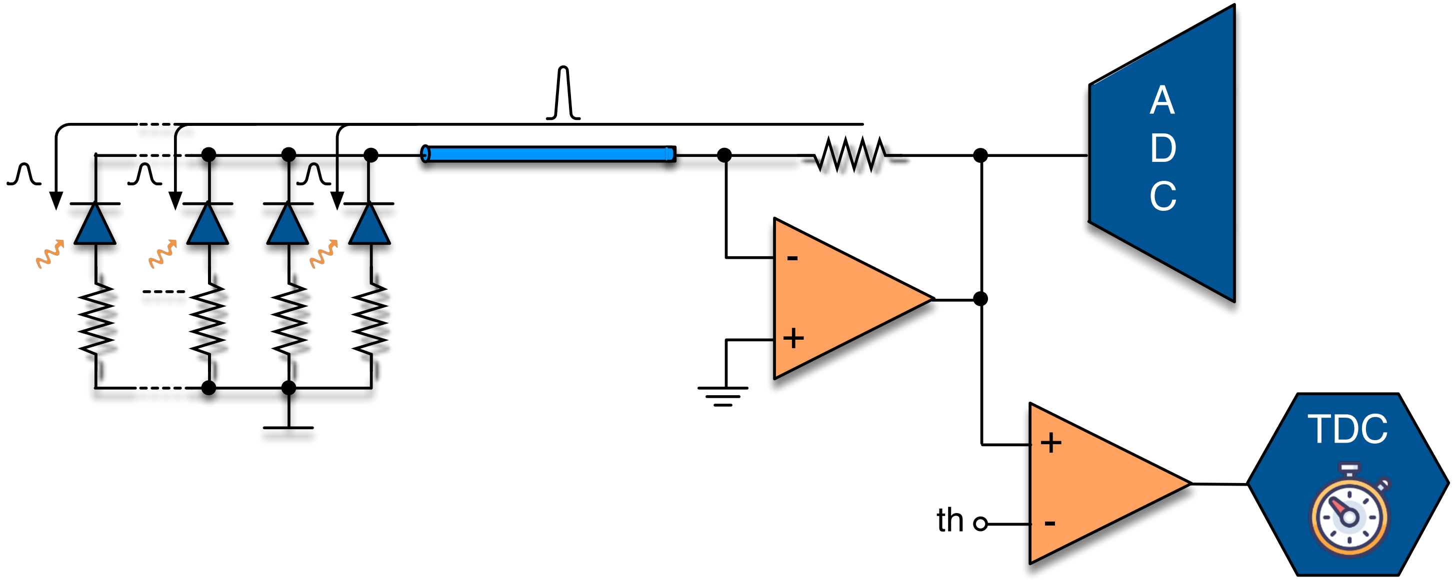
L. Ratti, T.M. Floris
Università di Pavia and INFN Pavia, Italy

on behalf of the ASPIDES collaboration

ASPIDES

INTERNATIONAL WORKSHOP
ON THE HIGH ENERGY CIRCULAR ELECTRON POSITRON COLLIDER
CEPC 2025
November 6-10, 2025 Guangzhou, China

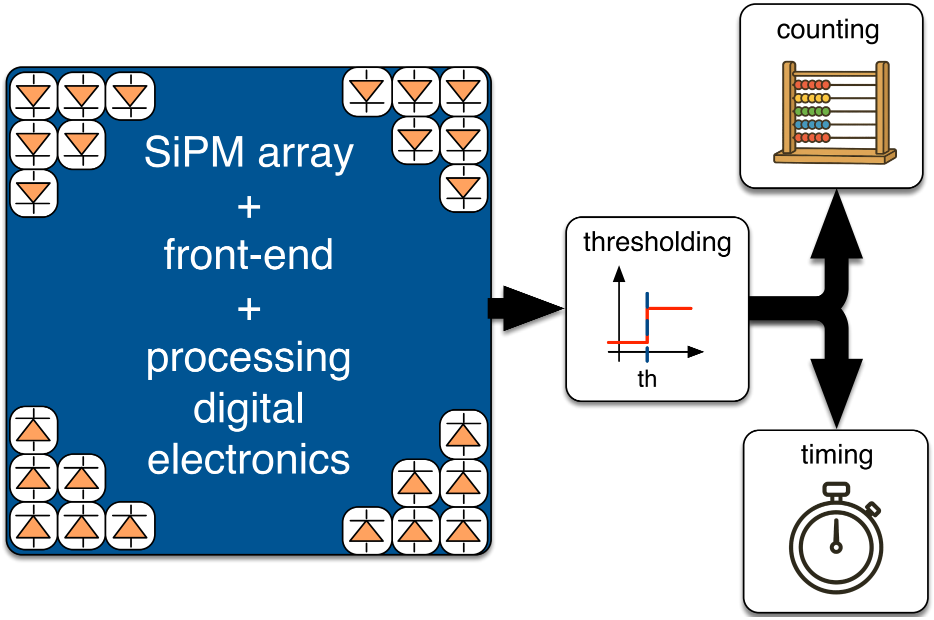
Analog vs digital SiPMs



- Analog SiPMs: hybrid approach for the readout of a SPAD array, need amplification and A/D
  - best technology can be selected for both sides of the system
- Digital SiPM: typically monolithic and CMOS-based, with direct numeric readout
  - simpler assembly phase

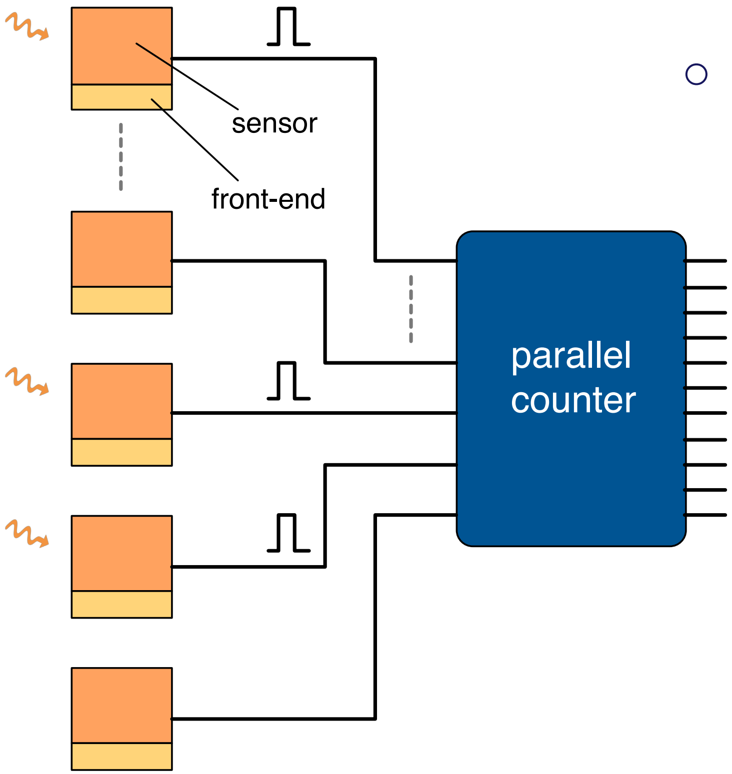
- Direct digital vs digital-to-analog-to-digital conversion
- No random noise from analog FE, no fixed-pattern noise, no quantization noise
- Easier linearization and calibration
- Preservation of timing signal integrity – local measurement of locally generated signals
- Possible issues: impact on PDE/fill factor, heat dissipation close to the sensor

- Parallel readout of current signals → analog SiPMs are much faster

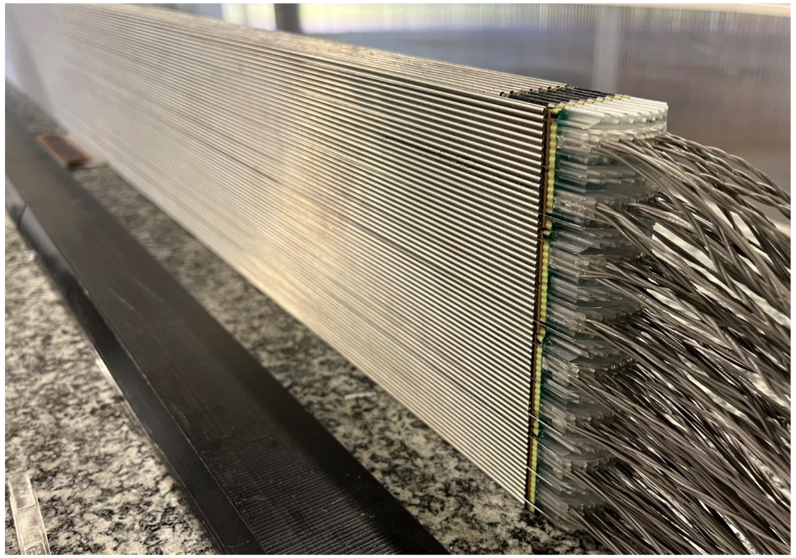


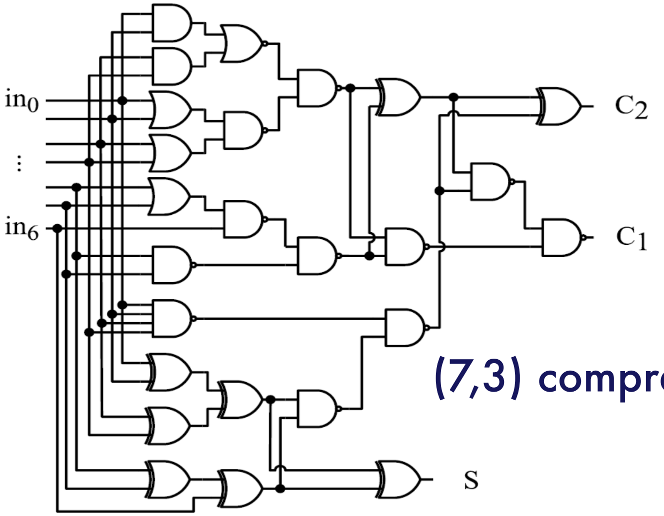
Fast counting with digital SiPMs

- Development of a digital SiPM for applications with scintillating fibers in dual-readout calorimetry
- Proposal: implement a digital version of the current adding architecture used in analog SiPM readout



- Parallel counter: asynchronous digital network collapsing *p* input lines into *q* output bits
  - $p \,\overline{<}\, q^{2}\text{-}1$, the output binary word representing the number of input lines set to 1
  - large number of parallel connections
  - trade-off between area and modularity





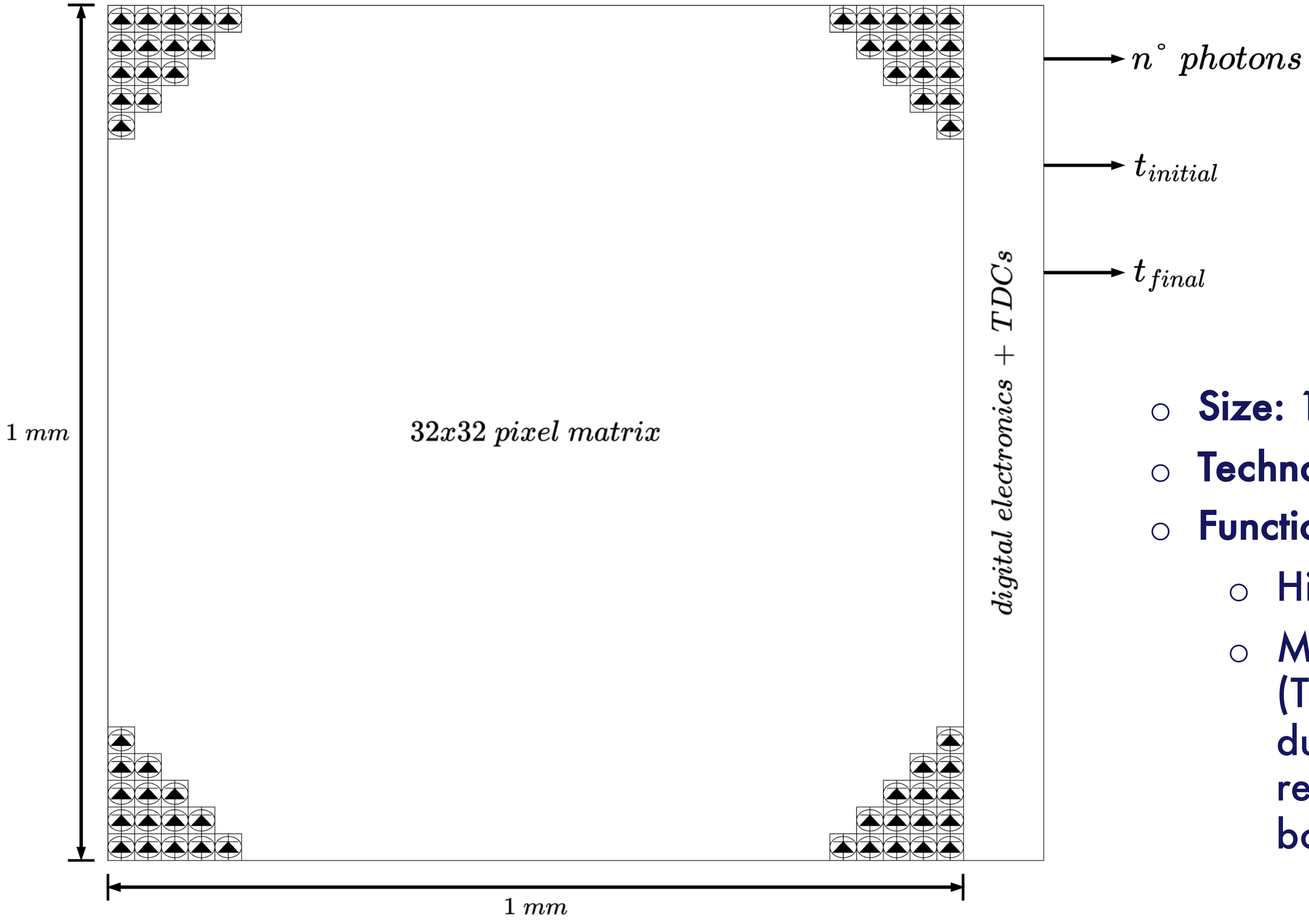
(7,3) compressor

Mehta et al. 1991

Requirements for dual-redout calorimetry

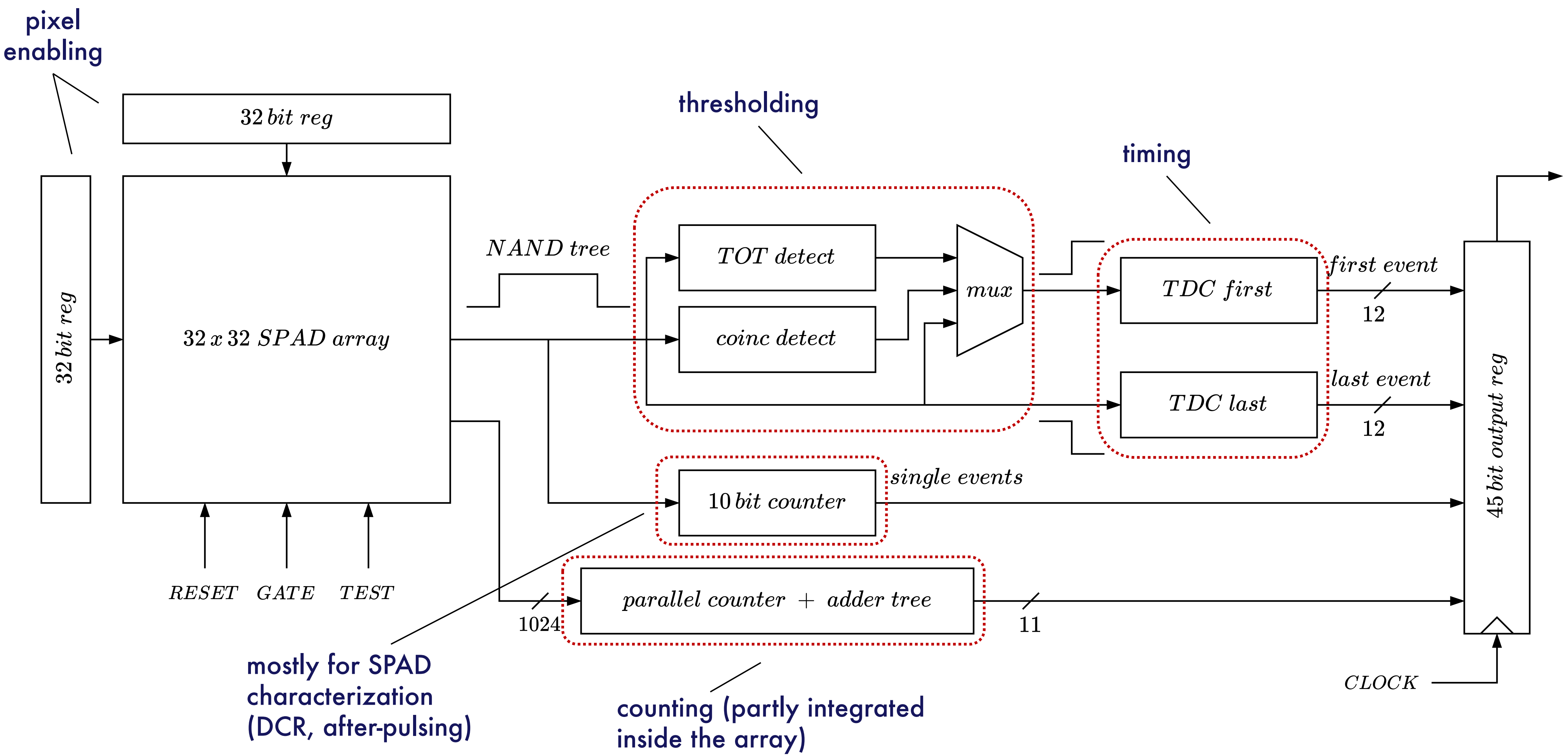
	Scintillating
Unit area (mm^2)	1 x 1
Micro-cell pitch (μm)	25 to 30
Macro-pixel (μm^2)	500 x 500 (or less)
PDE (%)	$\geq$20
DCR (kHz)	Not crucial
AP (%)	As low as possible ($\approx$ 1)
Xtalk (%)	As low as possible (few %)
Trigger	External
Data: light intensity	Number of fired cells in 1 or 2 time windows (tenths ns long)
Data: time	Time of Arrival in the time window (< 100 ps), possibly TOT
Final - Package	Strip with 8 units
Connection	BGA

Digital SiPM prototype

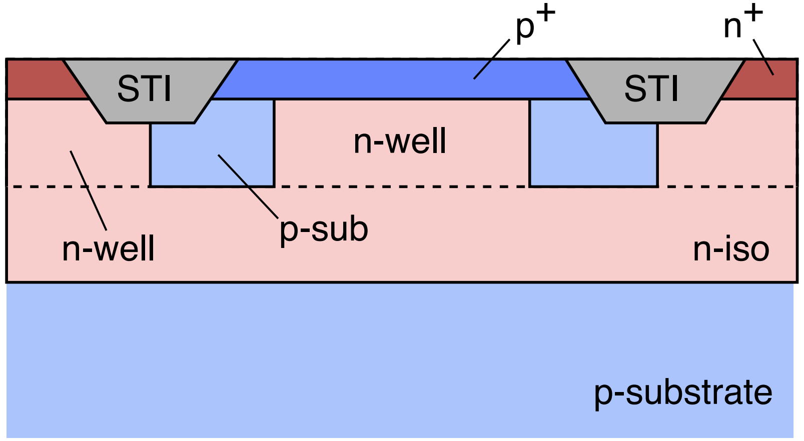


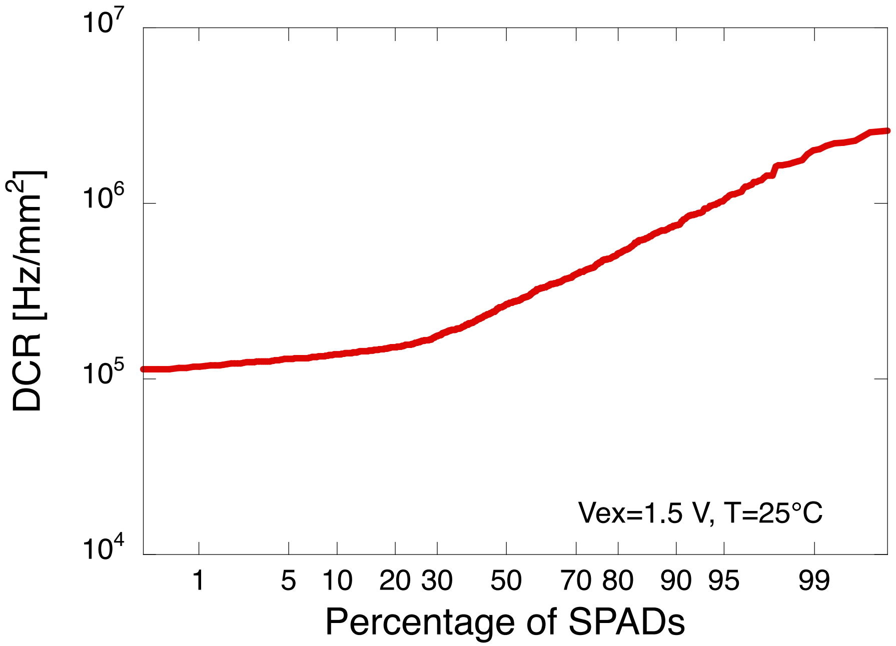
- **Size:** 1024 pixels, about1 mm^2
- **Technology:** 110 nm CIS
- **Functions:**
  - Hit pixel counting, 11 bits
  - Measurement of time of arrival (ToA) of the first photon and duration of the signal (ToT), 12 bit resolution and LSB<100 ps for both

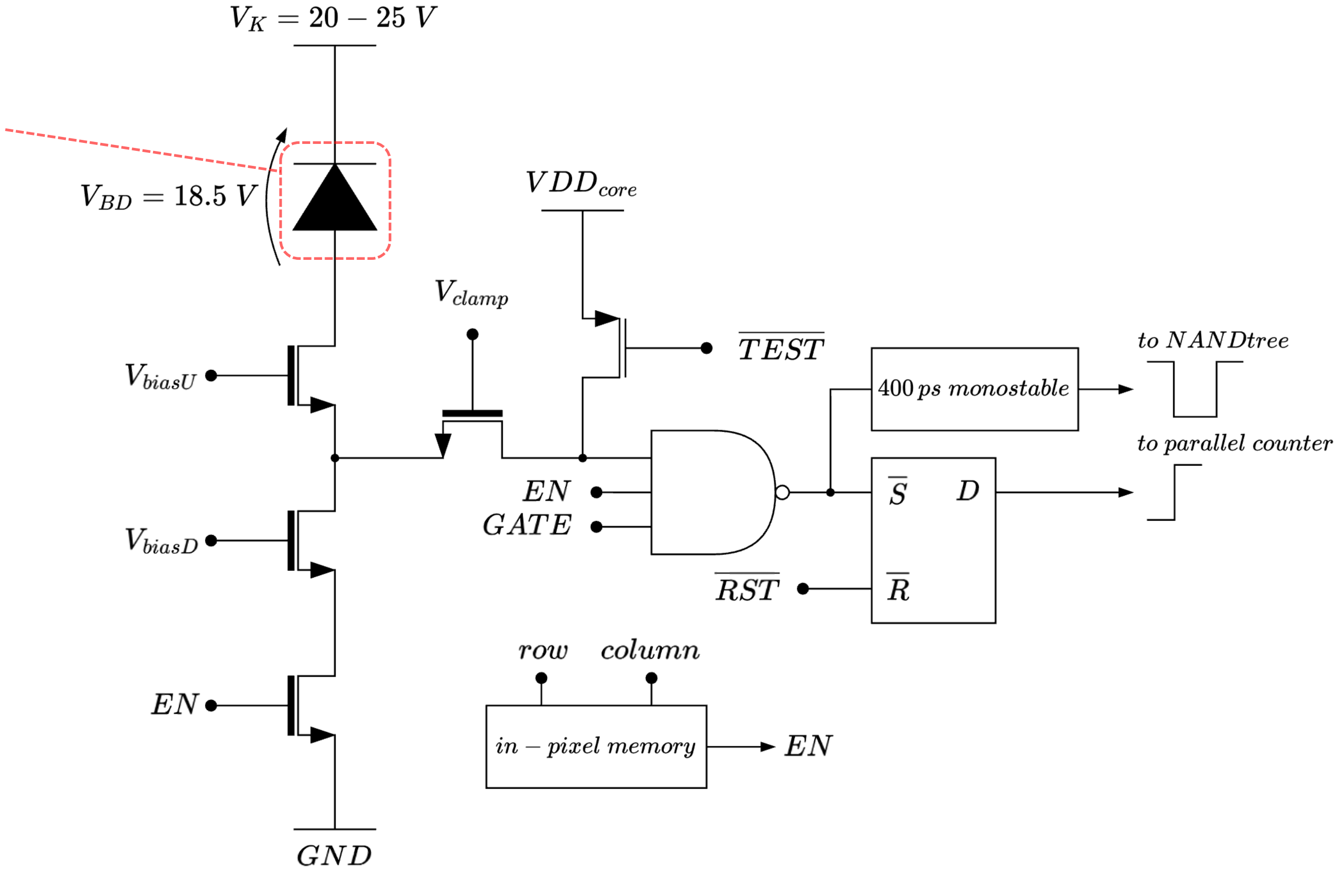
Chip architecture



SPAD and front-end

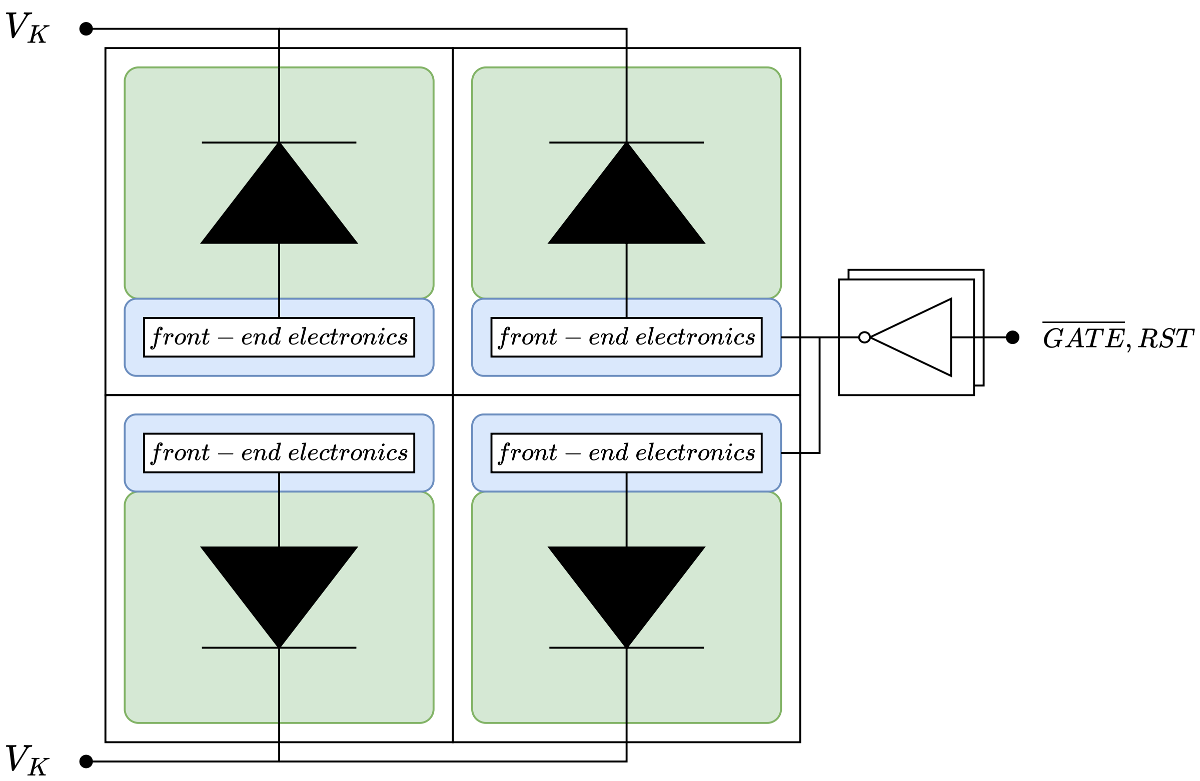


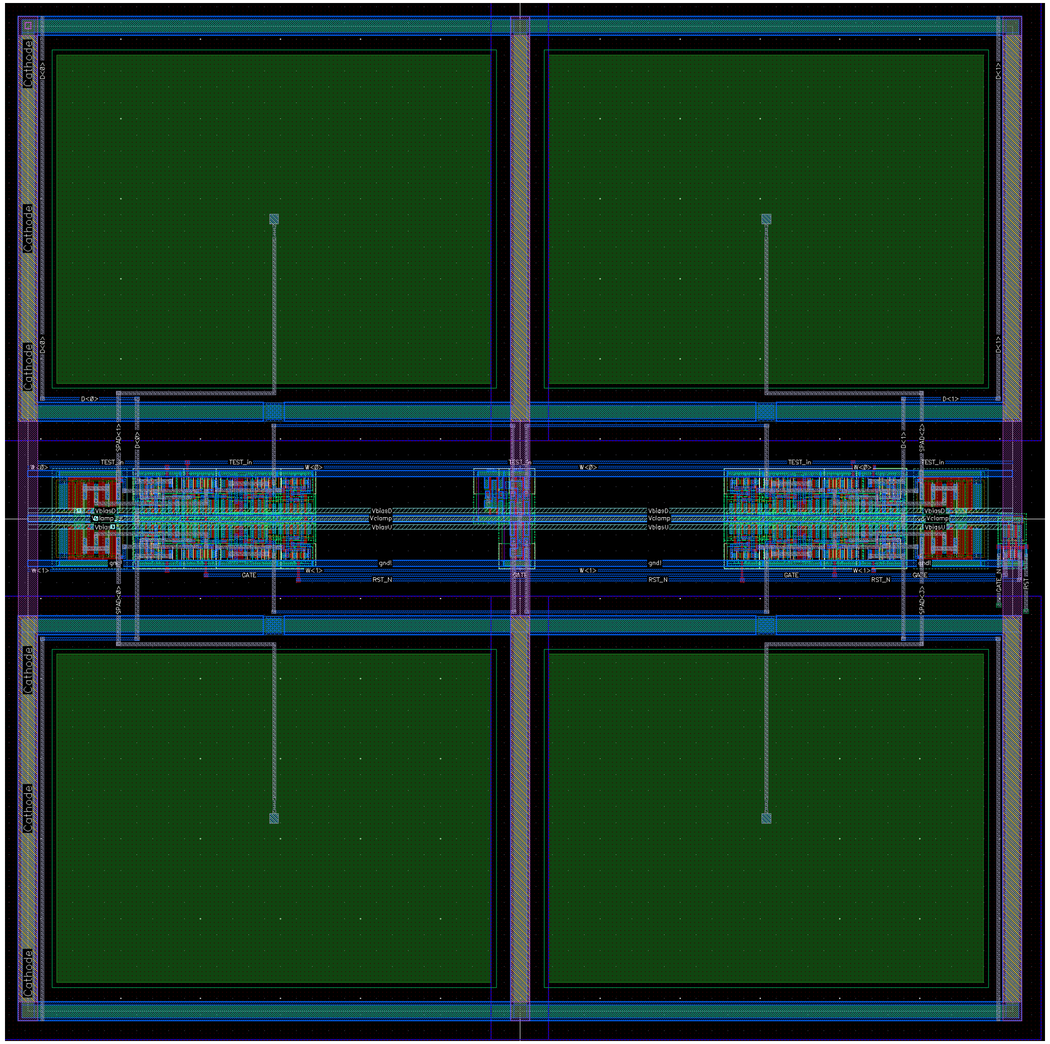




- Cascode quenching network to sustain up to 6 V excess voltage
- Individual pixels can be enabled/disabled
- Global gate signal

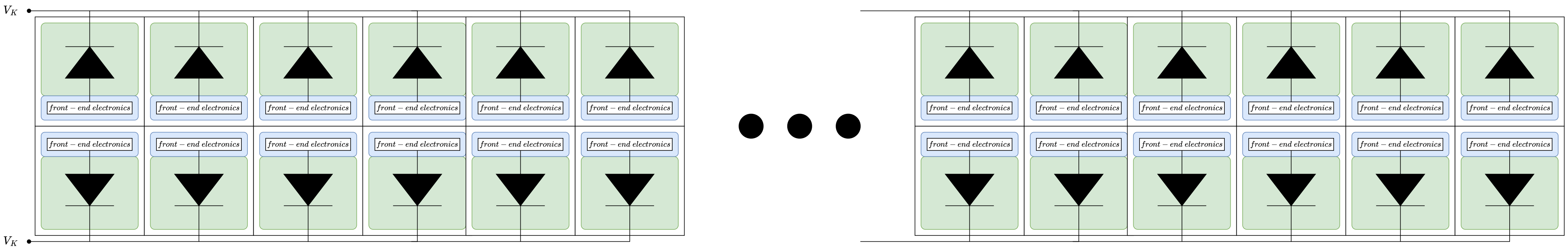
Macro-pixel

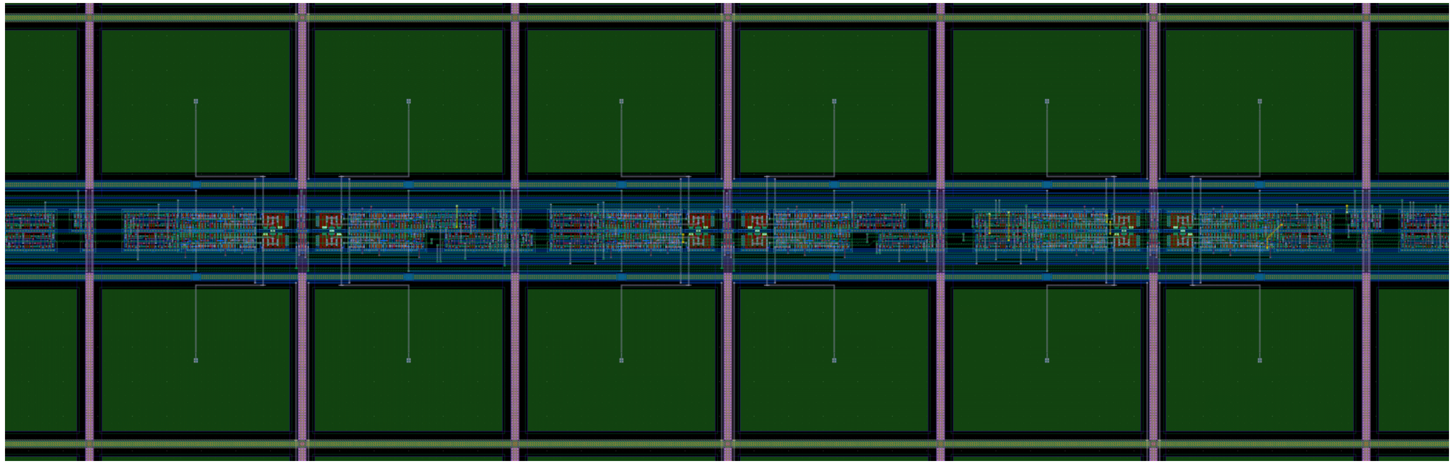




- Macropixel with 4 pixels sharing n-well and bias for fill-factor optimization (50%)
- 30 µm pitch pixel, active area + electronics

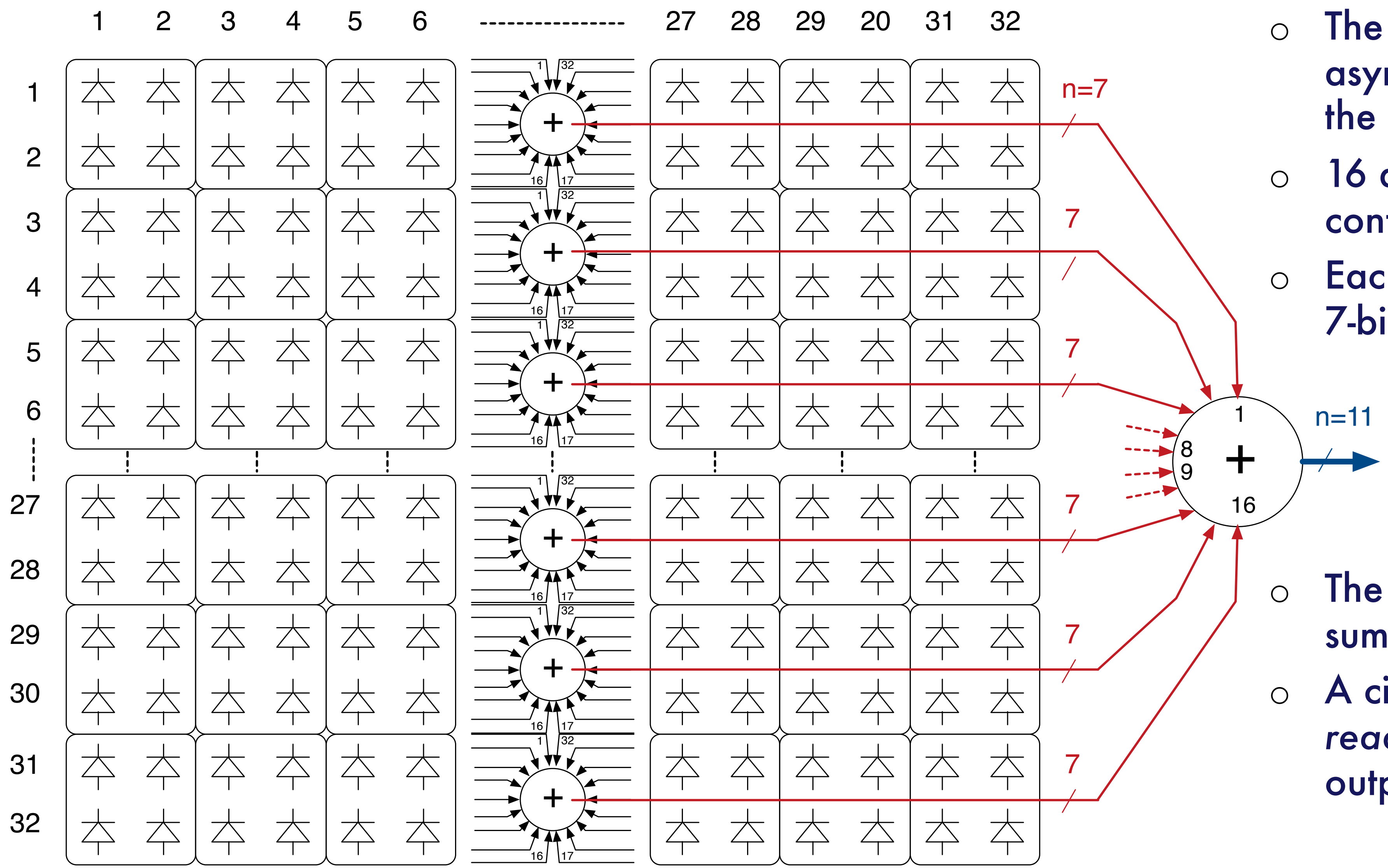
Double-row





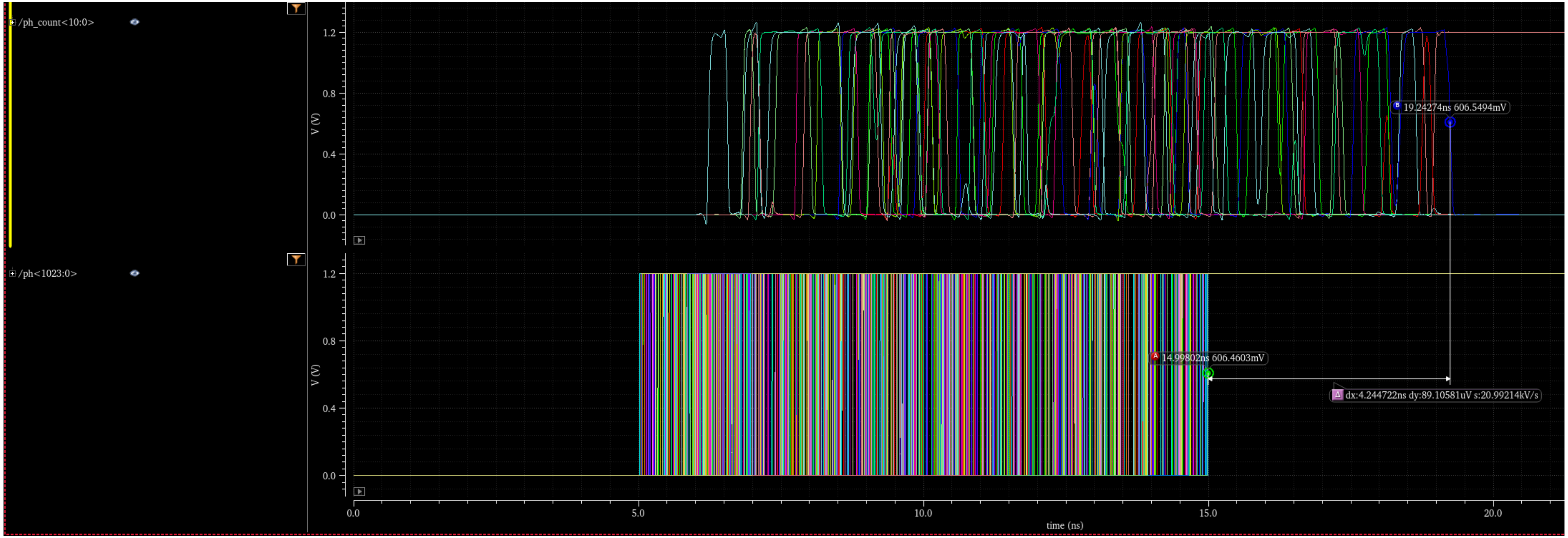
- A double-row consists of 16 macro-pixels and represents a counting and a timing module
- Outputs of the double-rows are combined outside the array
- Stacking 16 double-rows makes a full 32x32 array

Parallel counter architecture



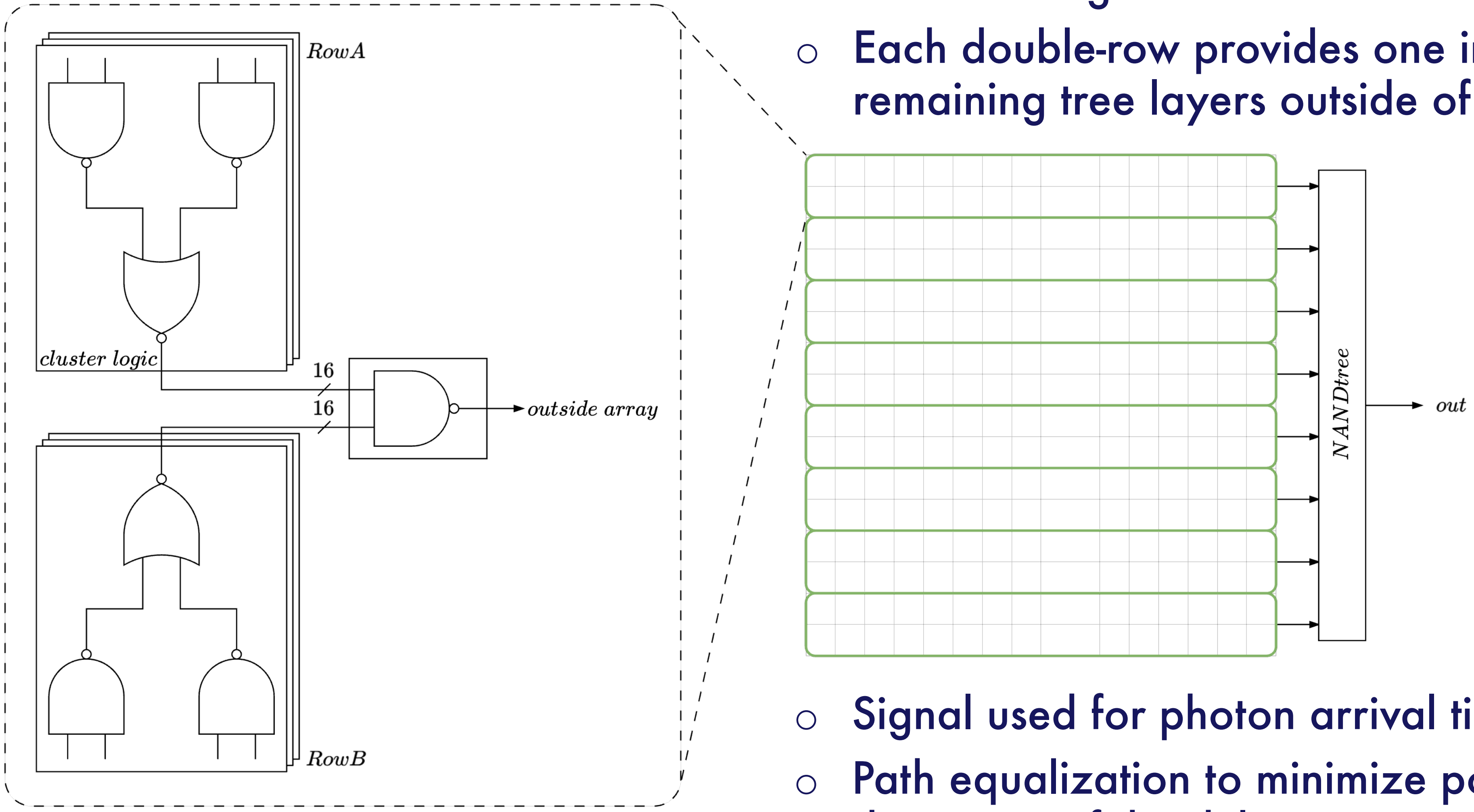
- The parallel counter is an asynchronous circuit providing the number of hit cells
- 16 double-rows, each containing 64 pixels
- Each double-row generates a 7-bit word
- The 16 output words are summed up outside the array
- A circuit generates a *sum-ready* signal once the counter output has settled

Parallel counter simulations – signal settling



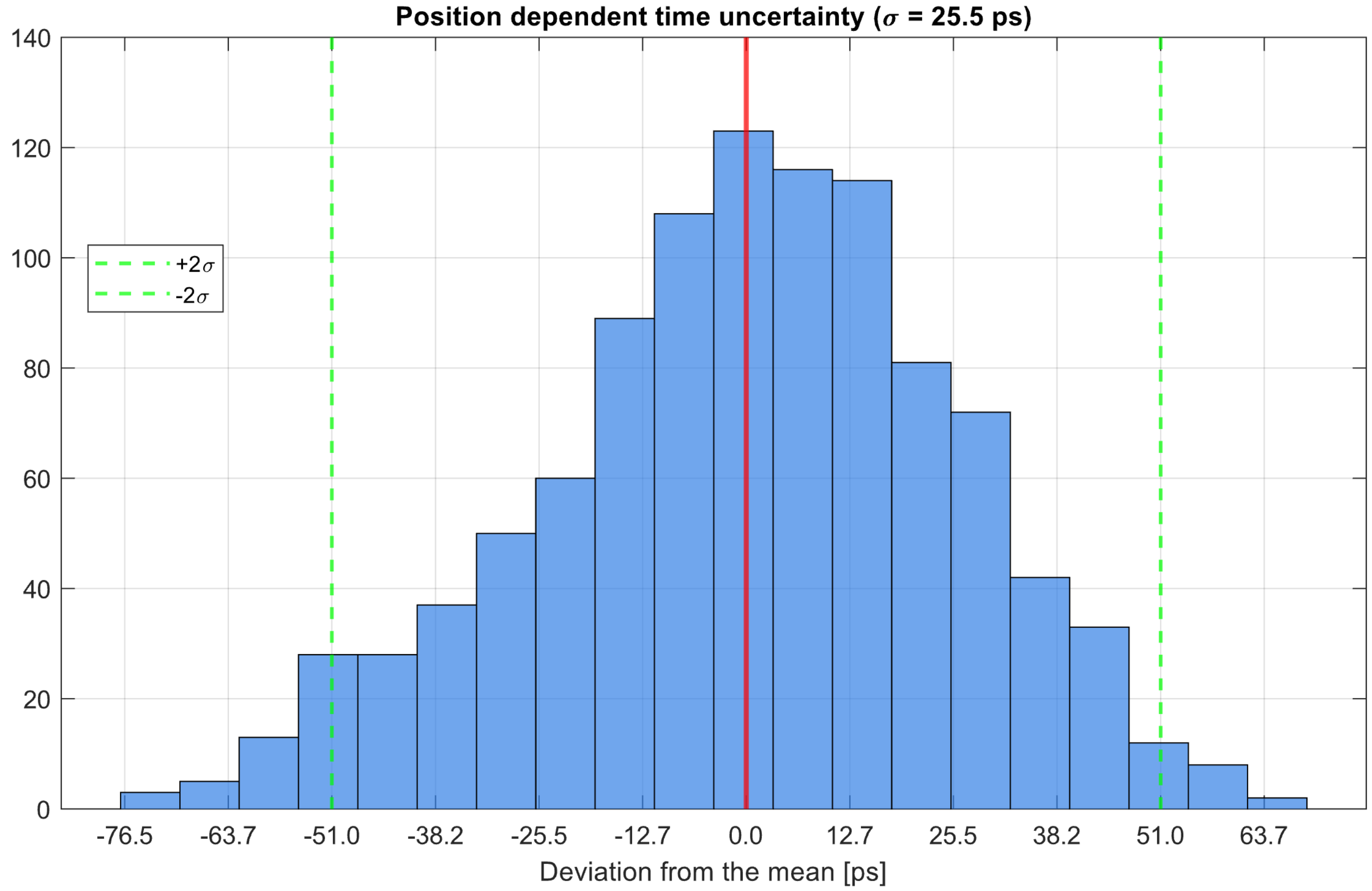
- Case of all of the pixels (1024) hit randomly within 10 ns (t=5 ns to t=15 ns) in the slow-slow corner: delay between last photon and signal settling at the counter output
  - 4.2 ns from schematic simulations (picture above)
  - 15.8 ns from post-layout simulations – if needed, delay can be reduced by increasing the driving strength of the logic gates, room still available in the array

Timing circuits – NAND tree



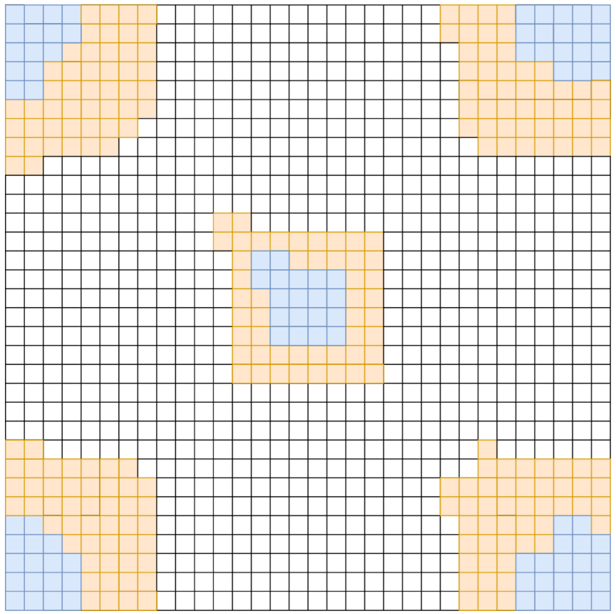
- Reads the signal from the front-end monostable
- Each double-row provides one input to the remaining tree layers outside of the array
- Signal used for photon arrival timing
- Path equalization to minimize position dependent dispersion of the delay

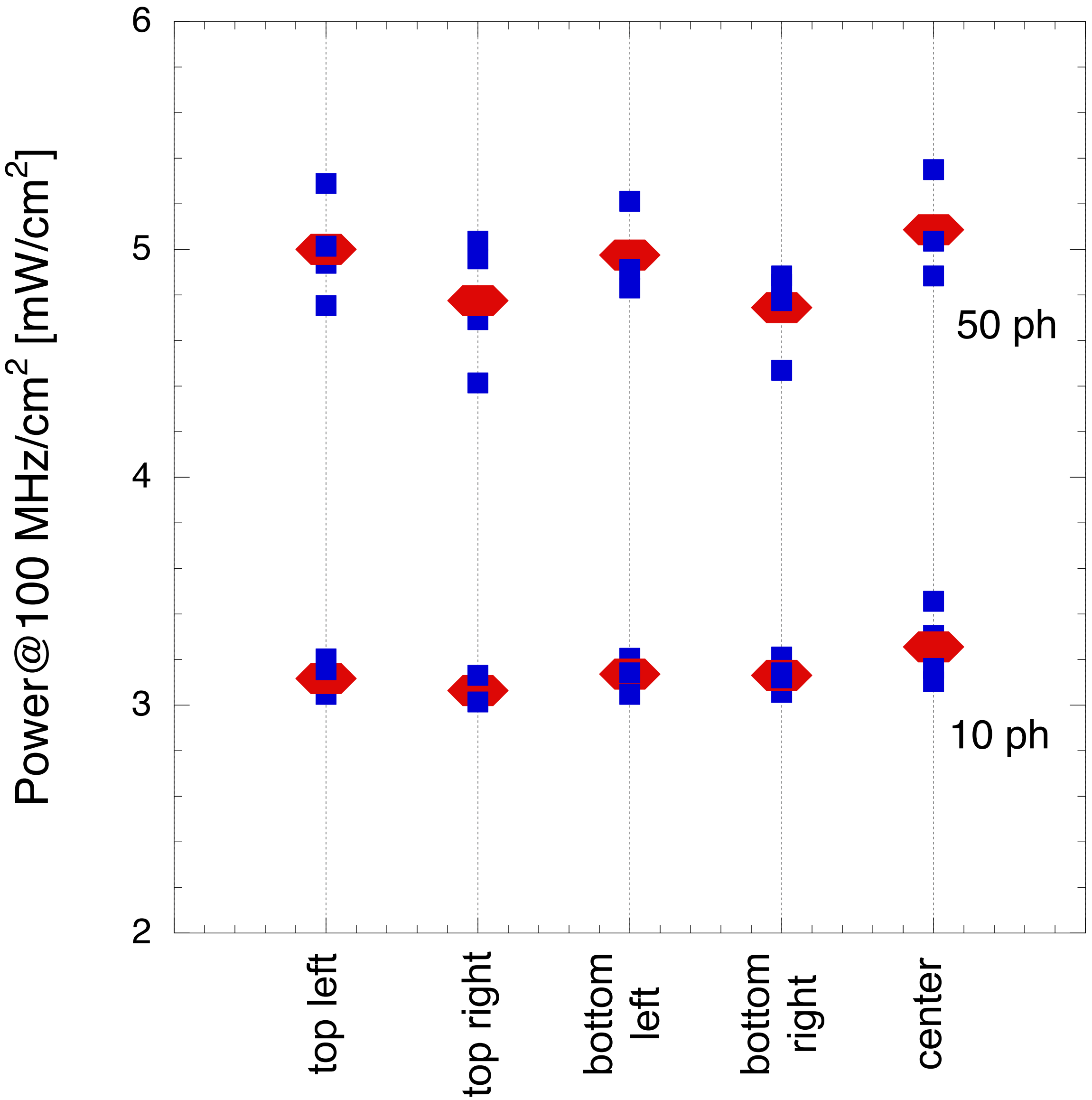
Fixed-pattern uncertainty



- Rising edge of NAND tree signal is used to trigger the TDC (<100 ps resolution) for photon ToA measurements
- Distribution of the rising edge time when one pixel at a time is stimulated - Std dev=25 ps (fixed-pattern time uncertainty)

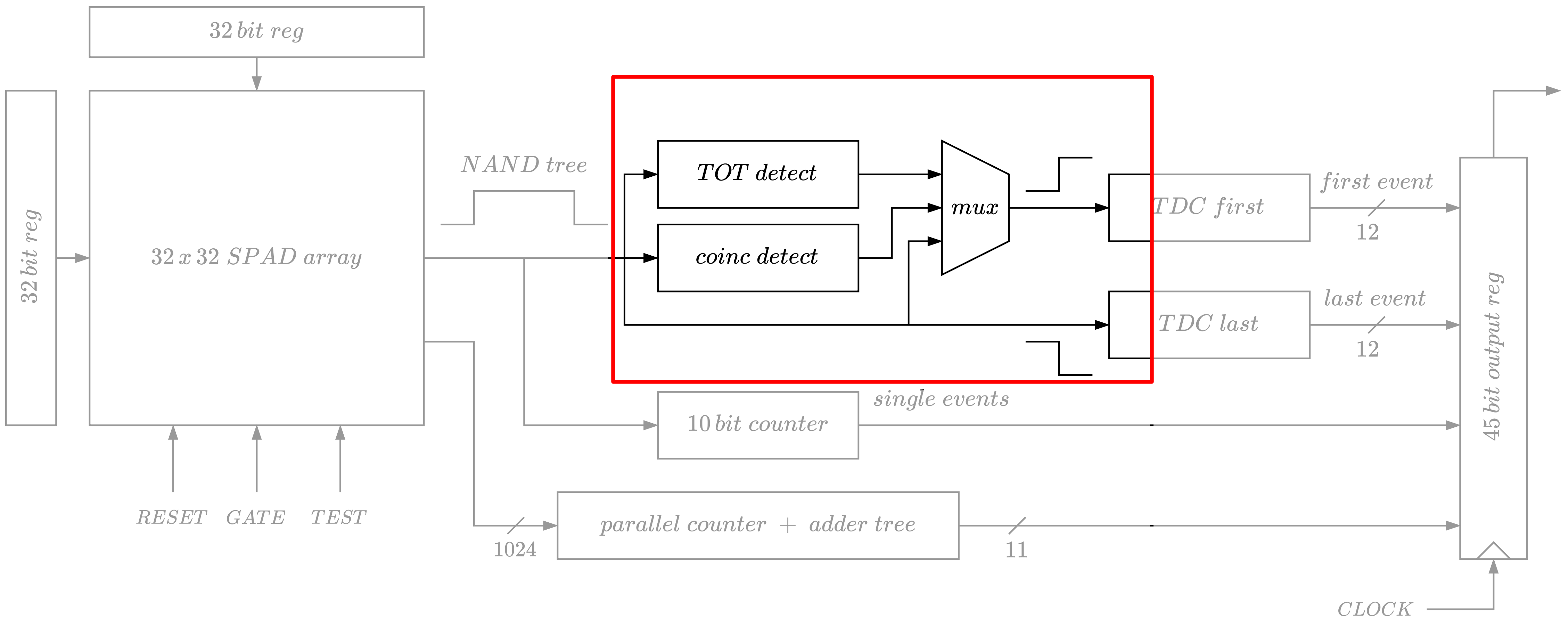
Power dissipation



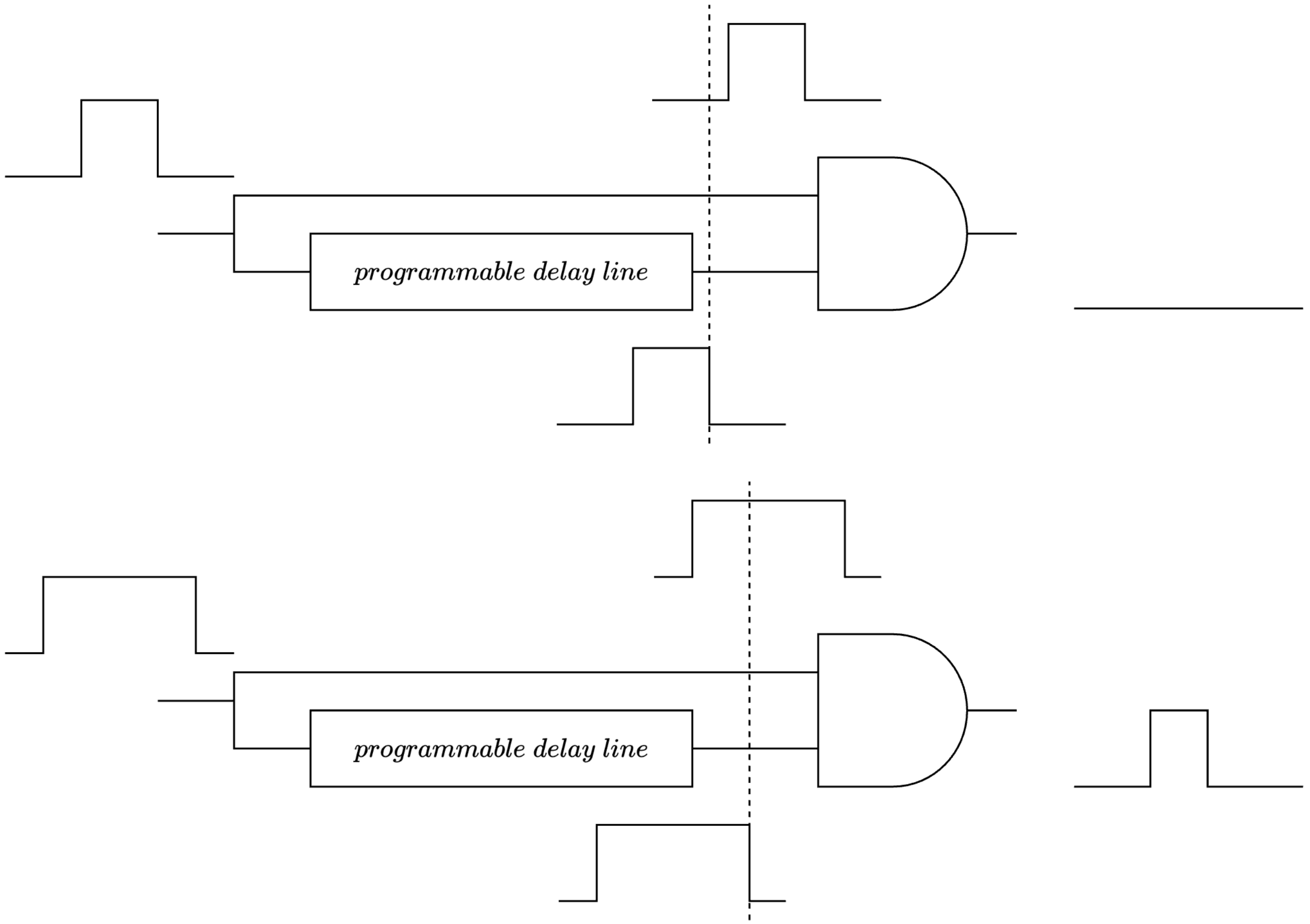


- Simulation performed on the extracted view of the entire SiPM
- Power dissipation depends on the number of hit cells and duty cycle
- Power dissipation from TDCs not included
  - about 200 pJ per TDC to convert a 200 ns time interval, corresponding to about 40 mW/cm^2 at a hit rate of 100 MHz/cm^2

TDC triggering options



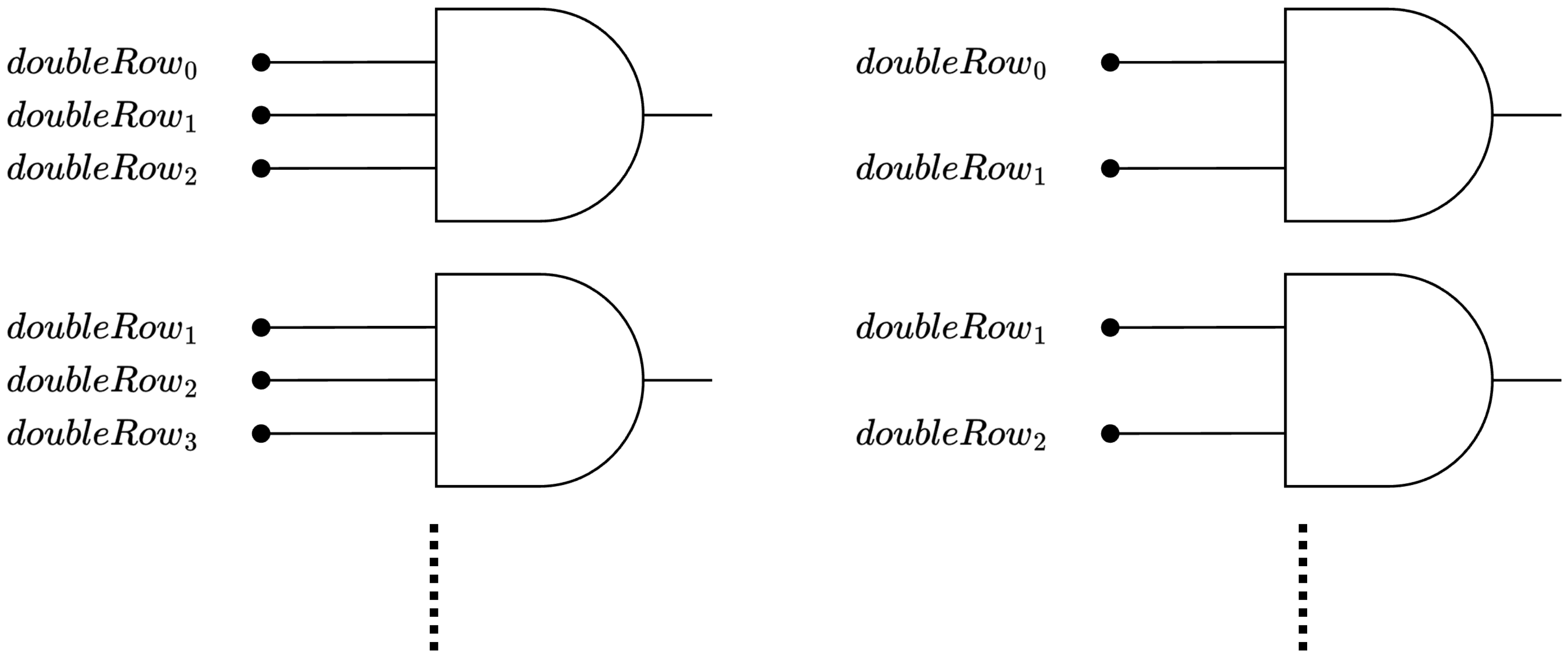
Time over threshold



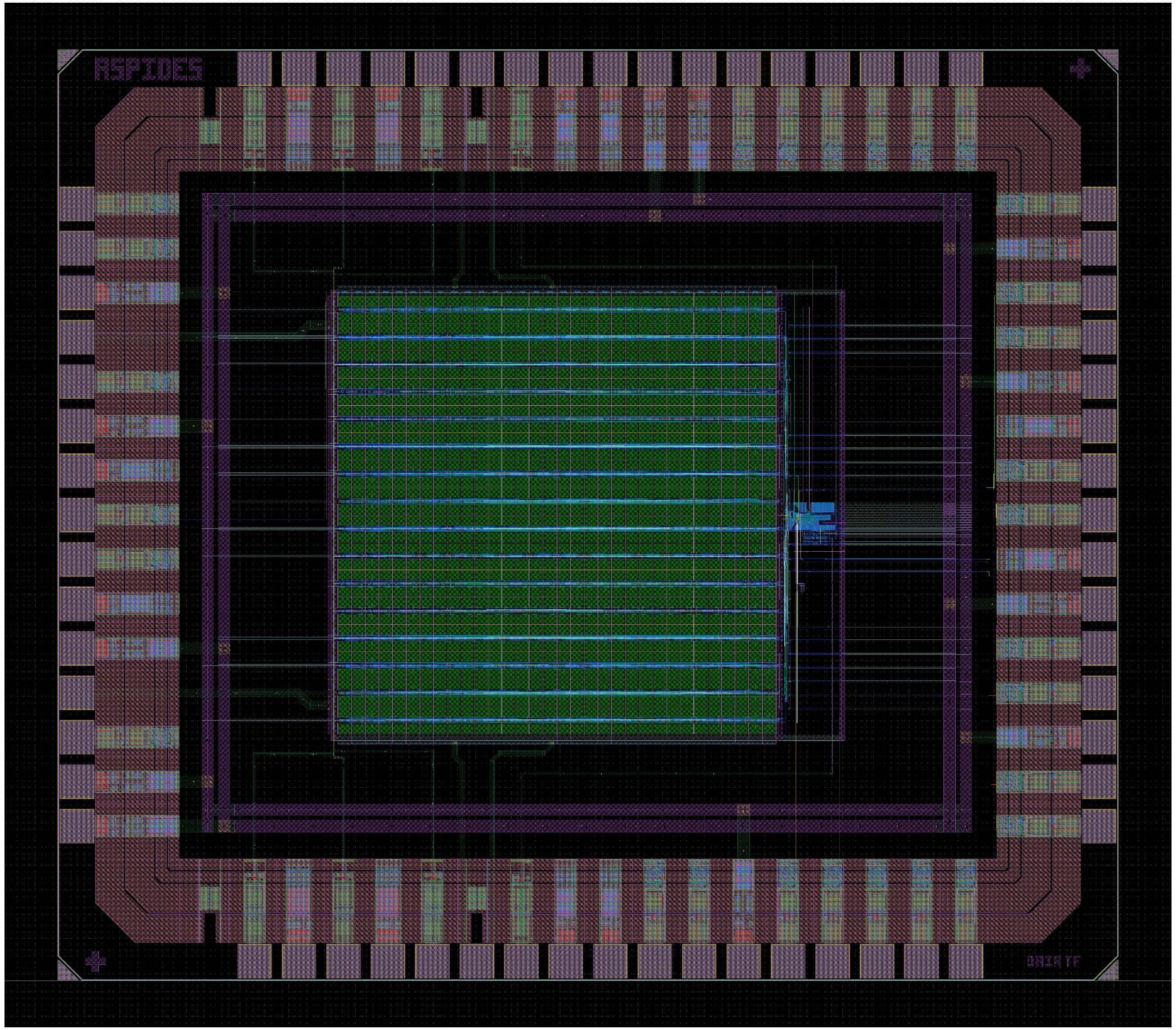
- Provides a trigger signal for the TDC in case the NAND tree signal exceeds a given duration
- Programmable 3-bit delay line

Coincidence detection

- Provides a trigger signal to the start TDC when a coincidence is detected
  - between two adjacent double-rows or
  - among three adjacent double-rows



Prototype layout



- CIS 110 nm, 6 ML 1P
- 5 mm^2
- 64 PADS
  - 14 digital input
  - 14 digital output
  - 8 bias voltage
  - 24 power supply
  - 4 SPAD bias
- MPW run to start in December 2025, chip expected for end Q1/beginning Q2 2026

Conclusion and outlook

- Fully digital SiPM in 110 nm CMOS under development, with potential for fast counting and ToA and ToT measurement with 100 ps resolution
  - distributed parallel counter ensuring measurement times not exceeding a few tens of ns
  - ToA and ToT measurement based on two 12 bits TDCs with less than 100 ps resolution
  - different approaches available for noise mitigation, including pixel enable/disable, global gating and a few thresholding options
  - MPW run to start end of 2025
- Next steps
  - characterization of the prototype in the first semester of 2026
  - design of a demonstrator including 8 SiPMs which can be operated based on a minimum set of I/O signals + bias
  - gathering idea for (almost) individual photon timing in a shower