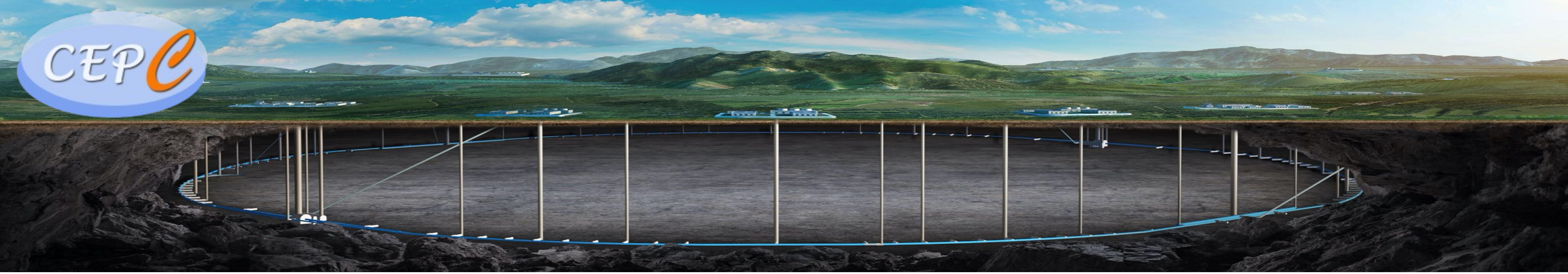

The overall readout electronics for the reference detector at CEPC

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On behalf of the CEPC electronics group

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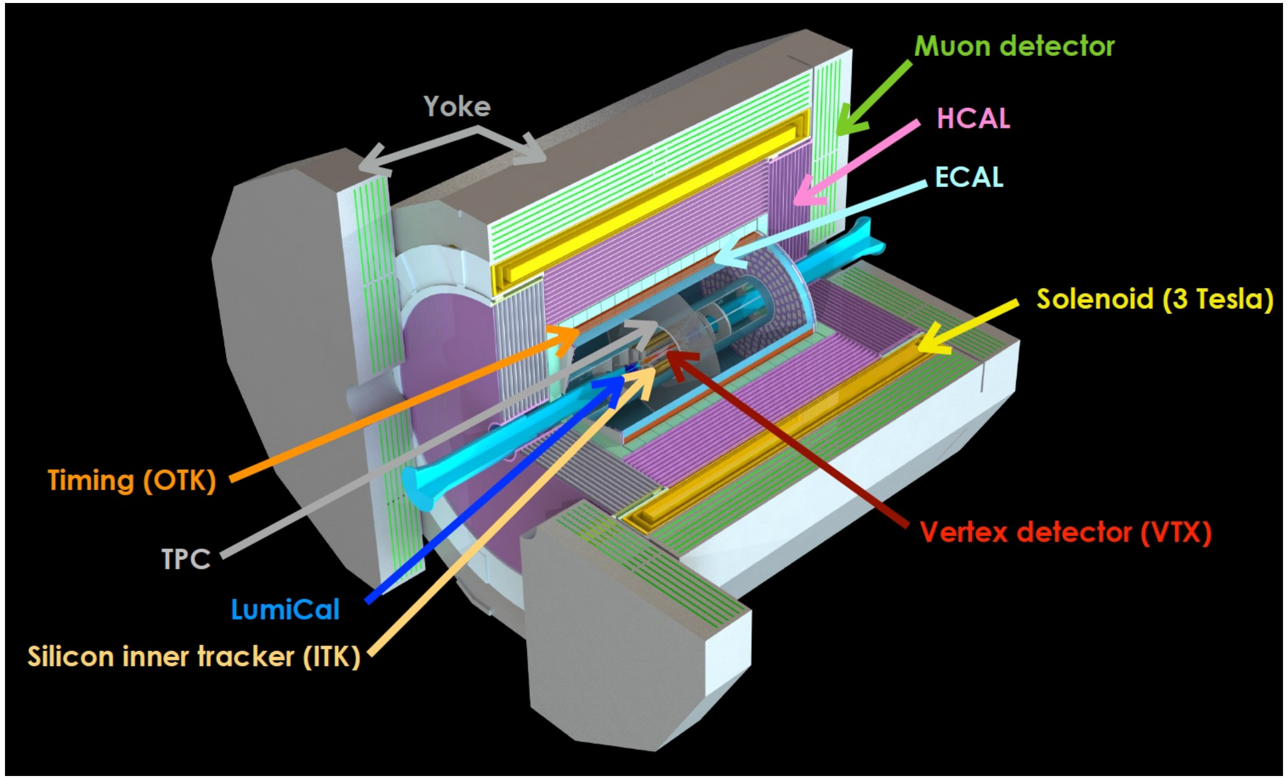
November 8th, 2025 - CEPC Workshop 2025, Guangzhou

Outline

- Requirements for the electronics
- Global framework of the electronics system
- Common electronics design & frontend ASICs
- Research team and working plan
- Summary

The Reference Detector



Sub-system	Technologies
Beam pipe	Beryllium, ϕ 20 mm
LumiCal	Silicon tracker + LYSO crystals
Vertex	Si Pixels: CMOS MAPS+stitching
Inner tracker (ITK)	Si Pixels: CMOS MAPS 55-nm
Gas detector	TPC with high granularity
Outer tracker (OTK)	AC-LGAD → TOF
ECAL	4D transverse crystal bars
HCal	Glass scintillator, SiPM + Fe
Magnet	LTS Solenoid
Muon	Plastic scintillator bars, SiPM

The electronic system is to readout tens of millions of detector channel in real time.

Requirements for the electronics

CEPC Baseline Operation Scenario

Operation mode	$\sqrt{s}$ (GeV)	SR power (MW)	$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	$\int \mathcal{L}$/year (ab^{-1})	Years	Total $\int \mathcal{L}$ (ab^{-1})	Event yields
H	240	30	5	0.65	15	10	2.0×10^6
Z	91	12.1	26(*)	3.2	4	13	5.6×10^{11}
W^+W^-	155-170	30	16	1.2	1	1.2	1.0×10^7(†)

This talk will focus on electronics baseline design

CEPC Upgraded Scenario

Operation mode	$\sqrt{s}$ (GeV)	SR power (MW)	$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	$\int \mathcal{L}$/year (ab^{-1}, 2 IPs)	Years	Total $\int \mathcal{L}$ (ab^{-1}, 2 IPs)	Event yields
H	240	50	8.3	2.2	10	21.6	4.3×10^6
Z	91	50	192(*)	50	2	100	4.1×10^{12}
W^+W^-	155-170	50	26.7	6.9	1	6.9	5.5×10^7
$t\bar{t}$	360	50	0.8	0.2	5	1.0	0.6×10^6

Future upgrade possibility considered

Critical Input from Sub-Det & MDI

	VTX	ITK	OTK	TPC	ECAL	HCAL	Muon
Chn/ chip	512×1024	512×128	128	128	4-16 (common SiPM ASIC)		
Data Width	32 bit / hit	42 bit / hit	48 bit / hit	48 bit / hit	48 bit / hit		
Cluster size	3 pixel	1.5 pixel	2 strip	N/A	N/A		
Module Size/ Link	32.7 cm^2 / stch chip	423.3 cm^2 / stave	365.7 cm^2 / stave	461 cm^2 / module	856 chn w/ 1.5 cm bar	600 GS / Agg Brd	Agg Brd
Beam-induced background rate (MHz/cm^2)							
Higgs	6.4	3.0×10^{-3}	1.9×10^{-3}	2.4×10^{-3}	6.2×10^{-2}	2.4×10^{-4}	1.4×10^{-6}
LowZ	15.0	5.4×10^{-3}	3.1×10^{-3}	5.2×10^{-3}	1.0×10^{-1}	2.4×10^{-4}	9.2×10^{-7}
Data rate per Link (Mbps)							
Higgs	2.00×10^4	80.0	66.7	53.1	2.55×10^3	6.91	< 10
LowZ	4.71×10^4	144	109	115	4.11×10^3	6.91	< 10

Time window and data rate for TDAQ system

	VTX	ITK	OTK	TPC	ECAL	HCAL	Muon	Total
Time windows (ns)	69	69	69	34000	69	1000	69	
50 MW Higgs mode Full Data (Gbps)	130	21.2	82.7	26.4	752	26.6	<1	1040
Data size / bunch (kB)	12.1	1.98	7.71	2.46	70.1	2.48	<0.1	96.9
Data size / event (kB)	12.1	1.98	7.71	303	70.1	9.92	<0.1	405
12.1 MW Z mode Full Data (Gbps)	307	37.8	139	57.1	1202	27.2	<1	1771
Data size / bunch (kB)	3.20	0.394	1.45	0.595	12.5	0.283	<0.1	18.4
Data size / event (kB)	6.40	0.788	2.90	293	25.0	4.53	<0.1	333

- Safety factor of 2 used for background rate estimation from MDI study
- Endcap detectors have the highest hit rate, mostly from the beam background

Max data rate for the detector:

- 1040 Gbps (for Higgs)
- 1771 Gbps (for LowLumZ)

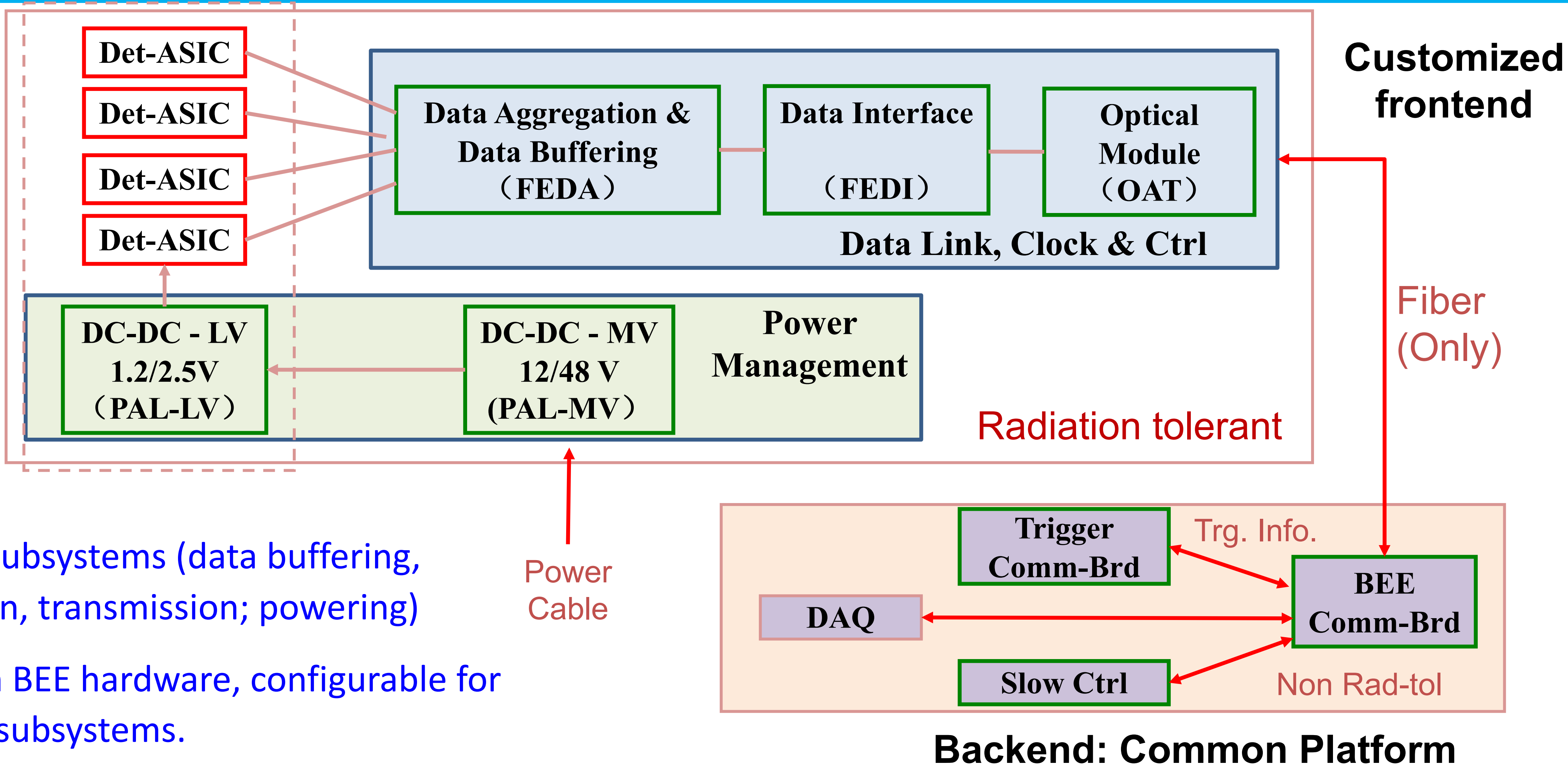
Do we need hardware trigger？

Two main frameworks for the electronics-TDAQ can be simply categorized as full data transmission (FEE-Triggerless readout) & readout with hardware trigger.

	Full data transmission	Hardware Trigger
Where to acquire trigger info	On BEE	On FEE
Trigger latency tolerance	Medium-to-long	Short
Compatibility on Trigger Strategy	Hardware / software	Hardware only
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm
Upgrade possibility on new trigger	High	Limited
FEE data throughput	Large	Small
Maturity	Mature but relatively new	Very mature
Resources needed for calculation	High	Low
Representative experiments	CMS, LHCb, …	ATLAS, BELLE2, BESIII, …

Global framework of the CEPC Electronics

Figure 11.2



- Common subsystems (data buffering, aggregation, transmission; powering)
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is only on BEE

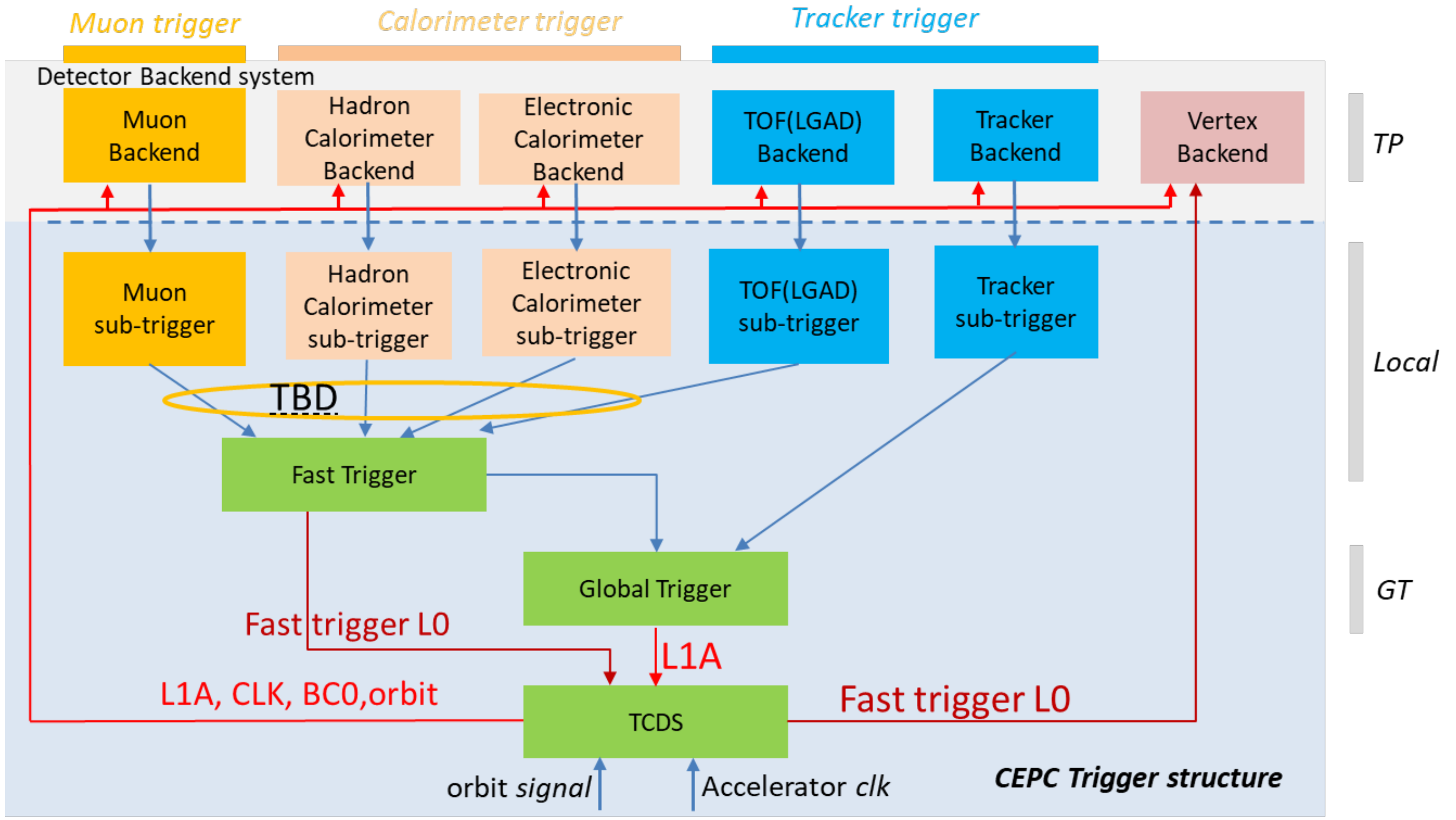
Backup scheme of the framework

The proposed framework was based on the estimated background rate of all sub-det.

Background rate indicated the data link capability can manage the Phase I operation of Higgs & LowLumiZ for first ten years.

For high LumiZ, the detector will upgrade

- VTX, ITK.. (replaceable) can be upgraded with new chips
- ECAL, HCAL (unreplaceable) will have more fiber channels



The hardware trigger scheme can serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency.

Key Electronics Components

Frontend ASICs for sub-detectors

Common Data Link

Common Powering

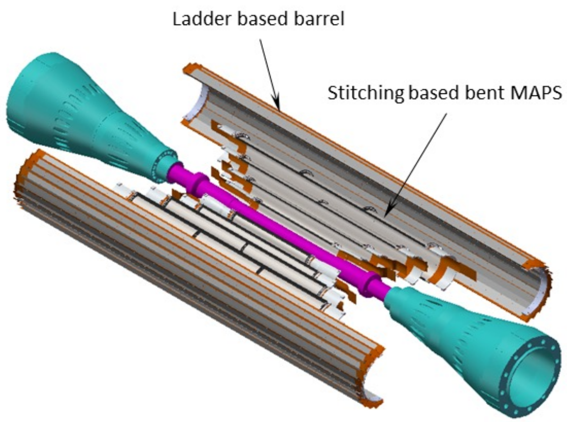
Common Backend Electronics

Alternative Scheme based on Wireless Communication

See Ying Zhang's talk (11:30)

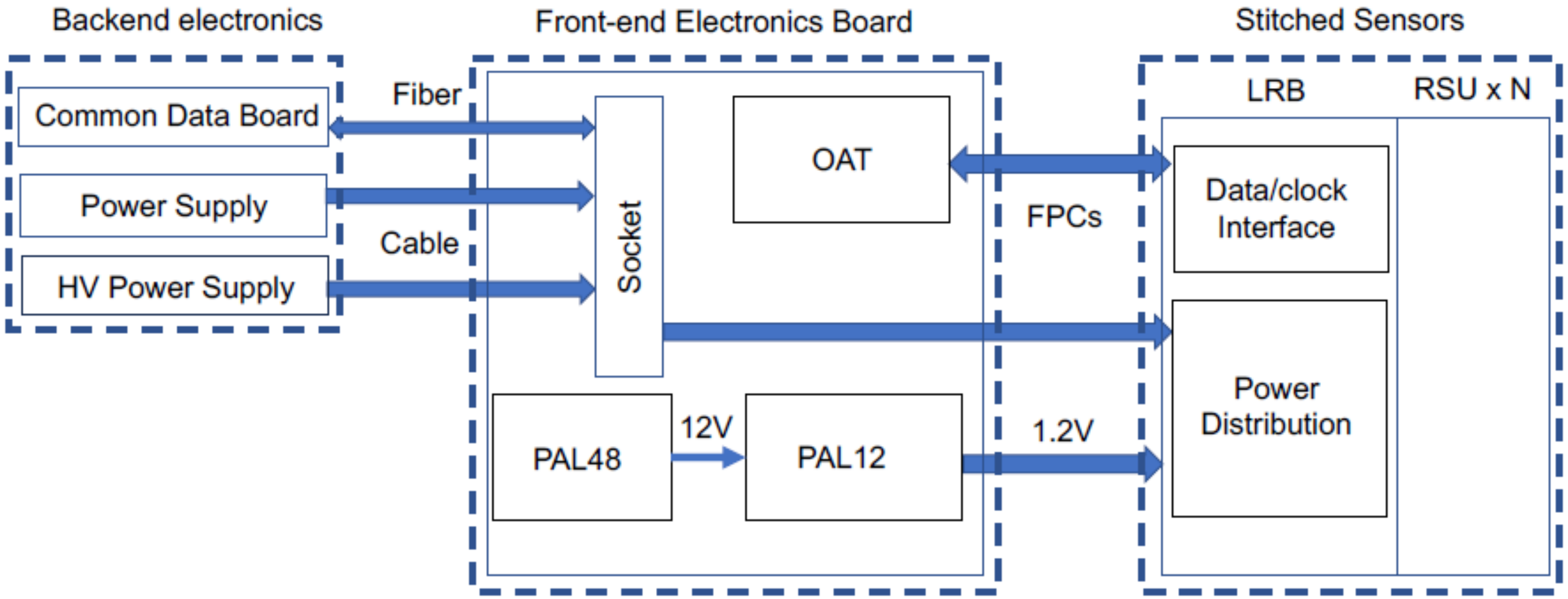
Vertex Detector Baseline layout

- Baseline :4 single layer of bent MAPS + 1 double layer ladders
- Inner layer: Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X_0 per layer
  - Different rotation angle in each layer to reduce dead area
- Outer layer: Double layer Ladder (~0.28% X_0 per layer)

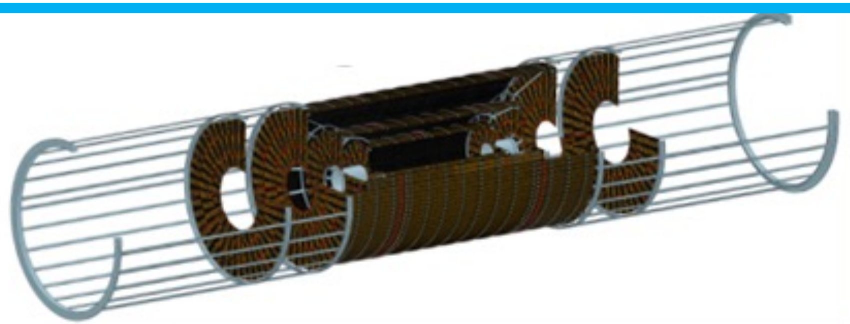


Long barrel layout covering cos θ<=0.991

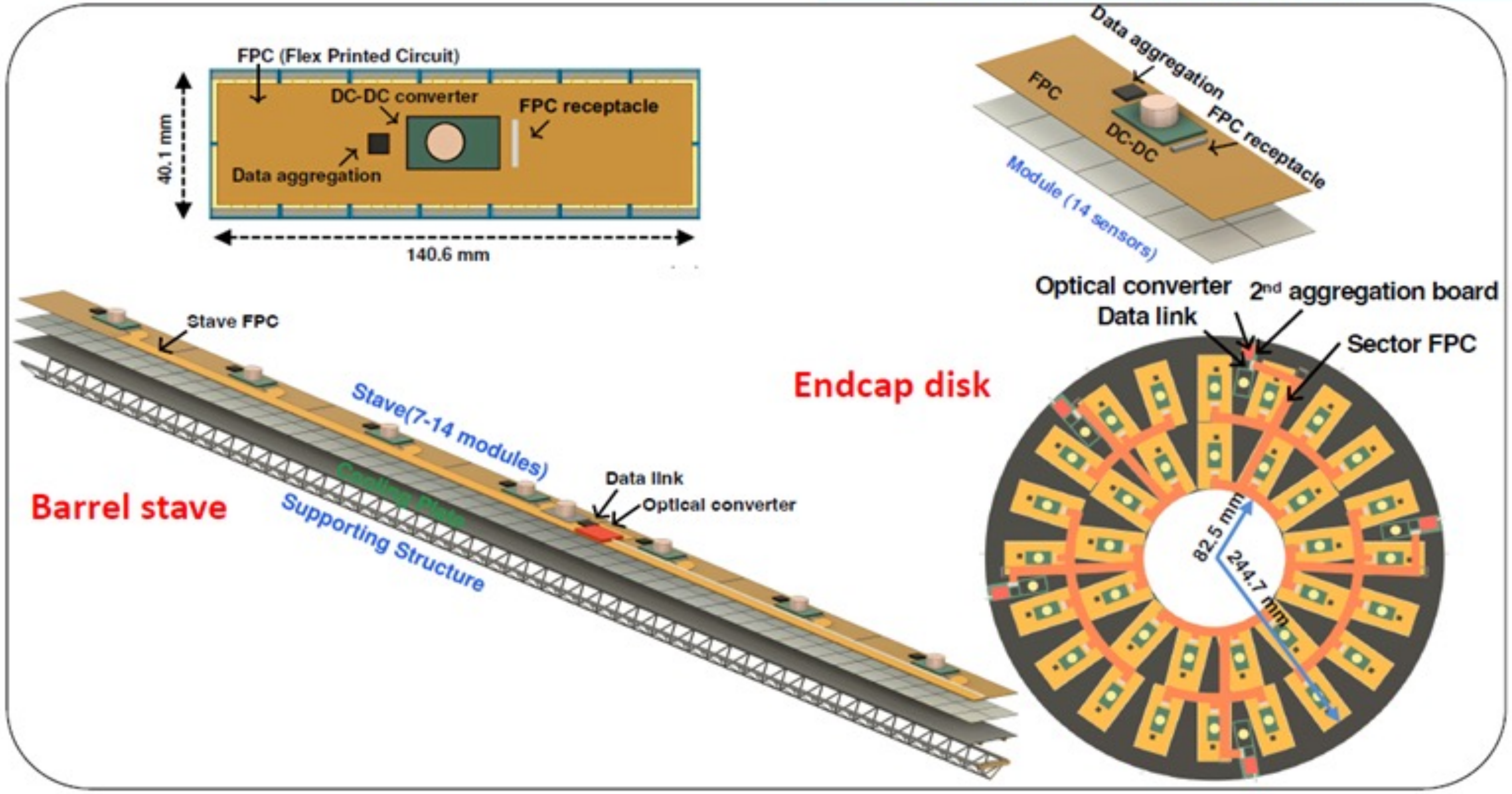
CVTX/ PVTX X	radius mm	length mm
CVTX 1	11.1	161.4
CVTX 2	16.6	242.2
CVTX 3	22.1	323.0
CVTX 4	27.6	403.8
PVTX 5	39.5	682.0
PVTX 6	47.9	682.0



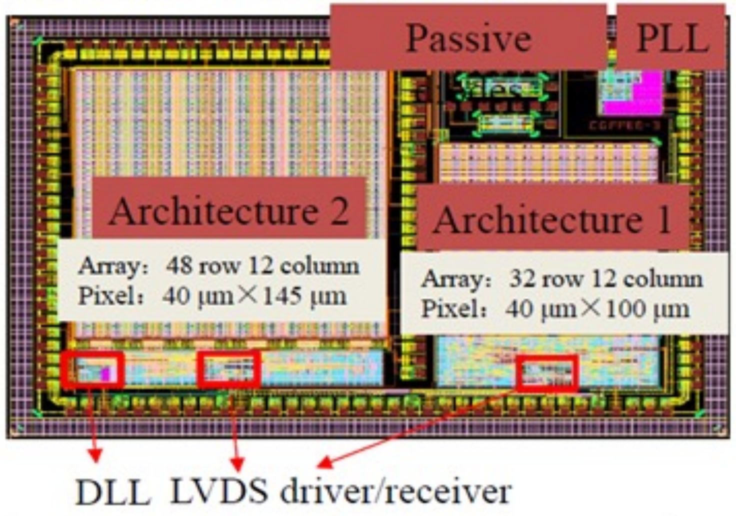
ITK Design with HV-CMOS Pixels



- Three barrel and four endcap layers (~20 m^2).
- HV-CMOS sensor COFFEE2 has verified the sensor process and in-pixel analog front-end.
- The latest COFFEE3 sensor, submitted for tape-out in Jan and received in May 2025, is currently undergoing testing.

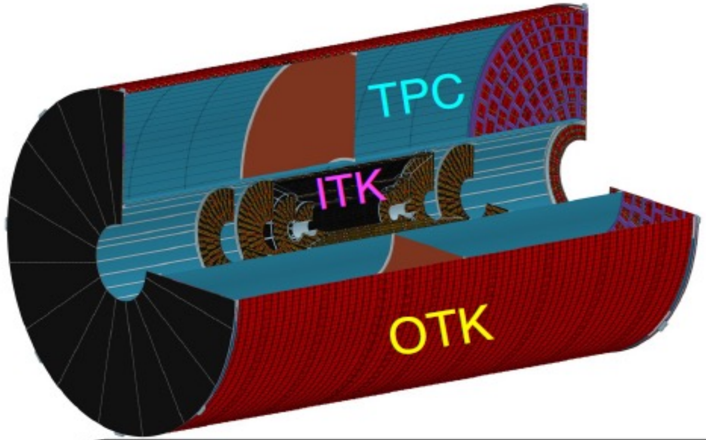


HV-CMOS sensor prototype (COFFEE3)

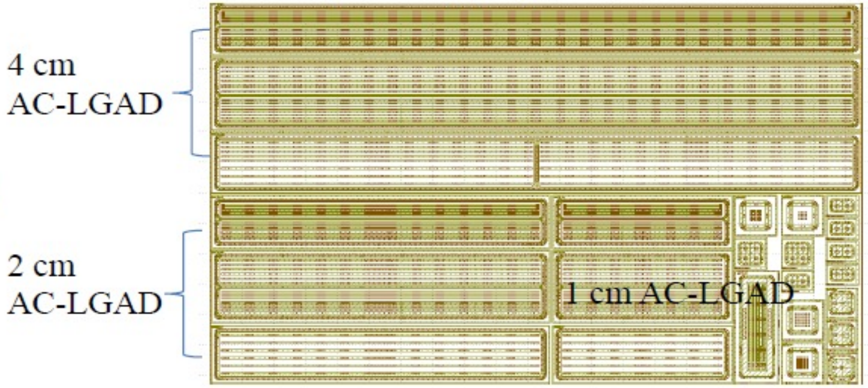


HV-CMOS sensor specification for ITK	
Sensor size	2 cm × 2 cm
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Timing resolution	3-5 ns
Power	200 mW/cm^2
Process node	55 nm

OTK Design Based on AC-LGAD Strip Sensor

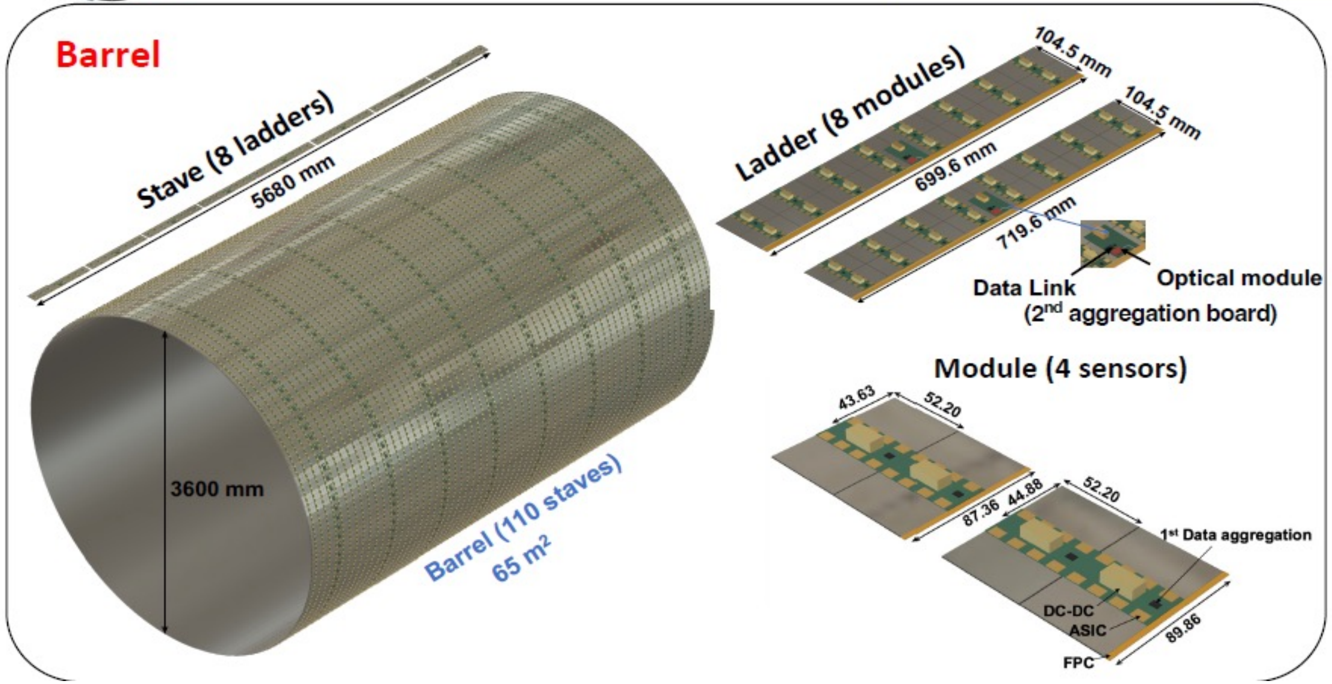


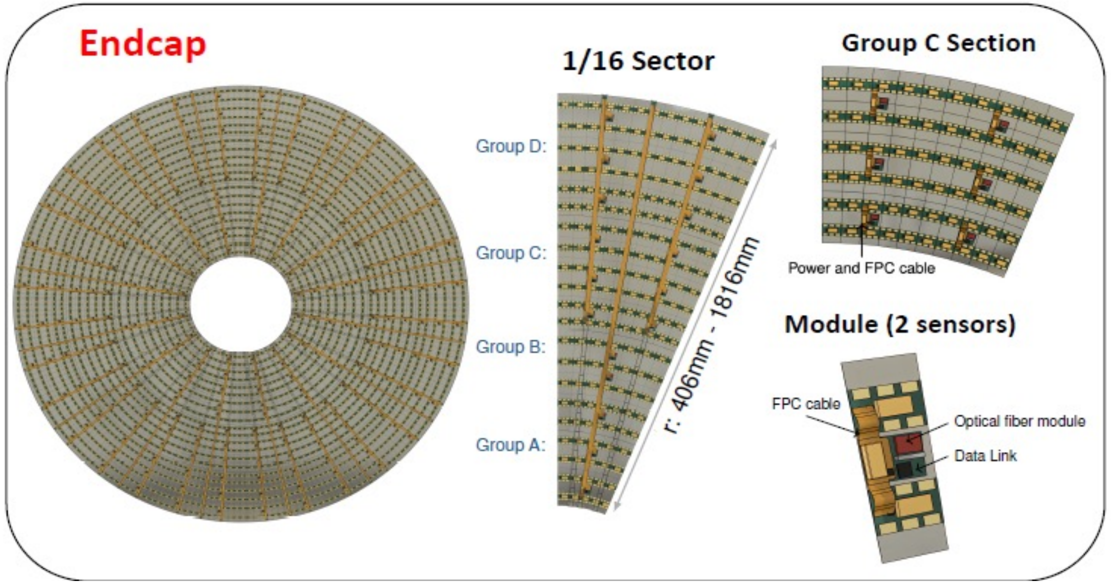
AC-LGAD prototype (latest submitted)



- One barrel layer and one endcap layer (~85 m^2).
- The latest LGAD sensor was submitted for tape-out in March and waiting for the return.

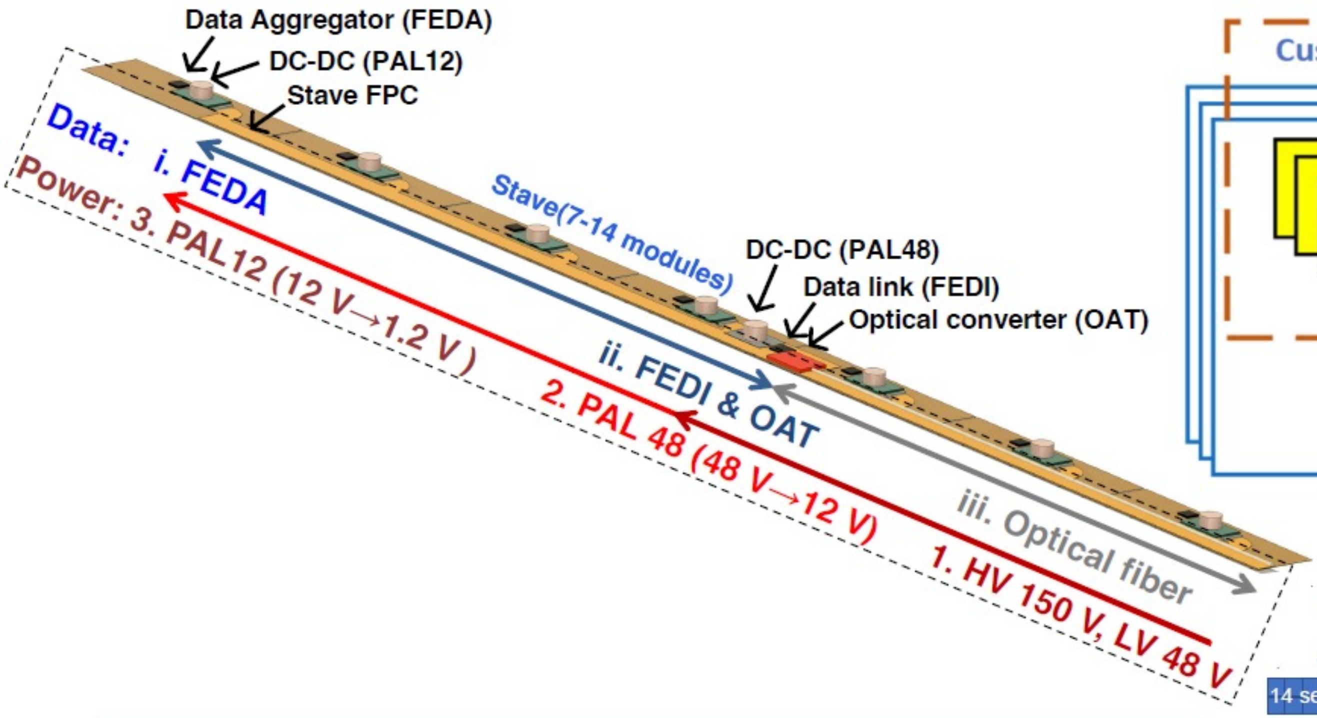
LGAD sensor specification for OTK	
Sensor size	(3-4.5) cm × (3-5) cm
Strip pitch	~100 μm
Spatial resolution	10 μm
Timing resolution	50 ps
Power	300 mW/cm^2

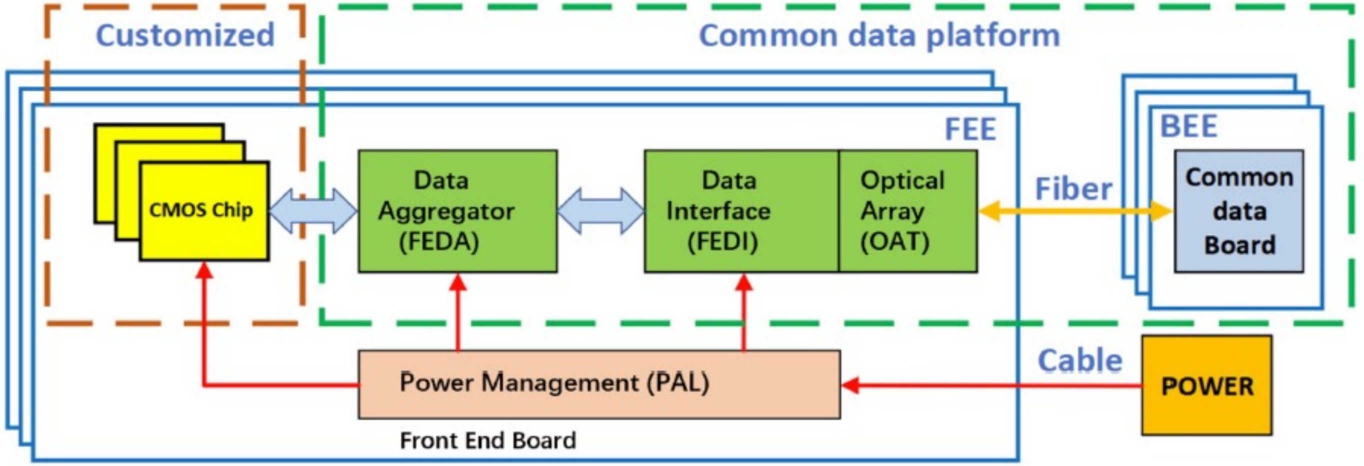


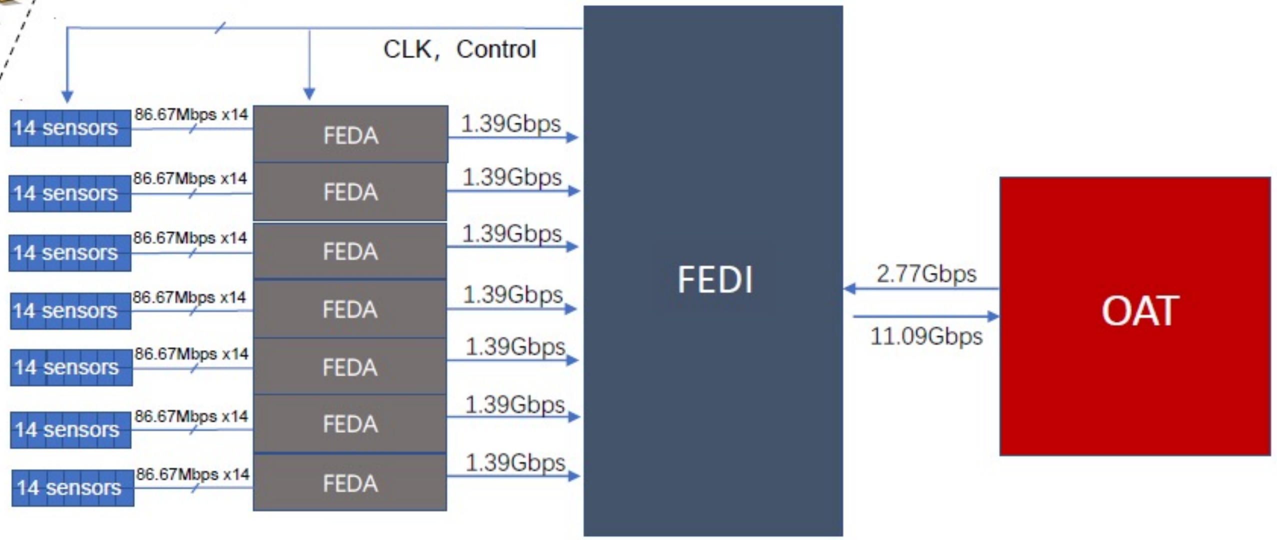


Readout Electronics framework for TRK

See Xiongbo yan 's talk (11:50)



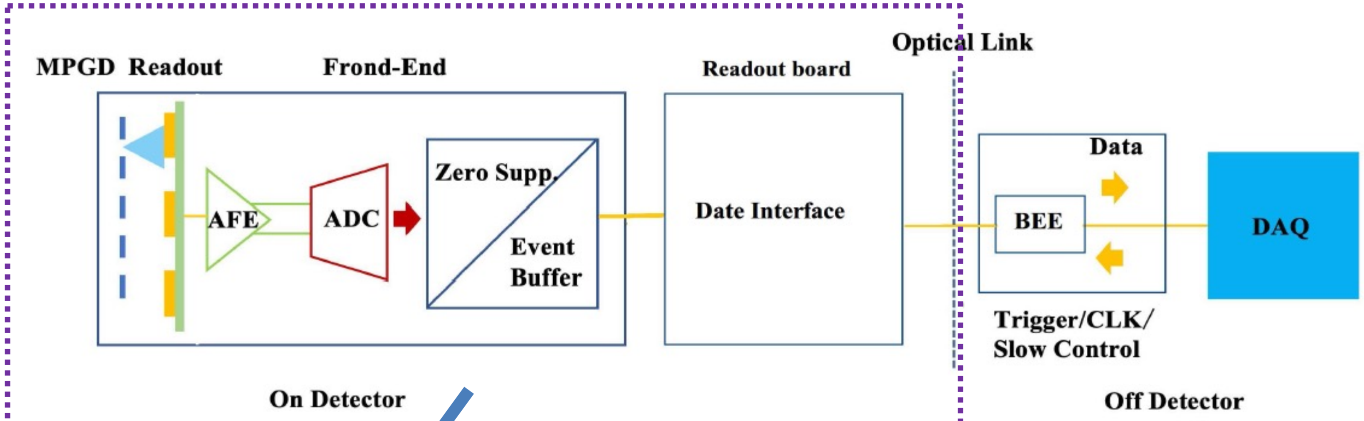


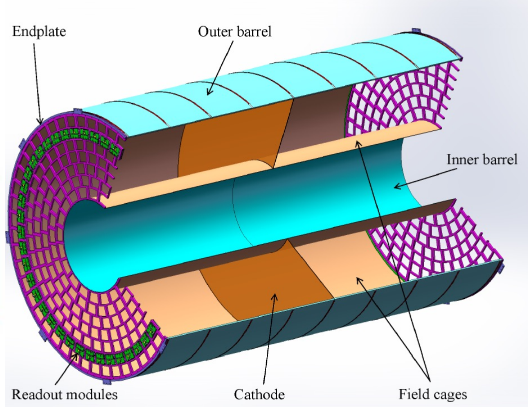


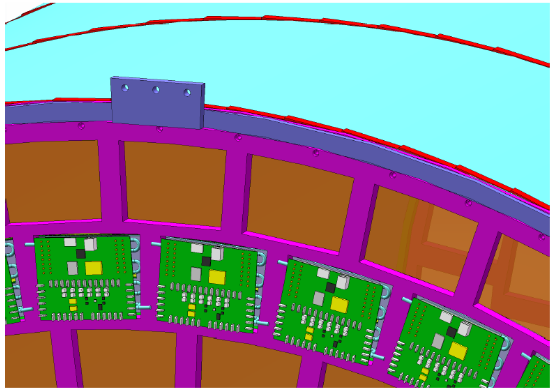
- In the readout design, each sensor can tolerate up to 86.67 Mbps, corresponding to a maximum hit rate of 4.1×10^5 Hz/cm^2 – about 42 times higher than the estimated peak background hit rates (9.9×10^3 Hz/cm^2) under the most challenging high-luminosity Z-pole operation mode.

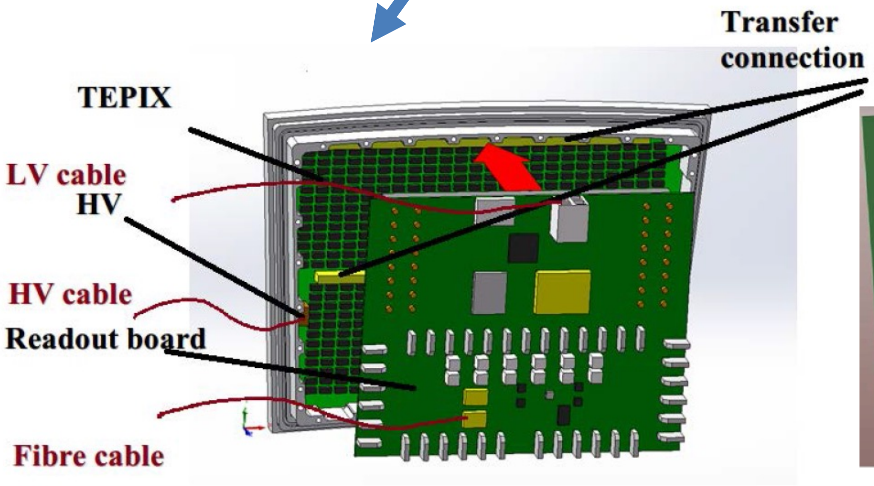
See Zhi Deng's talk (12:10)

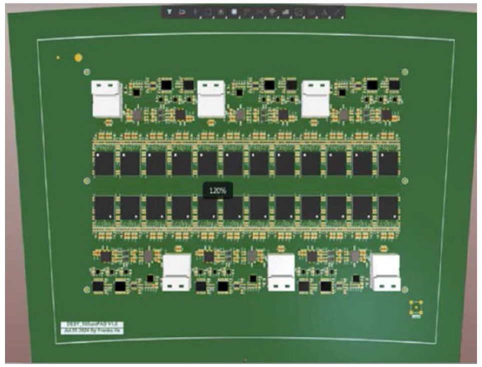
TPC electronics











On detector: readout modules

- Double-mesh Micromegas with high granularity readout (500μm × 500μm pad size)
- FEE board: a readout ASIC chip array. Interposer connection between pads and ASIC chis
- Readout board: data interface and data concentrator

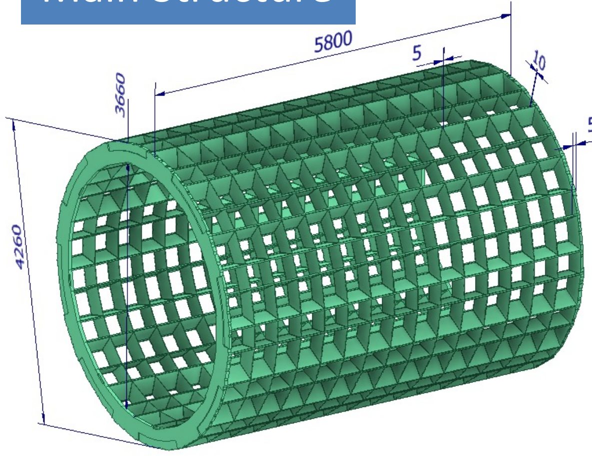
Off detector:

- High-speed optical links
- Off-detector BEE
- Data Acquisition (DAQ) system

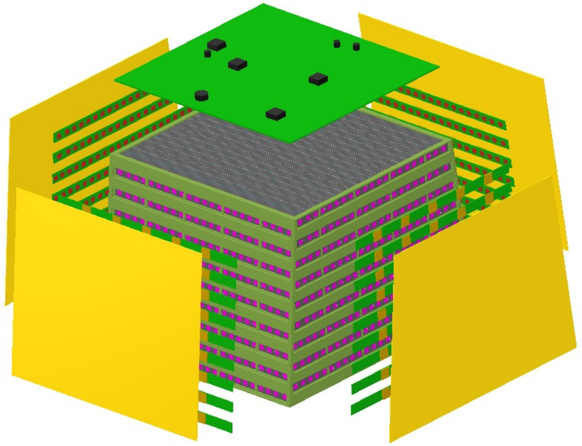
ECAL electronics

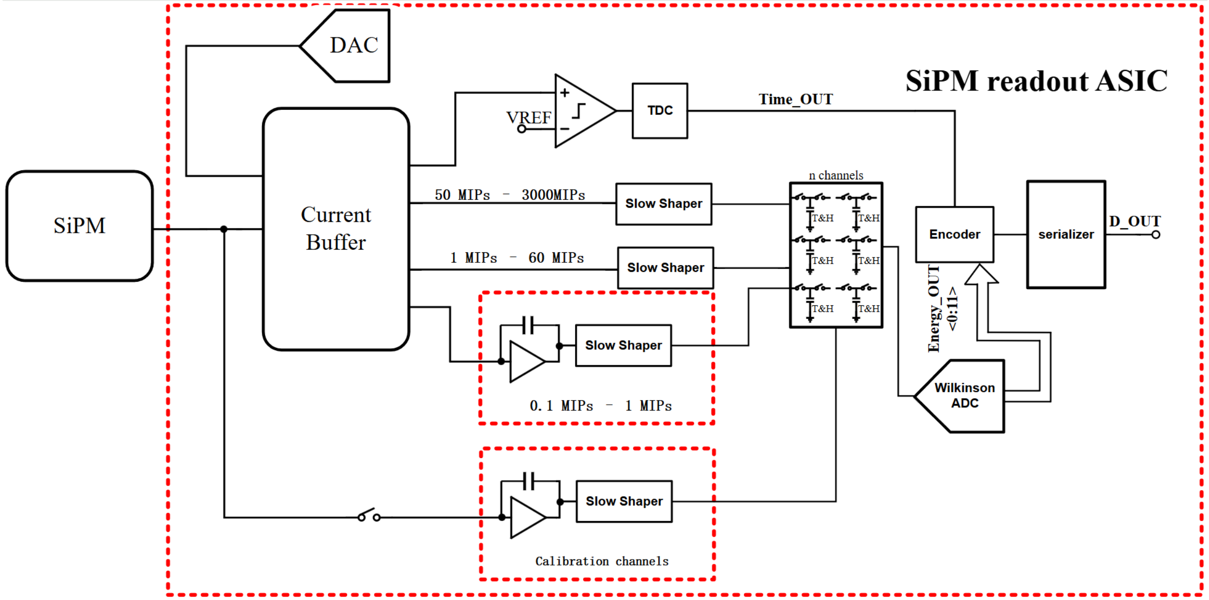
See Jinfan Chang's talk (14:00)
See Huaishen Li's talk (14:30)

Main Structure



Module Integration





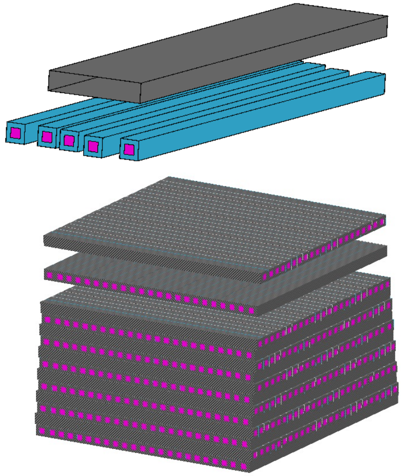


Table 11.2: Requirements of ECAL/HCAL SiPM for electronics

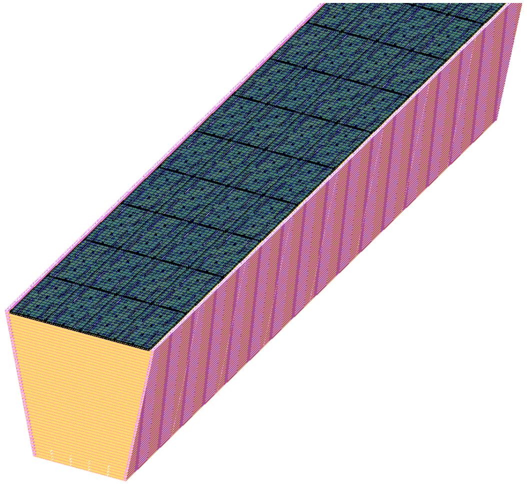
Parameters	Requirement of ECAL	Requirement of HCAL
Charge Dynamic Range	0.128 pC~3.84 nC (0.1~3000MIPs@100 p.e./MIP)	0.8~800pC (0.1~100MIPs@100 p.e./MIP)
Timing Measured Range	TBD from electronics	TBD from electronics
Charge Resolution	30% @ 0.1 MIP, 10% @ 1.0 MIP, 1% @ 100 MIPs	10% of 1.0 MIP, i.e. 10 p.e.
Timing Resolution	200 ps @ 1 MIP, 100 ps @12 MIPs	
Integral Non-linearity	Better than SiPM's	
SiPM Capacitance	$\leq$ 50 pF	$\leq$ 100 pF
SiPM Gain	8×10^4	$\geq 5 \times 10^5$
Average Event Rate/channel	13 kHz	Lower than ECAL's
Max Event Rate/channel	230kHz	Lower than ECAL's
Typical Signal Rising Edge	40ns	
Typical Signal Width	$\geq$ 1 µs (BGO decay time is 300ns)	$\geq$ 1 µs (Glass decay time is longer than 300ns)
Other Requirement	SiPM bias voltage fine tuning 0.5V	

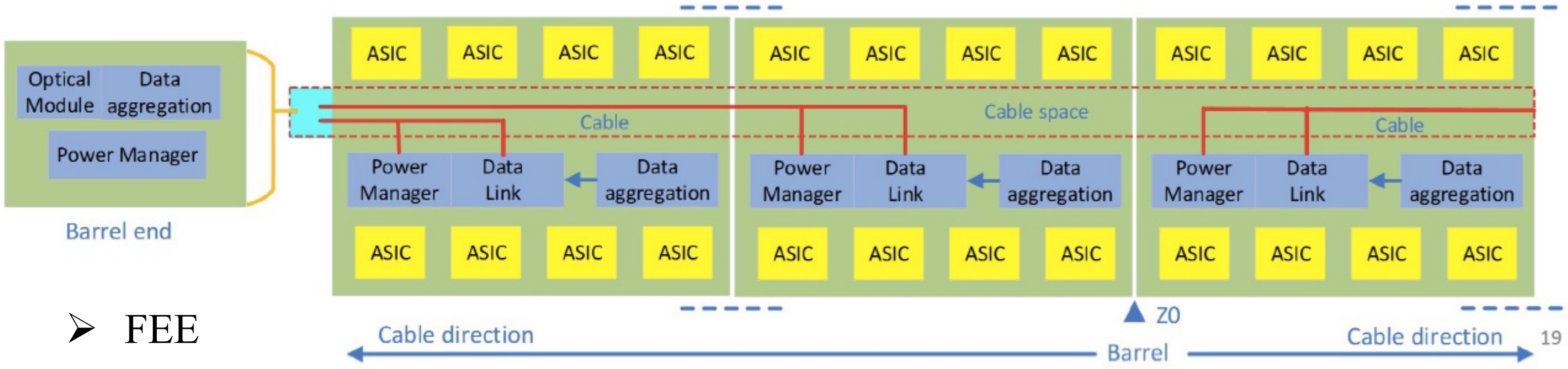
Table 11.3: Specifications of the SIPAC ASIC

Characteristics	Value
Charge Dynamic Range	0.128 pC~3.84 nC
Charge resolution	30%@0.128pC, 10%@1.28pC, 1%@128pC 1%@100 MIPS
Time resolution(RMS)	200 ps @1.28pC, 100 ps @12.8pC
Detector Capacitance	$\leq$ 100 pF
Max signal rate/channel	500 kHz/ch
ADC	10-bit
TDC resolution	8-bit
TDC bin width	100 ps
Power consumption	15mW/channel
Num. of channels	4

See Jinfan Chang's talk (14:00)

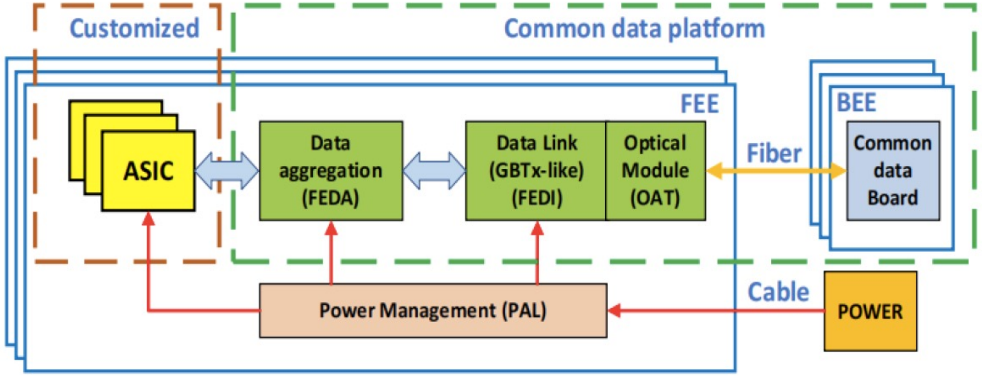
HCAL electronics





➢ FEE

- **Front-End boards in HCAL cell Box**
  - thickness limited: 3.2mm = PCB 1.2mm + ASIC 2mm
  - SiPMs, ASICs and Data Aggregation
  - PCB dimensions: flexible in different positions
- **SiPM-readout ASIC**
  - customized for CEPC calorimeter system
  - functionality: energy and time measurements
  - power consumption: 15mW/ch
- **Aggregation board at the end of barrel, cable connection**



Energy Measurement: ASIC for ECAL & HCAL
Data transmission: common
Trigger mode: FEE triggerless readout

See Jie Zhang's talk (14:15)

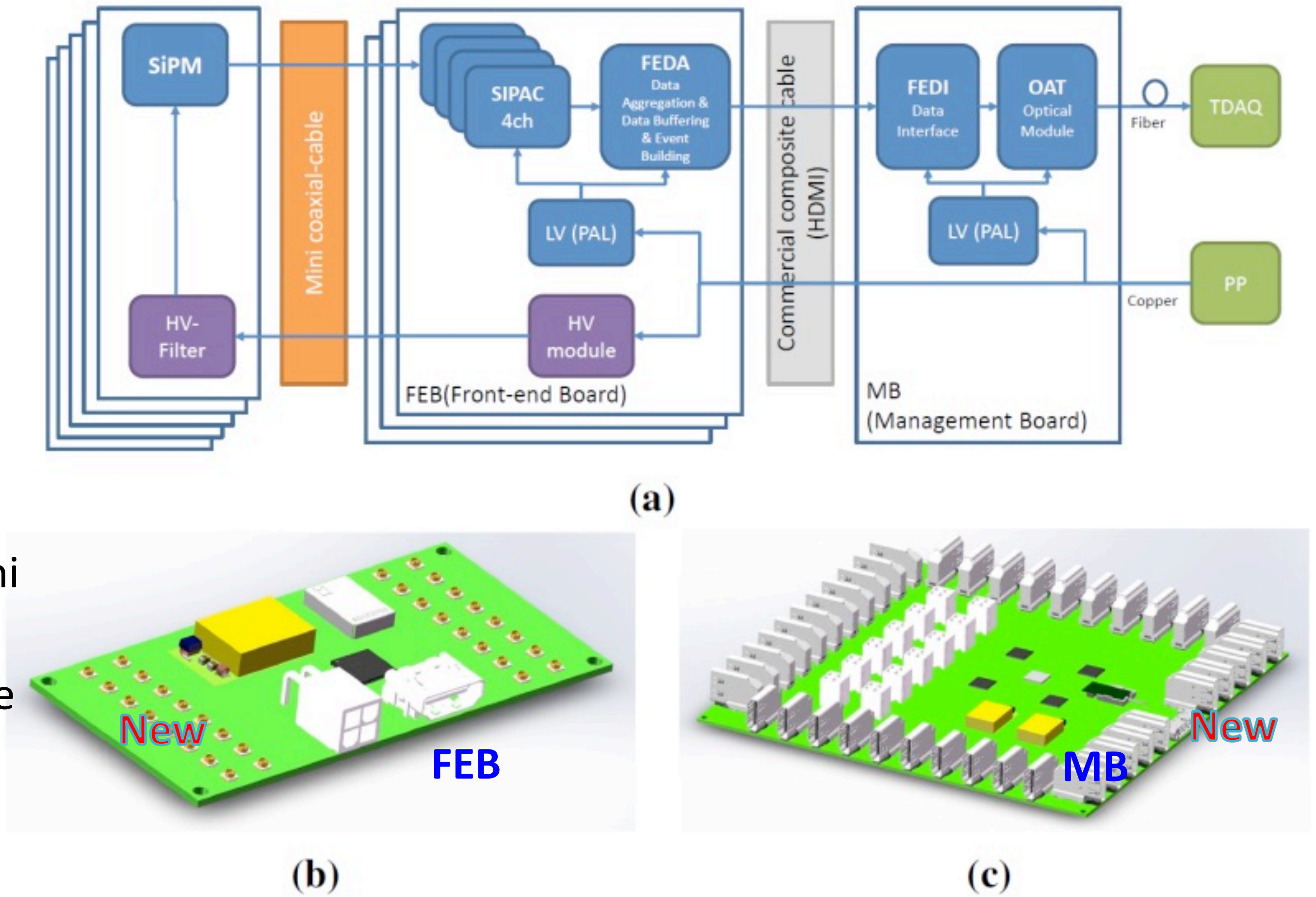
Muon electronics

According to the R&D results and required performance: $N_{pe} > 200, \sigma_T < 0.5ns$

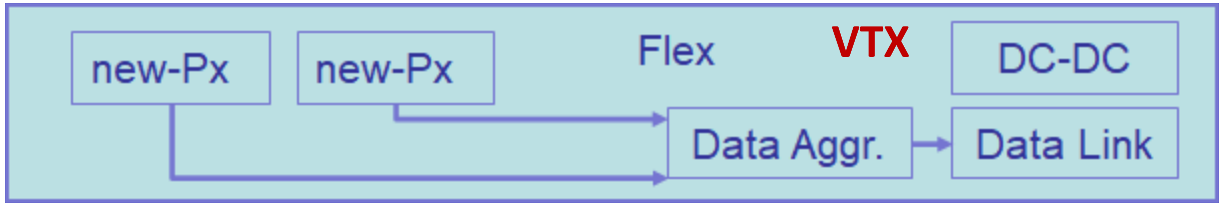
Use the same chip designed for calorimeter, but customize the FEB based on ASIC according to the constraints in detector modules.

Three stages for readout

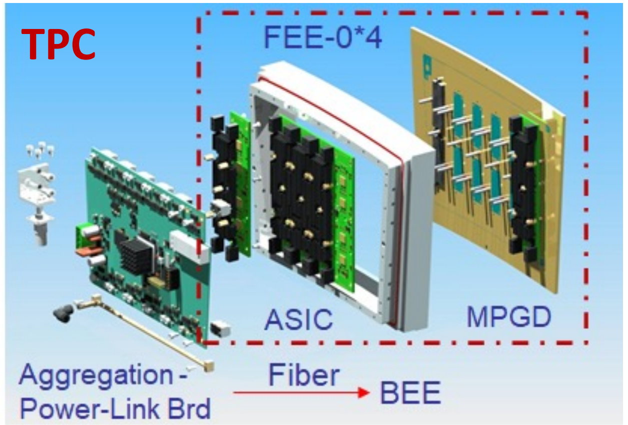
- SiPM tile: SiPM on PCB
- FEB: Front-End Electronics Board, 32 channel, mini HV generator integrated.
- MB: Management Board, central node for multiple functions.

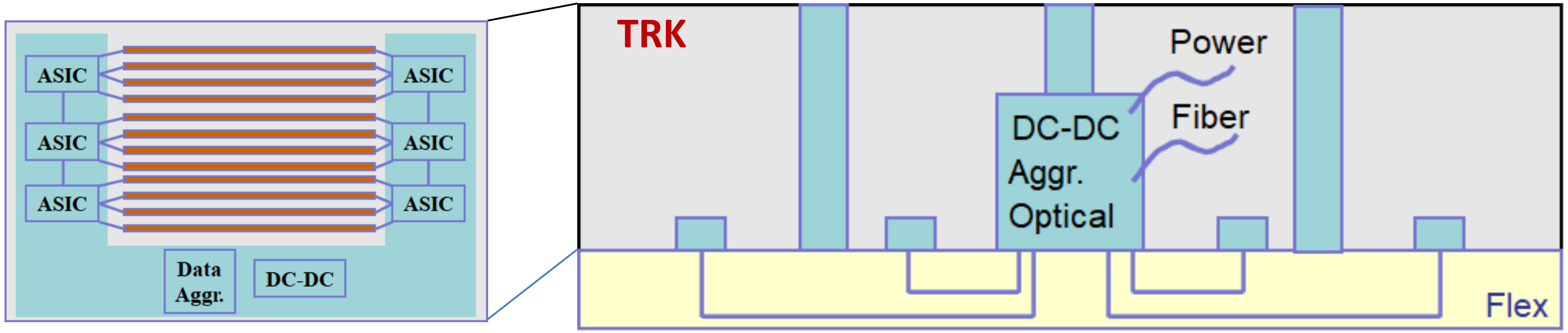


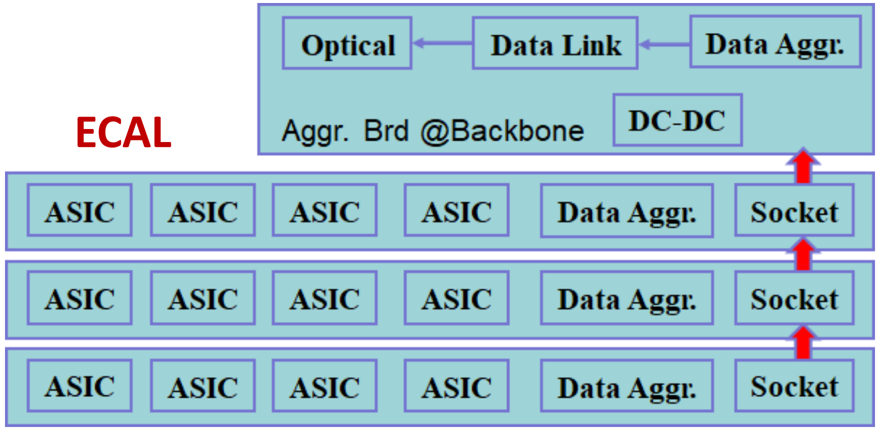
An overview of the sub-detector electronics

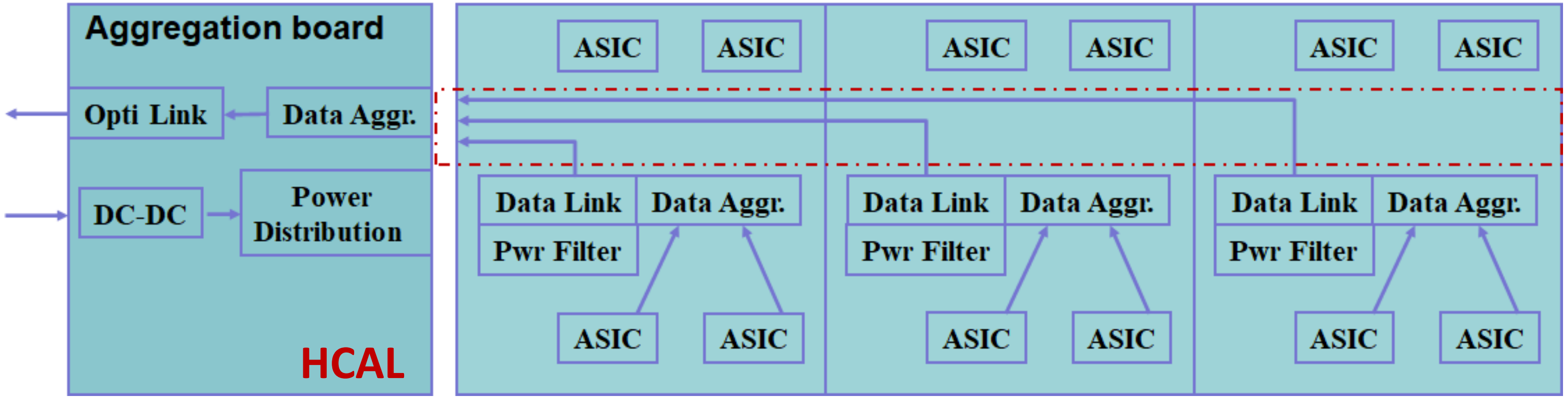


All sub-det readout electronics were proposed based on this unified framework, maximizing common design, easy for production and maintenance.









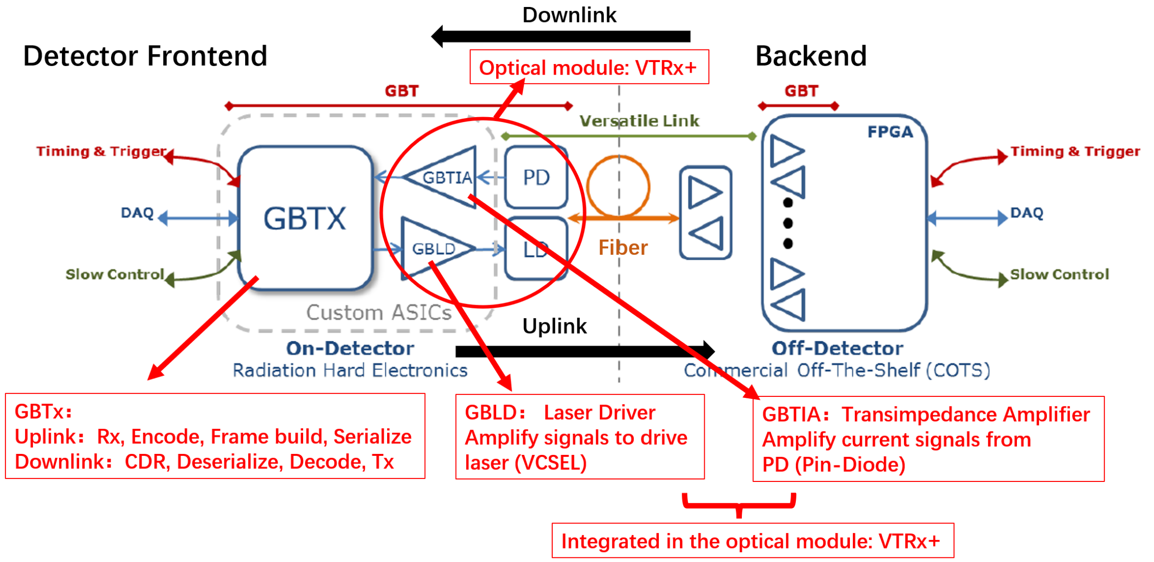
Technical Survey on Data Transmission

GBT Project:

- The lpGBT & VTRx chip series, developed by CERN, are widely used by LHC.
- Core components:
  - GBTx: Bidirectional Serdes ASIC
  - GBLD: Laser driver
  - GBTIA: Transimpedance amplifier
  - Customized Optical Module
- However the base clock frequency of CEPC 43.3MHz is not compatible with lpGBT system

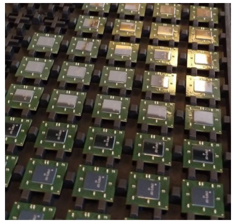
Our choice:

- Build a GBT-like universal bidirectional data transmission system
- Take the lpGBT as a reference, the protocol can be a minimum & necessary set for the readout, clocking & control

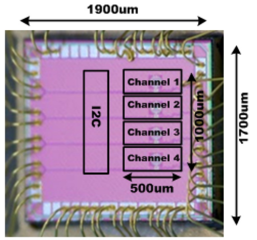


GBT Architecture Developed by CERN

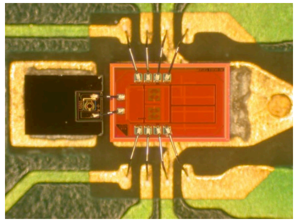
Ref. P. Moreira, The GBT Project, 2007



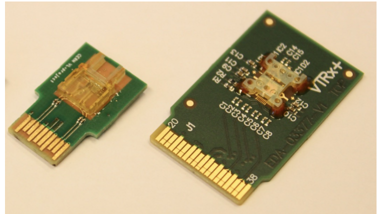
lpGBTx
Uplink: 10.24Gbps
Downlink: 2.56 Gbps



GBLD (LDQ10)
10.24 Gbps x 4ch



GBTIA
2.56 Gbps



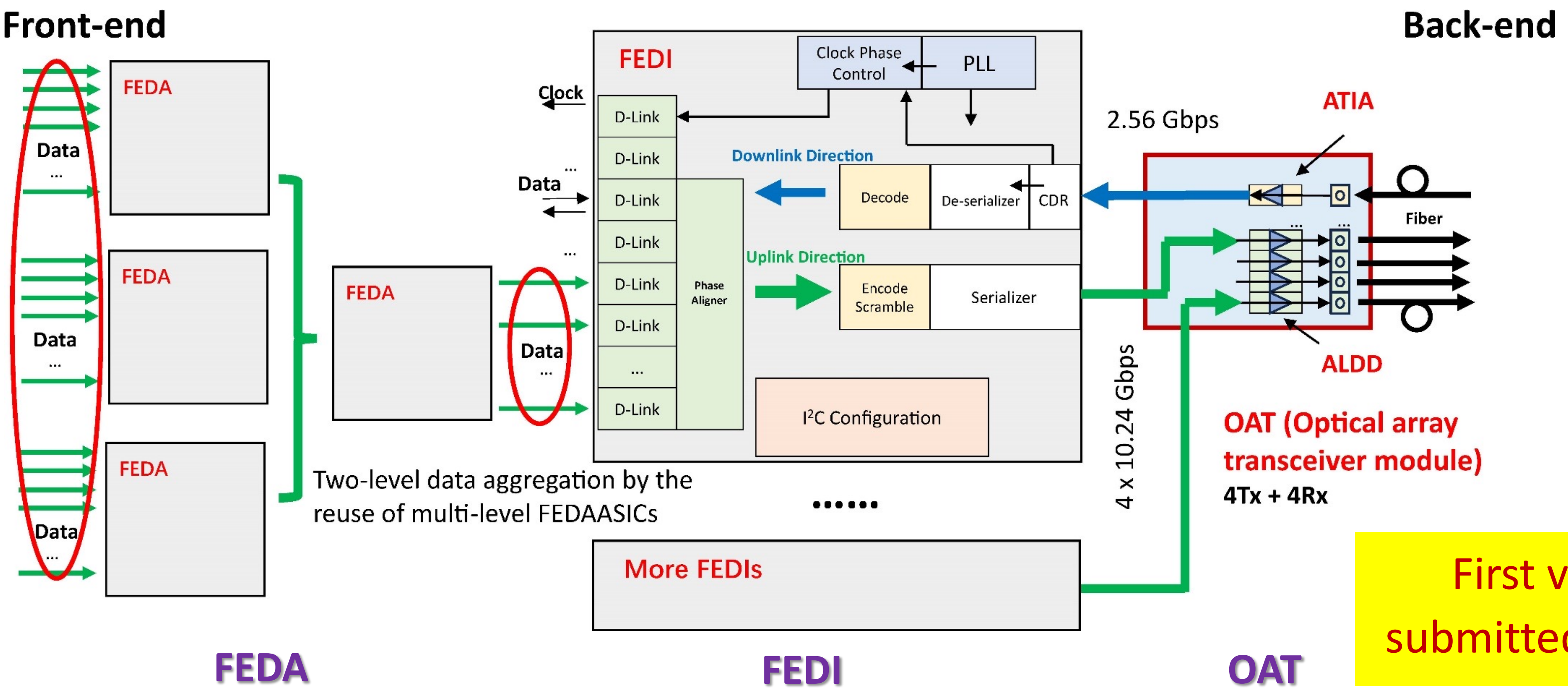
VTRx+
4Tx + 1Rx
Array Optical Module

GBT Series ASICs and optical module

Ref. P. Moreira, GBT Chipset Status and Production Plans, 2013

Detailed design on Data Transmission Structure

See Xiaomin Wei's talk (15:10)
See Guoxiang Zhang's talk (16:00)



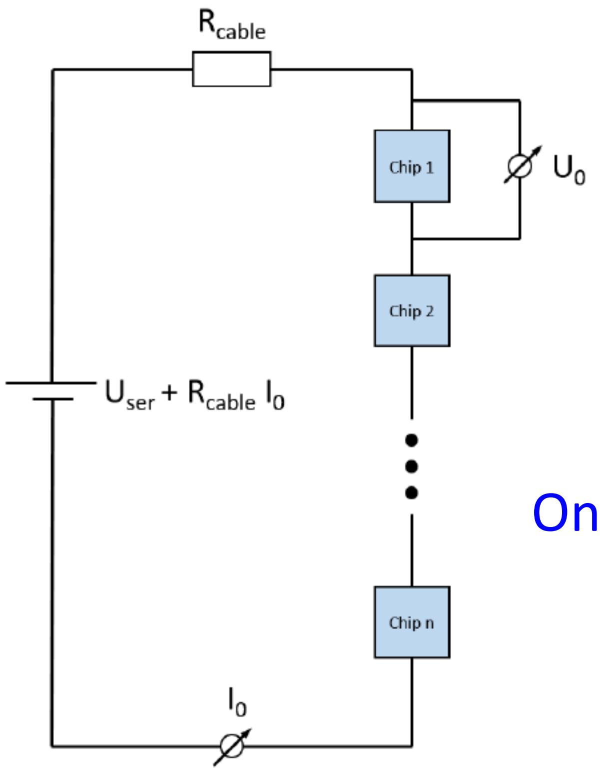
First version ASICs submitted October, 2025

Pre-Aggregation ASIC (FEDA): Intend to fit with different front-end detector (different data rates/channels)

GBTx-like Data Link ASIC (FEDI): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …

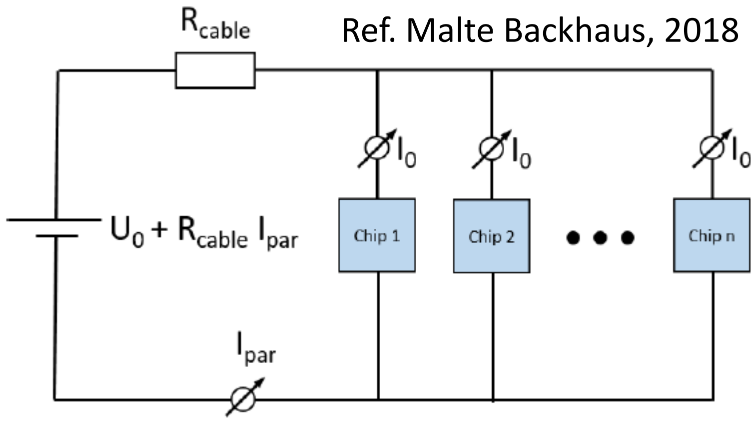
Array Laser Driver ASIC (ALDD) + TIA ASIC (ATIA) + Customized Optical module (OAT)

Technology Survey and Scheme on Powering



Serial Powering

Ref. Malte Backhaus, 2018



Parallel Powering

	Serial Power	Parallel Power
Material	Much less	
Cabling	Much less	
Installation	Much easier	
Maturity	New	Very mature
System Reliability	Potential issue	Very robust

On powering distribution

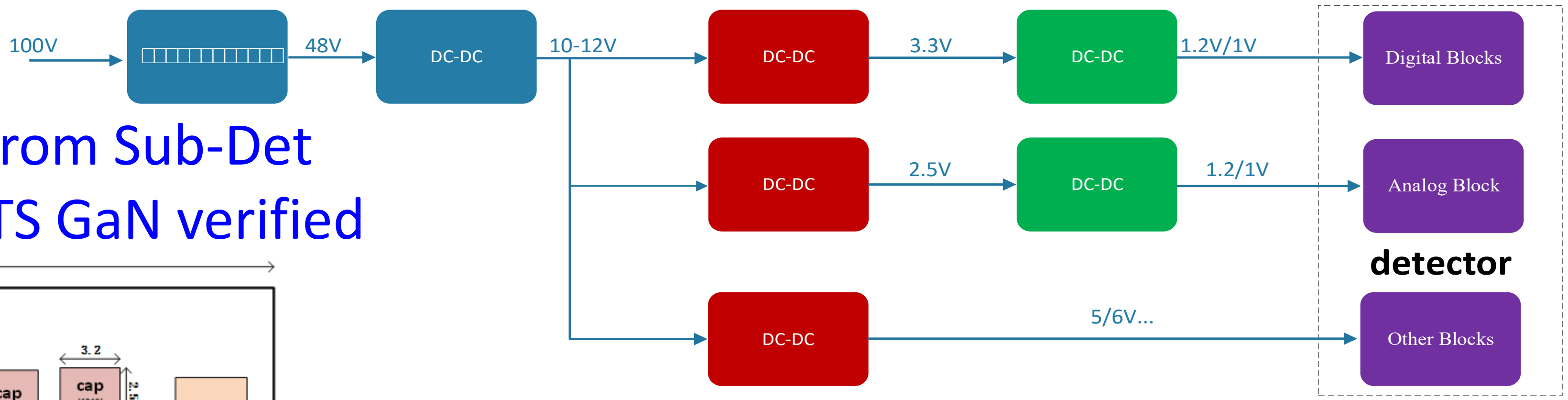
- Serial Powering is superior in many aspects (material, cabling and installation…) than Parallel Powering, especially on VTX & TRK
- It is also a hot area with a lot of focused R&D
- However, due to the common substrate at negative voltage for the stitching sensor in VTX, serial powering is not feasible

Our choice

- As a general platform, we chose (conventional) Parallel Powering as the baseline scheme, while to keep pace on R&D of Serial Powering as the backup scheme

See Jia Wang's talk (16:55)

R&D efforts preliminary design on powering



- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified

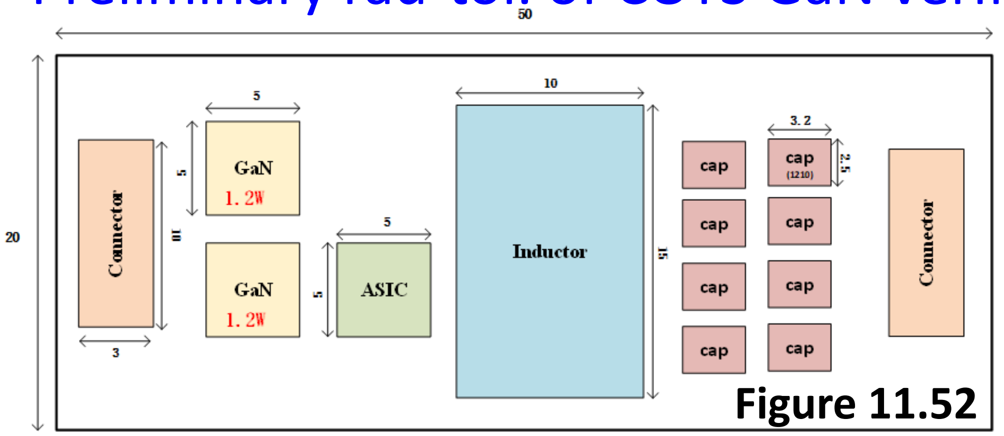
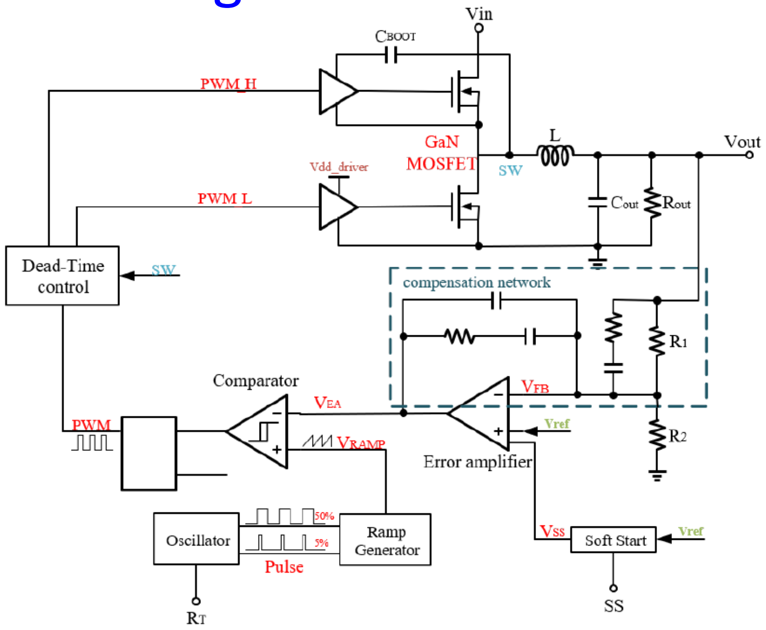


Figure 11.52

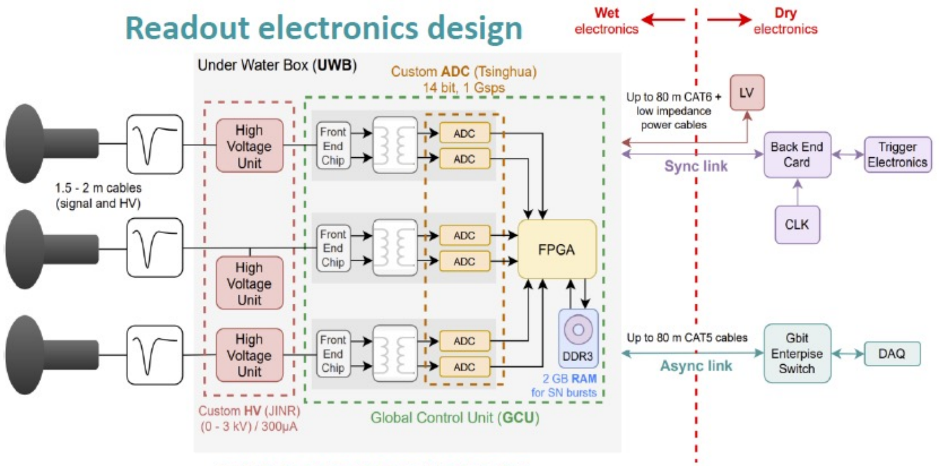
	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、3.3V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

- Proposed design of BUCK DC-DC convertor

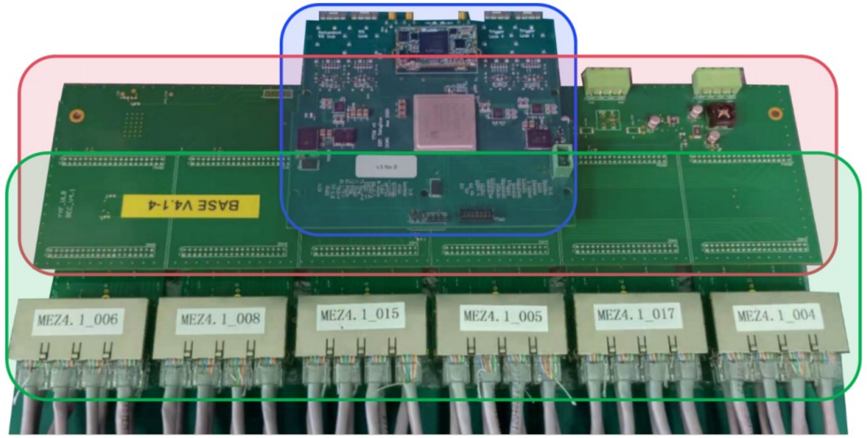


PAL Series

Related R&D and experience on BEE



NIM A 1052 (2023) 168255



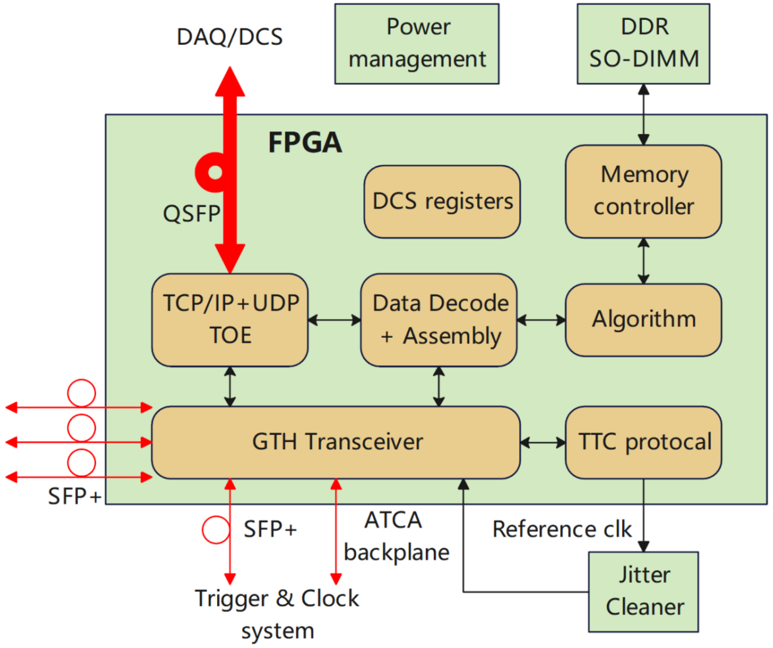
The back-end box for the JUNO experiment

- located between trigger system and front-end electronics,
- Collects the incoming trigger request for trigger system,
- Fanout the synchronized clock and the trigger decisions to front-end electronics.

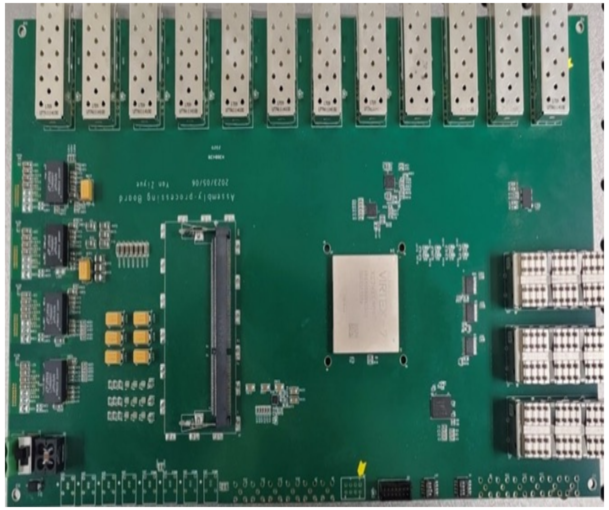
- Red box: The base board provides the power supply,
- Blue box: Trigger and Time Interface Mezzanine (TTIM) with WR node,
- Green box: The extenders interface with ethernet cables coming from underwater front-end boxes.

See Jun Hu's talk (17:10)

Detailed design on common BEE



The back-end Card structure



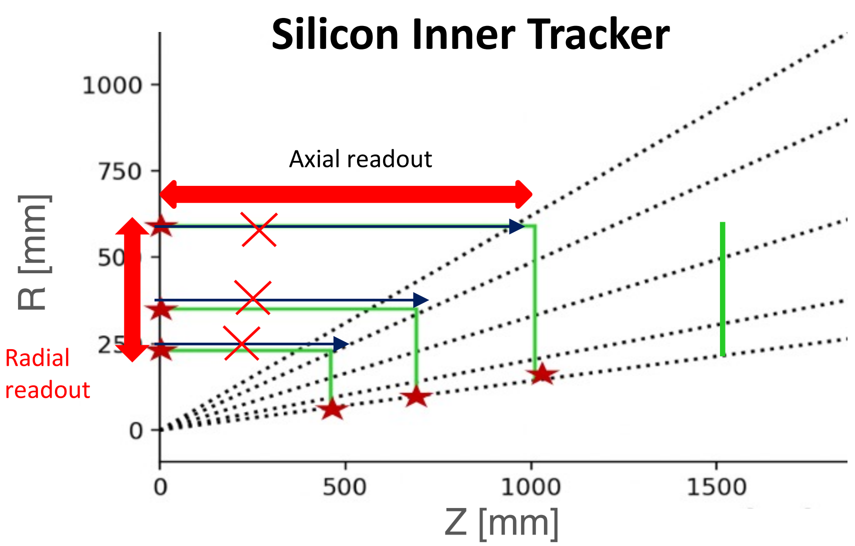
Data aggregation and processing board
Prototype for Vertex detector

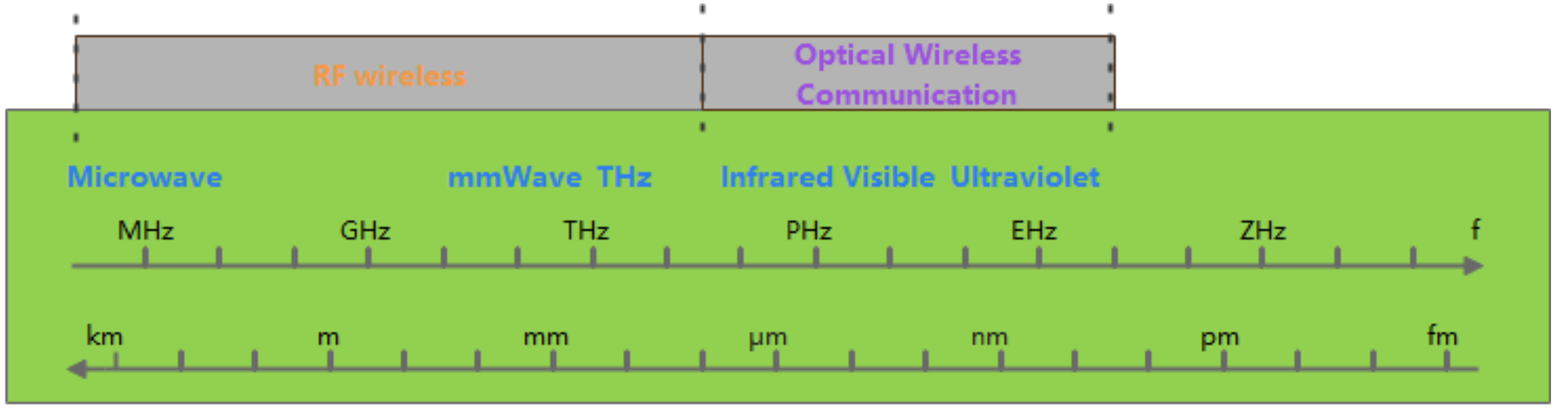
	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data from front-end optical link to highspeed network to DAQ.
- receives clock, global control from TTC, and synchronized and fanout to front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board storage for data buffering.
- Xilinx Kintex UltraScale series preferable, cost-effective/availability.

- Interface： SFP+ 10 Gbps ✖12 + QSFP 40 Gbps ✖ 3
- FPGA based machine learning for clustering, hit point searching, and tracking algorithms

Alternative scheme based on wireless communication



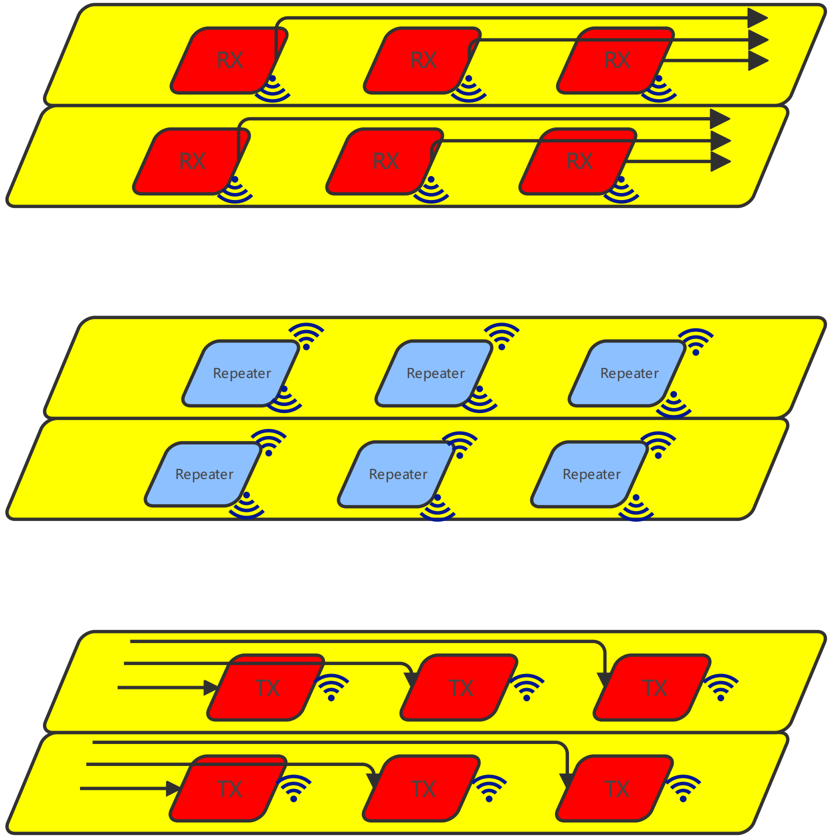


- Radial readout with mm-wave
  - 12- 24 cm distance
  - Data rate : < 30Mbps
- Axial readout to endcap
  - Only at the outermost layer or dedicated aggregation layer.

- WiFi (2.4GHz, 5GHz)
  - large antenna volume, high power consumption, narrow frequency band, and high interference
- Millimeter Wave (24GHz，45GHz，60GHz，77GHz)
- Optical wireless communication (OWC) / Free Space Optical (FSO)

Wireless communication based readout scheme was proposed to mitigate the cabling problem, as a backup scheme.

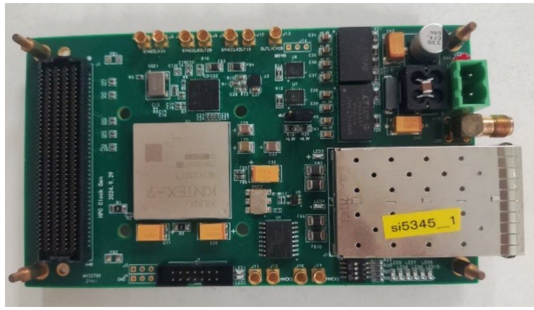
Recent progress on mm-wave transmission



Multi-channel Millimeter-Wave transmission prototype


Dummy Flex with MMW


MMW transmission module


FPGA data source board

- Single-channel MMW RX/TX verified
  - Max distance: 1.25Gbps @ 67.5cm
  - Max line rate: 6.6Gbps @ 22.5cm
- Multi-channel Millimeter-Wave transmission prototype in development
  - Millimeter-wave modules mass produced and tested
  - TX/RX flex PCBs and adapter boards produced, assembly in progress
  - FPGA data source board produced and tested
  - Repeater design: double-sided PCB, in progress
  - Focus: Multi-channel crosstalk validation

Electronics interface to the counting room

Data Link, Fibers & BEE

Detector	Max Data Rate/ Fiber (Gbps)	Fibers/ Module	Fibers	BEEs	Crates
VTX	8	1–2	96	6	1
TPC	0.1	1	496	32	4
ITK-Barrel	2.88	2–3	376	24	2
ITK-EndCap	4.4	2	148	6	1
OTK-Barrel	1.4	1	880	55	4
OTK-EndCap	1.4	1–2	544	34	4
ECAL-Barrel	4.8	2 (4)	960 (1,920)	60 (120)	6 (12)
ECAL-EndCap	4.8	2 (4)	448 (896)	28 (56)	4 (8)
HCAL-Barrel	0.14	1	5,568	348	36
HCAL-EndCap	1.75	1	3,072	192	20
Muon-Barrel	0.01	1	24	2	1
Muon-EndCap	0.01	1	16	1	-
Total (Upgraded)	-	-	12,628 (14,036)	788 (876)	83 (93)

On-detector LV, HV & cables

Detector	Power Channels (Composite Cables)	Total LV Power (kW)	LV Crates	Max. HV (V)	HV Crates
VTX	96	0.45	2	-10	1
TPC	496	16	6	-500	4
ITK-Barrel	128	26.6	6	300	2
ITK-EndCap	74	13.8	4	300	2
OTK-Barrel	880	195	42	500	4
OTK-EndCap	288	60	14	500	2
ECAL-Barrel	480	17.5	5	60	4
ECAL-EndCap	224	9.5	4	60	2
HCAL-Barrel	5,568	66.1	58	60	26
HCAL-EndCap	3,072	41.3	32	60	14
Muon-Barrel	24	0.76	1	60	1
Muon-EndCap	16	0.45	1	60	-
Total	11,346	447.46	175	-	62

- Fibers：12,628
- Power cables: 11,346
- Total power consumption: 450 kW

Research team

- Electronics working group was founded: IHEP + universities, ~50 staffs (not full time) + 60 posdoc/student. We are looking for more collaborators.
- IHEP joined DRD7 collaboration in July 2025.

- Overall electronics and BEE: IHEP(5)
- Sub-detector readout electronics: IHEP(11), Tsinghua(5), CCNU(3), NPU(7), SDU(4), NJU(3)
- Data link: CCNU(3), IHEP(3), USTC(2), NPU(4)
- Powering: NPU(3), IHEP(2), USTC(2)

ASIC development & teams

Chip	Application	Functional	Foundry & technology	Similar chips	Leading person	Development team	Staff	Students
Taichu	VTX	VTX-Stitching	Towerjazz 180nm / 65nm	MOSAIX	Wei Wei (IHEP)	NPU, CCNU, SDU, NJU	10	8
TEPIX	TPC	Pixel TPC	TSMC 180nm (SMIC 55nm)	Timepix3/4	Zhi Deng (THU)	IHEP	1	4
COFFEE	ITK	HVCMOS	SMIC 55nm HV	MightyPix	Yiming Li (IHEP)	ZJU, NPU, DMU，SDU, NJU	8	12
LATRIC	OTK	LGAD-TOF	SMIC 55nm	ALTIROC	Xiongbo Yan (IHEP)	CCNU, WTU, HPU	9	10
SIPAC	SiPM ASIC	ECAL, HCAL, Muon	SMIC 55nm	HGCROC、SPIROC	Huaishen Li (IHEP)	CCNU, NPU	5	6
FEDI	Common Elec	Data Link	SMIC 55nm	lpGBT	Di Guo (CCNU)	IHEP, NPU, USTC, WTU, HPU	9	16
OAT	Common Elec	Optical	SMIC 55nm	VTRx+	Di Guo (CCNU)	IPAS, IHEP	3	3
FEDA	Common Elec	Data Aggregation	SMIC 55nm	lpGBT	Di Guo (CCNU)	IHEP, NPU	2	4
PAL	Common Elec	DC-DC	SMIC 180nm HV	bPolx	Jia Wang (NPU)	IHEP, USTC, TECHORILUX	7	3

ASIC Development Schedule

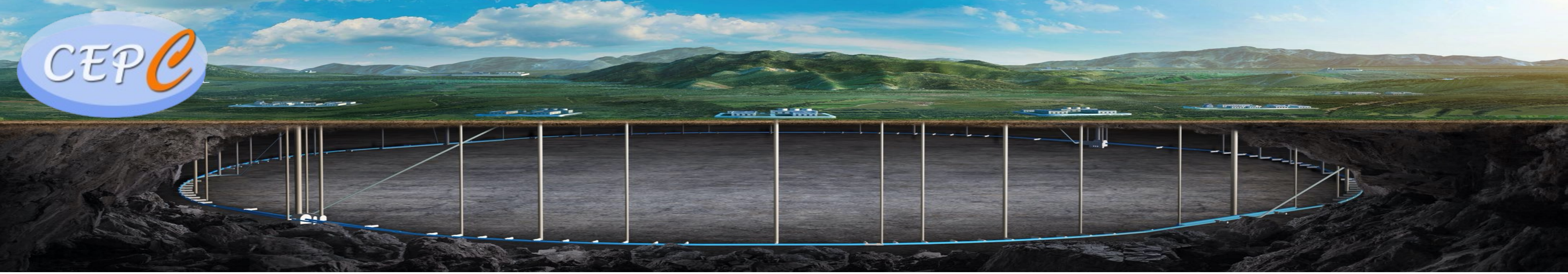
Overall Electronics system	Elec TDR Draft1 2024.12				Final Design Review 2027.12	Towards final CEPC detectors	Production Readiness Review 2029.12
Power & DC-DC (PAL)	2024.11 GaN Selection	2025.1 DC-DC Controller schematic design	2025.4 1st tapeout	2026.12 PAL func module prototype	2027.12 Module on detector test	2028.12 Rad enhancement & Inductor design	2029.12 Rad-tol & Mag proof PAL prototype
Data Link (FEDA, FEDI & OAT)	2024.10 Protocol define	2025.1 Scheme define	2025.10 1st tapeout Chip set	2026.12 FEDI & OAT func prototype	2027.12 FEDI & OAT on detector test	2028.12 Rad enhancement & FEDA development	2029.12 Rad-tol FEDI DataLink prototype
VTX STCH (Taichu-Stitching)	2024.12 Preliminary scheme for Stitching	2025.1 Taichu-stitching-180 development	2025.12 1st design of wafer-level stitch onTJ180 TJ65 design kit finalization	2026.12 TJ65 single chip design	2027.12 wafer-level stitching mechanical prototype TJ65 single chip prototype		2029.12 TJ65 wafer-level Stitching detector prototype
PIX TPC (TEPIX)			2025.6 Prototype beamtest	2026.12 Chip optim for optimized TPC	2027.12 Optimized Prototype beamtest		2029.12 Chip Finalization
OTK AC-LGAD (LATRIC)	2024.12 FPMROC chip test (for FASTPMT) Preliminary scheme	2025.4 1st tapeout	2025.12 FPMROC prototype test (for FASTPMT) OTK detector optimization	2026.6 ASIC-128chn tapeout	2027.10 AC-LGAD detector co-test		2029.12 Chip Finalization & detector co-test
ECAL/HCAL/Muon SiPM ASIC (SIPAC)	2025.1 Spec finalization & device selection	2025.4 1st tapeout	2025.12 1st SiPM ASIC test	2026.12 N: Existing chip based modification Y: SiPM ASIC optimization	2027.12 HCAL module prototype		2027.12 Chip Finalization

Working plan

- Most chips' development followed the schedule.
- Toward end of 2025:
  - **Submitted** October MPW tapeout
    - 1st full chip tapeout for FEDI, core chip of the data interface
    - 2nd ver chips fixed bugs founded
  - Thorough test after chips come back.
- Longer term:
  - develop with detector group for the first prototypes, with available sister chips or newly developed chips.

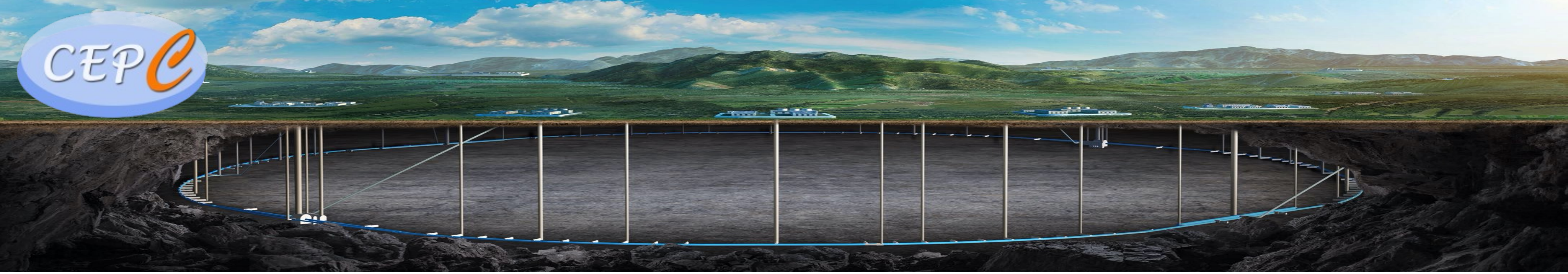
Summary

- The CEPC Reference TDR electronics design has been completed, incorporating full data transmission and a backend trigger scheme while preserving the potential for future upgrades.
- ASIC development is progressing with a dedicated team; the first version of the ASIC designs have been submitted, and fully functional chips are expected within 2–4 years.
- Collaborations are very welcome.



Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences



Backups

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Manpower for electronics system

	Overall	BEE	VTX	TPC	ITK+OTK (LATRIC)	CAL (SiPM)	Muon	Data Link	Power	Wireless
Staff	5	1	10	1	9	5	1	9	7	4
Postdoc + Student	0	3	8	4	10	6	0	16	3	5
Total Sum	5	4	18	5	19	11	1	25	10	9

The headcounts are not to the FTE

Some staffs are shared by multiple projects, while postdocs / students are dedicated to the projects

ITK Barrel Design with HV-CMOS Pixels

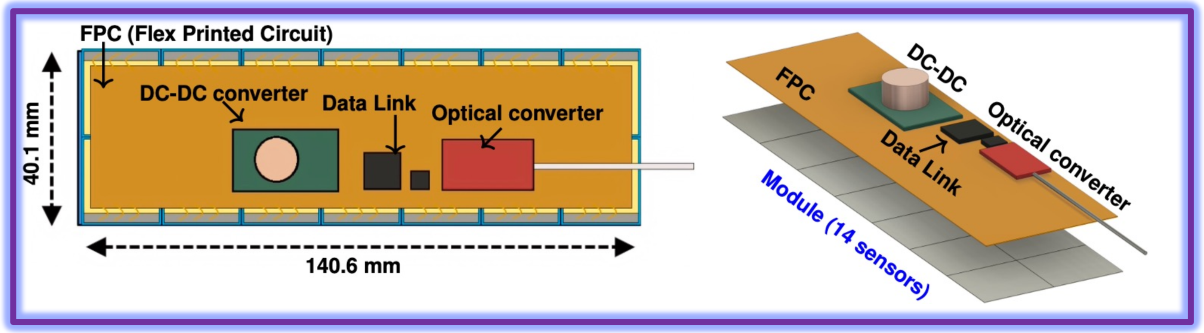
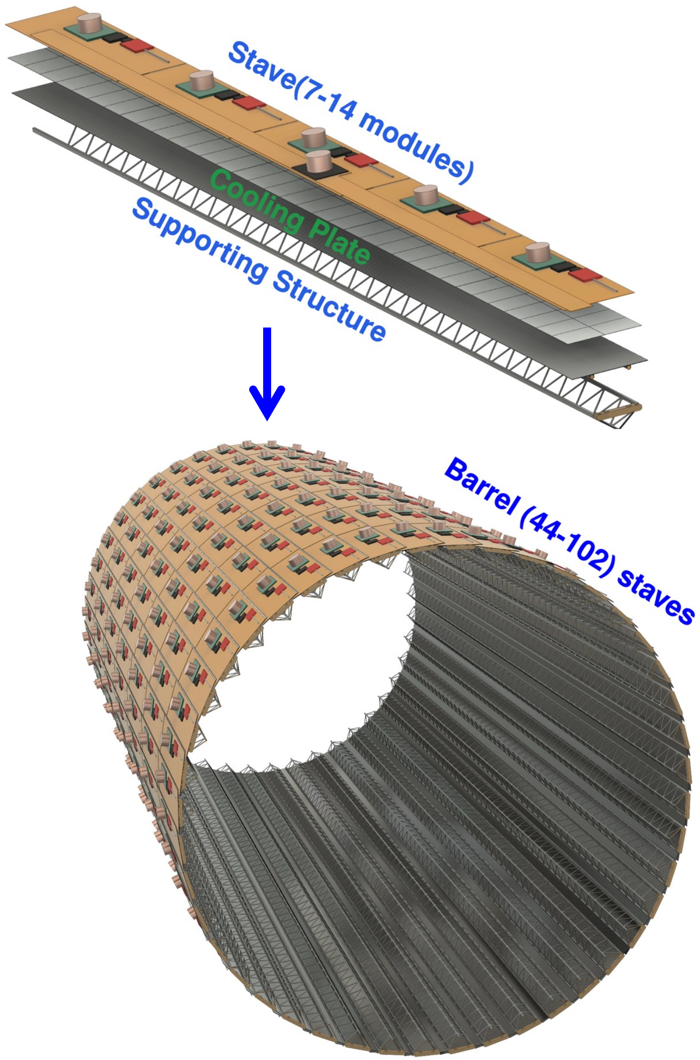


Figure 5.37



- HV-CMOS pixel sensor:
  - Sensor size: 20 mm × 20 mm
  - Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
- Module:
  - 14 sensors (2 rows × 7 columns)
  - Module dimensions: 140.6 mm × 40.1 mm
- Stave length: 986.6 mm (ITKB1), 1,409.6 mm (ITKB2), and 1973.2 mm (ITKB3)
- Barrel radii: 235 mm (ITKB1), 345 mm (ITKB2), and 555.6 mm (ITKB3)

The designed 3 ITK barrel layers has a total surface area of 13.3 m², including 33,264 sensor chips, with a power consumption of ~26.6 kW.

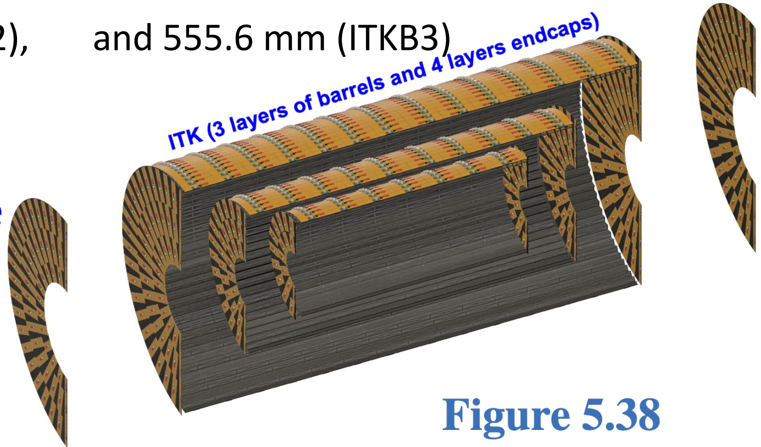


Figure 5.38

Summary of FEE power

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Technology	65nm CIS	55nm HVCMOS	55nm HVCMOS	55nm CMOS		65 CMOS	55nm CMOS (or 180 CMOS?)				
Power Supply Voltage (for DC-DC) (V)	1.2	1.2	1.2	1.2		1.2	1.2 (or 1.8?)				
Power@chip	40mW/cm^2 200mW/chip	200mW/cm^2 800mW/chip	200mW/cm^2 800mW/chip	20mW/chn 2.56W/chip		280μW/chn 35mW/chip 100mW/cm^2	15mW/chn 240mW/chip				
Max chips@module	29	14	14	22	22	1115	64	120	8	92	167
Power@module (W)	5.8	11.2	11.2	27.6	27.6	32.2	30	30	9	11	4.7

The Counting room

Minimum crates from current MDI

- 107 data crates, 227 power crates, 78 Det-HV crates, 20 Trigger crates

Minimum racks from current MDI

- 37 data racks, 24 power racks, 23 Det-HV racks, 10 trigger racks (94 in total)
- More 2 racks for AC-DC power for all the above racks
- 96 racks in total

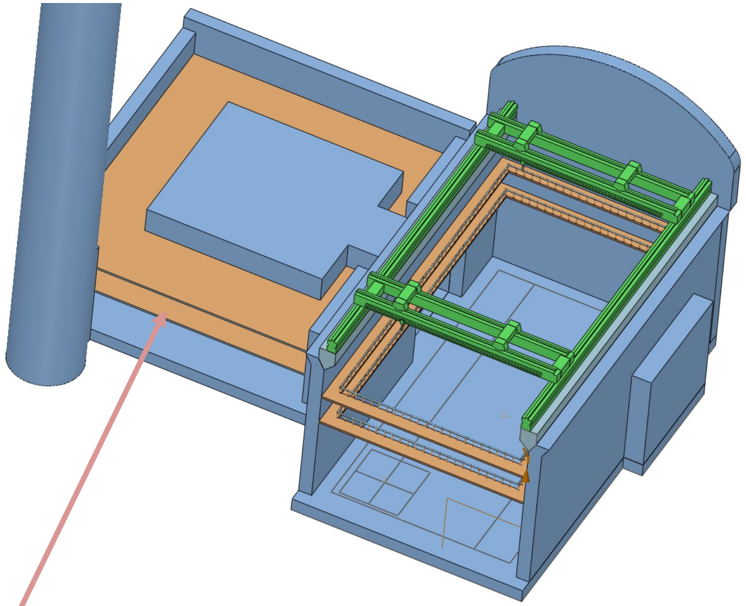
Racks Size: 0.5m × 0.5m

Side clearance 1.5m for heat, face clearance 2m for cabling & heat

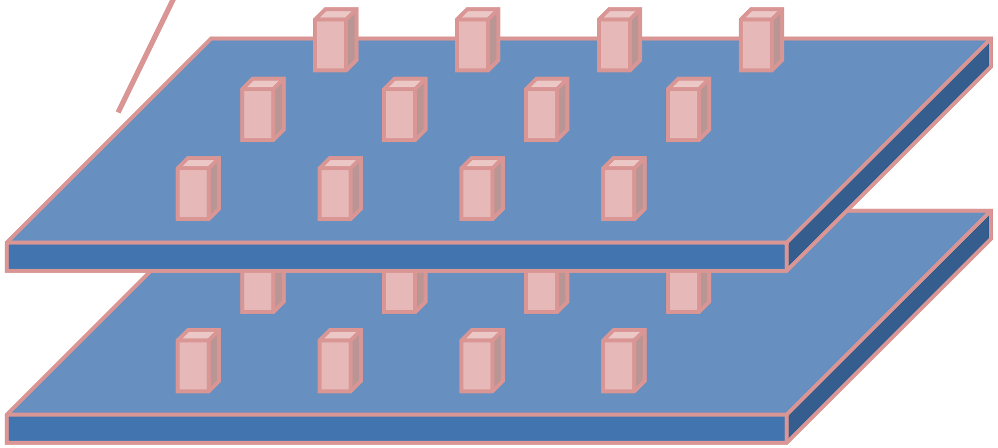
- Very rough estimation: 20% more power will be consumed due to the crate efficiency

Total room: $500\text{m}^2 \times 2$floor = 25m × 20m × 2floor

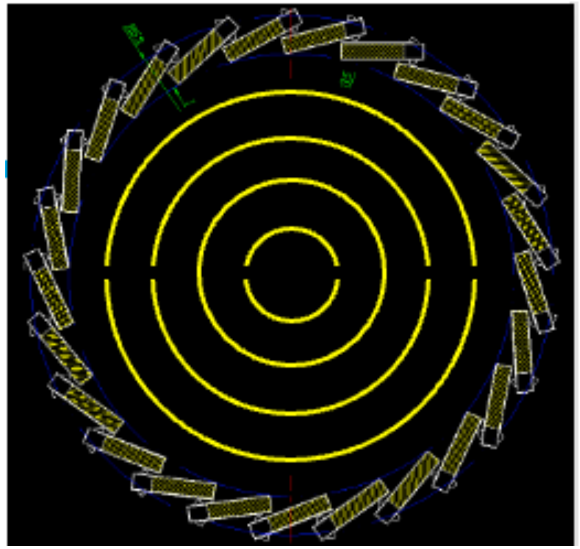
- 10 × 10 × 2=200 racks capacity
- Necessary redundancy for future upgrade

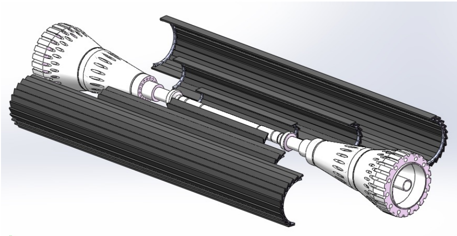


See Quan Ji's talk on Mechanics



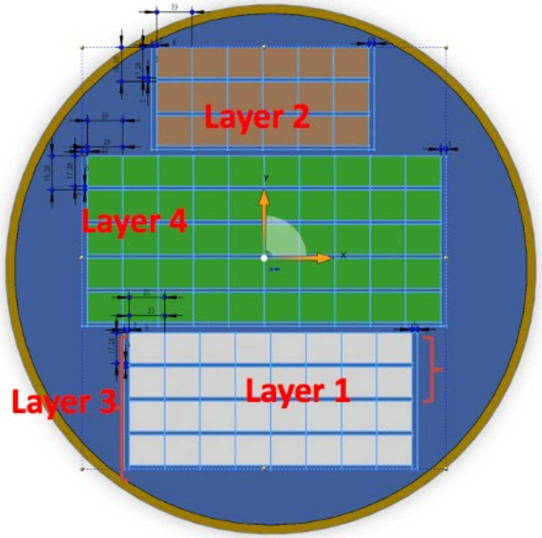
VTX-Data Link





Layer	Hit density (Hits/cm2/BX)	BXRate (Hz)	Hit density (kHits/cm2/s)	Safe factor	Cluster size
VTX-1 (Higgs)	0.65	1.34E+06	870	1.5	3
VTX-2 (Higgs)	0.43		580	1.5	
VTX-3 (Higgs)	0.09		116	1.5	
VTX-4 (Higgs)	0.08		110	1.5	
VTX-5 (Higgs)	0.05		70	1.5	
VTX-6(Higgs)	0.05		68	1.5	

- VTX scheme: Inner 4 layers stitching, with 1 typical double-sided ladder (layer 5&6)
- Bkgrd rate @50MW @Higgs with safety factor 1.5
- Assume RSU@stitching = ladder chip = 1024*512 matrix, then data rate for the innermost layer for a "chip" is 2Gbps, other layers according the bkgrd ratio
- Inner 2 layers needs 2 fiber chns for each row, due to the high data rate
  - possible to merge into less optical MTX interfaces
- In total 88 fibers = 6 BEE Brd = 1 Data Crate



From Zhijun

Layer	Comment	Data Rate/chip	Chips/Row	Data rate/row	Rows	Links@10Gbps
1	Stitching	2Gbps	8	16G	2*2=4	2*4=8（2 fiber chns）
2	Stitching	1.3Gbps	12	15.6G	3*2=6	2*6=12（2 fiber chns）
3	Stitching	0.27Gbps	16	4.3G	4*2=8	1*8=8
4	Stitching	0.25Gbps	20	5G	5*2=10	1*10=10
5	Ladder-side0	0.16Gbps	29	4.64G	25	1*25=25
6	Ladder-side1	0.16Gbps	29	4.64G	25	1*25=25