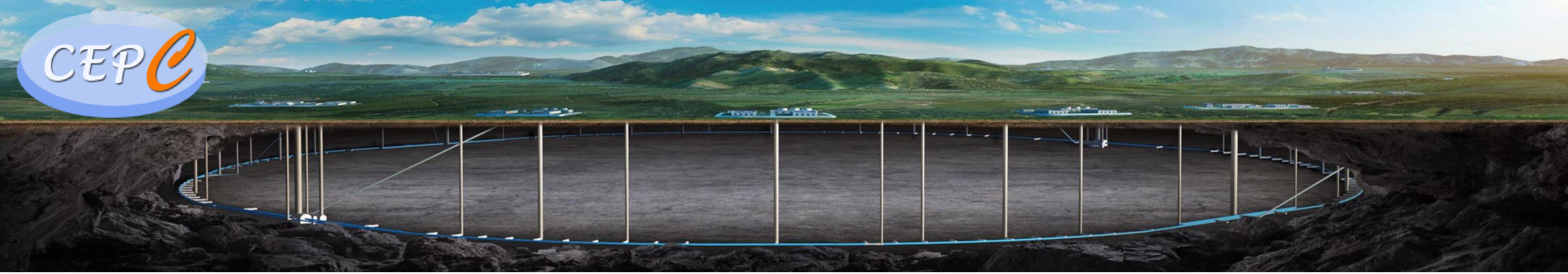

Sensor and electronics design for the Vertex Detector

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Content

- CEPC Vertex detector requirements
- R&D efforts and results
- Stitched sensor prototype design
- Readout electronics
- Summary

Vertex Requirement

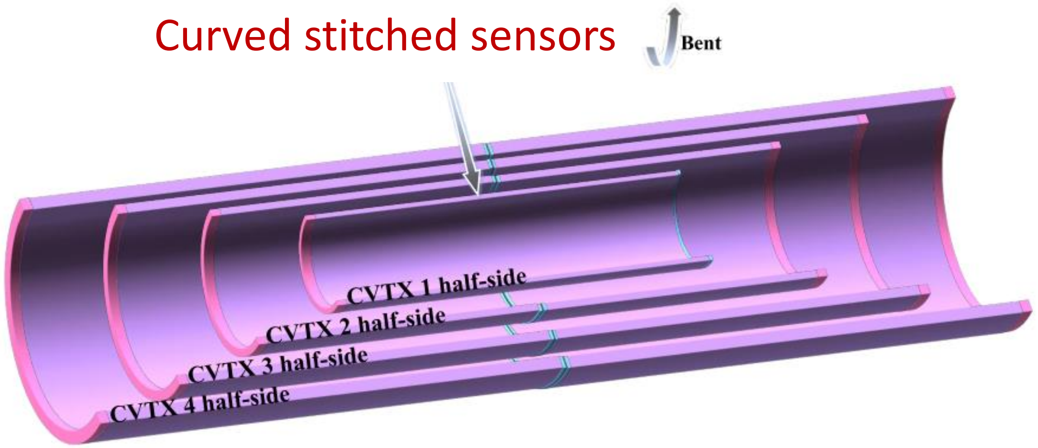
- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - Challenges: Radius (11.1 mm) is smaller compared with ALICE ITS3 (18 mm)

    Requiring wafer-scale stitched Monolithic Active Pixel Sensors (MAPSs)

Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	$\sim 5\ \mu\text{m}$
Detector material budget	$\sim 0.8\%\ X_0$
First layer radius	11.1 mm
Power Consumption	$< 40\ \text{mW/cm}^2$ (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}\ \text{Neq/cm}^2$ (for first 10 years)
Operation Temperature	$\sim 5\ ^\circ\text{C}$ to $30\ ^\circ\text{C}$
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

Curved stitched sensors



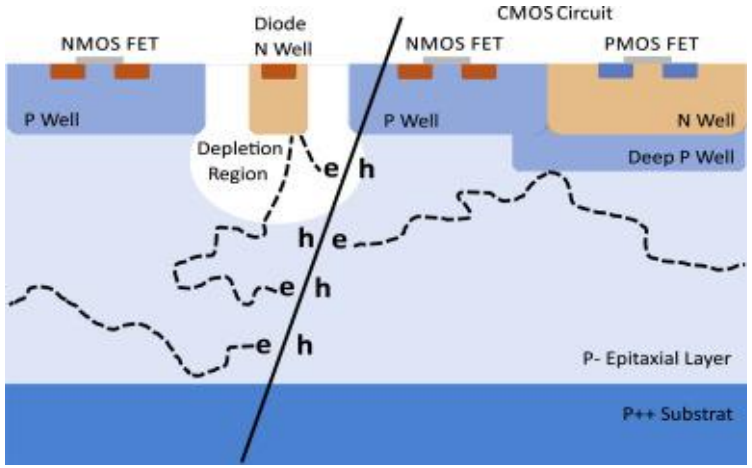
First four semi-cylinder layers for CEPC VTX

Ref: CEPC Detector Ref-TDR

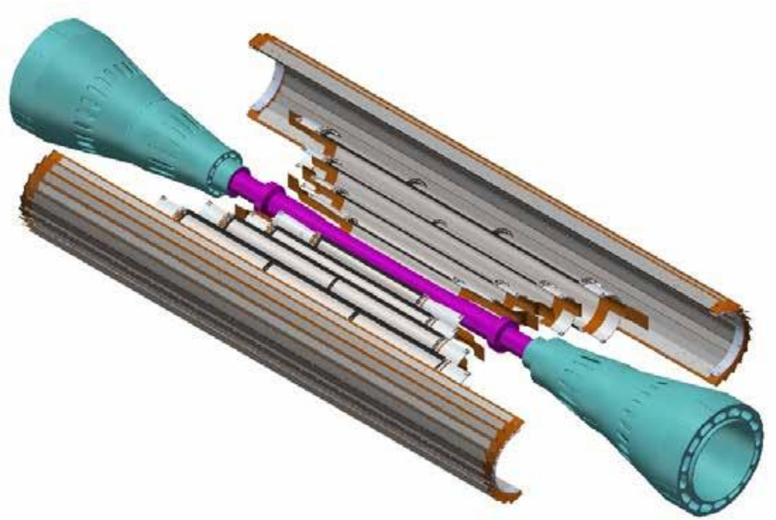
Technology for CEPC Reference TDR

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design [1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: ladder design based on CMOS MAPS

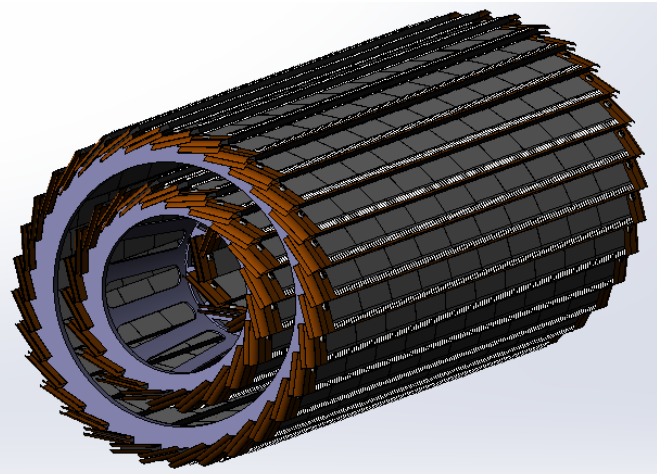
CMOS Monolithic Active Pixel Sensor



Baseline: curved MAPS



Alternative: ladder based MAPS

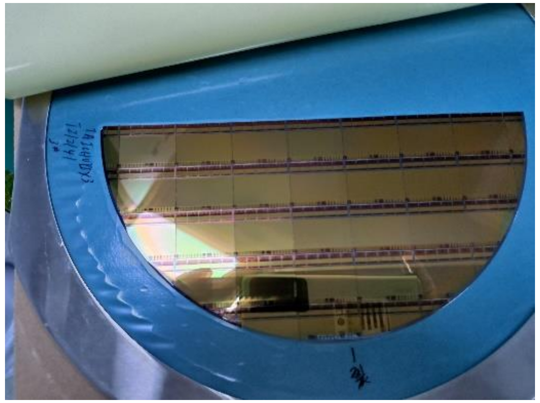


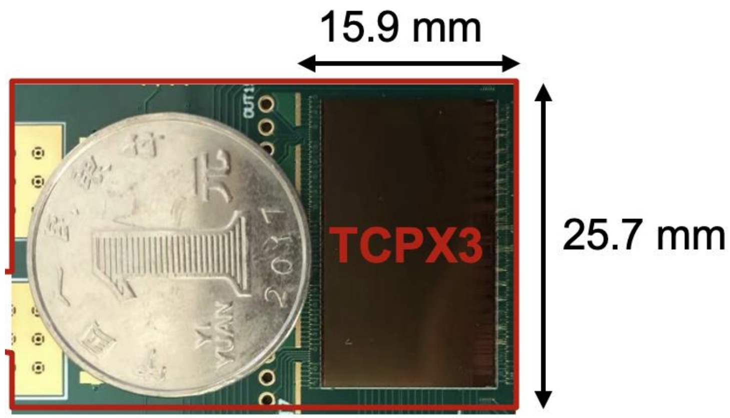
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

R&D efforts: Full-size pixel sensor chip

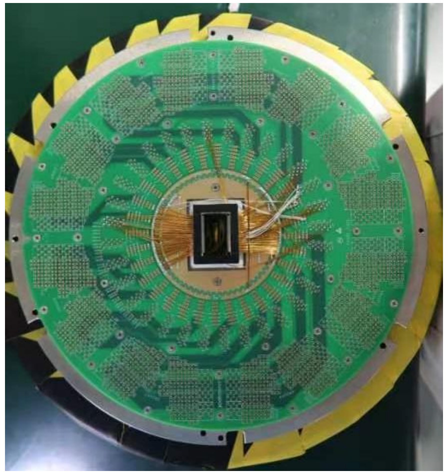
Full reticle-size CMOS MAPS developed, 1st engineering run

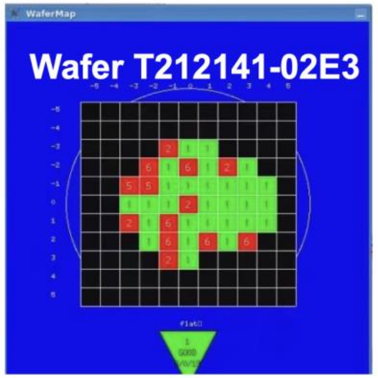
- 1024×512 pixel array, Chip Size: 15.9 mm×25.7 mm
- 25 μm×25 μm pixel size with high spatial resolution < 5 μm (@ detection eff. > 99%)
- Process: 180 nm CIS process
- Fast data-driven readout (50 ns/pixel) to cope with all operation modes in CDR
  - Dead time < 500 ns, Max. hit rate 36 MHz/cm^2





TaichuPix-3 chip vs. coin



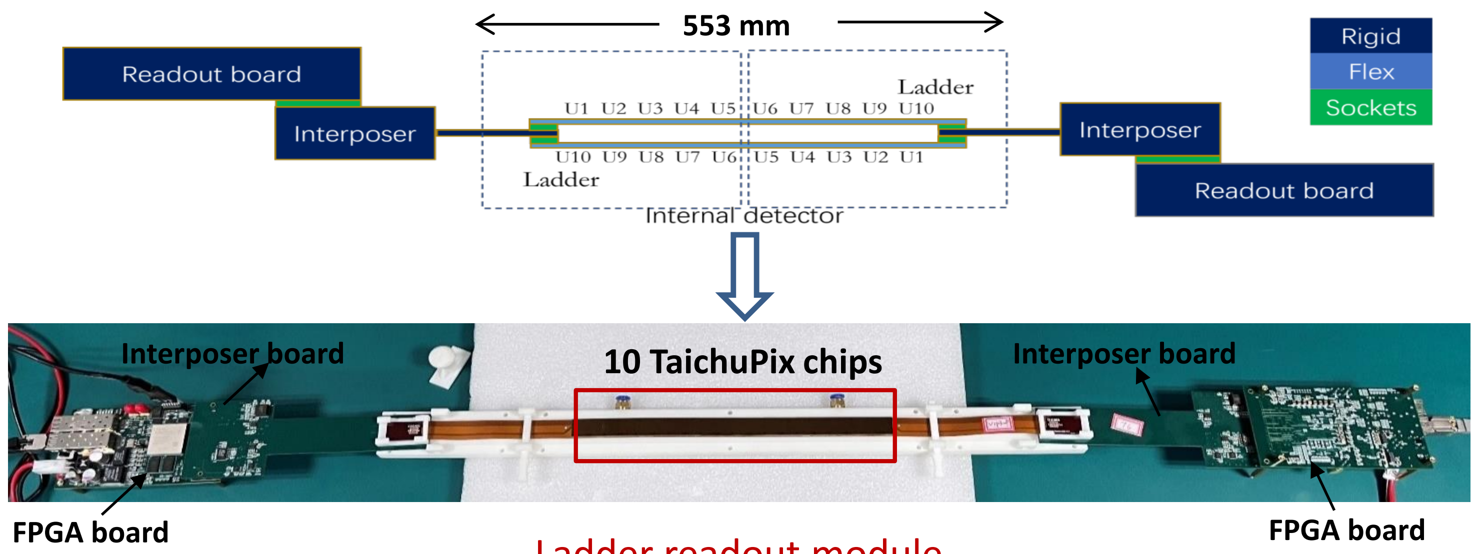


An example of wafer test result

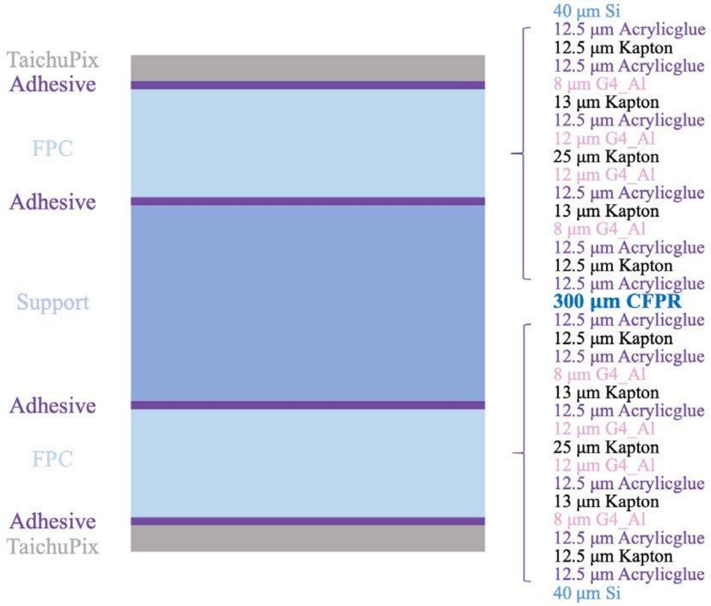
	Status	CEPC Final goal
CMOS chip technology	Full-size chip with 180 nm CIS	65 nm CIS

R&D effort: Ladder readout design

- Detector module (ladder) = 10 sensors (on oneside) + support structure + readout board
  - Sensors are wire bonded to the flexible PCB, supported by a carbon fiber support
  - Signal, clock, control, power, ground will be handled by readout board through flexible PCB
- Functionality of a full ladder readout was verified
  - Read out from both ends, with careful design on power placement and low noise



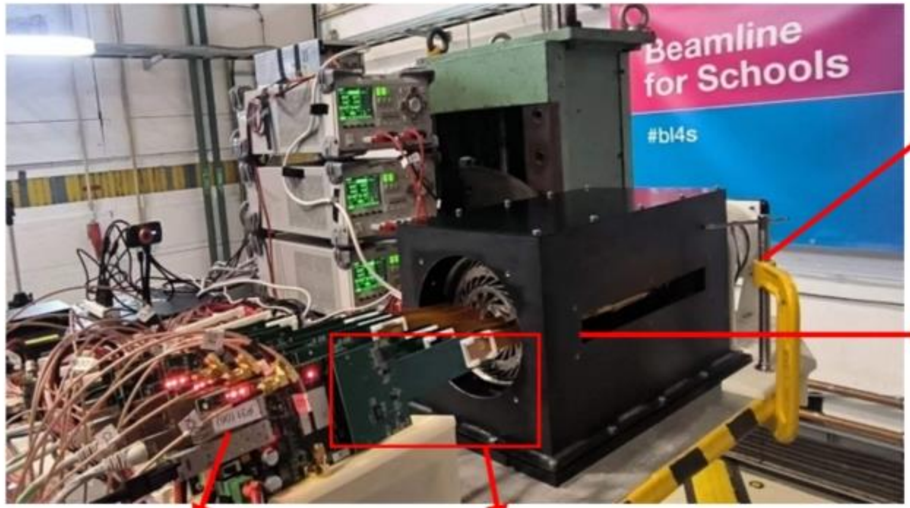
Ladder readout module



Transverse cross-section of a double-sided ladder

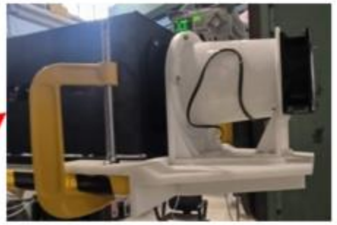
R&D effort: Vertex detector prototype

- 6 double-sided layers assembled on detector prototype
  - 12 flex boards with two TaichuPix-3 chips bonded on each flex
  - Readout boards on one side of the detector
  - Best spatial resolution 4.97 μm @ detection efficiency > 99%

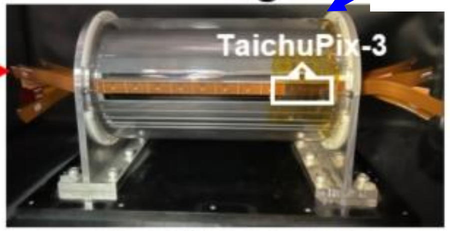


FPGA board

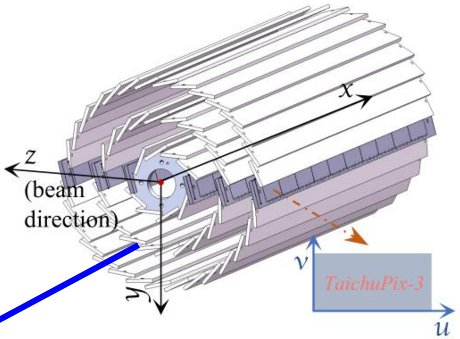
Interposer board

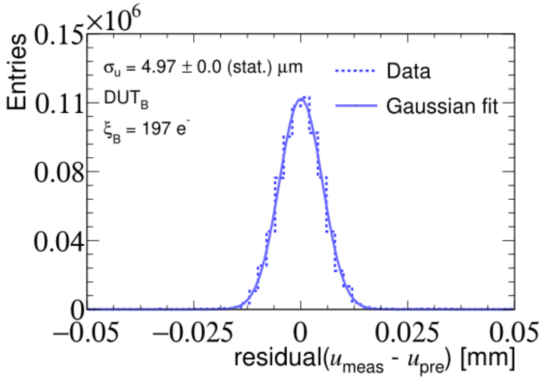


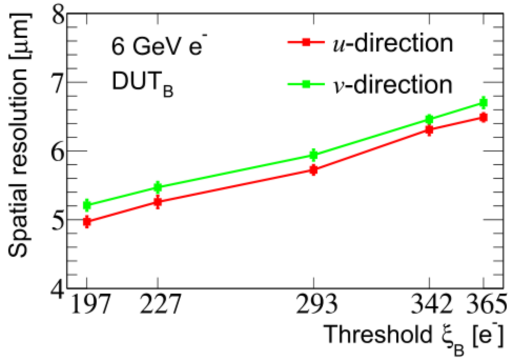
Air cooling fan

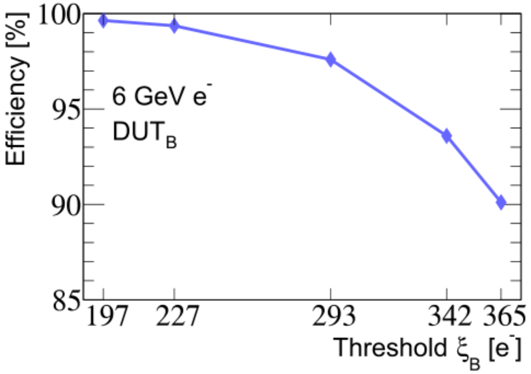


First vertex detector prototype





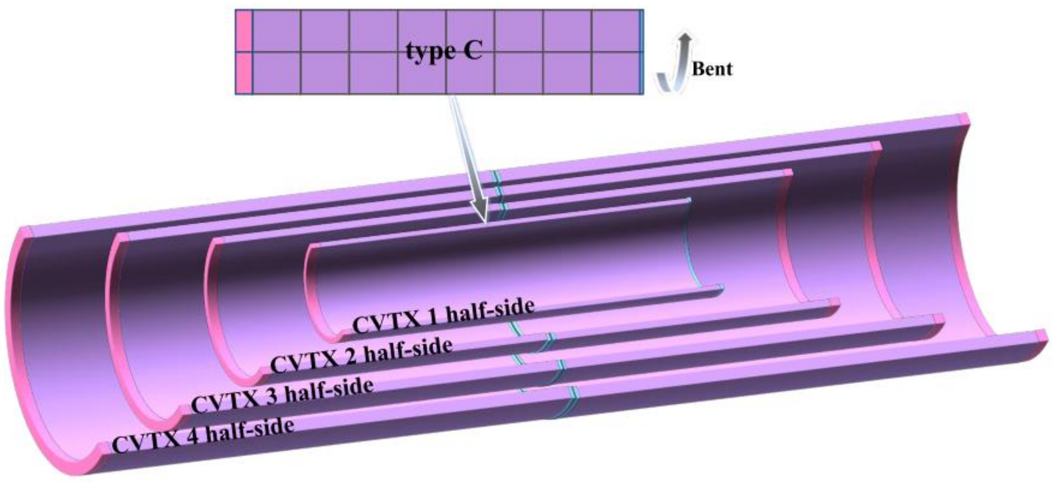




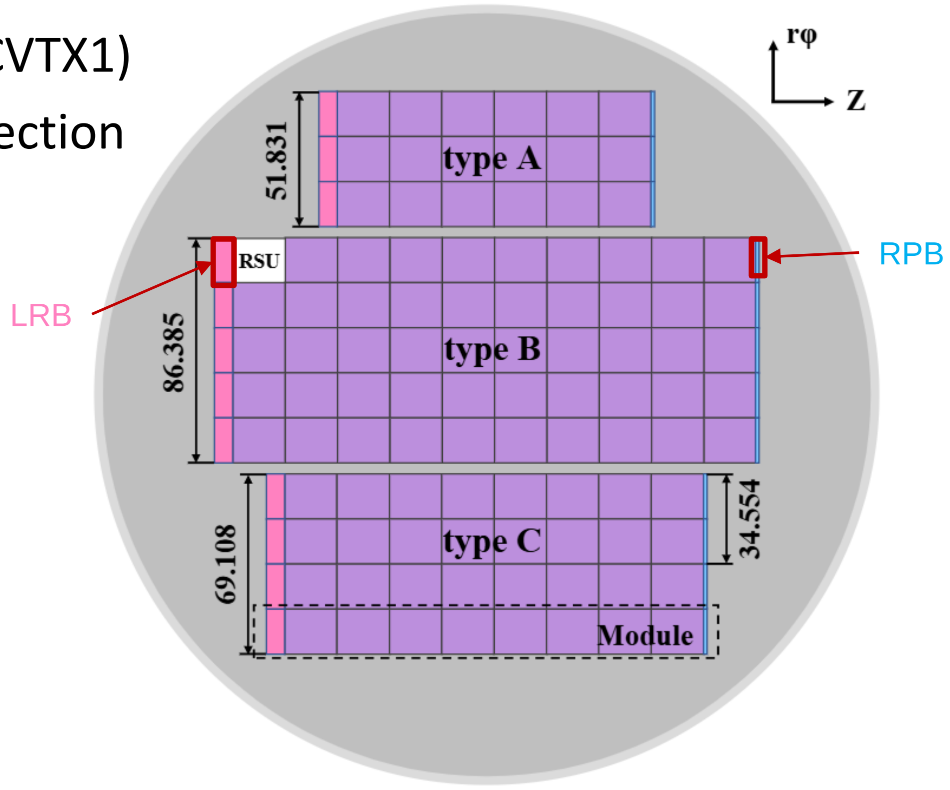
Ref: DOI-10.1109/TNS.2024.3395022

Stitched sensor prototype design

- Requiring wafer-scale bent pixel sensors for inner layers
  - Three types stitched sensors with different sizes on a wafer
    - Sharing same components (RUS, LRB, RPB)
    - One Type C sensor forms a semi-cylindrical for layer1 (CVTX1)
    - Two Type A/Type C/Type B sensors oriented along z-direction to form halves for Laye2/Layer3/Layer4



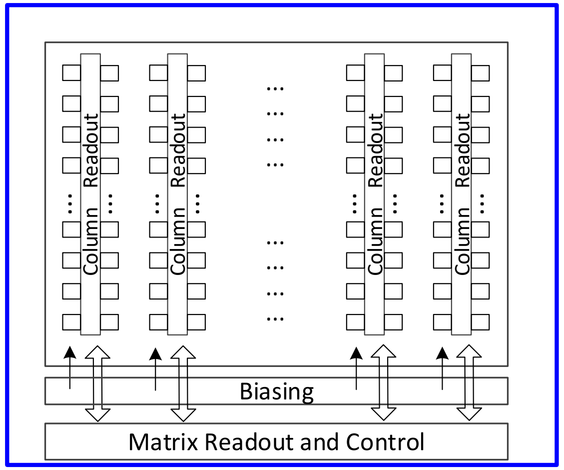
First four semi-cylinder layers for CEPC VTX



Stitching plan for a 300 mm wafer

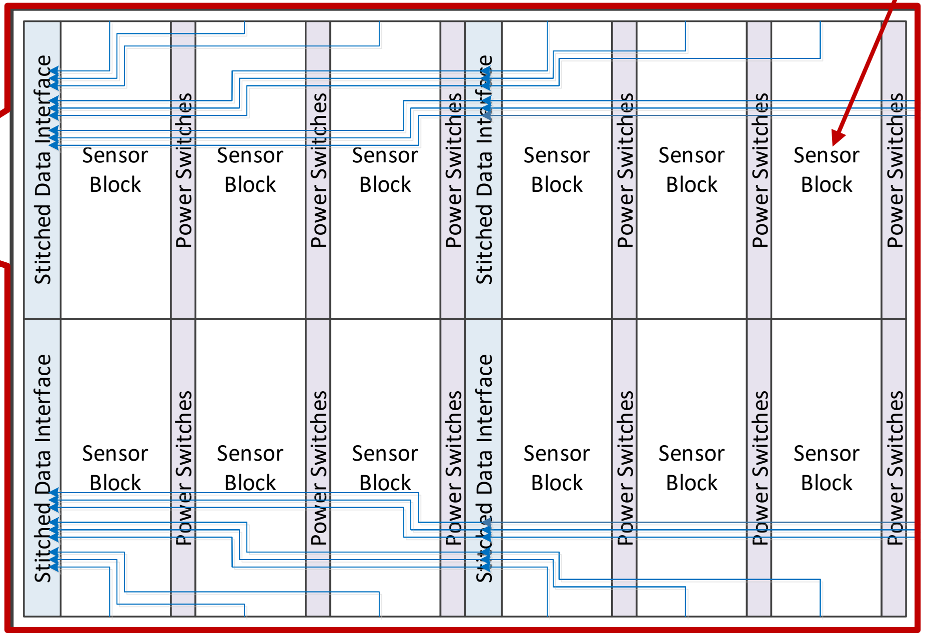
Stitched sensor prototype design

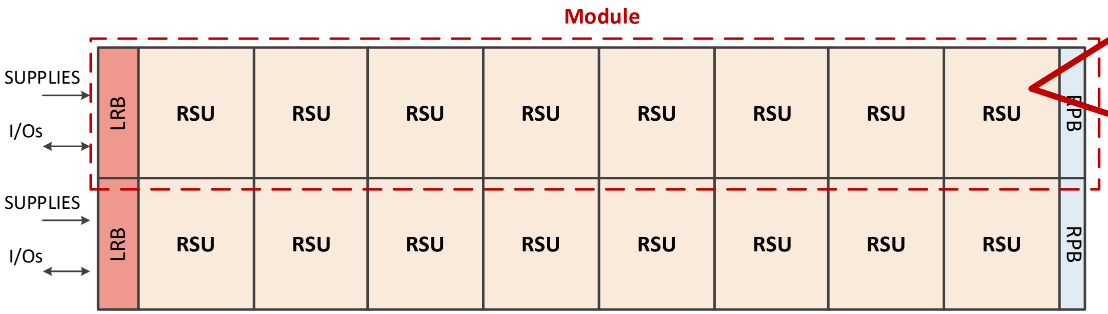
- Each stitched prototype consists of multiple RSUs (Repeated Sensor Unit), 1 LRB (Left-end Readout Block) and 1 RPB (Right-end Power Block)。
  - An RSU is composed of multiple independent Sensor Blocks, each transmits low-speed serialized data to the left edge of chip.
  - LRB acts as data collector, high-speed data interface and power supply with external.
  - RPB contains solely power transmission buses



Sensor Block (design derived from TaichuPix3)

RSU (Repeated Sensor Unit)



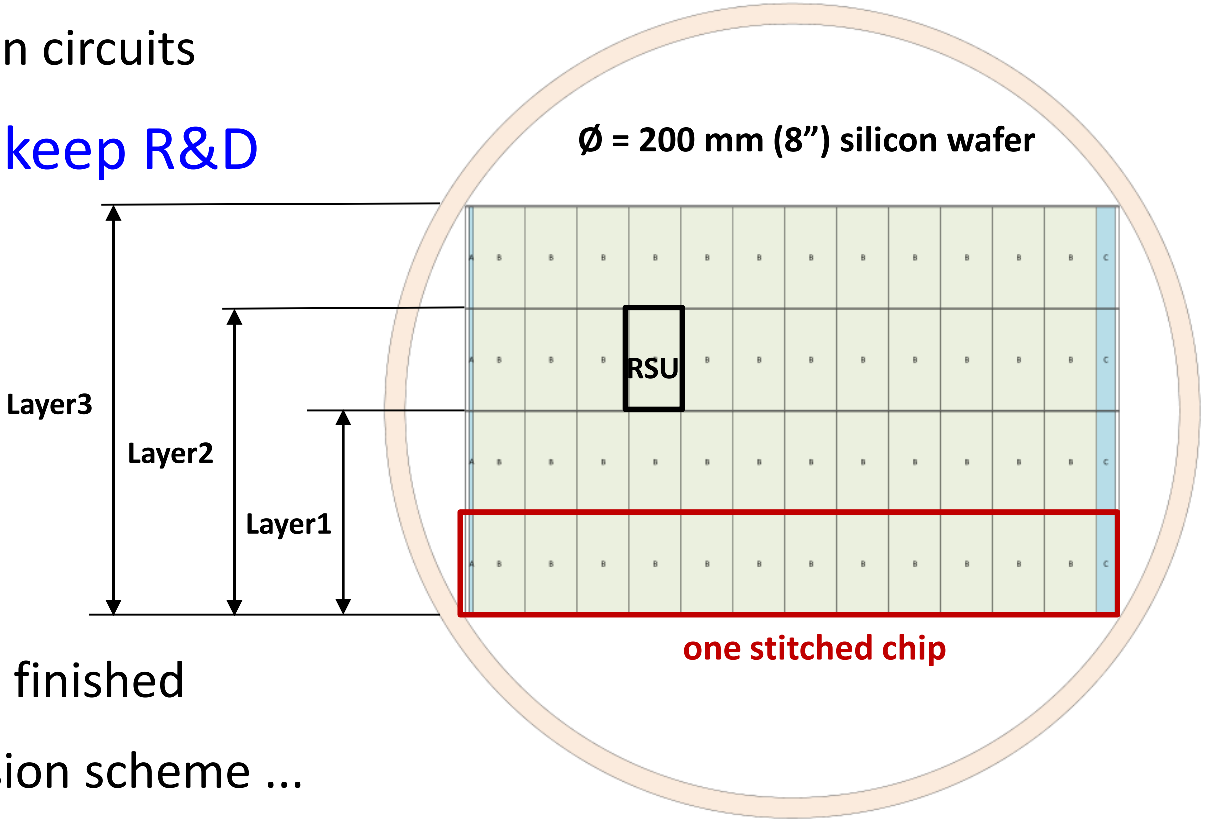


Schematic floorplan of the sensor for layer1

Design of the first stitched chip

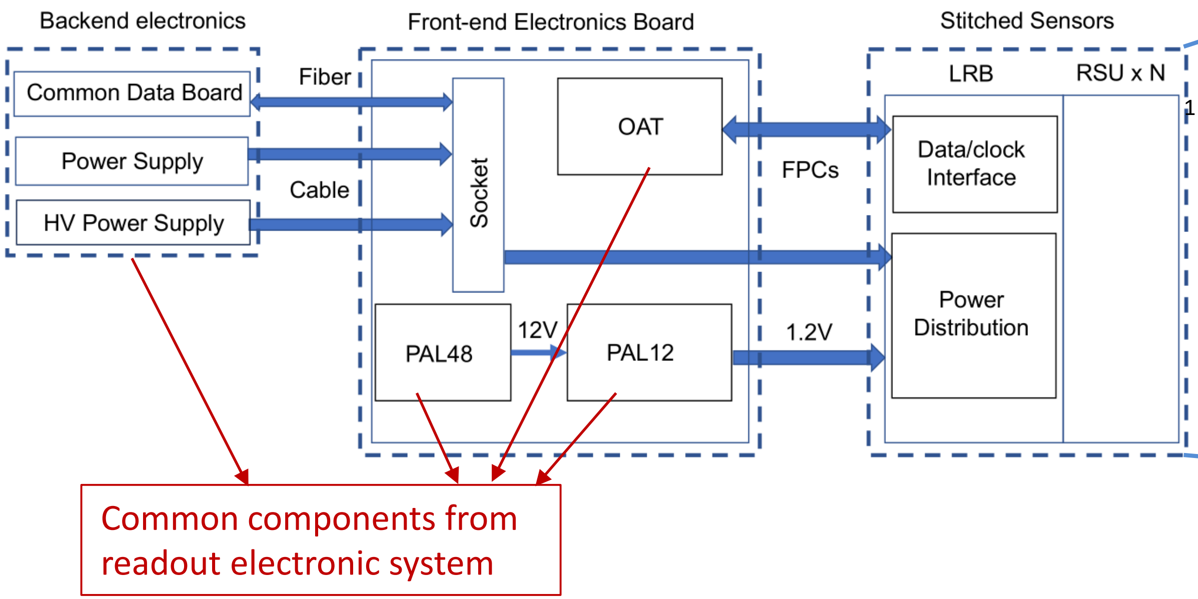
- Main goals:
  - Feasibility validation of the stitching technology
  - Architecture and functionality validation of the main circuits
- Design based on previous R&D prototypes, to keep R&D risks and costs within reasonable bounds.
- Design status
  - Preliminary design of stitching floorplan done
    - Four stitched chips per wafer
  - Preliminary architecture design of the stitched chip finished
    - Chip size, specific RSU floorplan, data transmission scheme ...
  - Detailed circuit design ongoing

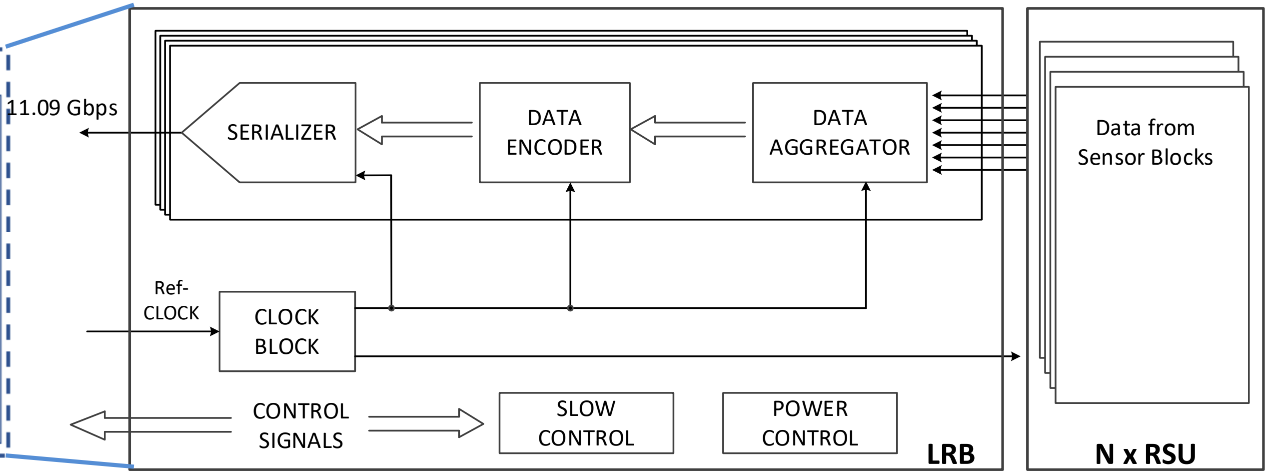
Stitching plan for a 200 mm wafer



Readout electronics

- Stitched sensors wire-bonded on FPCs to connect to Front-end Electronics Board (FEE)
  - LRB of stitched sensors aggregates data of RSUs, distributes clock and control signals, and handles local power distribution
- FEE boards include optical transceivers and power regulators
  - OAT (Optical Array Transceiver) converts electrical signals into optical signals and transmits them over fibers to Back-End Electronics (BEE)
  - Power management: two-stage DC-DC conversion scheme (two Power-at-Load (PAL) modules)

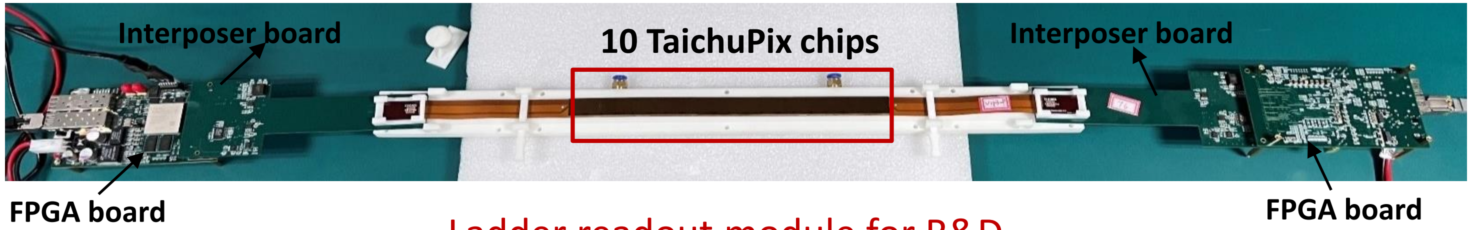




Simplified readout chain of a stitched sensor

Readout electronics

- Outer layer (L5-L6): flexible PCB (also used in alternative layout)
  - Preliminary ladder readout module verified in previous R&D
  - Customized rad-tolerant ASICs will be used for data link and DC-DC converter



Ladder readout module for R&D

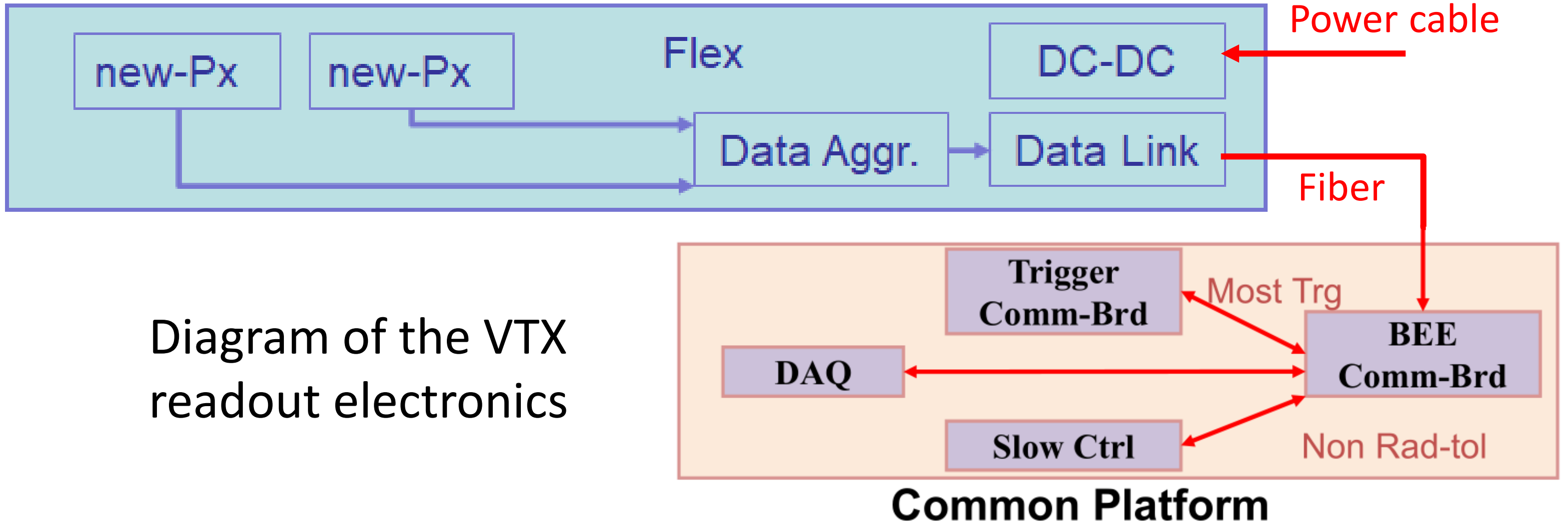


Diagram of the VTX readout electronics

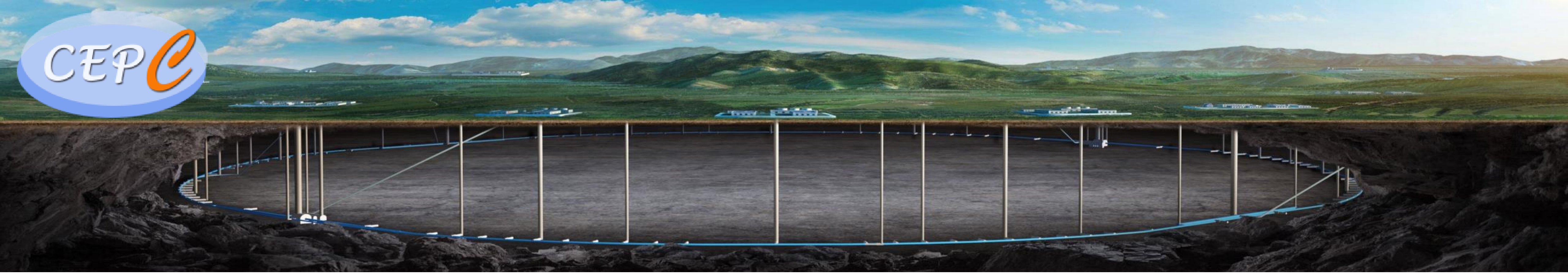
Background data rate and cabling on data

	Higgs	Low-Lumi Z
Background hit rate (MHz/cm^2)	6.4	15
Data rate/Link (Gbps)	20	47
Fiber channels to BEE	96	
BEEs	6	
Crates	1	

Talk on BEE: 5:10 PM, 8th Nov., Jun Hu

Summary

- CEPC vertex detector requires wafer-scale monolithic pixel sensors for the inner four layers
  - First stitched chip based on 180 nm process under designing
    - Feasibility validation of the stitching technology
    - Architecture and functionality validation of the main circuits
  - Next generation stitched chip expected to transition to 65/55 nm
- Customized front-end electronics (FEE) for VTX
  - For Layer1-4, FEE boards contain optical transceivers and power regulators
  - For Layer5-6, ladder readout will be built based on the previous R&D
- Back-end electronics (BEE) of VTX based on the common platform
  - Common platform for all sub-detector system



Thank you for your attention!

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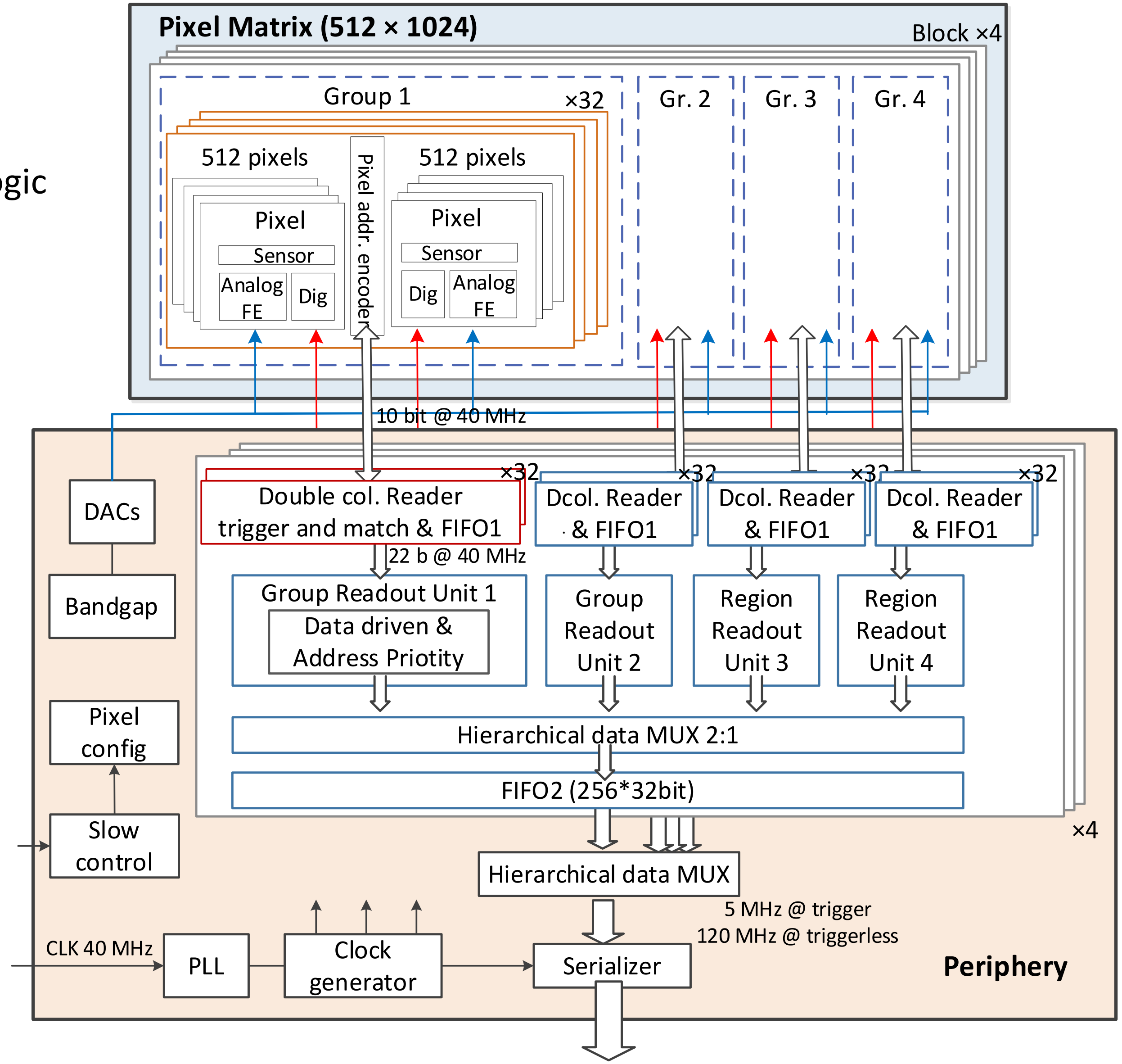
TaichuPix architecture

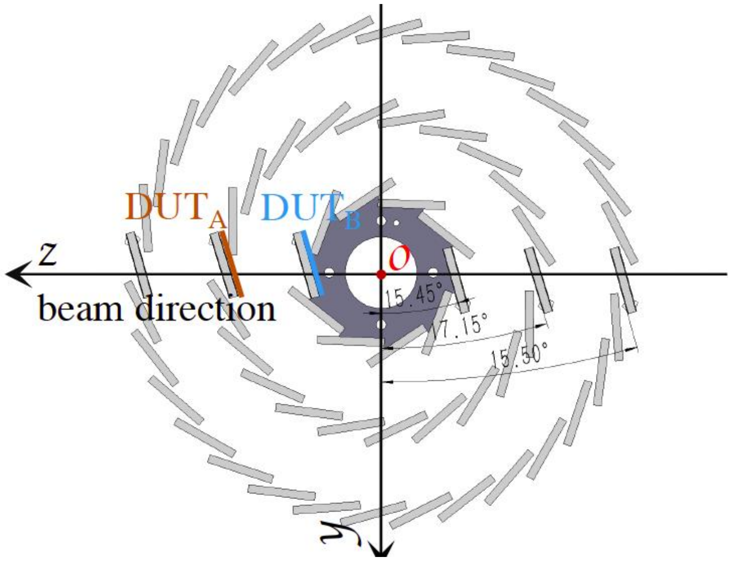
- Pixel 25 µm × 25 µm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Readout time: 50 ns for each pixel
- 2-level FIFO architecture
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- Features standalone operation
  - On-chip bias generation, LDO, slow control, etc

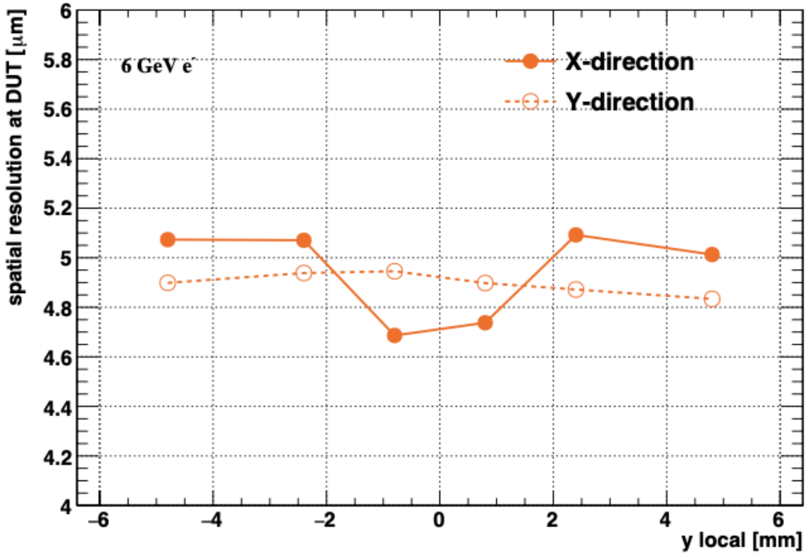


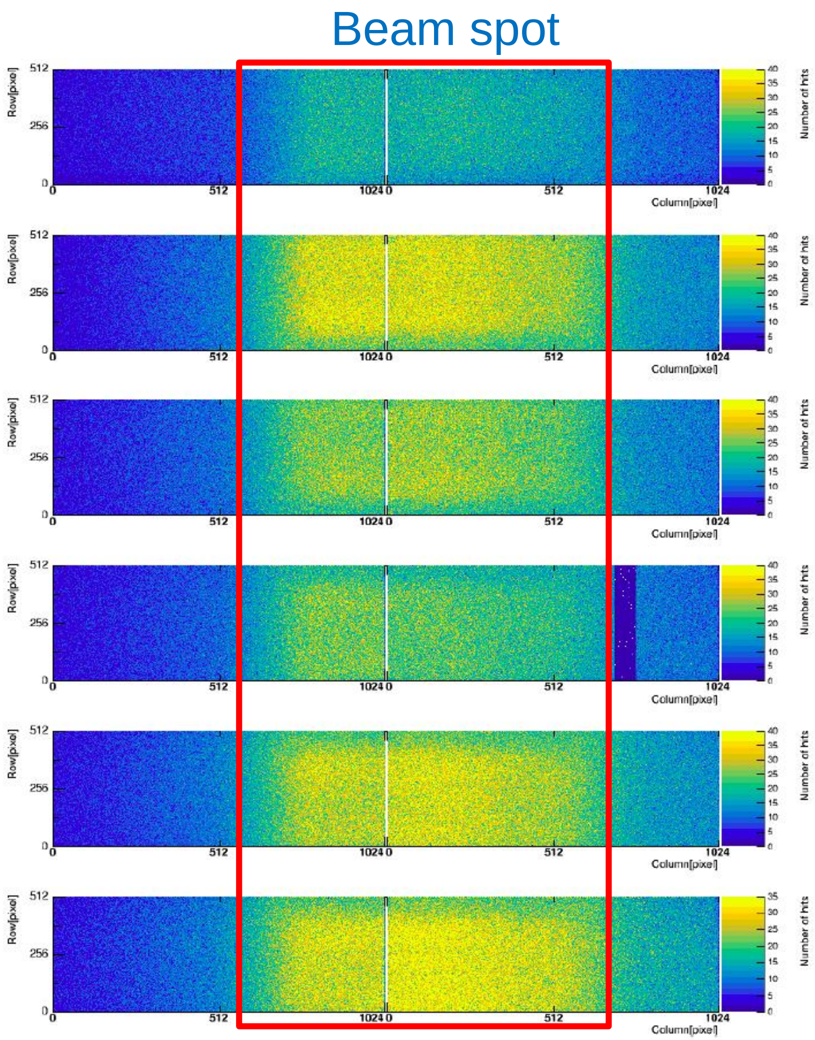
R&D efforts and results: vertex detector prototype beam test

Hit maps of multiple layers of vertex detector

Spatial resolution ~5 μm   Efficiency >99%







	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

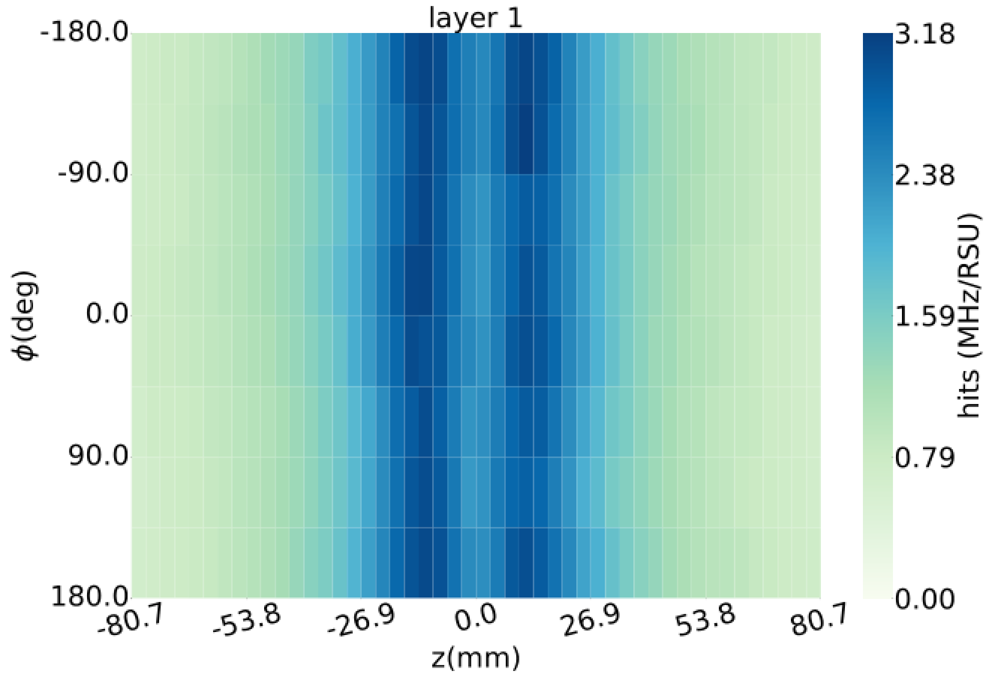
Background estimation

- Background rate are simulated
  - The data rate at low-lumi Z pole is about ~Gbps level in b-layer

Background rate for Higgs and low-lumi Z runs

Layer	Ave. Hit Rate (MHz/cm^2)	Max. Hit Rate (MHz/cm^2)	Ave. Data Rate (Mbps/cm^2)	Max. Data Rate (Mbps/cm^2)
Higgs mode: Bunch Spacing: 277 ns, 63% Gap				
1	6.2	12	760	1500
2	0.84	1.6	87	160
3	0.17	0.36	19	38
4	0.067	0.16	8.4	19
5	0.017	0.037	2.1	4.2
6	0.013	0.026	1.6	3.7
Low-luminosity Z mode: Bunch Spacing: 69 ns, 17% Gap				
1	15	39	2700	8100
2	1.7	2.6	240	400
3	0.72	1.2	110	240
4	0.43	0.94	70	210
5	0.10	0.19	14	31
6	0.078	0.15	11	23

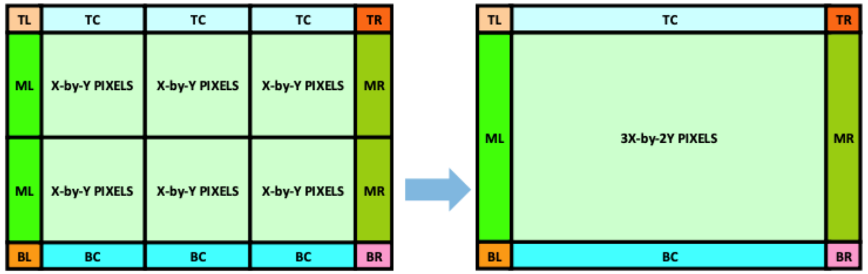
Hit rate map for 1st layer @ low-lumi Z run



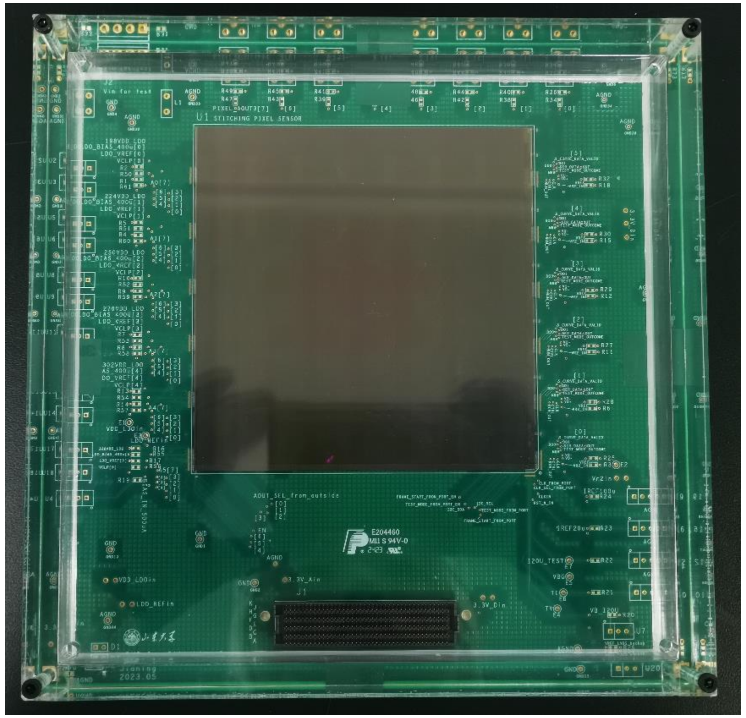
R&D efforts and results: R&D for curved MAPS

Stitching chip design (by ShanDong U.)

- 350 nm CIS technology Xfabs
- Wafer level size after stitching ~11 ×11 cm^2
- reticle size ~2 ×2 cm^2
- 2D stitching
- Engineering run, chip under testing



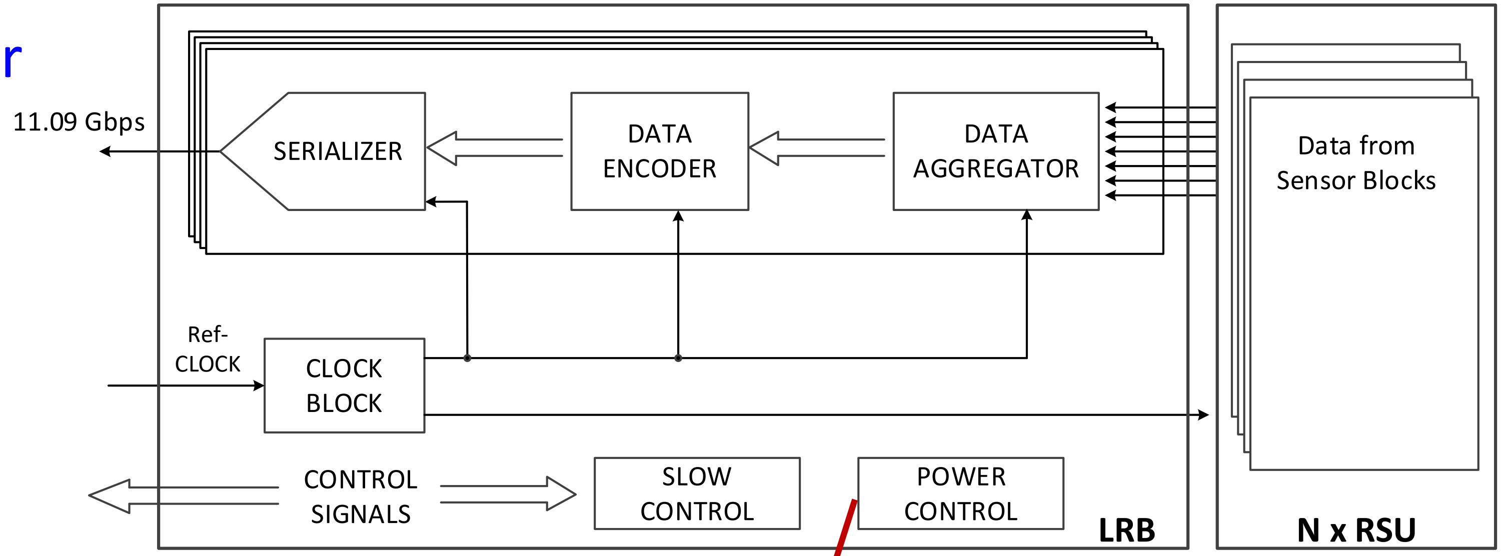
Stitching chip : 11 × 11 cm^2

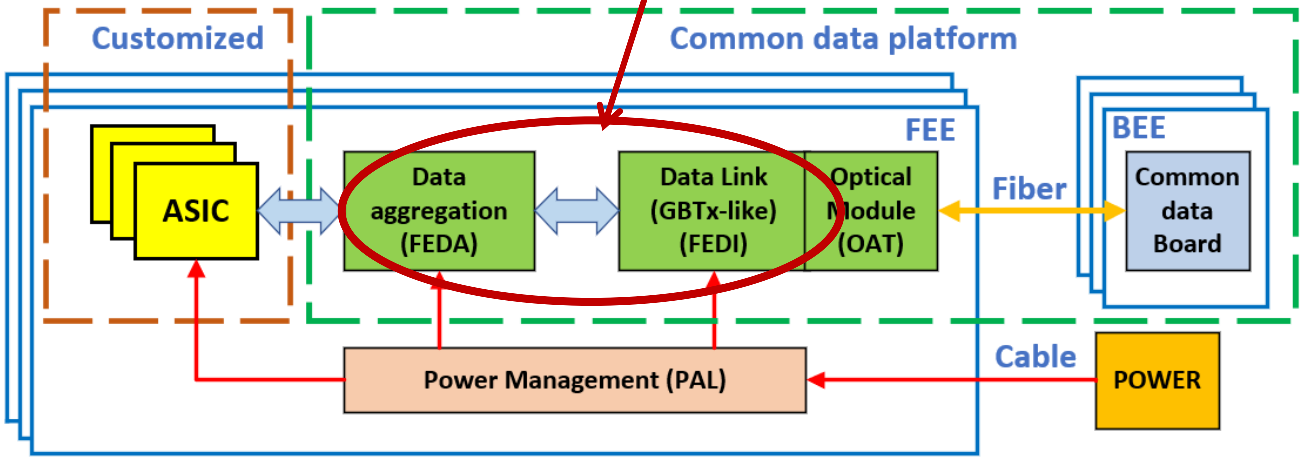


Key technology	Status	CEPC Final goal
Stitching	11*11cm stitched chip with Xfab 350 nm CIS	65 nm CIS stitched sensor

Data Transmission Structure

- LRB in stitched sensor





Common data transmission ASICS