The Readout for the Silicon Tracker

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& Electronics Group

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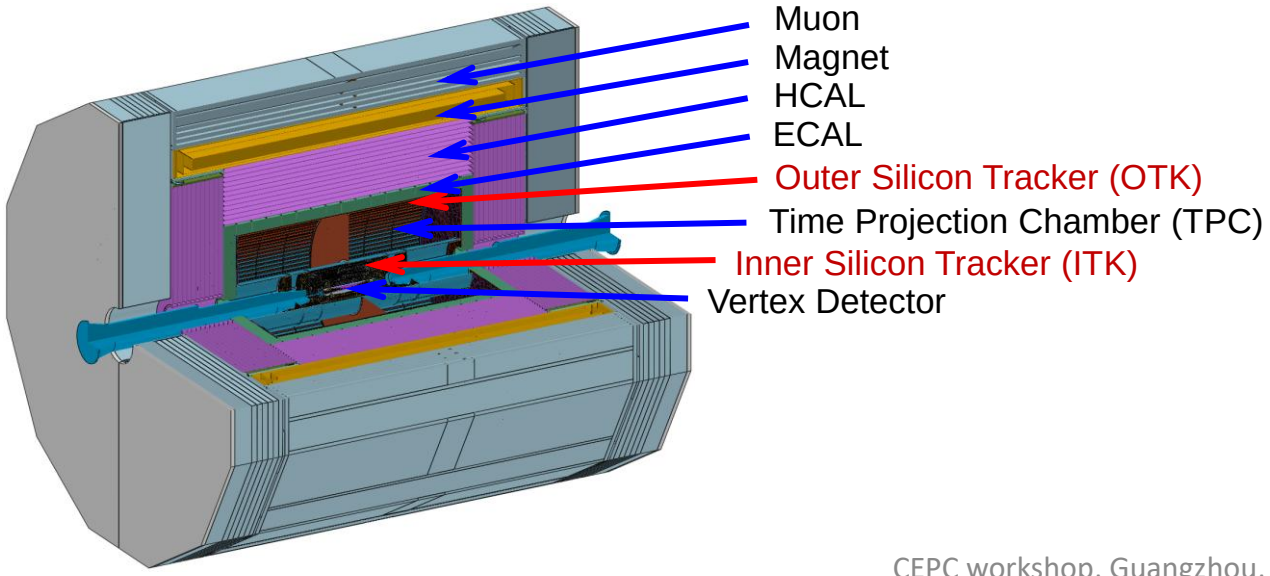
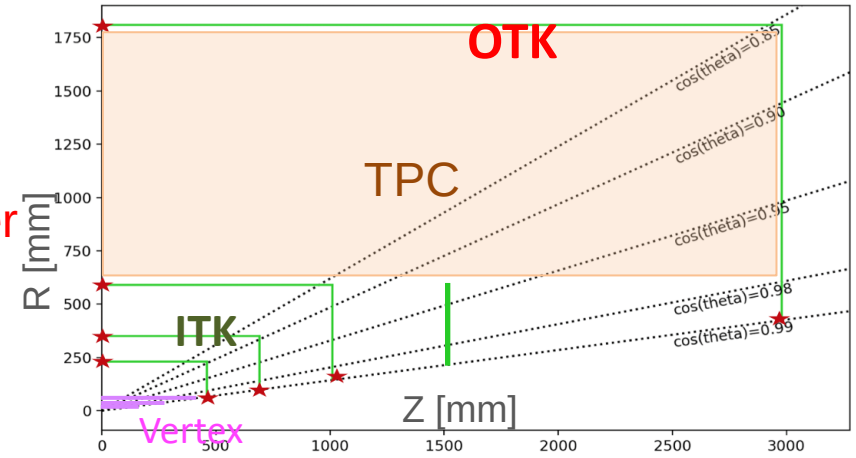
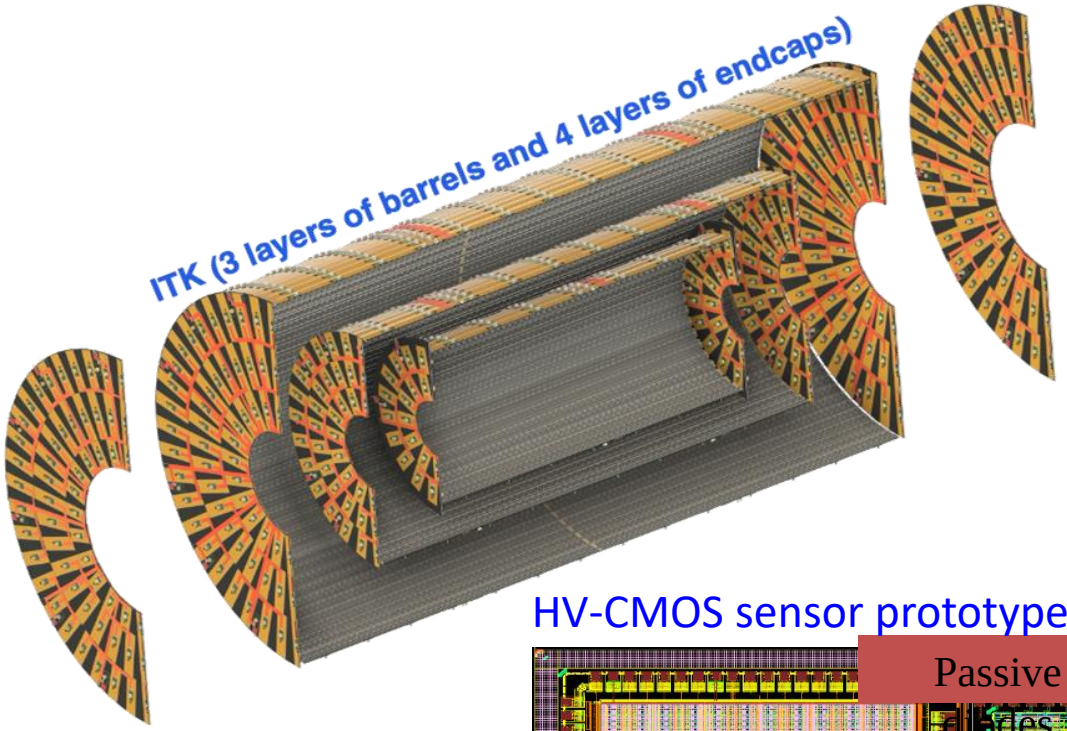
Introduction

- The CEPC tracker system includes several detectors: the Vertex Detector, Inner Silicon Tracker, Time Projection Chamber (TPC), and Outer Silicon Tracker.
- The ITK employs advanced CMOS sensor technology to achieve precise position measurements for accurate particle trajectory determination.
- The OTK integrates the AC-LGAD for precision time measurement of charged particles, significantly enhancing particle identification capabilities.



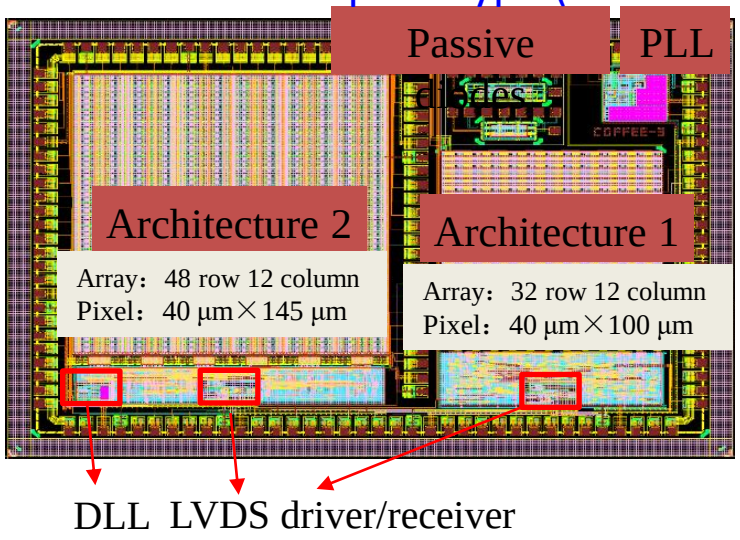


ITK Design Based on HV-CMOS Pixel Sensor



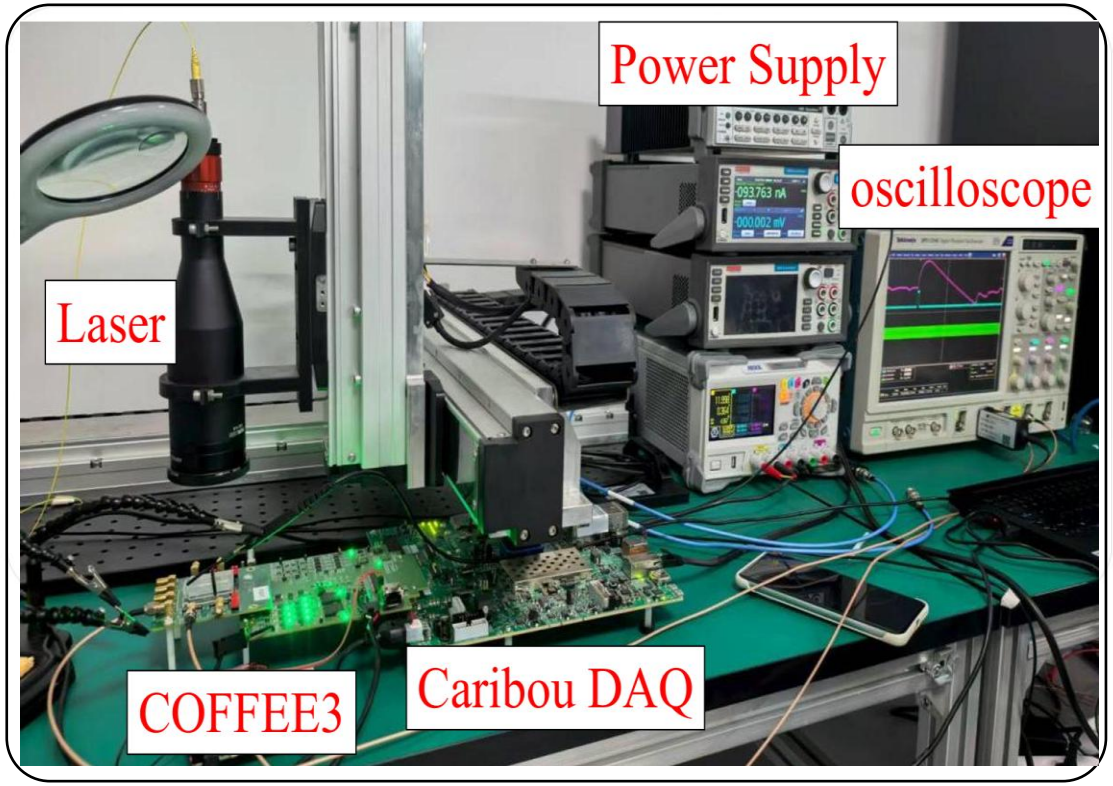
- Three barrel and four endcap layers (~20 m^2).
- Monolithic HV-CMOS pixel sensor is applied.
- Three rounds prototype tape-outs, including sensor, CSA, comparator, TDC, serializer.

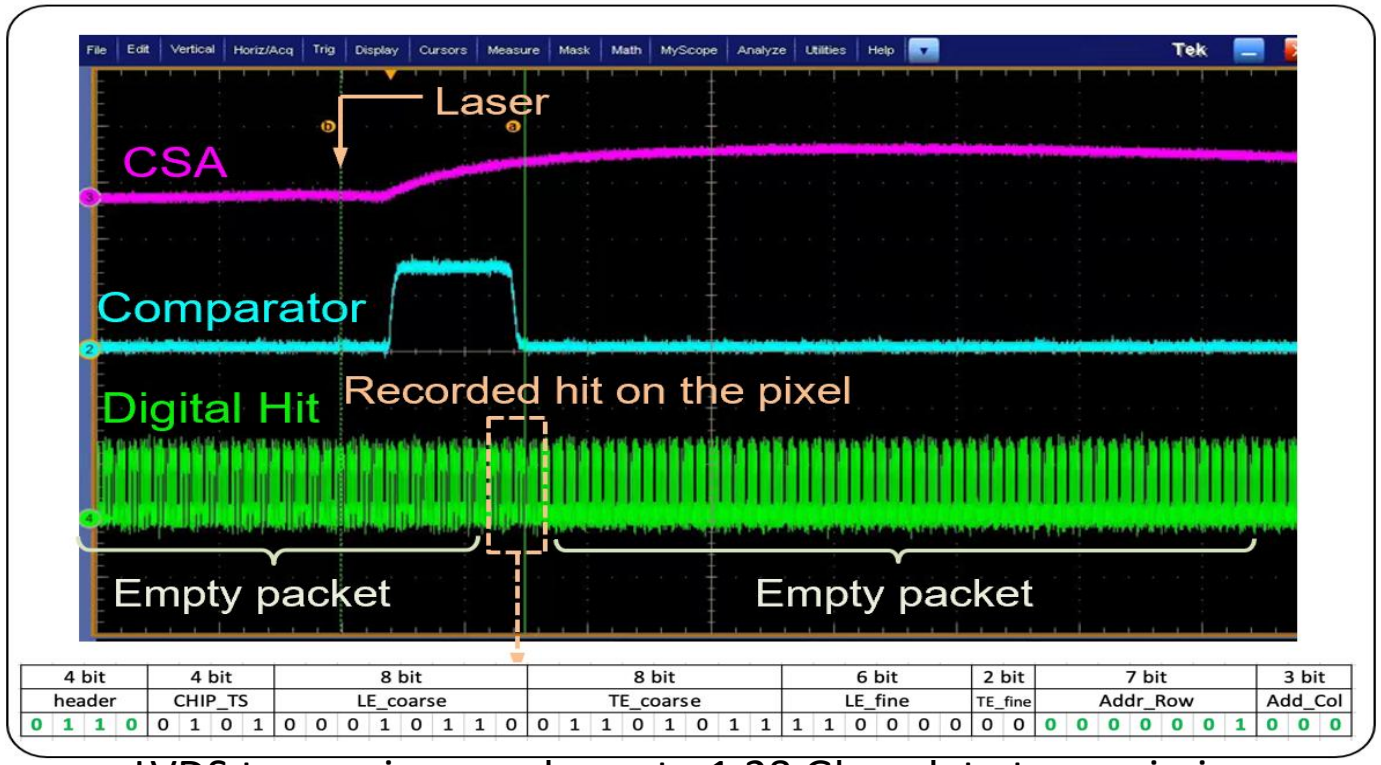
HV-CMOS sensor prototype (COFFEE3)



HV-CMOS sensor specification for ITK	
Sensor size	2 cm × 2 cm
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Timing resolution	3-5 ns
Power	200 mW/cm^2

R&D Progress on HV-CMOS Pixel Sensor



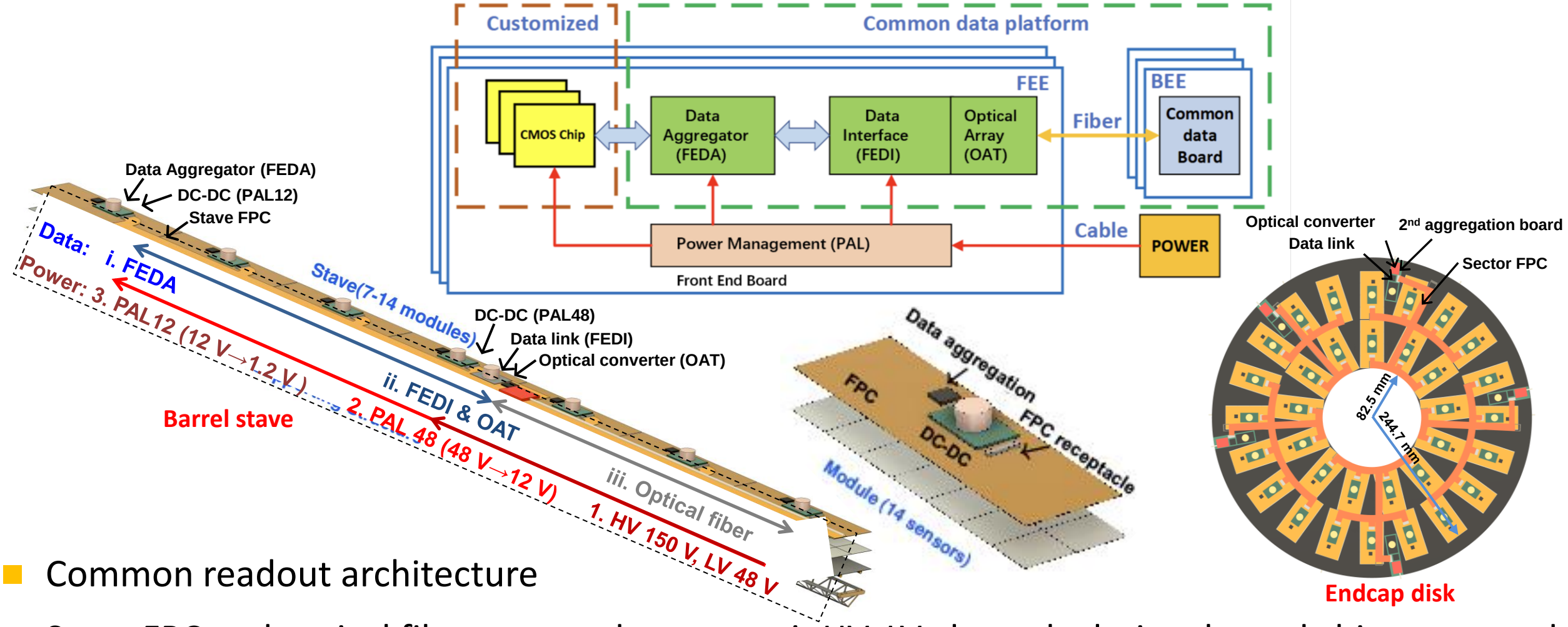


4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 0 1	0 0 0

LVDS transceiver works up to 1.28 Gbps data transmission

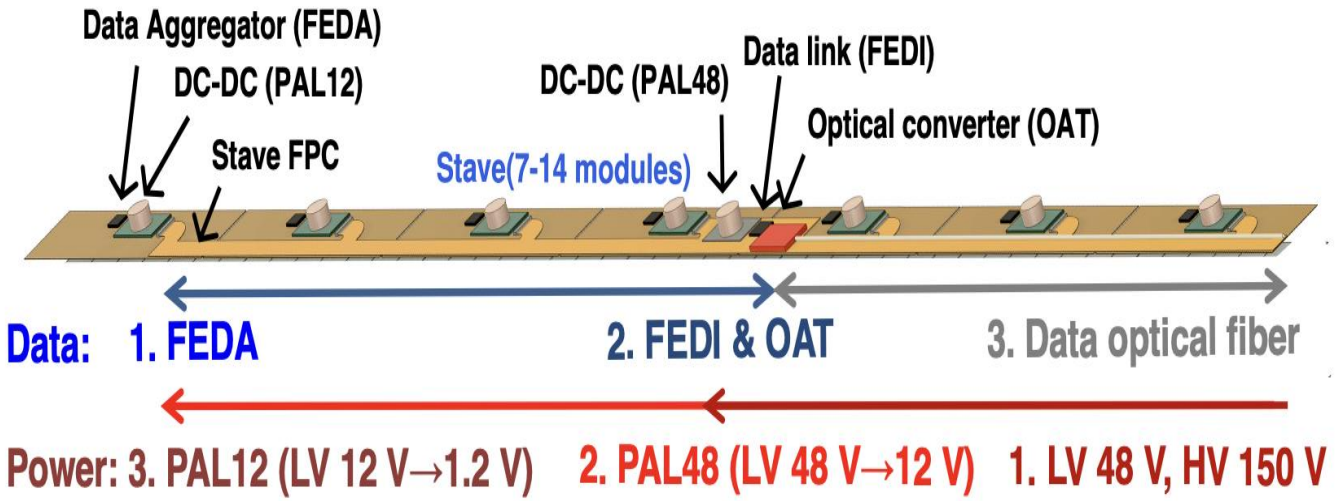
- The latest COFFEE3 sensor was submitted for tape-out and received in May 2025, is currently undergoing testing.
- Several aspects have already been validated,including preamp, comparator, and serializer and the remaining tests are currently in progress. [more details in Yang Zhou's talk]

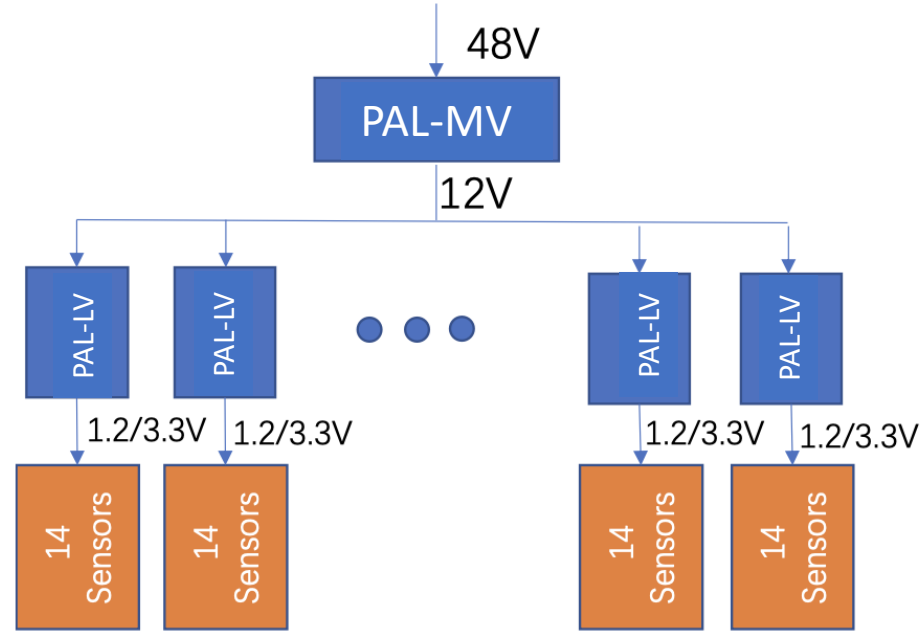
Design Including Power and Readout Electronics



- Common readout architecture
- Stave FPC and optical fiber are used to transmit HV, LV, data, clock signals, and chip commands.
- The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

Power Management for ITK

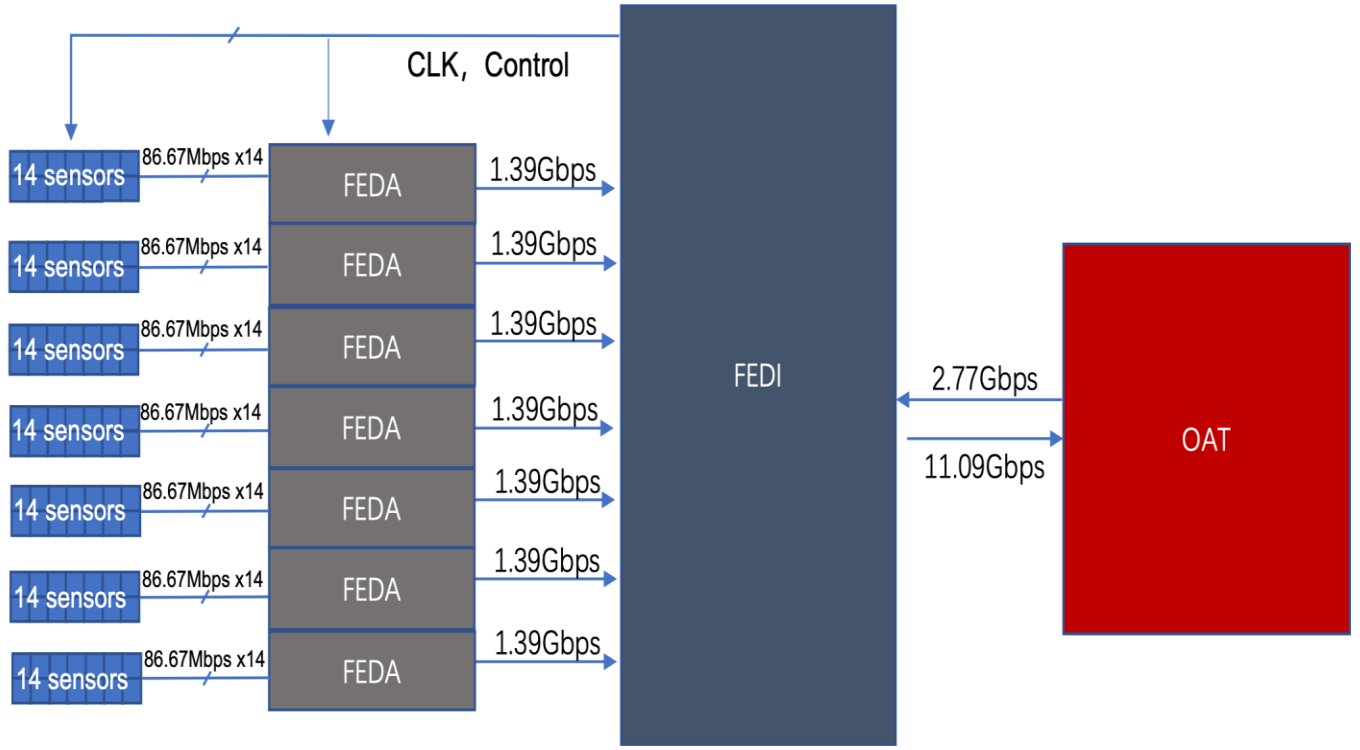




- The HV is delivered directly to individual modules for sensor biasing. HV switch is considered in case of HV short of individual module.
- The power is delivered by Flex PCB from the both sides for barrel.
- 1.2V for front end, FEDI, FEDA, 3.3V for VCSEL driver in optical convertor.
- Both of DC-DCs is supposed to be with output capability ~10A.

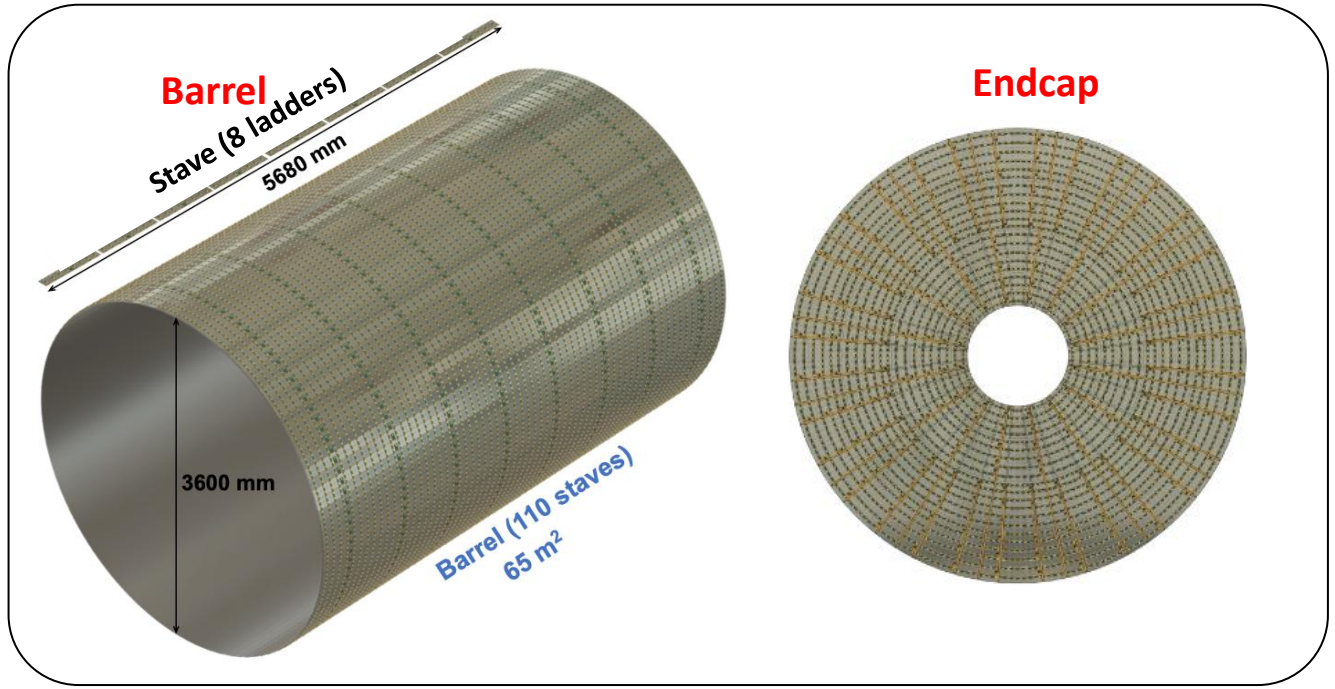
Data Readout Flow for ITK

- Each FEDA concentrates data from 14 sensors, 7 FEDAs to 1 FEDI
- FEDI provides clocks, uplinks from FEDA, downlinks to FEDA and Sensor such as configuration, reset and synchronization.
- Data frame from sensor includes TOA，TOT， adress， bunch ID, polarity.



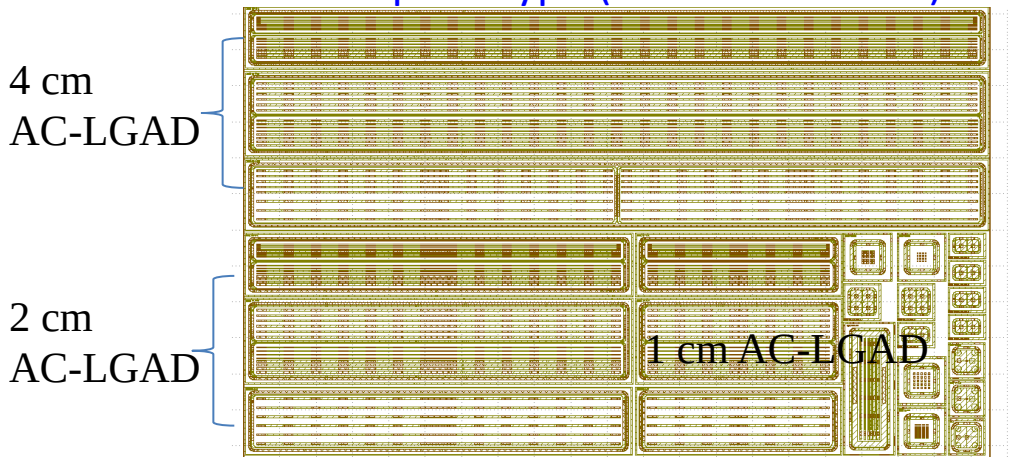
- In the readout design, each sensor can tolerate up to 86.67 Mbps

OTK Design Based on LGAD Strip Sensor



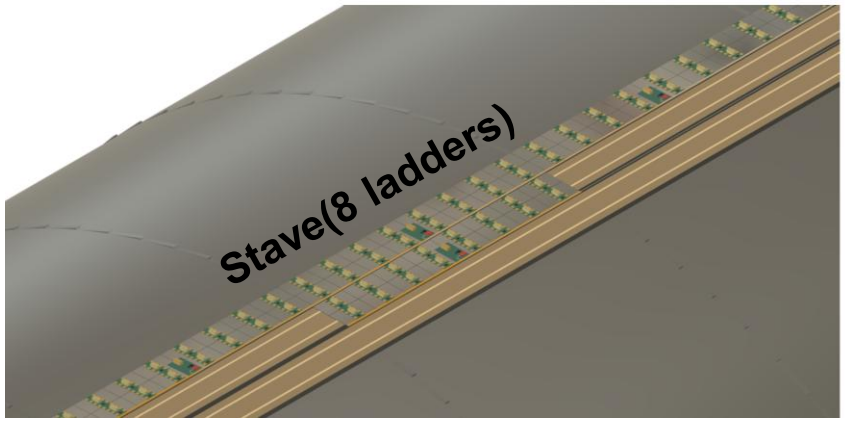
LGAD sensor specification for OTK	
Sensor size	(3-4.5) cm × (3-5) cm
Strip pitch	~100 μm
Spatial resolution	10 μm
Timing resolution	50 ps
Power	300 mW/cm²

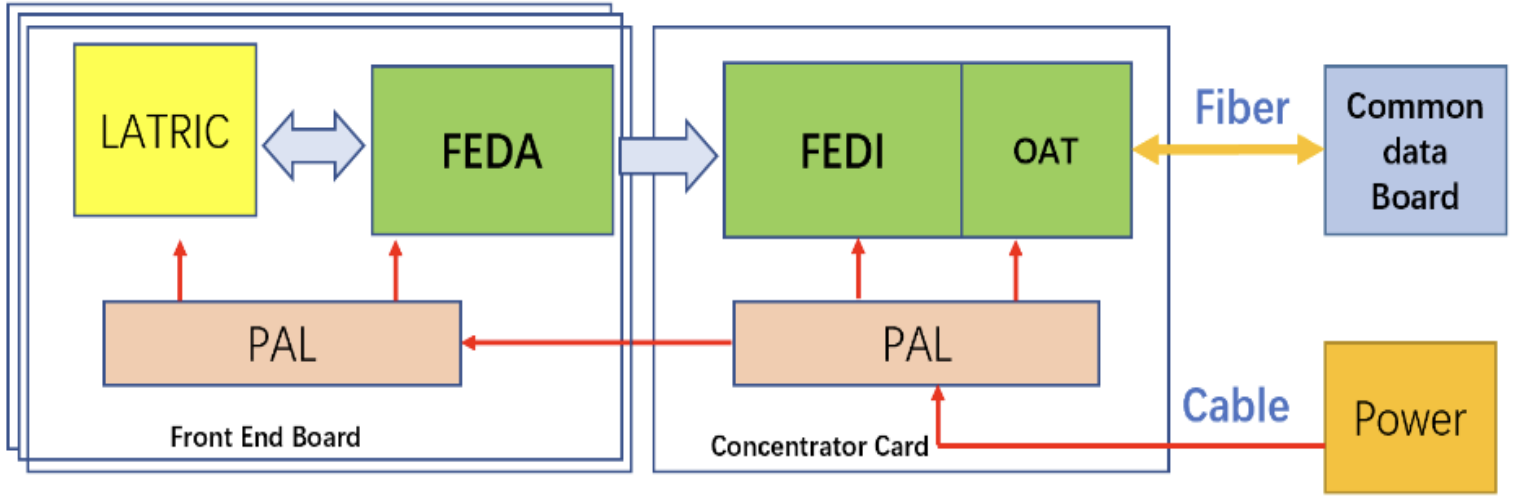
AC-LGAD prototype (latest submitted)



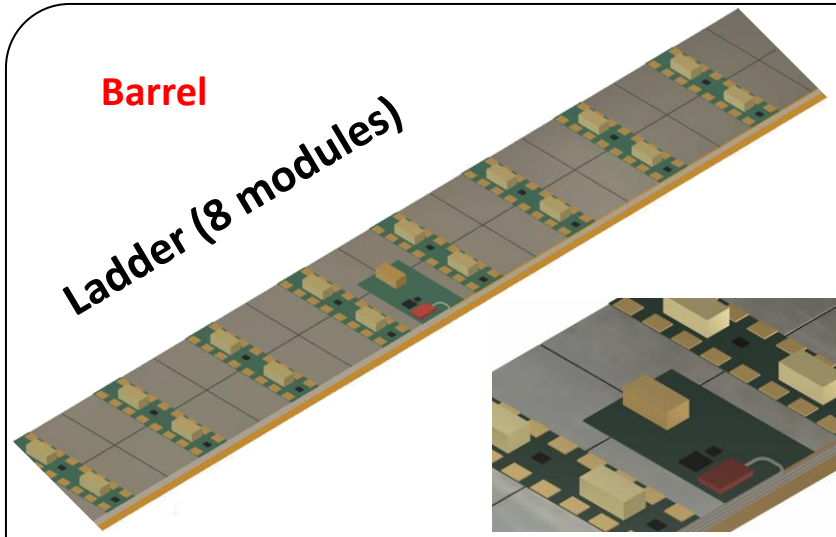
- One barrel layer and one endcap layer (~85 m²).
- The latest LGAD sensor with different length and pitch was submitted for tape-out in March and waiting for the return.

OTK Readout Electronics



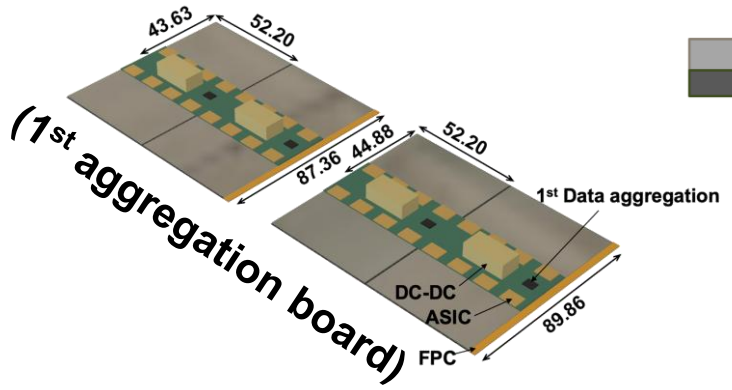


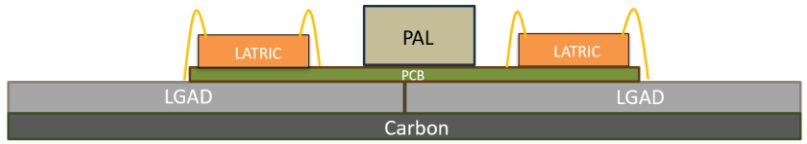
Barrel



(2nd aggregation board)

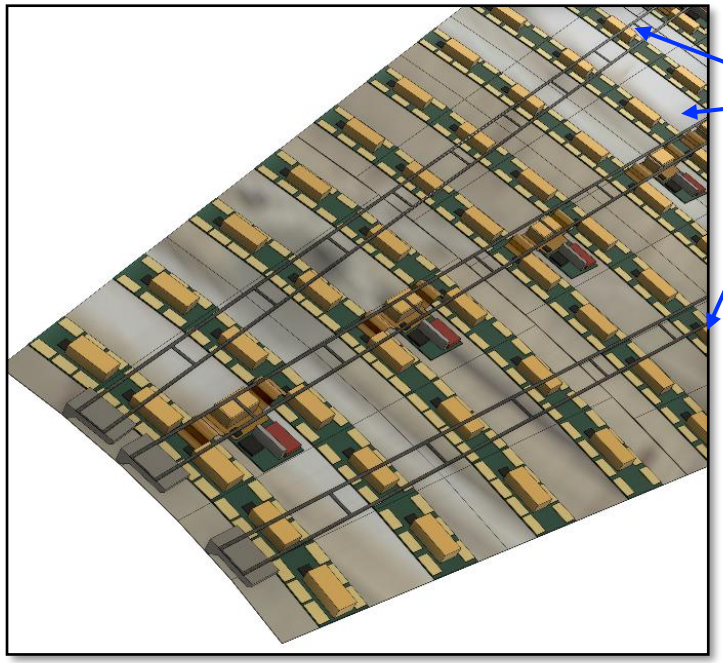
Module (4 sensors)





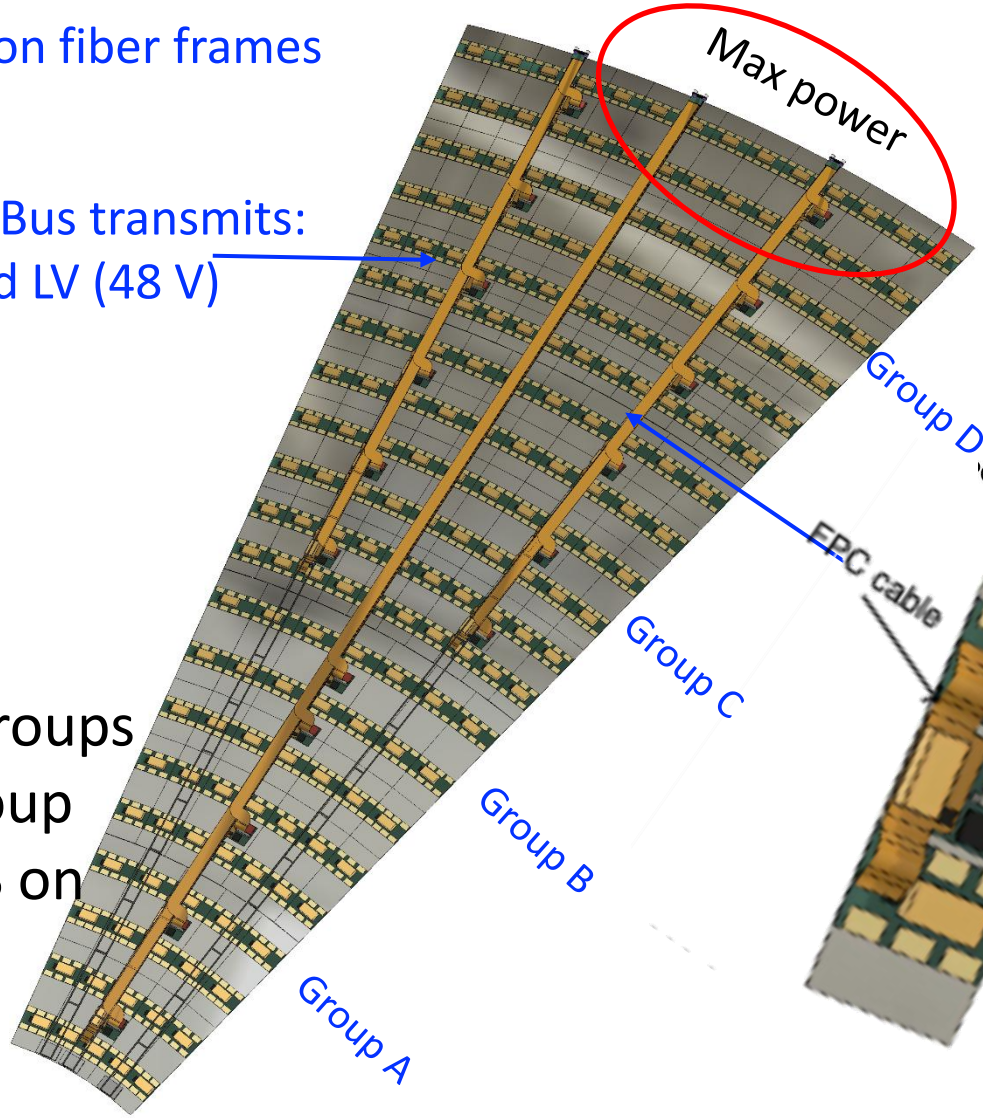
- Similar layout to ITK
- The readout ASIC is wire bonded to LGAD and PCB

OTK Readout Endcap layout

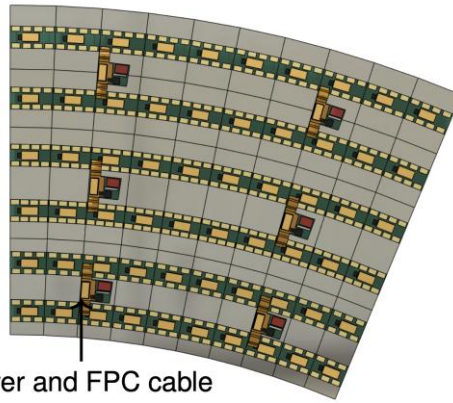


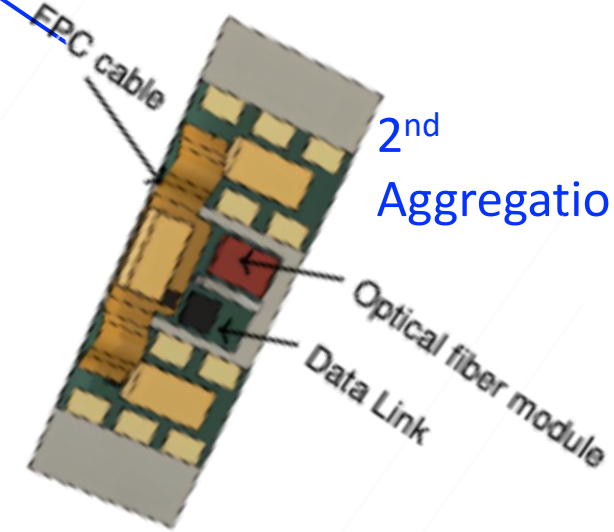
Carbon fiber frames

Power Bus transmits:
HV and LV (48 V)



Group C section

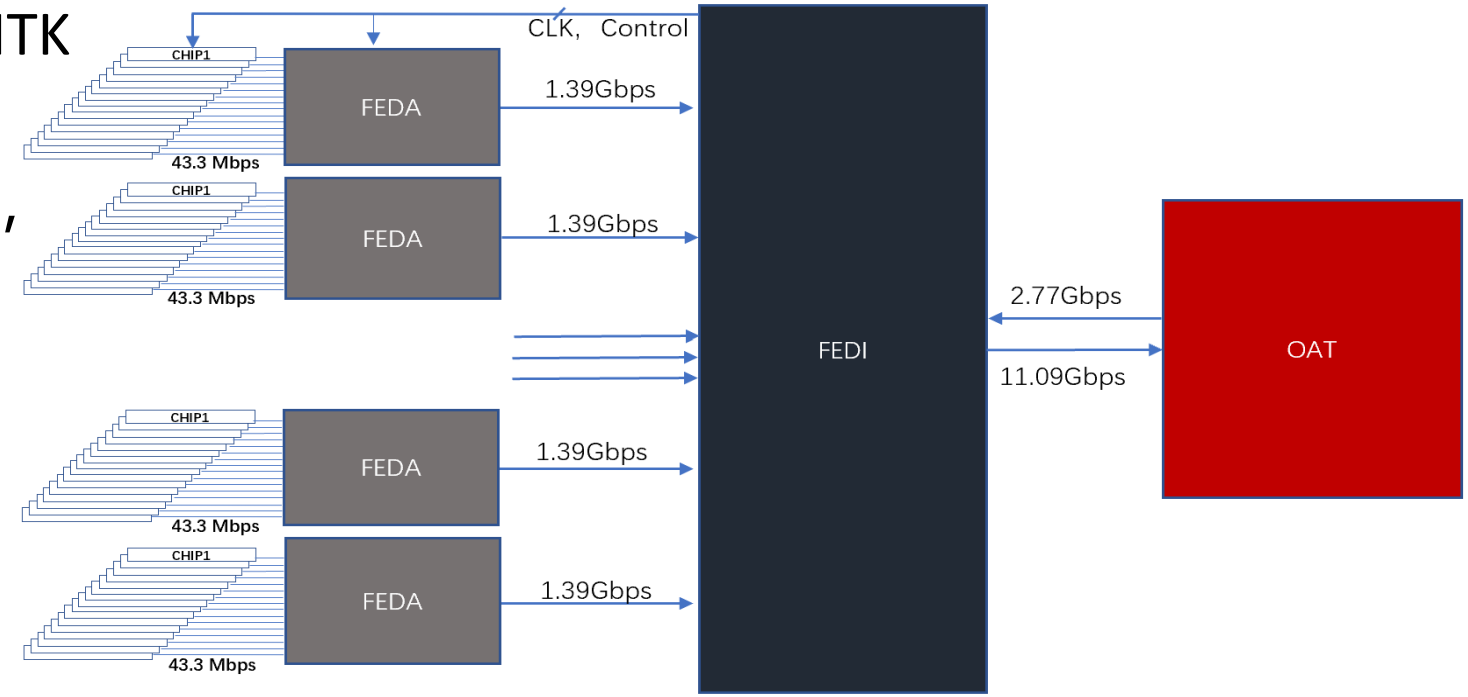




- The endcap section is comprised of 4 groups
- Different concentration for different group
- The power is provided through Flex PCB on the carbon fiber frames

Power and Data readout flow for OTK

- The power management is similar to ITK
- Data frame from sensor includes TOA, TOT, adress, bunch ID, polarity.
- Each FEDA concentrates data from 16 FEs.
- 43.3Mbps per LATRIC for barrel and 86.7 Mbps per LATRIC for endcap



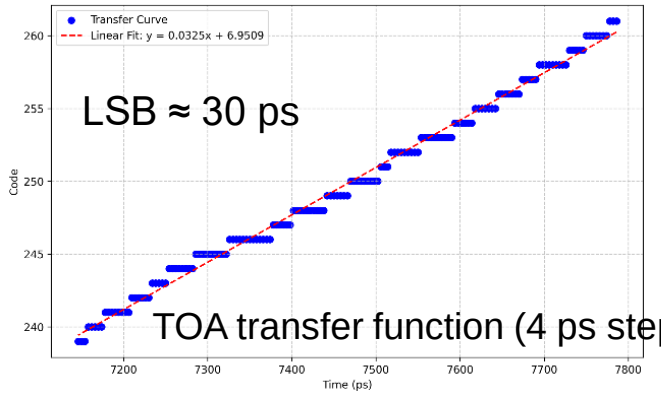
- The low noise PLL in FEDI ensures the precise clock distribution to the front-end system.
- Low-frequency clock jitter and potential phase instability, particularly caused by temperature variations, will require special attention.

R&D Progress on LGAD ASIC

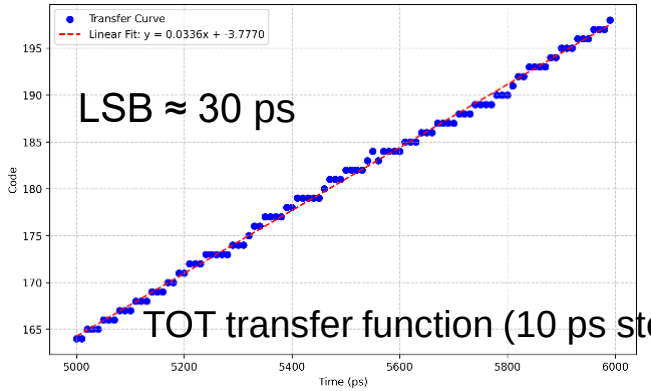
[more details in Chuanye's talk]

The first LATRIC prototype, LATRIC0, submitted for tape-out in April, was wire bonded and delivered to IHEP in Aug

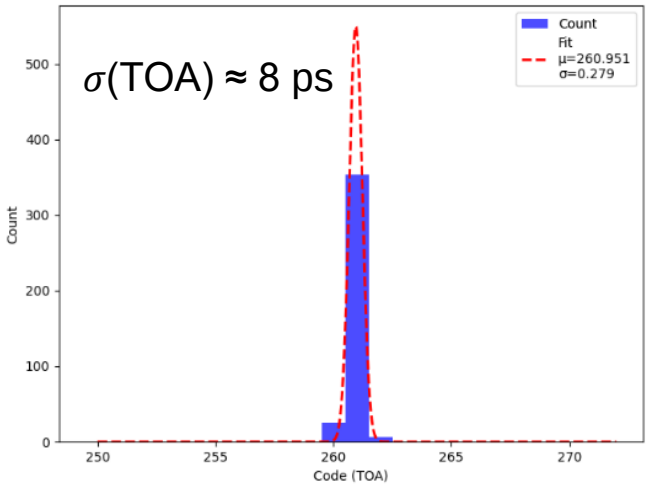
- The ASIC integrates a pre-amplifer, a discriminator, a TDC, and a serializer for data output.
- Tests find that the LSB is 29.8 ps, meeting the 30 ps design goal. The measured TDC power consumption is 0.1 mA (1.2 V) @ 0.5 MTPS (Mega-Trigger Per Second), 0.3 mA @ 1 MTPS, and 0.5 mA @ 2 MTPS, agreeing with the design.
- More in-depth tests are on-going..

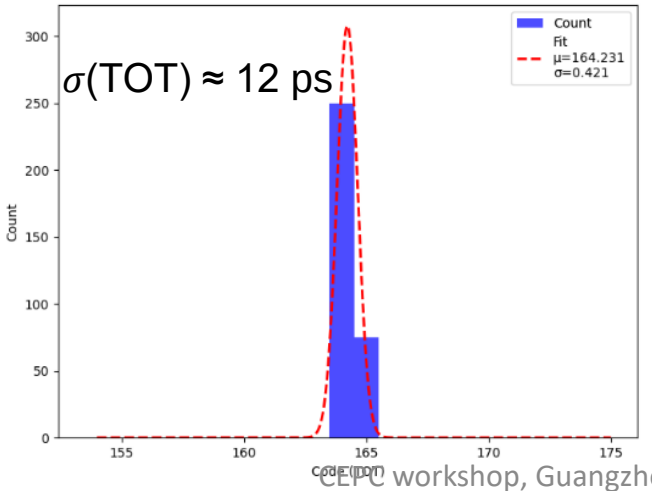


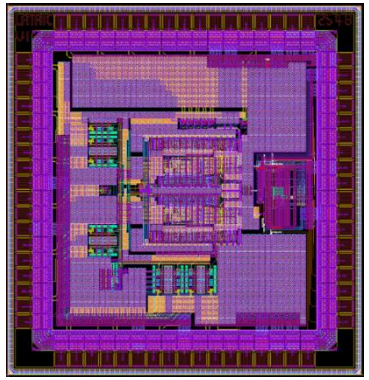
TOA transfer function (4 ps step)



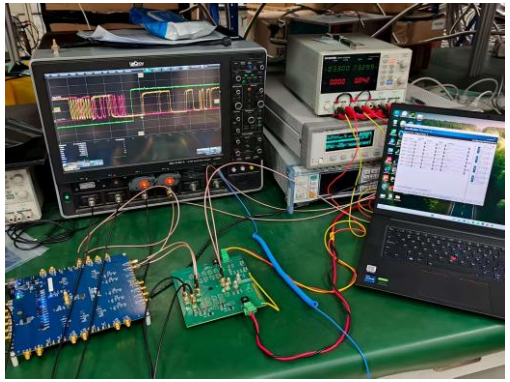
TOT transfer function (10 ps step)

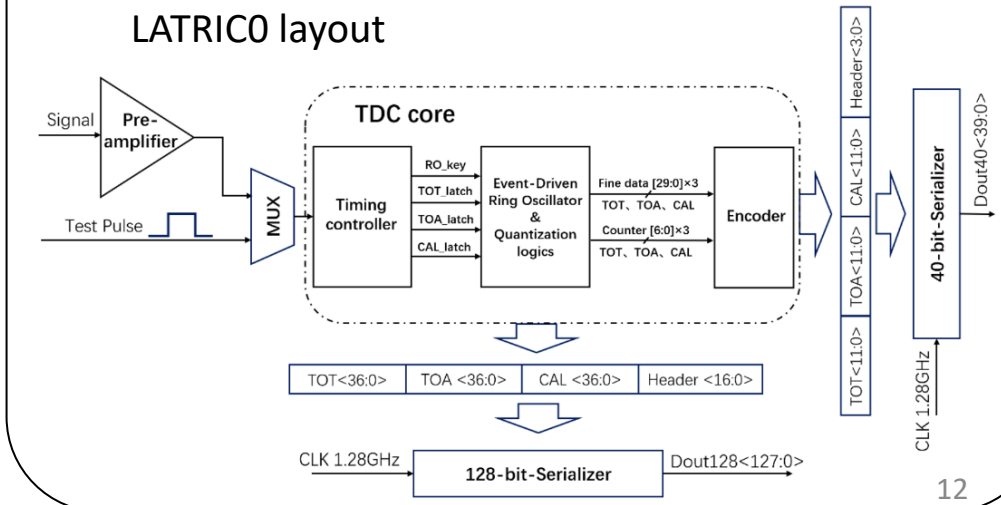






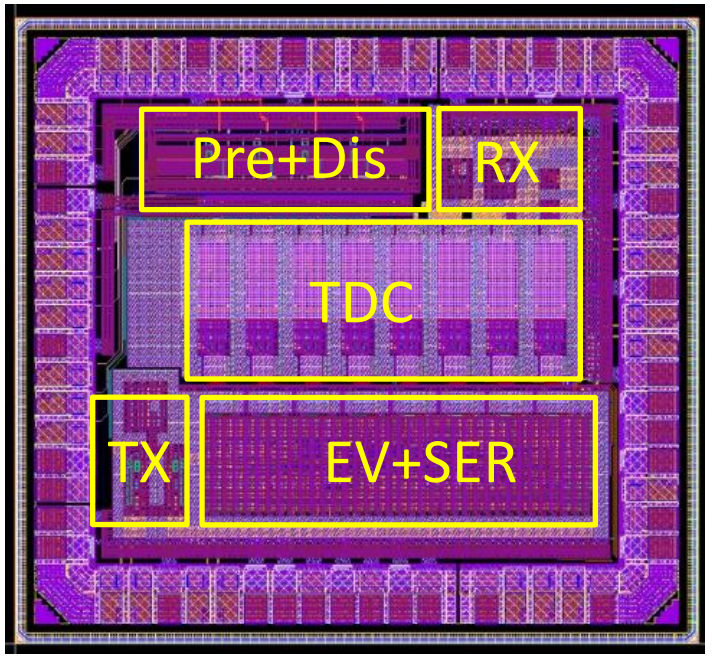
LATRIC0 layout





LATRIC1 Progress

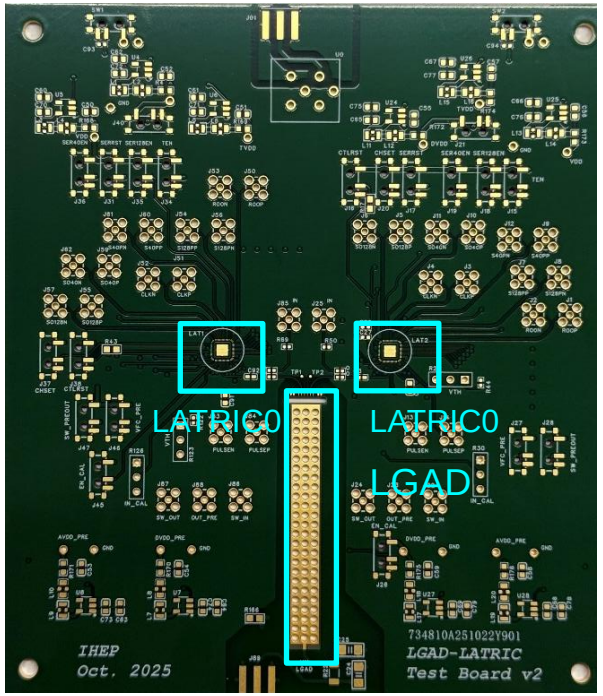
- Submitted for tape-out in October
  - 8 channels TDC
  - 4 channels with front end
  - Increase the gain of preamp
  - Improve the encoder logic
  - Add event builder and scramble logic
  - 100 um channel pitch match the LGAD
- Test PCB design is ongoing

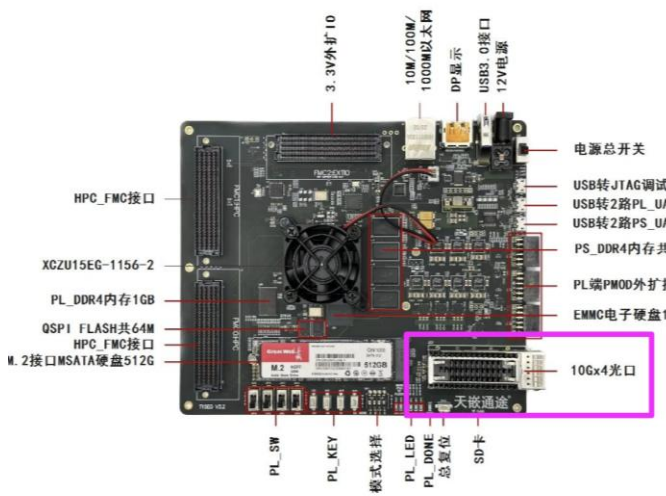


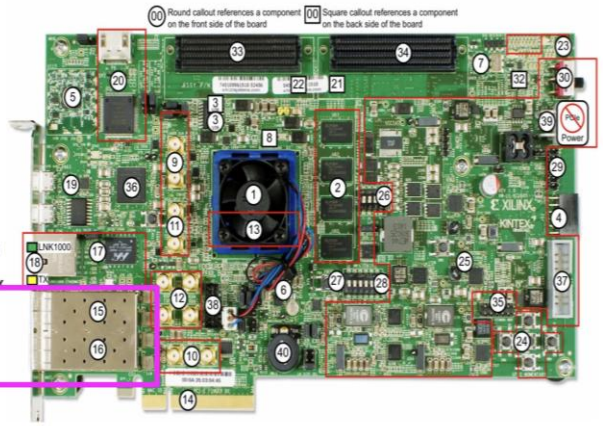
LATRIC1 layout

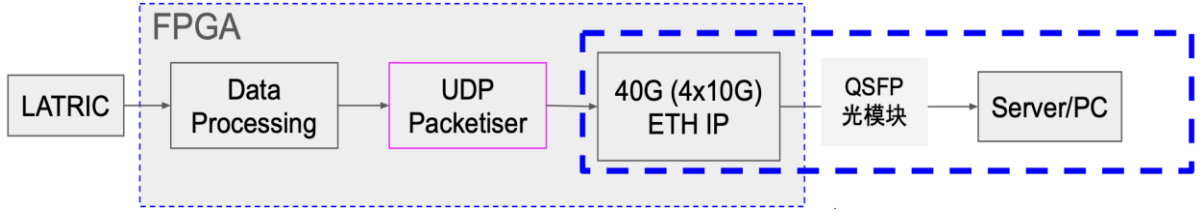
LATRIC test with LGAD

- 2 LATRIC0s on PCB are connected to LGAD.
- The PCB already came back and waiting for soldering and bonding.
- DAQ debug is ongoing.
- Laser for measurement is ready.



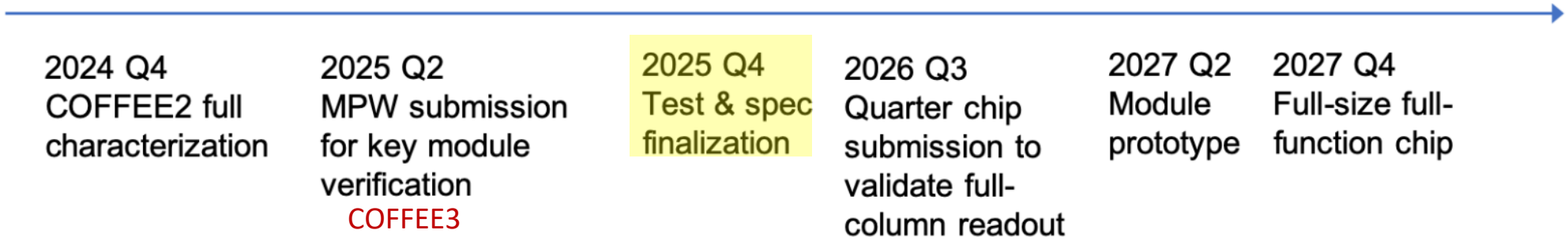




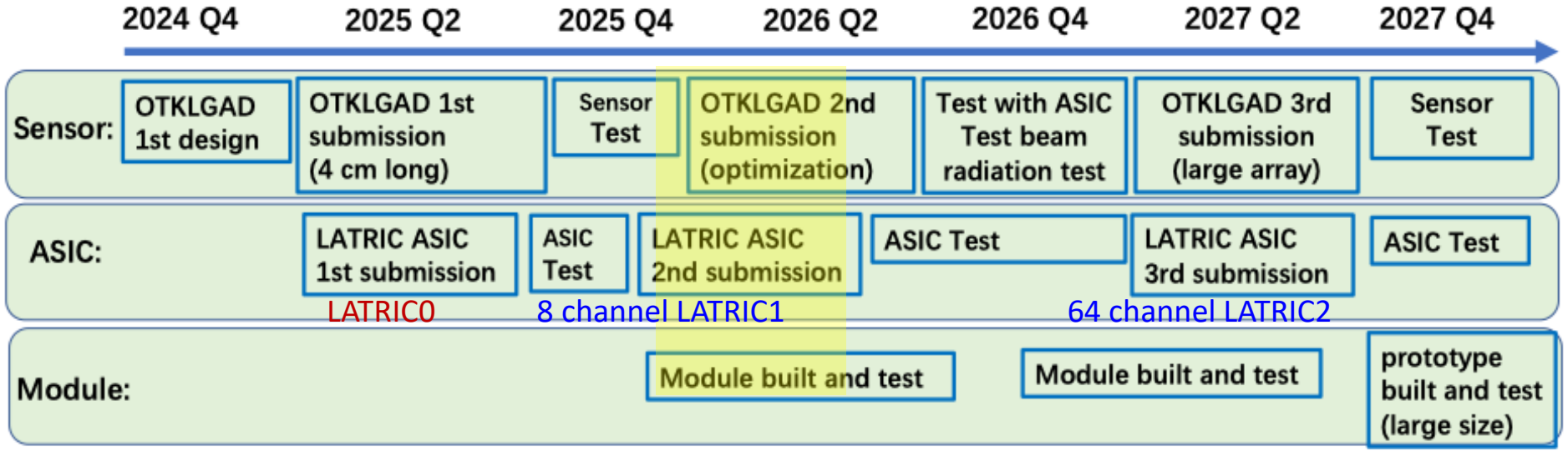


R&D Plan Following the Ref-TDR

- HV-CMOS pixels:



- AC-LGAD strips+ASIC:



Summary

- The design of readout electronics scheme for the Silicon Tracker and the latest R&D progress have been presented.
- Next focus will be on R&D, aiming front end ASIC (multiple channels integtation for LATRIC), sensor (seek process optimization for LGAD and COFFEE) and readout electronics prototype development.
- A multi-channel design with full component integration, is carefully planned to verify the sensor bonding and realistic performance characterization.

Our Research Team

- Currently active: 29 institutes, 50 staff, and 50+ postdocs & students

We welcome collaboration with partners worldwide.

Thank you for your attention!

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BACKUP

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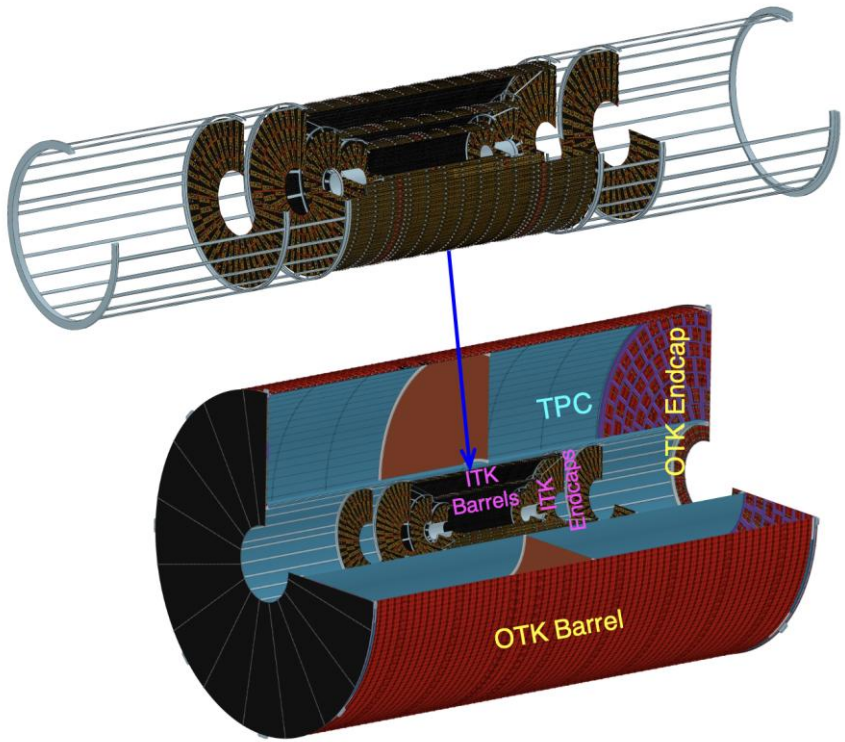

Figure 5.1: Layout of the Silicon Tracker (ITK and OTK). The ITK consists of three barrel layers and four endcap layers, together with two extended connection rings, forming the complete ITK assembly that is inserted into the inner barrel of the TPC. The OTK, as the outermost component of the tracker system, includes one barrel layer and one endcap layer, mounted outside of the TPC. It provides both high-precision spatial and timing measurements.

Table 5.1: Parameters and layout of the Silicon Tracker. The column labelled $\pm z$ shows the half-length of the barrel layers, and the z position of the end-cap disks. The column labelled σ_ϕ and σ_t represent the spatial resolution in the bending direction and time resolution, respectively.

Detector		Radius R [mm]		$\pm z$ [mm]	Material budget [% X_0]	σ_ϕ [μm]	σ_t [ns]
ITK Barrel	Layer 1 (ITKB1)	235.0		493.3	0.68	8	3-5
	Layer 2 (ITKB2)	345.0		704.8	0.68	8	3-5
	Layer 3 (ITKB3)	555.6		986.6	0.68	8	3-5
OTK Barrel	Layer 4 (OTKB)	1,800		2,840	1.6	10	0.05
		R_{in}	R_{out}				
	Disk 1 (ITKE1)	82.5	244.7	505.0	0.76	8	3-5
	Disk 2 (ITKE2)	110.5	353.7	718.5	0.76	8	3-5
ITK Endcap	Disk 3 (ITKE3)	160.5	564.0	1,000	0.76	8	3-5
	Disk 4 (ITKE4)	220.3	564.0	1,489	0.76	8	3-5
OTK Endcap	Disk 5 (OTKE)	406.0	1,816	2,910	1.4	10	0.05

Table 5.2: Estimated average and maximum hit rates of the Silicon Tracker [10^3 Hz/cm^2] for all layers across three operation modes.

$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	**Low Lumi Z** 26		**Higgs** 8.3		**High Lumi Z** 192	
	Average	Max	Average	Max	Average	Max
ITKB1	1.04	1.95	0.63	1.01	3.10	5.84
ITKB2	0.98	3.30	0.55	1.33	2.93	9.89
ITKB3	0.76	1.69	0.39	0.77	2.26	5.07
OTKB	0.66	1.11	0.37	0.58	1.96	3.32
ITKE1	3.46	15.78	2.35	11.70	10.37	47.28
ITKE2	3.99	24.50	2.06	9.82	11.95	73.38
ITKE3	2.29	17.26	1.14	7.46	6.86	51.71
ITKE4	2.54	8.55	1.26	3.71	7.59	25.61
OTKE	1.54	6.35	0.94	4.12	4.61	19.01