Muon electronics

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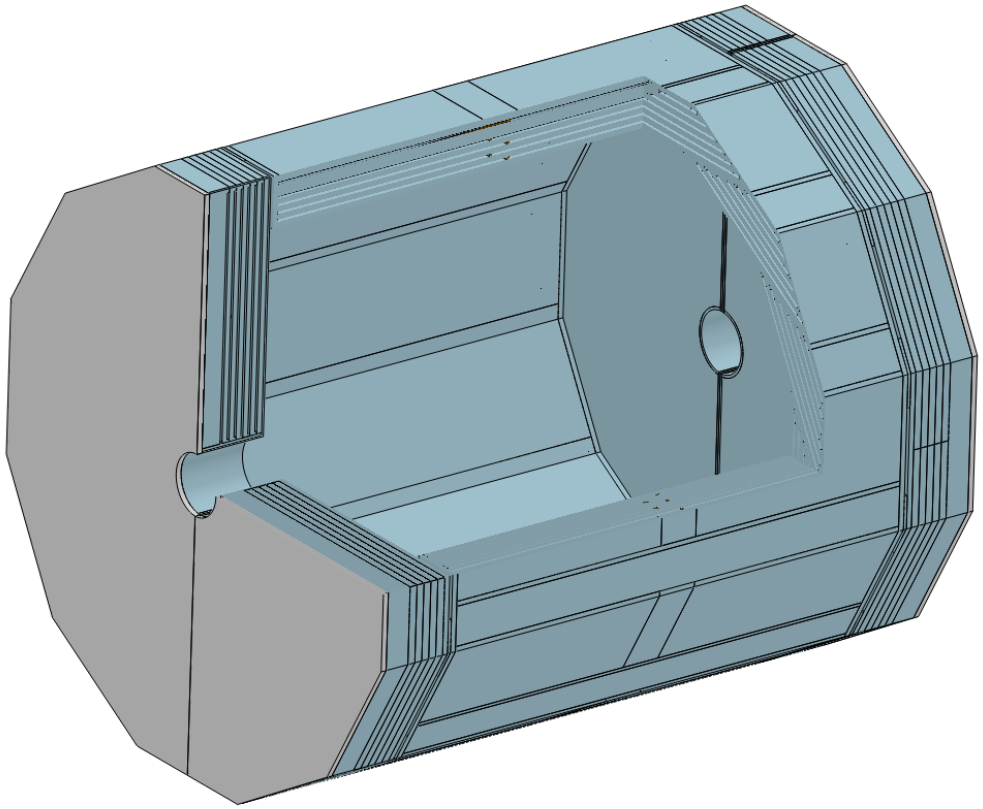
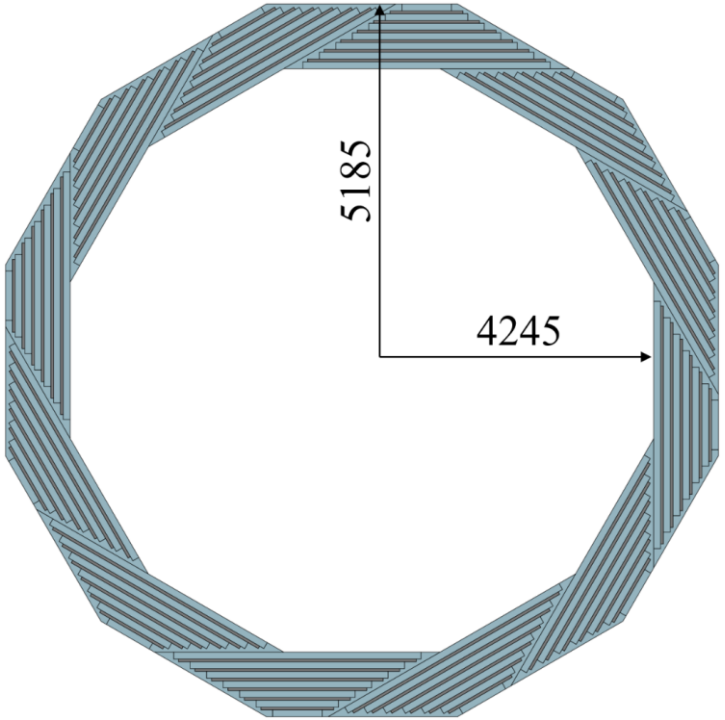
Muon detector

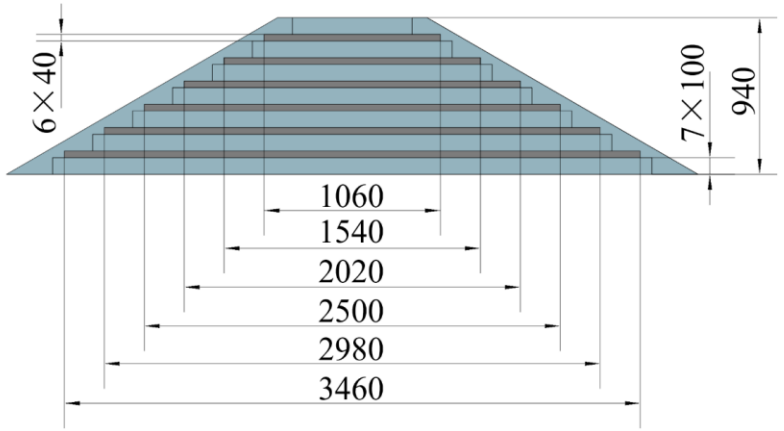
- Technology choice: extruded plastic scintillator, WLS fiber, and SiPM.
- Electronics system: similar to ECAL/HCAL, revise it for small nPE and high time resolution.
- 240 detector modules, 43k detector channels, 119 km sensitive length, $4.8 \times 10^3\ m^2$ detecting area.
- Requirements
  - Solid angle coverage: $> 98\% \times 4\pi$
  - Muon identification efficiency: $> 95\%$
  - Spatial resolution: $\sim 1\ cm$
  - Time resolution: $\sim 1\ ns$
  - Fake $\pi \to \mu$ rate: $< 1\%$
  - Rate capability: $50\ \mathrm{Hz}/cm^2$

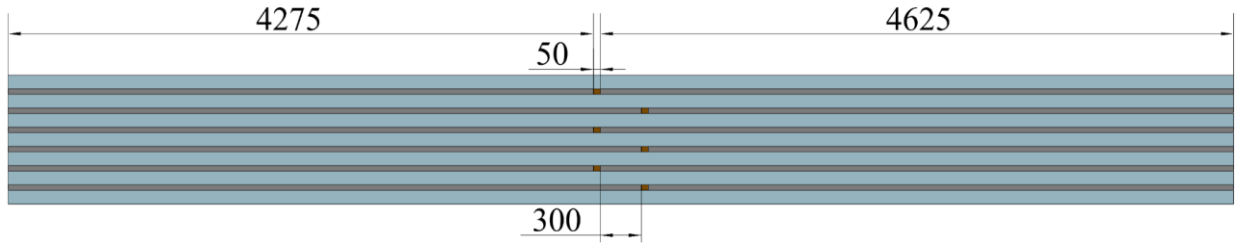


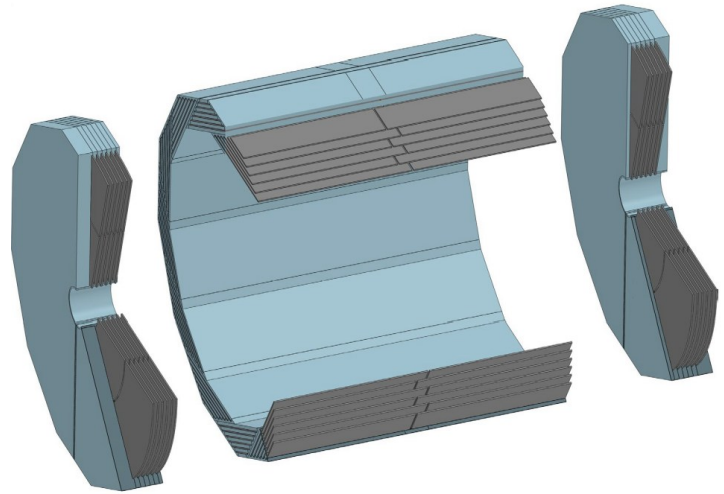
Detailed design: Barrel structure

- Geometry: 6 layers of modules
  - Barrel: Helix dodecagon sectors.
  - Rectangle modules inserted between iron plates.
  - Each layer has two modules with a length of 4.275m or 4.625m.





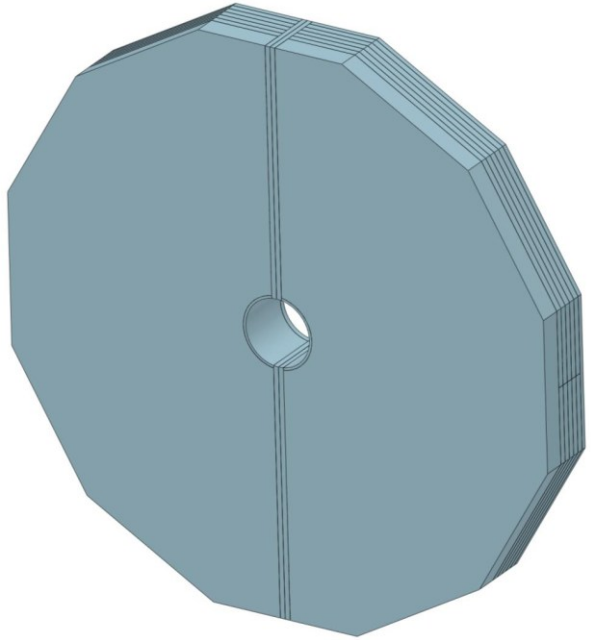




- Barrel
  - 12 sectors
- Endcap
  - 2 endcaps
    - Inner
    - Outer

Detailed design: Endcap structure

- Geometry: 6 layers of modules
  - Endcaps: inner and outer modules
    - Inner module: $R = 0.65 - 2.80m$
    - Outer module: $R = 2.85 - 5.08m$
  - Longest channel: $2.7m$ in inner module, $4.2m$ in outer modules
  - $10cm$ gaps occupy ~0.3% of the solid angle.



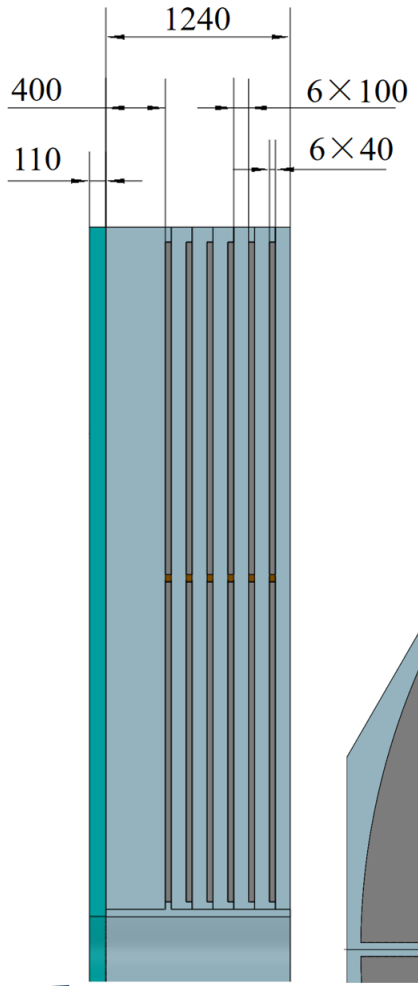
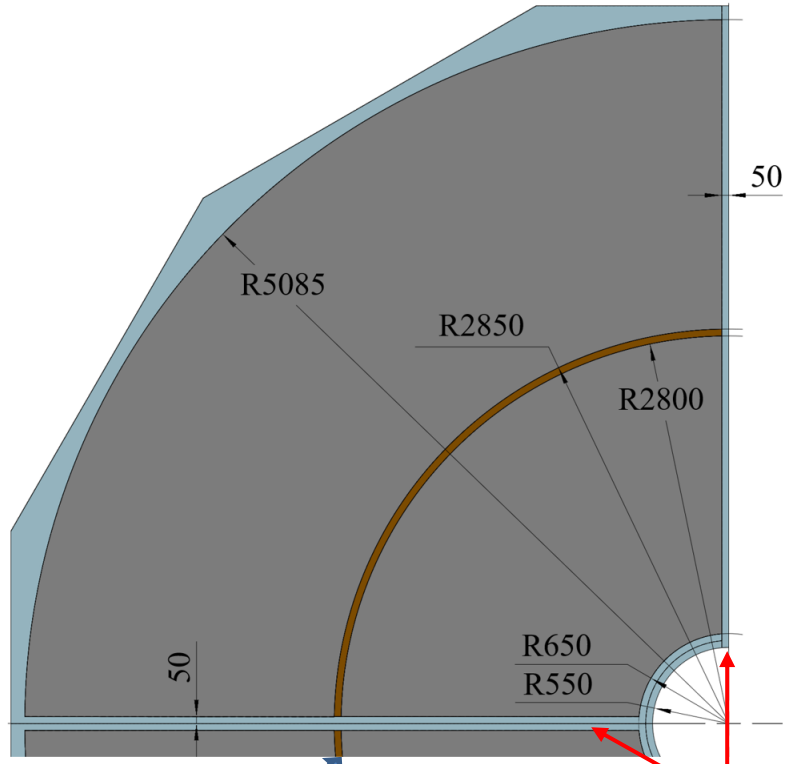


Fig. 9.3

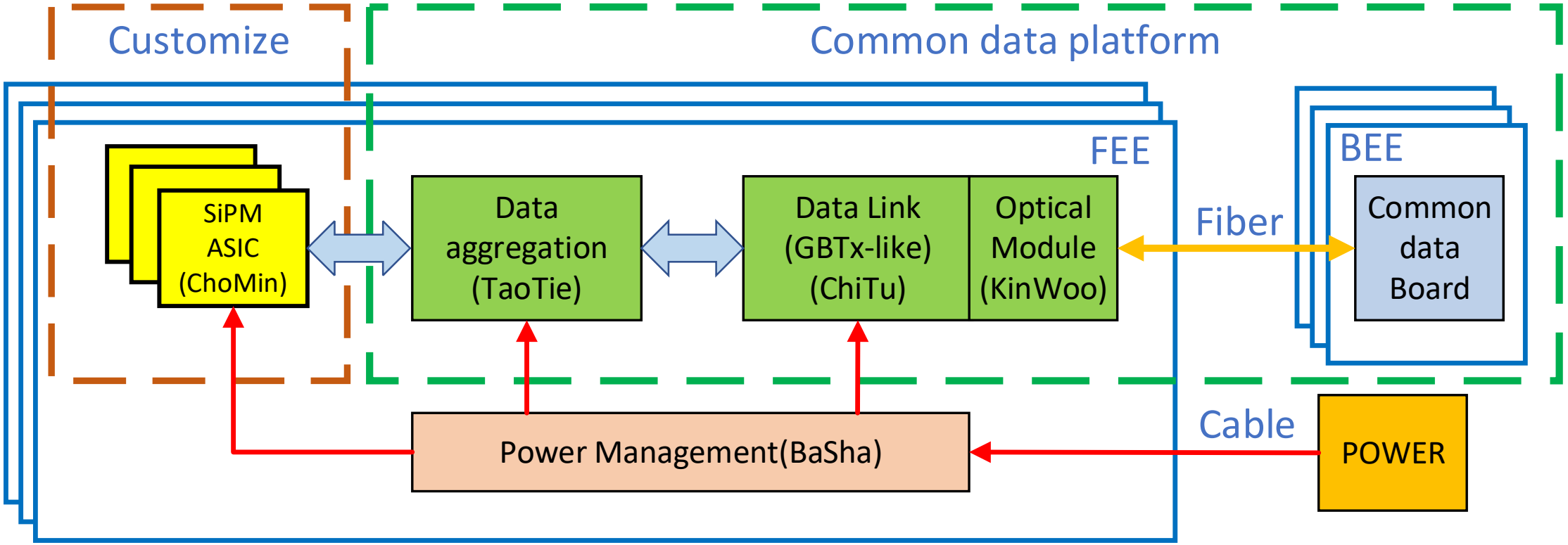


paraffin layer(new)

Stiffener

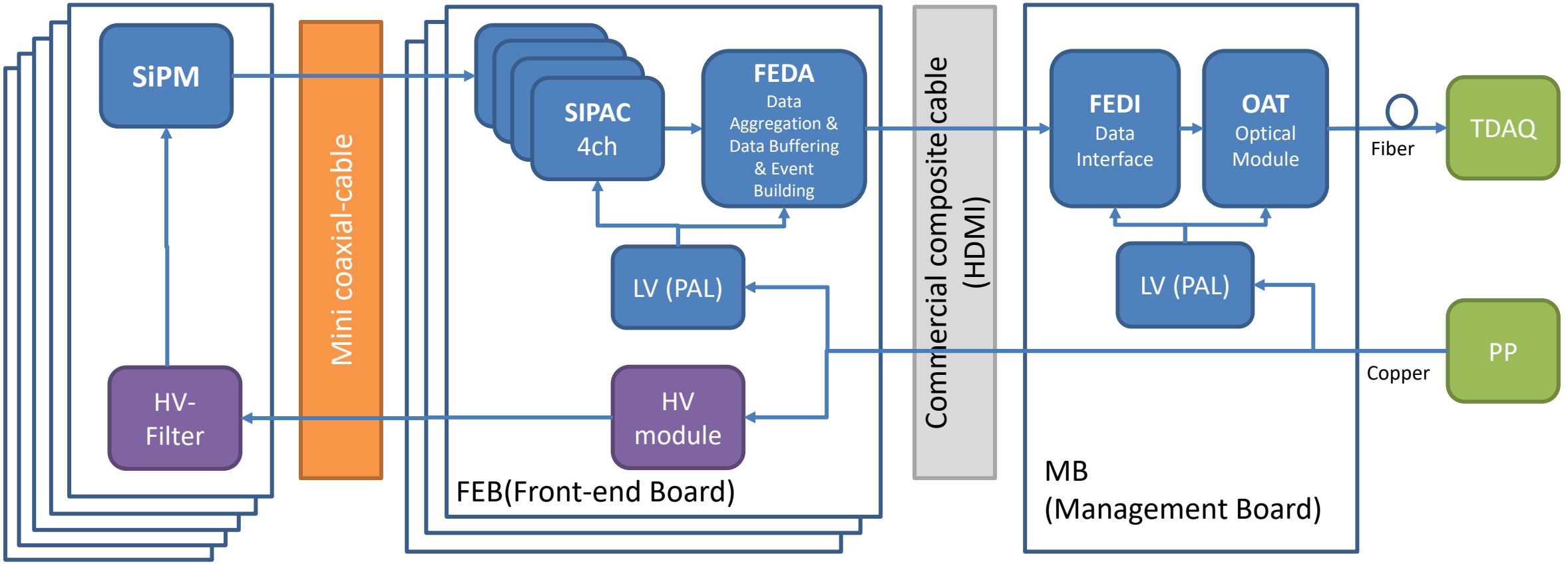
10 cm gap

Baseline for SiPM readout



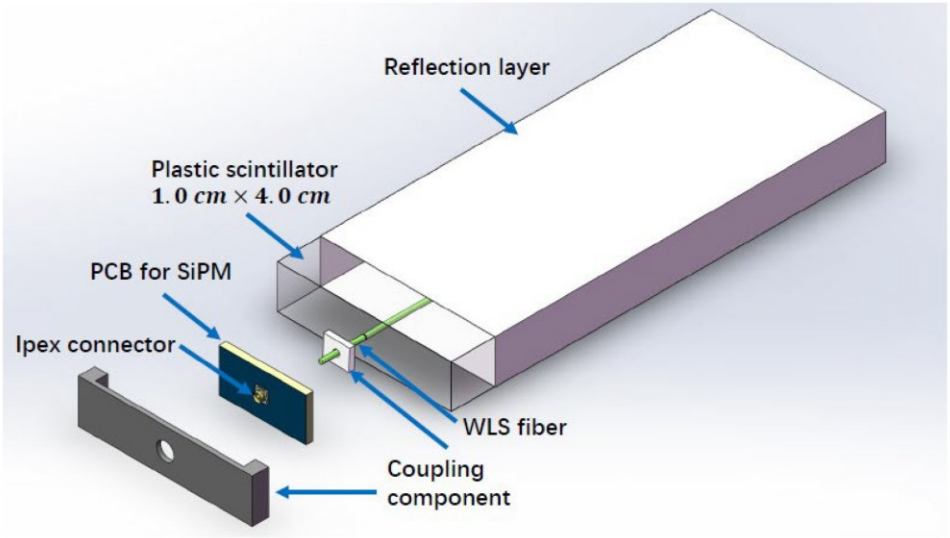
- Full custom-made ASICs
- Reuse the ASIC scheme (ChoMin) from ECAL or HCAL
- Revise according to the constraints from cooling and mechanical structure of the detector

Stage scheme M(SiPM) x N(FEB) x O(MB)

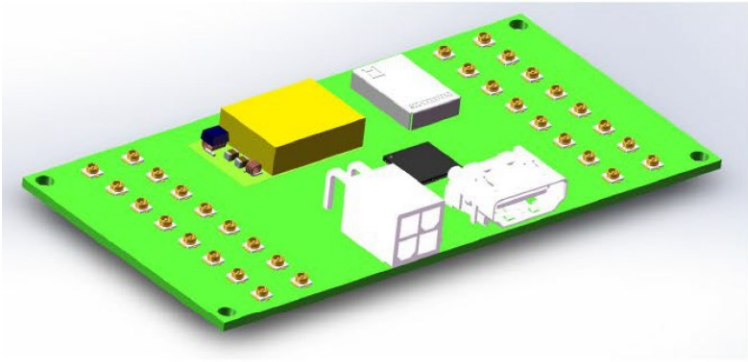


- Structure similar to calorimeters', with requirements: $N_{pe} < 200, \sigma_T < 0.5ns$
- Three stages for readout
  - SiPM tile: SiPM on PCB
  - FEB: Front-End Electronics Board, each having 32 chs, mini HV generator integrated.
  - MB: Management Board, Central node for multiple functions.

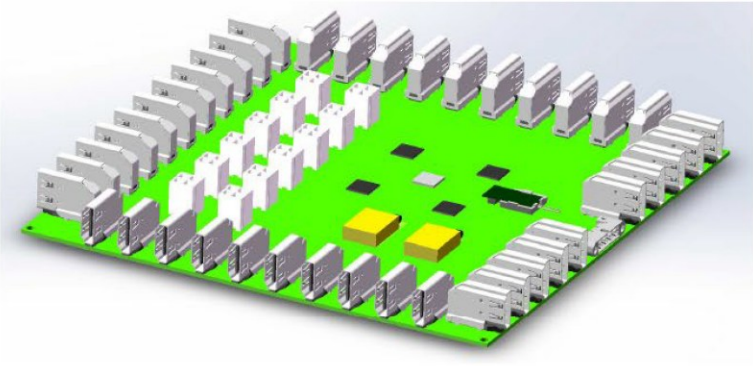
Stage scheme M(SiPM) x N(FEB) x O(MB)



(a) PSU: Plastic Scintillator Unit



(b) FEB



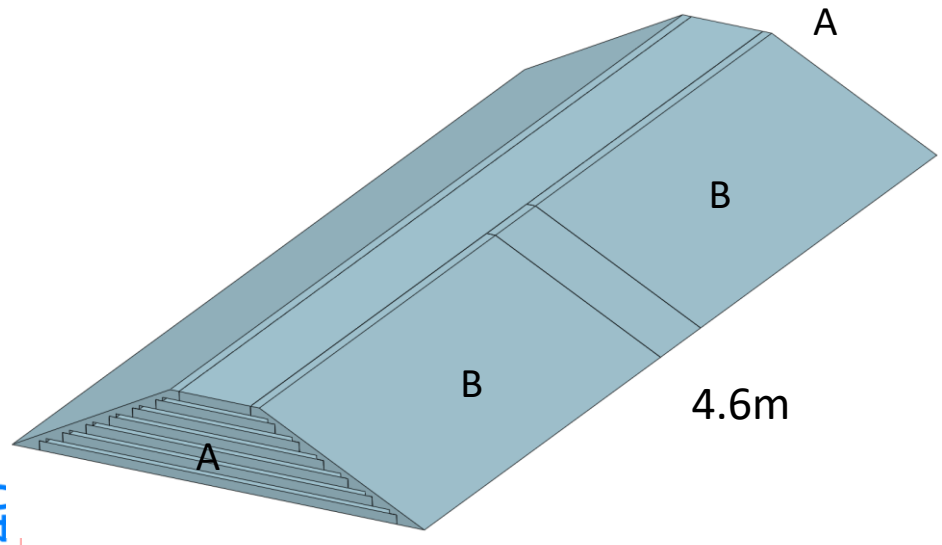
(c) MB

Ipex cable: Micro coaxial cable

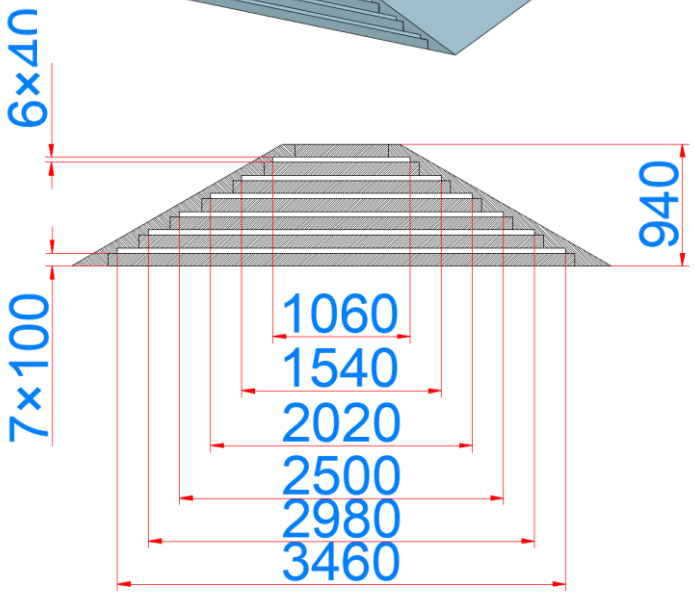
HDMI cable:
Commercial multi-core shielded cable

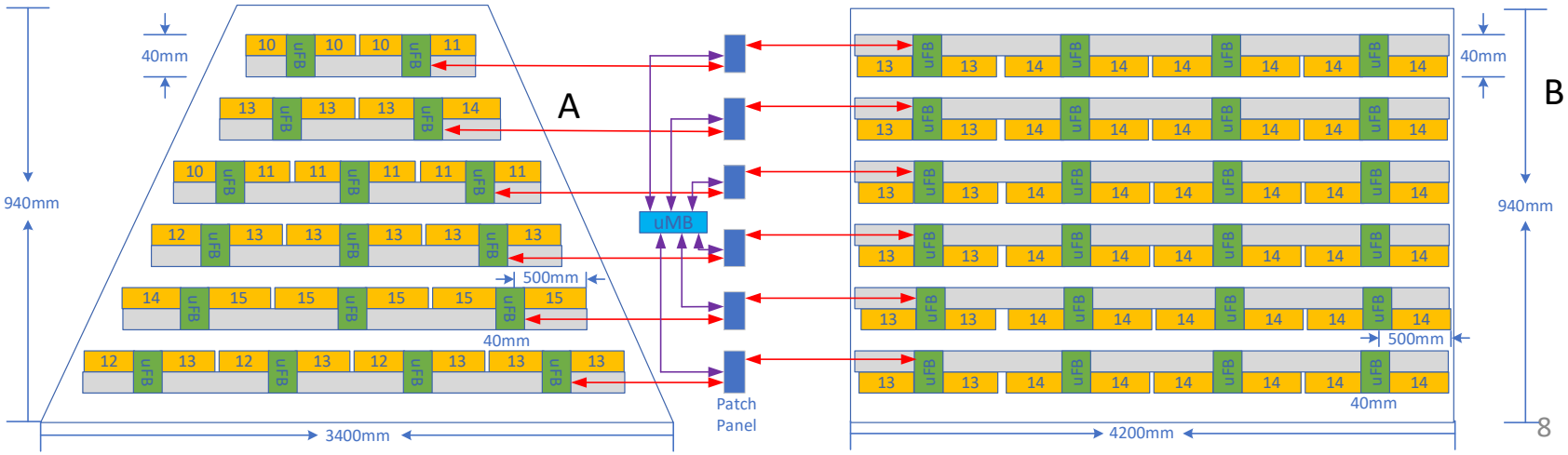
- Structure similar to calorimeters', with requirements: $N_{pe} < 200, \sigma_T < 0.5ns$
- Three stages for readout
  - SiPM tile: SiPM on PCB
  - FEB: Front-End Electronics Board, each having 32 chs, mini HV generator integrated.
  - MB: Management Board, Central node for multiple functions.

Barrel sector



	M (SiPM)	N (FEB)		O (MB)
	ch	32-ch TDC board	Raw data rate / bps	Management board
A	426	17	161.28 M	1
B	660	24	318.24 M	
Total per sector	2172	82	959.04 M	2
Total barrel (12 sectors)	26064	894	11.51 G	24

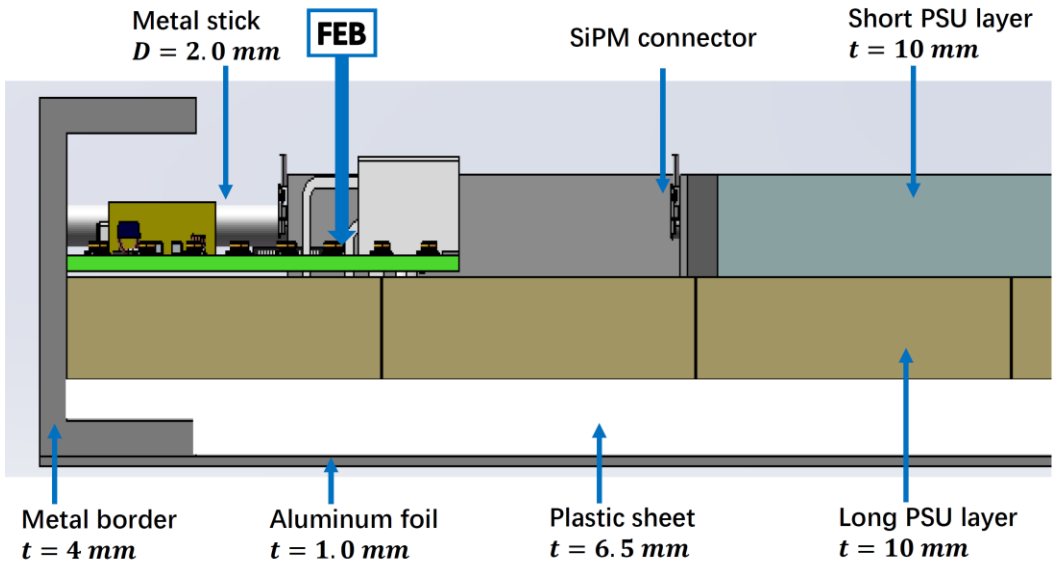




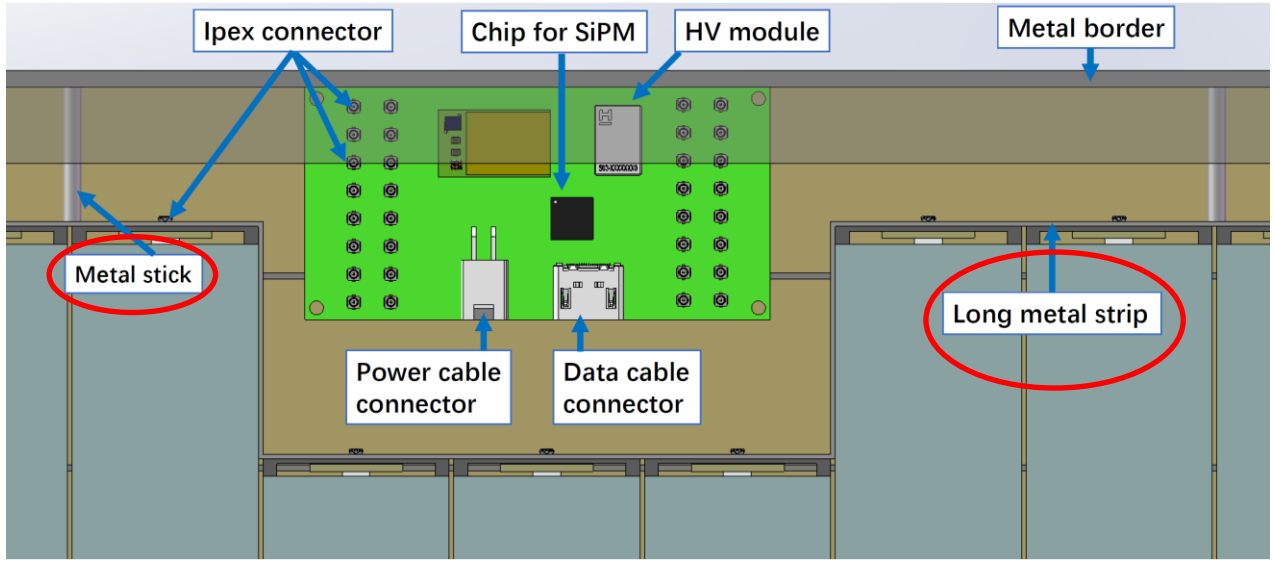
Details near FEB

- Structure layers of a module: aluminum foil × 2, plastic sheet × 2, PSU layer × 2, etc.
- FEB: $5\ cm \times 10\ cm$ and thickness less than $1.5\ cm$.
- Space for FEB and cables.
- New design: additional long metal strip to hold the top PSU layer, using metal sticks to keep the space.

New

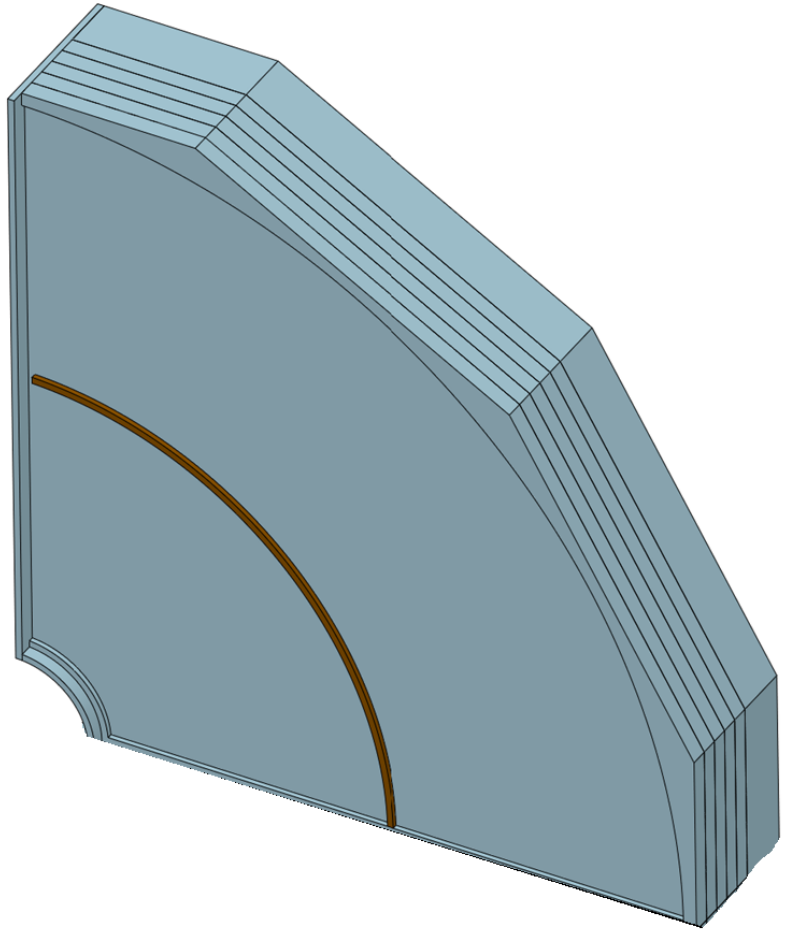


New



t: thickness; D: diameter

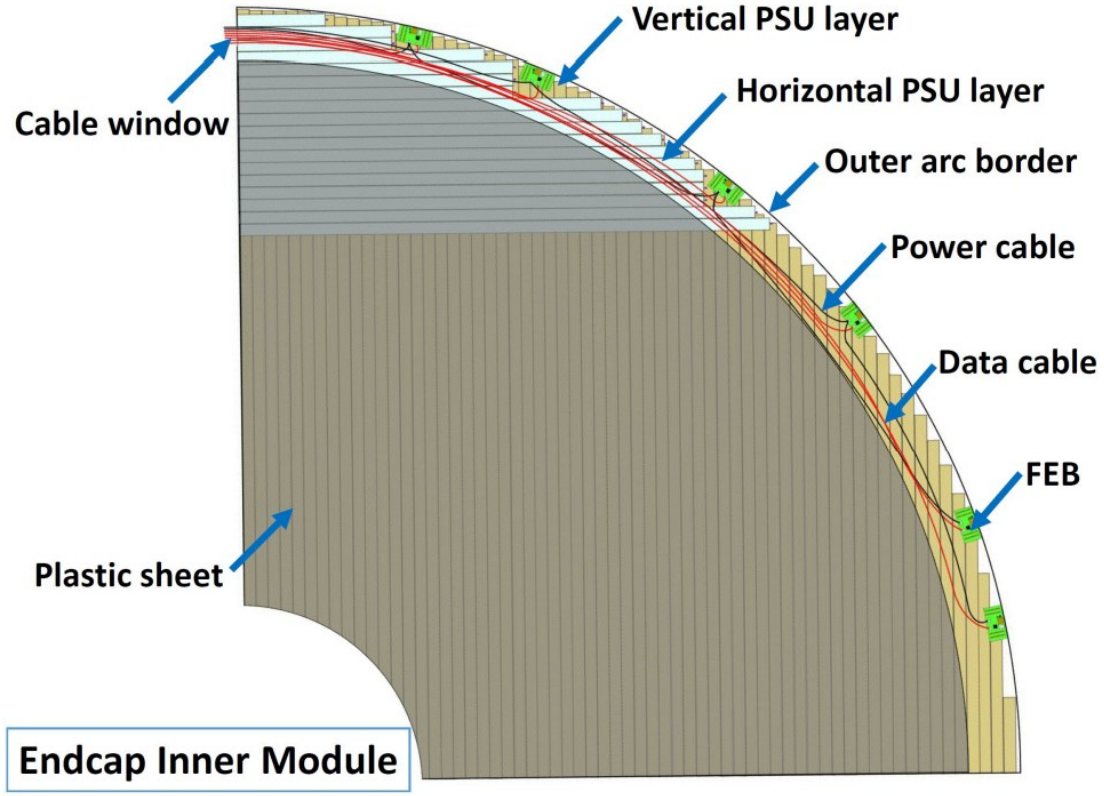
Endcap quadrant

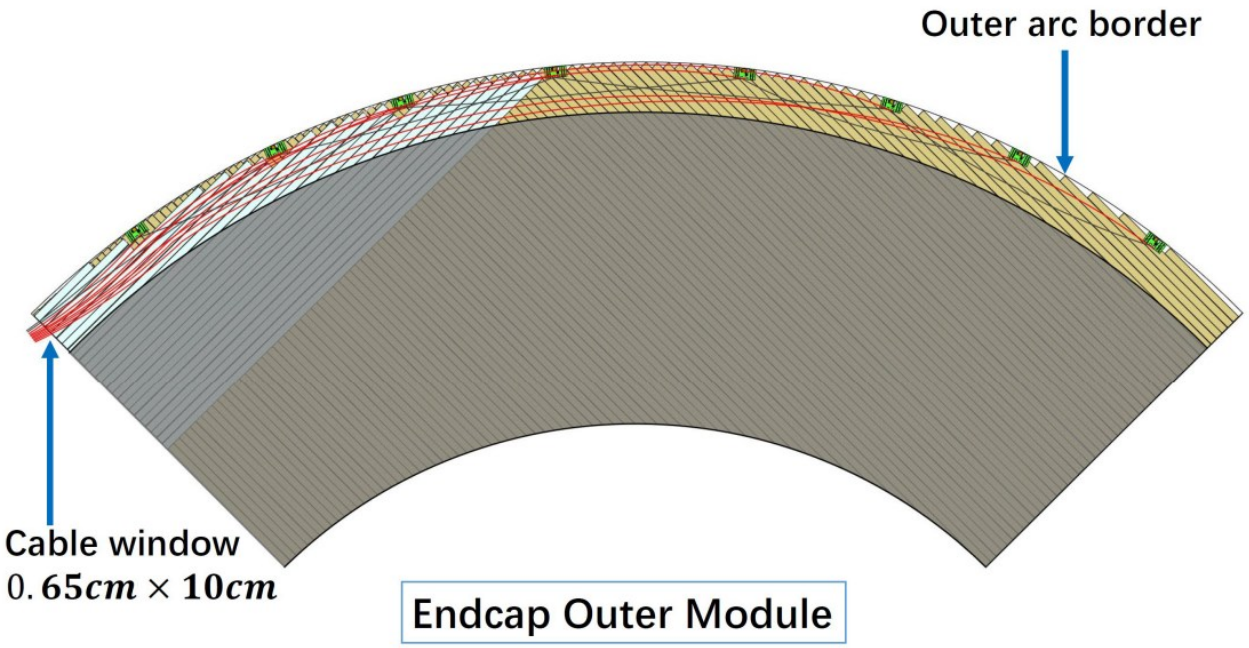


		M (SiPM)	N (FEB)		O (MB)
		ch	32-ch TDC board	Raw data rate / bps	Management board
Inner	layer	71	4	-	-
	quadrant	852	48	276.5 M	1
	endcap	3408	192	3.32 G	4
	Total	6816	384	6.64 G	8
Outer	layer	127	4	-	-
	quadrant	1524	48	737.3 M	1
	endcap	6096	192	2.95 G	4
	Total	12192	384	5.90 G	8

Detailed design: endcap modules

- Similar structure, but different shapes, compared to the barrel

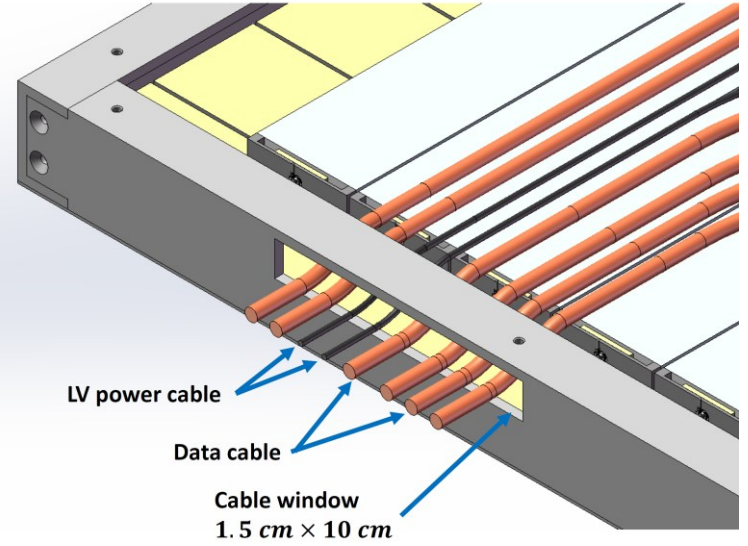




Cabling inside module

- Ipex cables between FEB and SiPMs.
- HDMI for data transmission between FEB and MB.
- MB distributes power to the FEBs in a daisy chain through LV cables.
- Power cable: input from MB or previous FEB, output to next FEB.

New



New

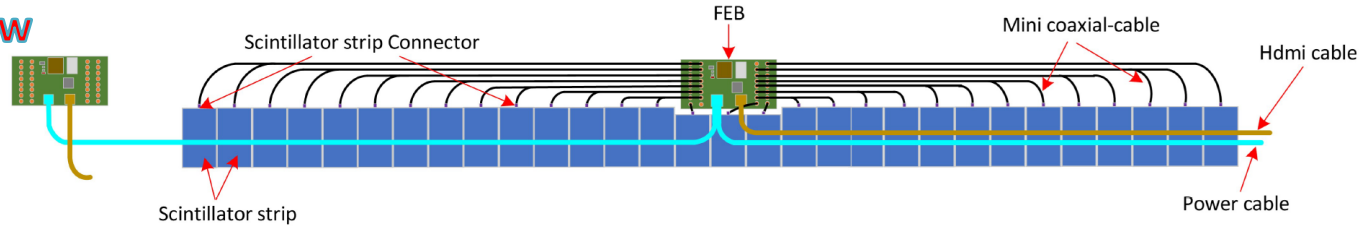
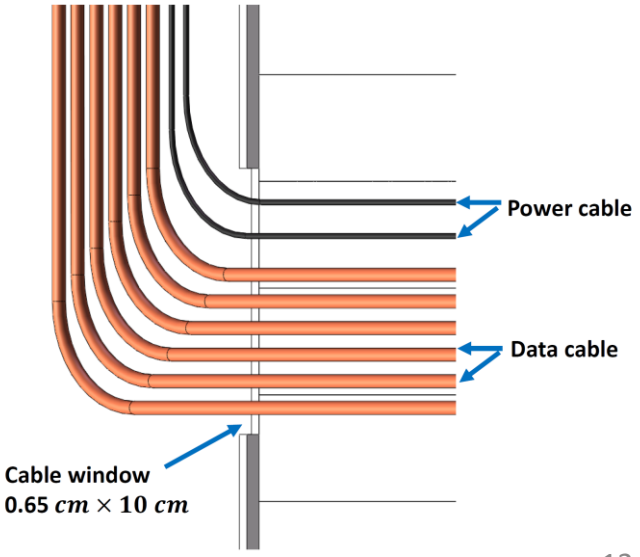


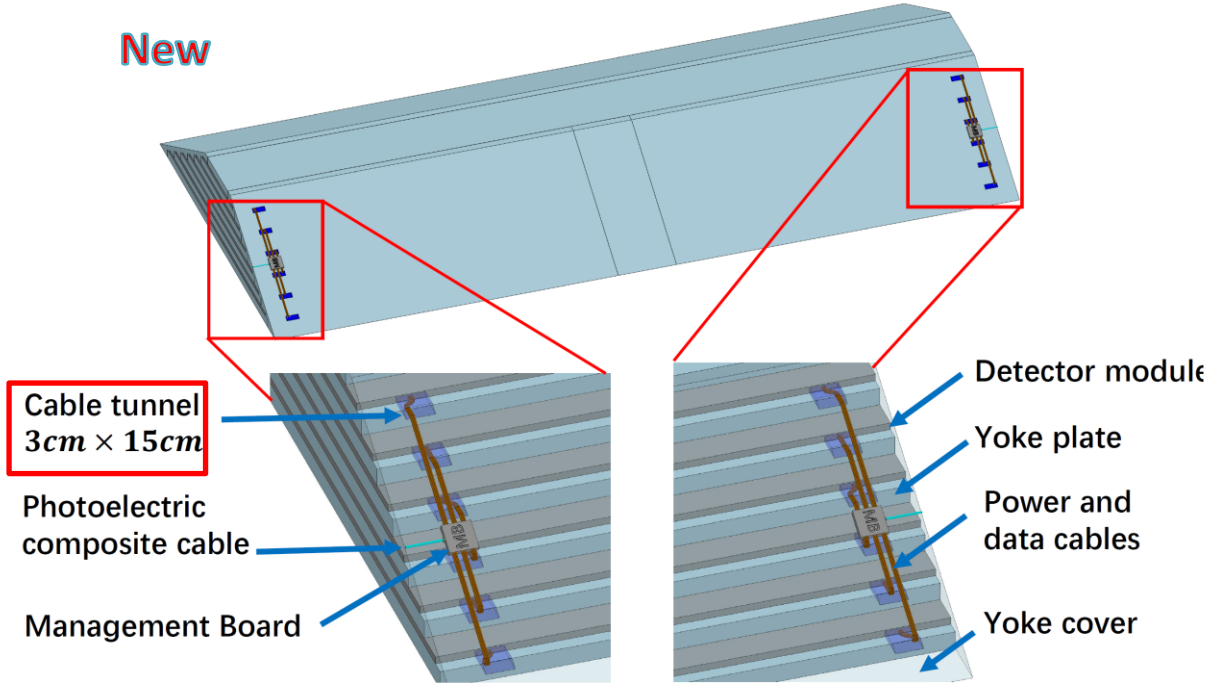
Figure 9.9: Diagram illustrating a FEB interfacing with its associated PSUs and MB. The FEB connects to the PSUs via 1 mm thin coaxial cables. The LV power is supplied to the FEBs from the MB through a daisy-chained LV cable network. Data communication between the FEB and MB is facilitated by dedicated HDMI cables.

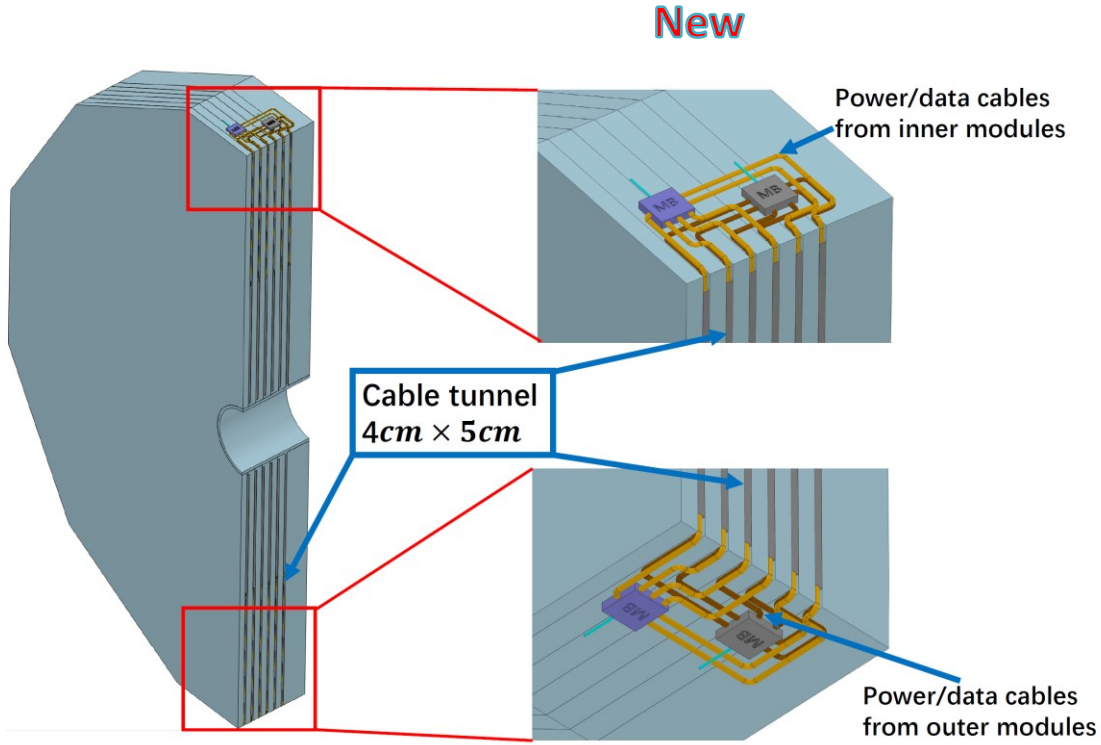
New



Cabling between FEB and MB

- Each MB connects to a group of six modules.
- Tunnels arranged for cabling between FEBs and MBs.
  - Barrel: tunnels on the cover plates.
  - Endcaps: tunnels created after modules being installed.





Summary

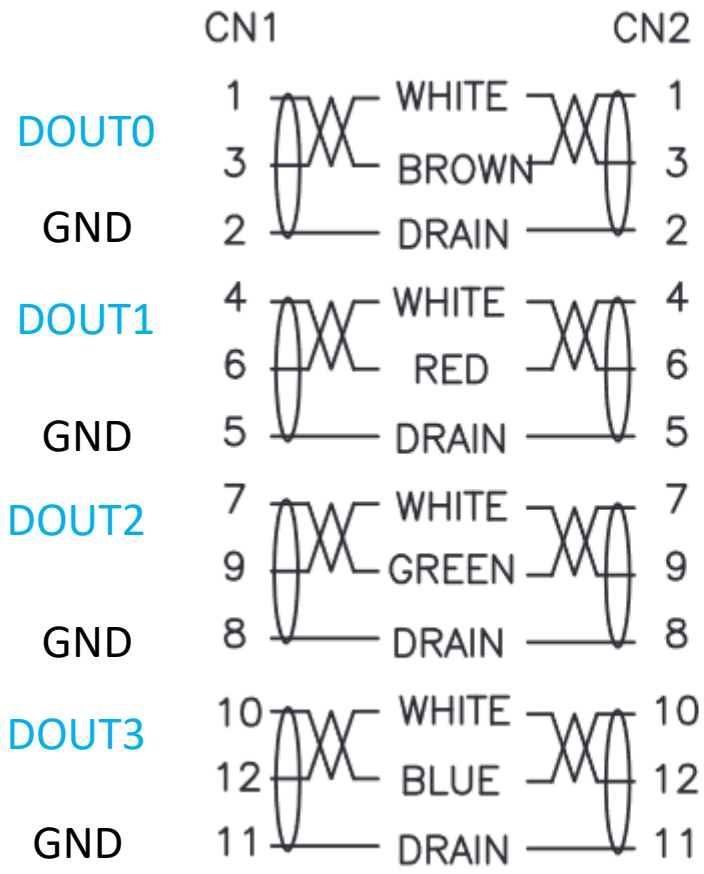
- CEPC muon detector uses ~45k SiPM channels across barrel and endcaps.
- Readout follows a 3-stage chain: SiPM tile → FEB → MB → backend.
- FEBs provide 32-channel digitization with ASIC TDC/ADC and integrated HV.
- MBs handle data aggregation, clock, control, and optical transmission.
- Total raw data bandwidth is ~24 Gbps under expected hit rates.

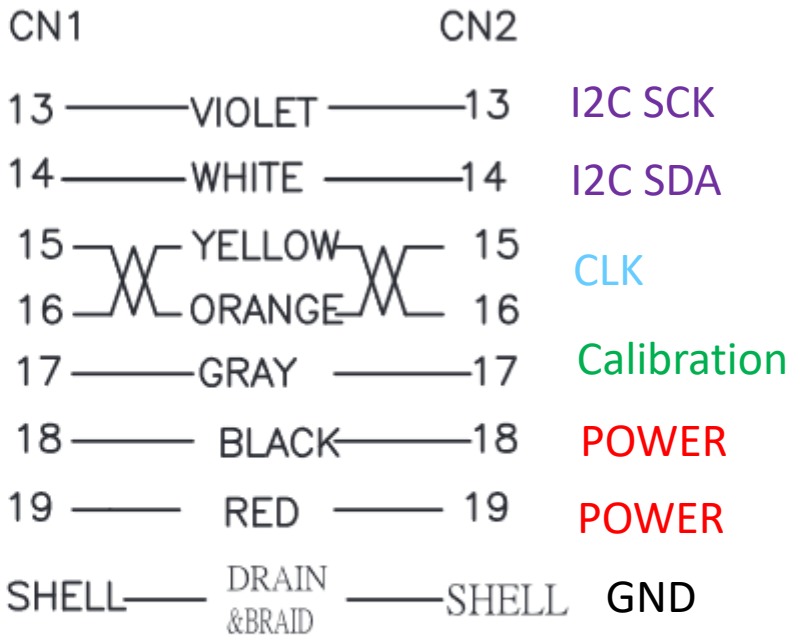
Backup

Summary

	M (SiPM)	N (FEB)		O (MB)
	ch	32-ch TDC board	Raw data rate / bps	Management board
Total barrel (12 sectors)	26064	894	11.51 G	24
Inner end-cap	6816	384	6.64 G	8
Outer end-cap	12192	384	5.90 G	8
Total	45072	1662		40

Pin re-definition for HDMI





- 4 ASICs require at least 500mA

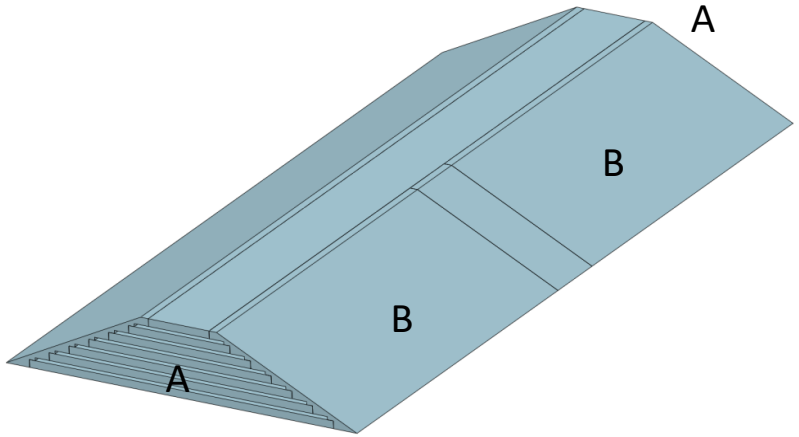
3.1 Rated voltage (Maximum): 40V AC (RMS)
3.2 Rated current (Maximum): 0.5A AC (RMS)/DC

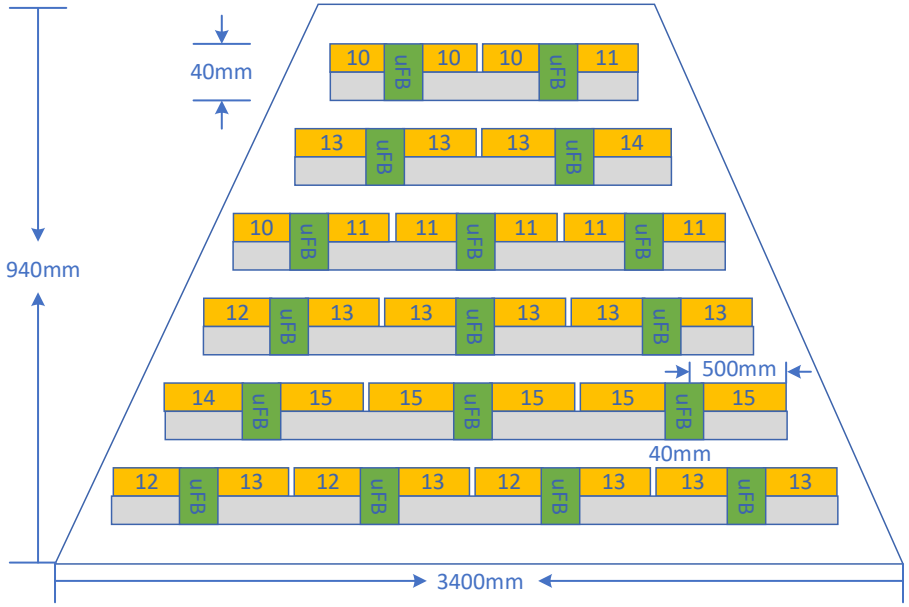
Back-end cables

- Fiber
  - 1.1 mm diameter
  - Quantity: 40
- Power
  - AWG 16 (2.35mm)
  - Quantity: 40 x 4

Electronics at A side

- Row 6, Col 110



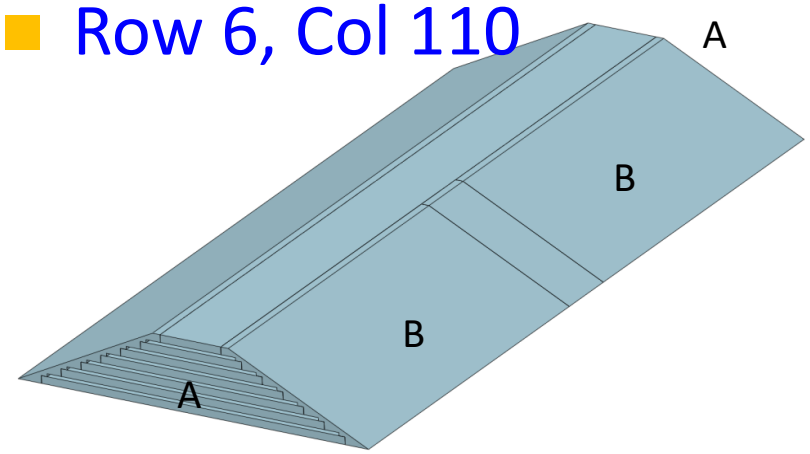


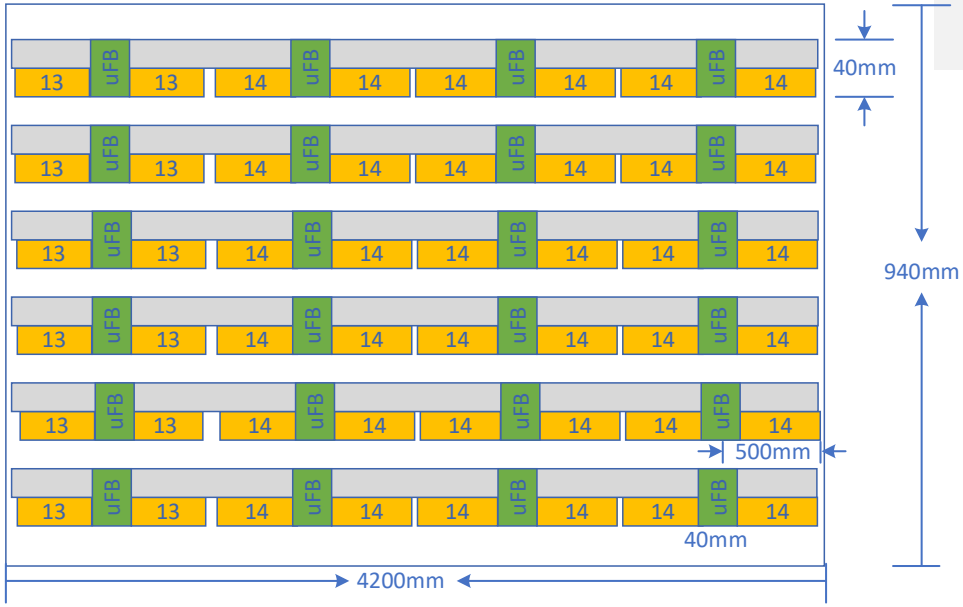
- SiPM tile: Muon SiPM tile
  - Small FR4 PCB
  - Mini coaxial connector
- Mini coaxial cables
  - Up to 14 lengths according to the locations of SiPM and FEB
- FEB: Muon front-end board, 17 pcs
  - 32 ch input, Mini coaxial connectors
  - HDMI and power connector

- MB: Muon management board, 1 pc
  - Fiber to backend
  - Power input (AWG16 x4), 48V

Electronics at B side

- Row 6, Col 110

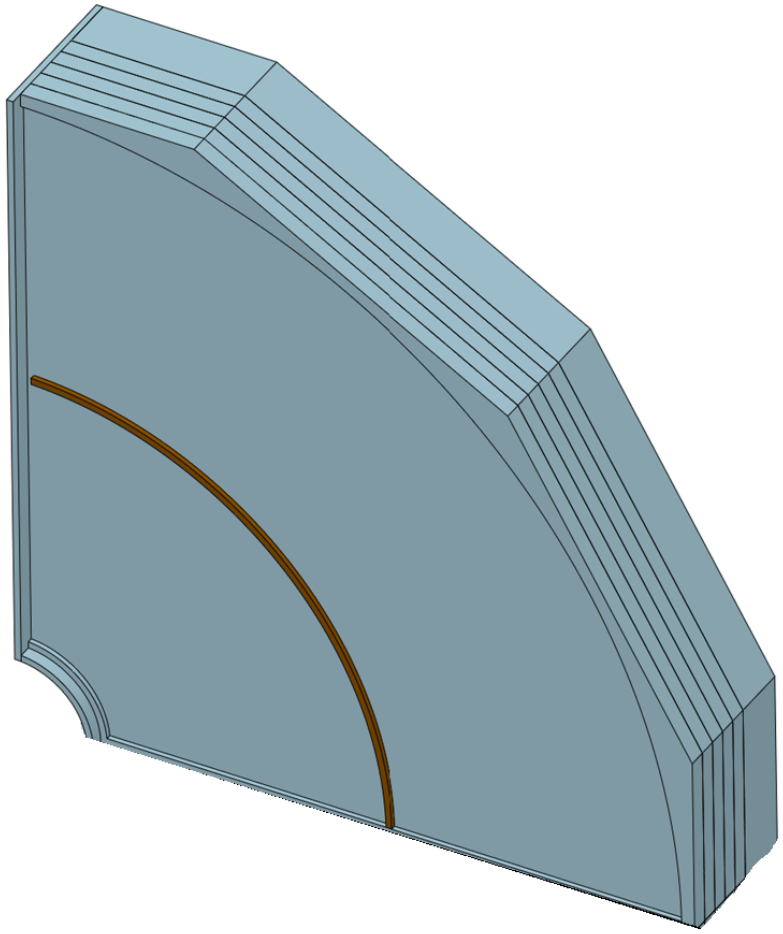




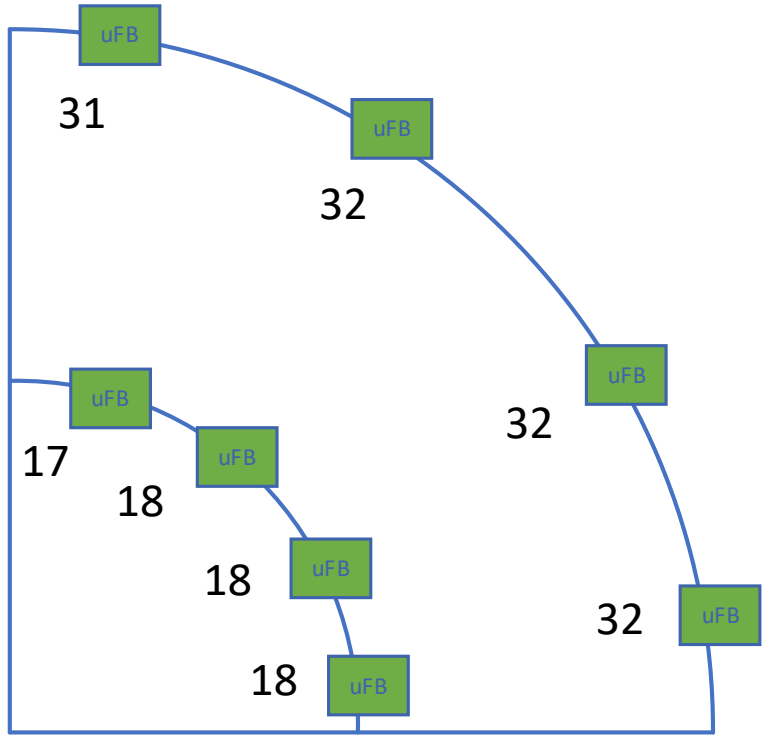
- SiPM tile: Muon SiPM tile, 660 pcs
  - Small FR4 PCB
  - Mini coaxial connector
- Mini coaxial cables
  - Up to 14 lengths according to the locations of SiPM and FEB
- FEB: Muon front-end board, 24 pcs
  - 32 ch input, Mini coaxial connectors
  - HDMI and power connector

- MB: Muon management board, 1 pc
  - Fiber to backend
  - Power input (AWG16 x4), 48V

Electronics at Endcap



12 layers



One layer

- SiPM tile: Muon SiPM tile, 198 pcs
  - Small FR4 PCB
  - Mini coaxial connector
- Coaxial cable
  - 2mm diameter
- FEB: Muon front-end board, 8 pcs
  - 50 mm x 40 mm FR4 PCB
  - 32 ch input, Mini coaxial connector
  - HDMI and power connector

- MB: Muon management board
  - Fiber to backend
  - Power input (AWG16 x4), 48V

Bandwidth requirement

Muon	Readout Channel	Hit rate/Hz (preliminary worst case)	Data format	Raw data rate / Gbps
Barrel	26064	10 k	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)	11.51
Inner endcaps	6816	10k~100 k, Average 20 k		6.64
Outer endcaps	12192	10 k		5.90
Total	~45 k			~24.04

bandwidth requirement

	Vertex	Pix(ITKB)	Strip (ITKE)	OTKB	OTKE	TPC	ECAL-B	ECAL-E	HCAL-B	HCAL-E	Muon
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Ref. Signal processing	XY addr + BX ID	XY addr + timing	Hit + TOT + timing	ADC+TDC/TOT+TOA		ADC + BX ID	TOT + TOA/ ADC + TDC				
Data Width /hit	32bit (10b X+ 9b Y + 8b BX + 5b chip ID)	42bit （9b X+7b Y +14b BX + 6b TOT + 5TDC + 1b polarity）	32bit (10b chn ID + 10b BX + 6b TOT + 5b chip ID)	40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID ）		48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)				
Max Data rate / chip	2Gbps/chip@Triggerless@Low LumiZ Innermost	Avg. 3.53Mbps/chip Max. 68.9Mbps/chip	Avg. 21.5Mbps/chip Max. 100.8MHz/chip	Avg: 2.9Mbps/chip Max: 3.85Mbps/chip	Avg: 38.8Mbps/chip Max: 452.7Mbps/chip	~70Mbps/ module Inmost	~9.6Gbps/module @dual-end readout	Needs bkgrd rate	Needs bkgrd rate	Needs bkgrd rate	
Data aggregation	10~20:1, @2Gbps	14:1@O(100Mbps)	22:1 @O(100Mbps)	i. 22:1 @O(5Mbps) ii. 7:1 @O(100Mbps)	i. 22:1 @O(50Mbps) ii. 10:1 @O(500Mbps)	1. 279:1 FEE-0 2. 4:1 Module	i. 4~5:1 side ii. 7*4 / 14*4 back brd @ O(100Mbps)	Needs detector finalization	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)	Needs detector finalization	
Detector Channel/module	1882 chips @Stch &Ladder	30,856 chips 2204 modules	23008 chips 1696 modules	83160 chips 3780 modules	11520 chips 720 modules	492 Module	0.96M chn ~60000 chips 480 modules	Needs detector finalization	3.38M chn 5536 aggregation board	2.24M chn 1536 Aggregation board	
Avg Data Vol before trigger	474.2Gbps	101.7Gbps	298.8Gbps	249.1Gbps	27.9Gbps	34.4Gbps	4.6Tbps (needs finalization)	Needs det & bkgrd finalization	Needs det & bkgrd finalization	Needs det & bkgrd finalization	

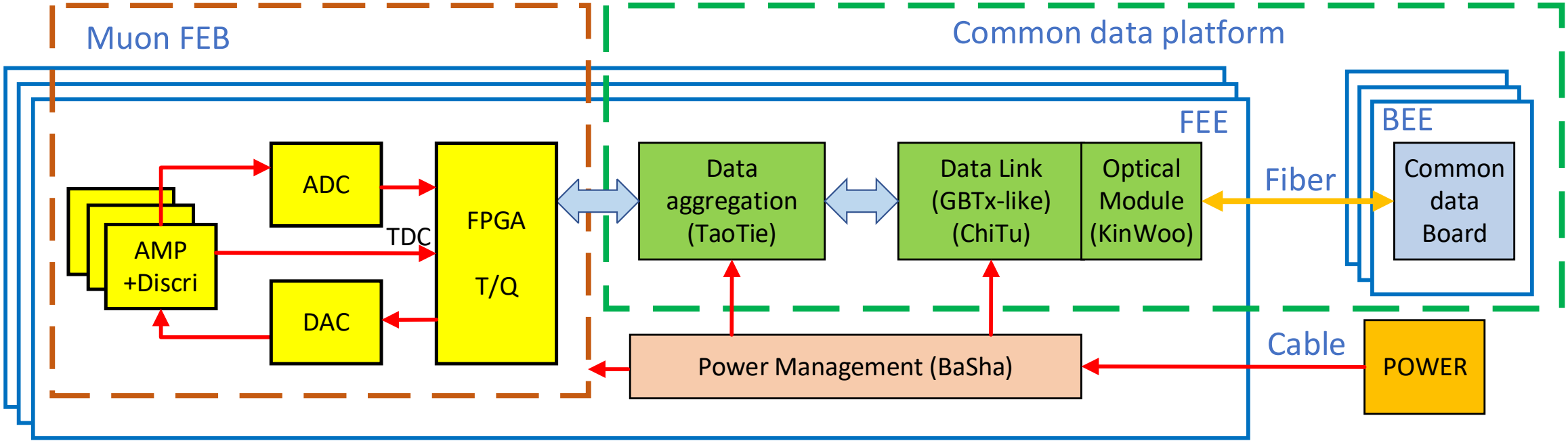
Avg. 15.36 Mbps/chip
Max. 153.6 Mbps/chip

<=24:1
@ O (368.7 Mbps)

43.2k ch
40 Aggregation board

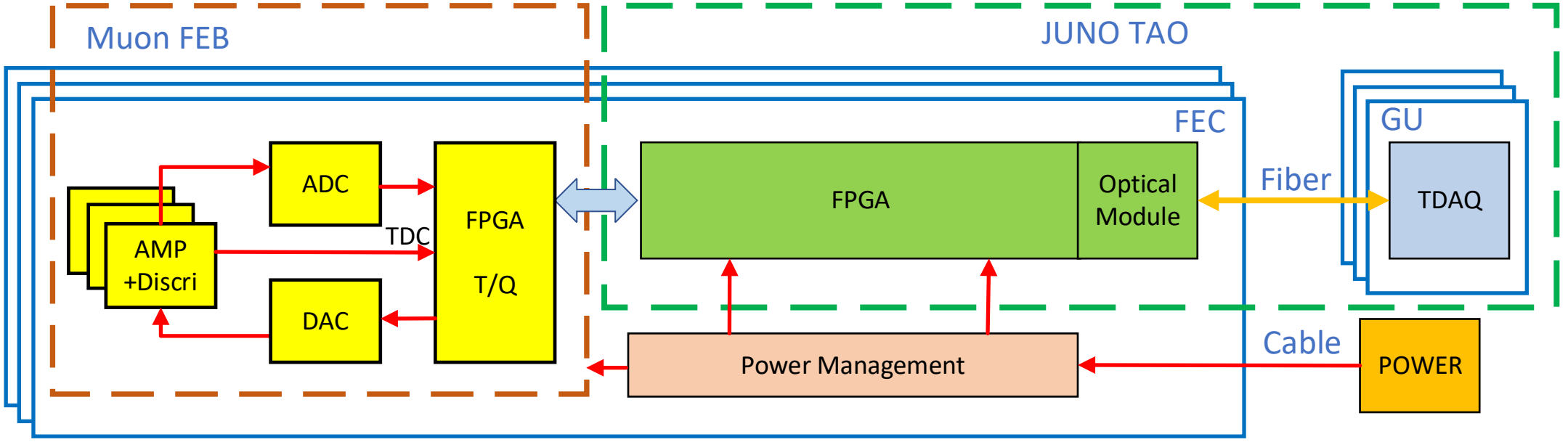
~ 24.04 Gbps

Alternative: discrete device scheme



- FEB (Front-end Electronics Board)
  - Commercial chips with radiation tolerance based on past studies for particle physics experiments
  - FPGA based TDC for TOA and TOT measurement with ~1 ns time resolution
  - ADC for charge measurement or TOT calibration
  - DAC for threshold setting or SiPM bias voltage adjustment

Near-term test environment



- Reuse JUNO-TAO electronics for readout, clock synchronization and TDAQ
  - To accelerate the development schedule