Design and Verification of the Digital System for the FEDI

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CEPC International Workshop, Guangzhou, Nov. 8, 2025

1. The Concept of the FEDI

2. Design of the FEDI

3. Verification of the FEDI

4. Conclusion

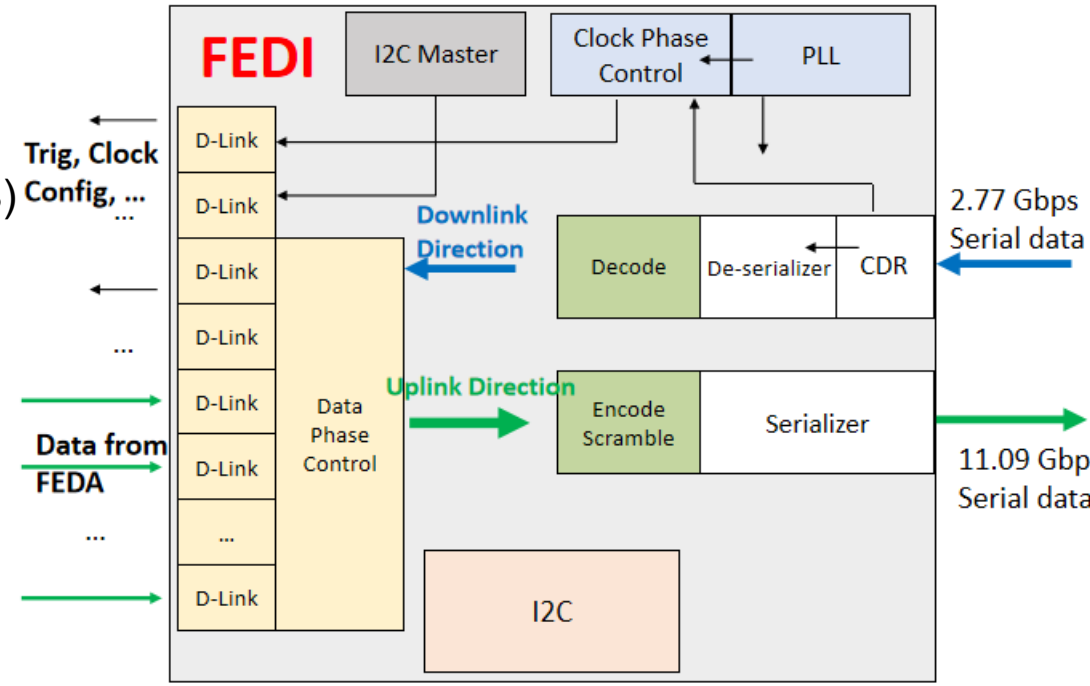
Concept of the Front End Data Interface*

- **What are the requirements of the detector front-end for communication with the back-end?**
  - **Massive data uplink** transmission requirements (High data throughput) 10 Gbps/ch +
    → Various detectors have various channel numbers and various data rates
  - Front-end electronics need **clock**
    → Maybe different frequency or different phases are needed
  - Front-end electronics need **trigger signal, control signal** from the back-end
    → Relatively low data throughput (**Downlink**)
    → Massive front-end units need to be configured (I2C, …)
  - Front-end units need to transmit current, temperature, **status… monitoring** information to the Back-end
  - All these transmissions need to be robust and **radiation-tolerant.**
- **The concept of the Front End Data Interface(FEDI)**
  - Aims to build **a universal, bi-directional, high-speed data link system** between the front-end and the back-end for various detector requirements in CEPC.

**Taken from 2024 CEPC A common project for detector data links -Di Guo*

FEDI Overview

- Main modules
  - Uplink Direction:
    - Up to 1.39 Gbps/ch Data Rx (Inside D-Link)
    - Multi-channel Data Phase Control
    - Data Scrambler, Encoder, Frame Builder
    - 11.09 Gbps Serializer + High-speed Tx (Pre-emphasis)
  - Downlink Direction:
    - 2.77 Gbps Clock Data Recovery (CDR)
    - 2.77 Gbps Deserializer
    - Data Decoder
    - Data Tx (Inside D-Link)
  - Other sub-modules:
    - 5.54 GHz Phase-Locked Loop (PLL)
    - Clock Phase Control
    - I2C Master and related configuration submodules



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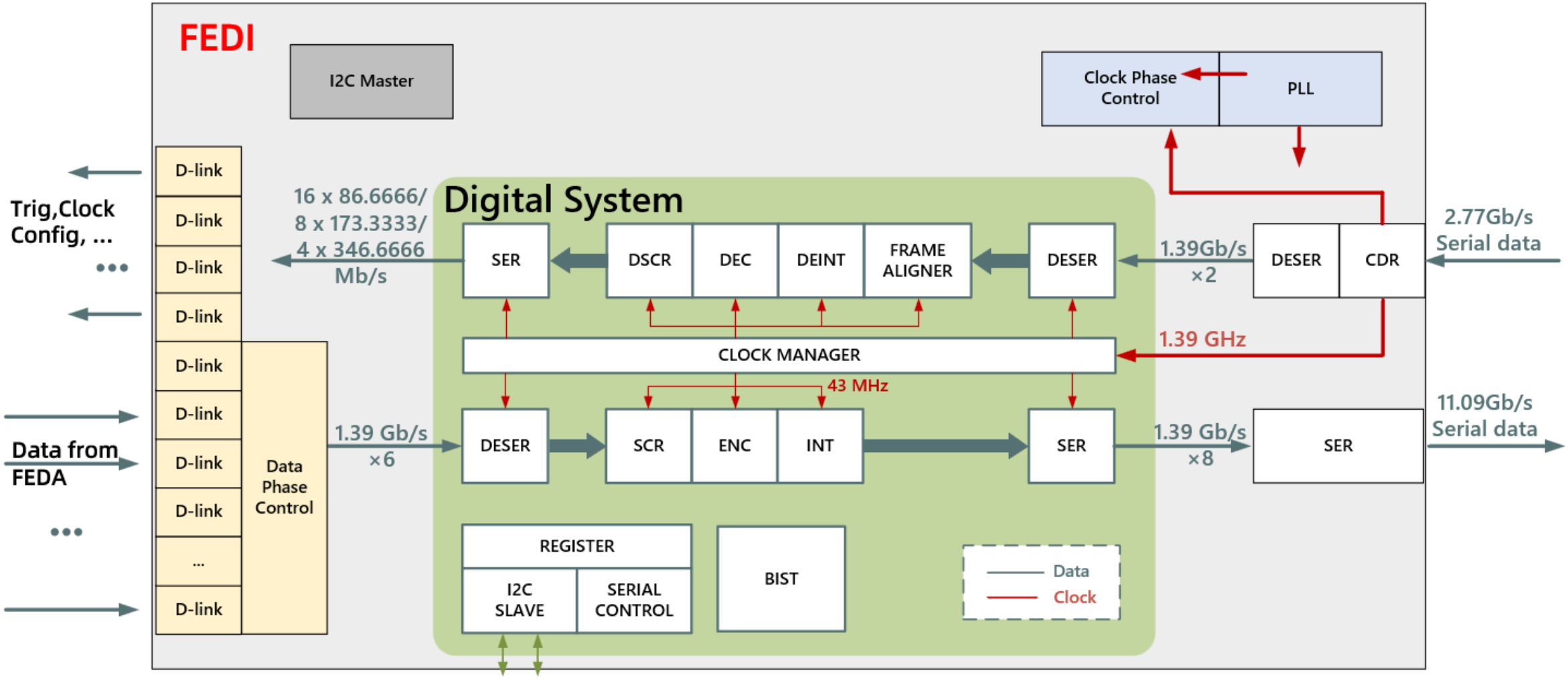
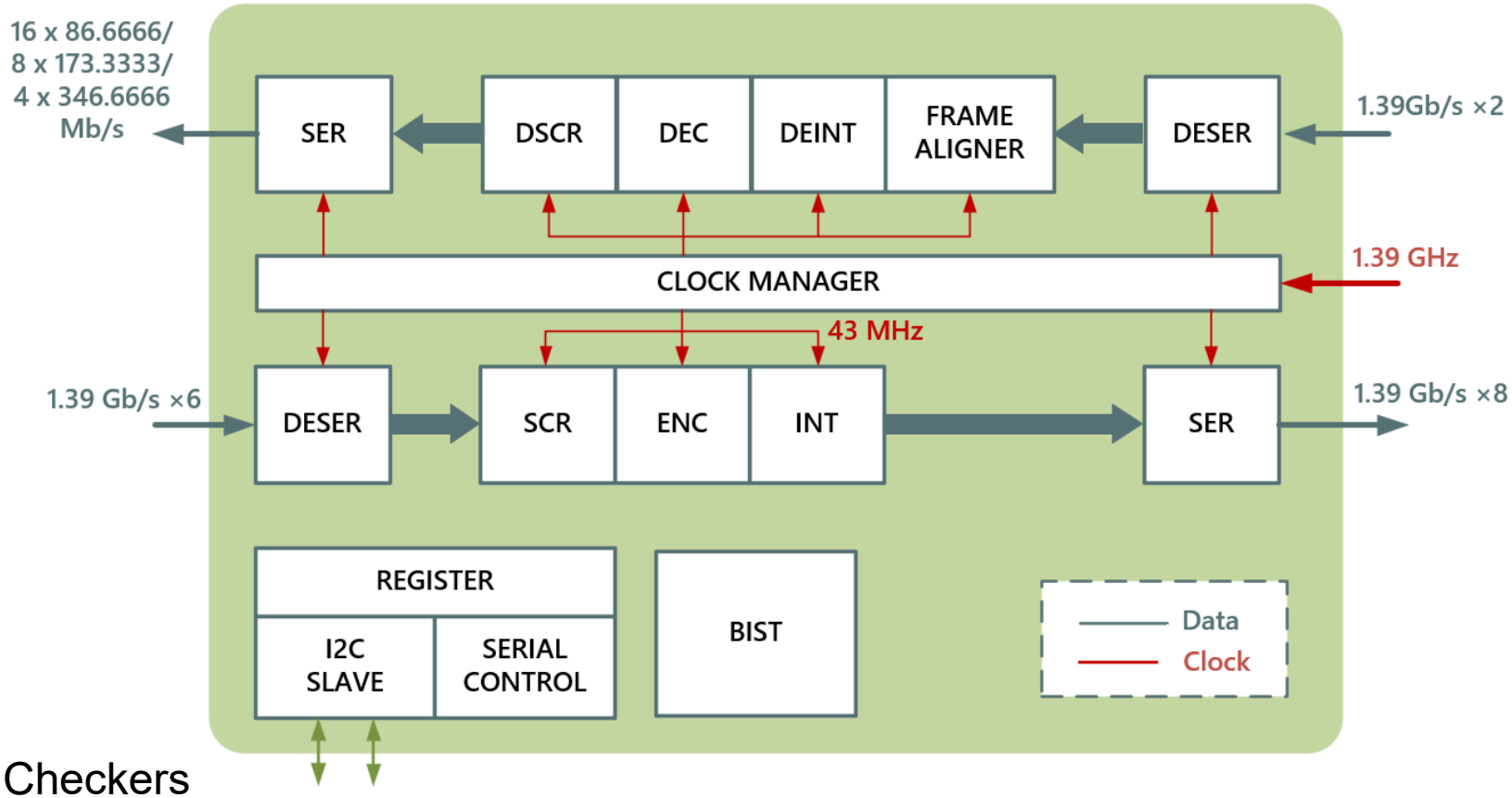
Block diagram of FEDI



FEDI Digital System

- Structure of FEDI Digital System
  - Clock & Reset :
    - Clock Manager
    - Reset Gen
  - System Configuration :
    - Serial Control
    - I2C Slave
  - Data Path:
    - Uplink
    - Downlink
  - Built-in Self-Test, BIST:
    - Test Pattern Generators & Checkers
    - Loopbacks



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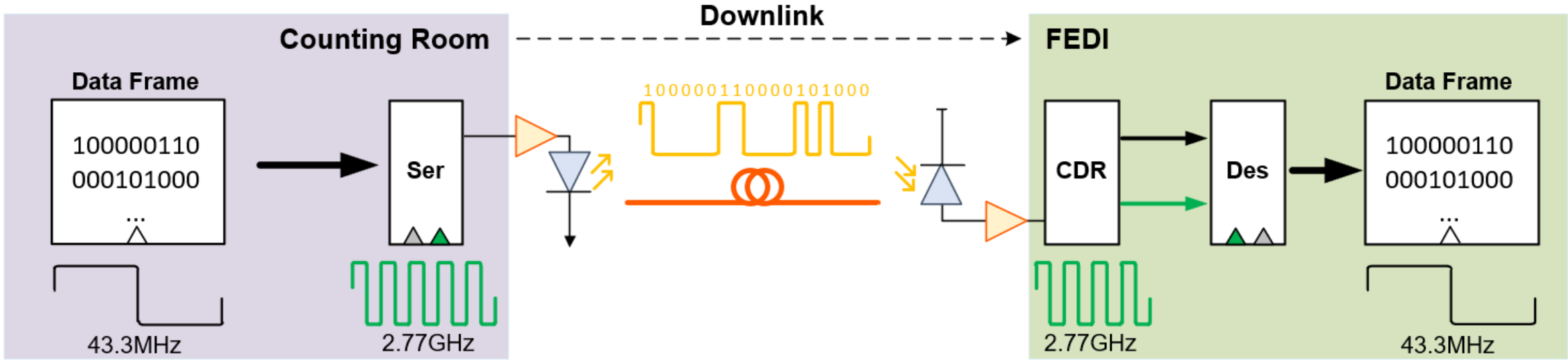
Downlink

- Downlink: from the counting room to the FEDI over optical links
- In the counting room, a 43.3 MHz data frame is serialized up to a 2.77 GHz data stream
- On the FEDI side, the CDR recovers the 2.77 GHz clock and the Deserializer reconstructs the original data frame

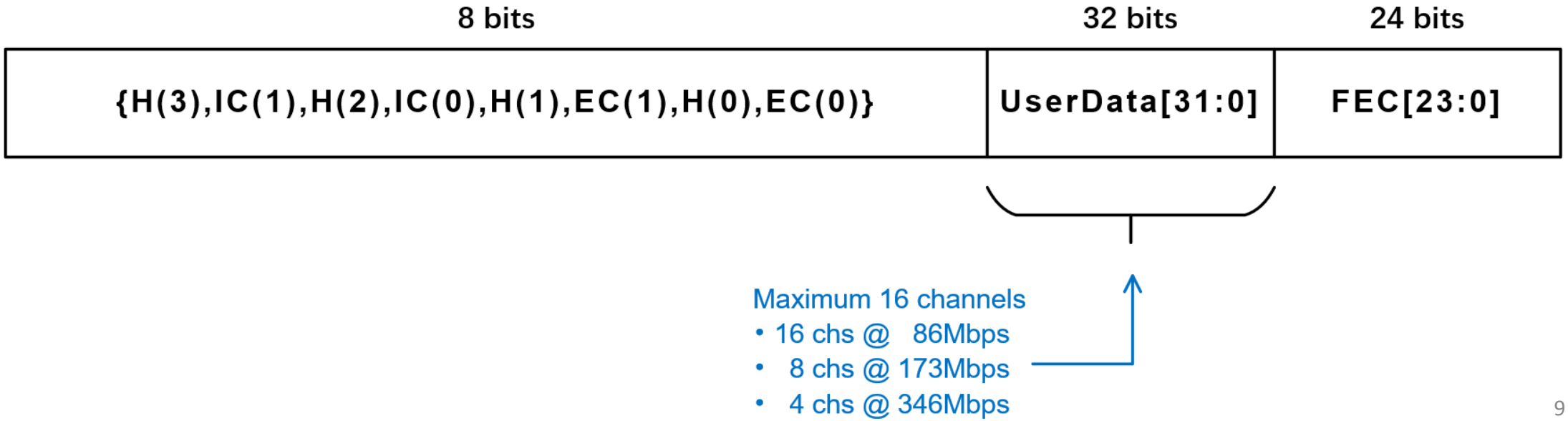


For our digital system, **processing the data frame** is a core function for both uplink and downlink.

**The figure adapted from: E. B. S. Mendes, Ph.D. Thesis, CNAM, 2025*

Downlink Frame

- Downlink frame (64-bit @2.77Gb/s)
  - **Header (4 bits):**
    - Frame delimiter for synchronization.
  - **Data (36bits):**
    - This field combines the user payload with the control channels.
    - User Data (32 bits): Main data payload (1.39 Gb/s)
    - Serial Control (4 bits): IC (internal) & EC (external) control channels.
  - **FEC (24 bits):**
    - Forward Error Correction , detects and corrects transmission errors.



Downlink DataPath

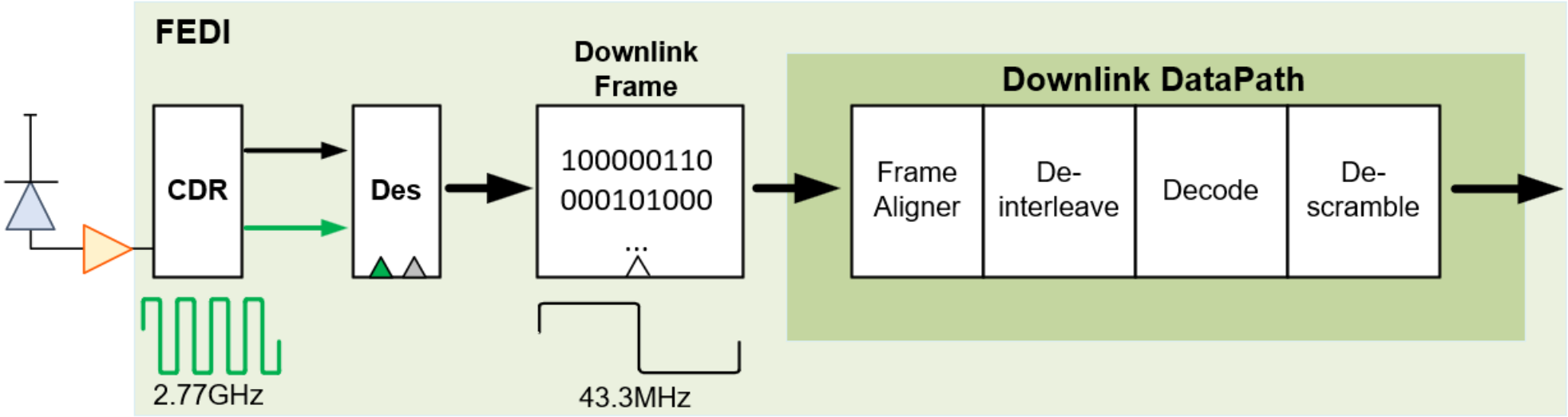
Once the downlink frame is received and deserialized, it enters the Downlink DataPath in the digital system:

Frame Aligner → De-interleaver → FEC Decoder → De-scrambler

For Downlink FEC:

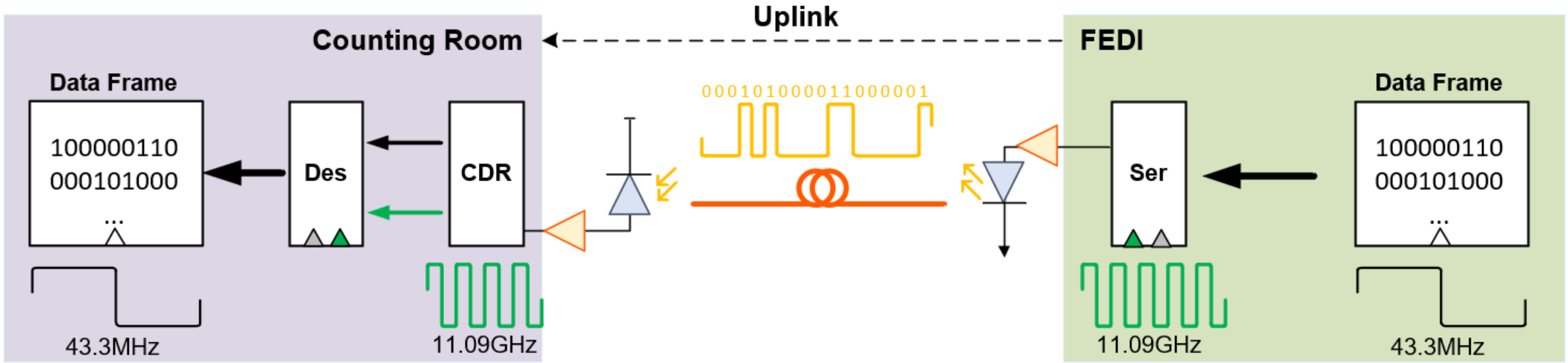
- 4 codes interleaved
- RS(5,3), m = 3 bits

The coding can correct any 10-bit burst errors (12-bit burst error in maximal).



Uplink

- Uplink: from the FEDI to the counting room



- Uplink Frame(256-bit @11.09Gb/s)

2 bits	2 bits	2 bits	10 bits	192 bits	48 bits
H[1:0]	IC[1:0]	EC[1:0]	{8'b0,DownIC[1:0]}	UserData[191:0]	FEC[47:0]

Uplink DataPath

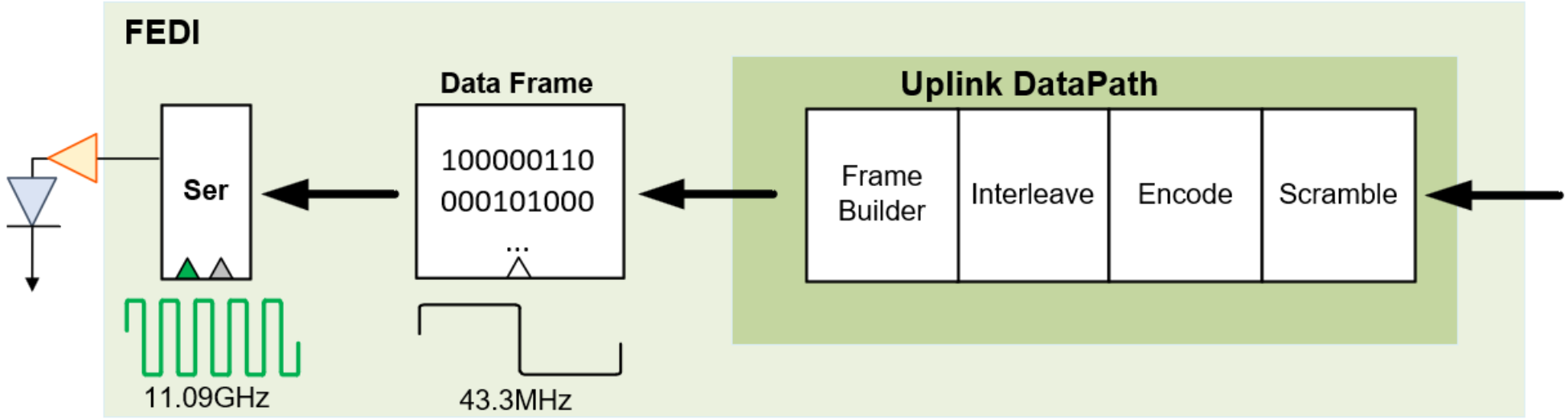
After the data from FEDA is deserialized, it enters the Uplink DataPath in the digital system:

Scrambler → FEC Encoder → Interleaver → Frame Builder

For Uplink FEC:

- 6 codes interleaved
- RS(15,13), m = 4 bits

The coding can any 21-bit burst errors (24-bit burst errors in maximal).



Chip Operating Modes and Configuration

Chip Operating Modes:

- The chip supports transceiver, transmit (TX), and receive (RX) modes.

Configuration Access:

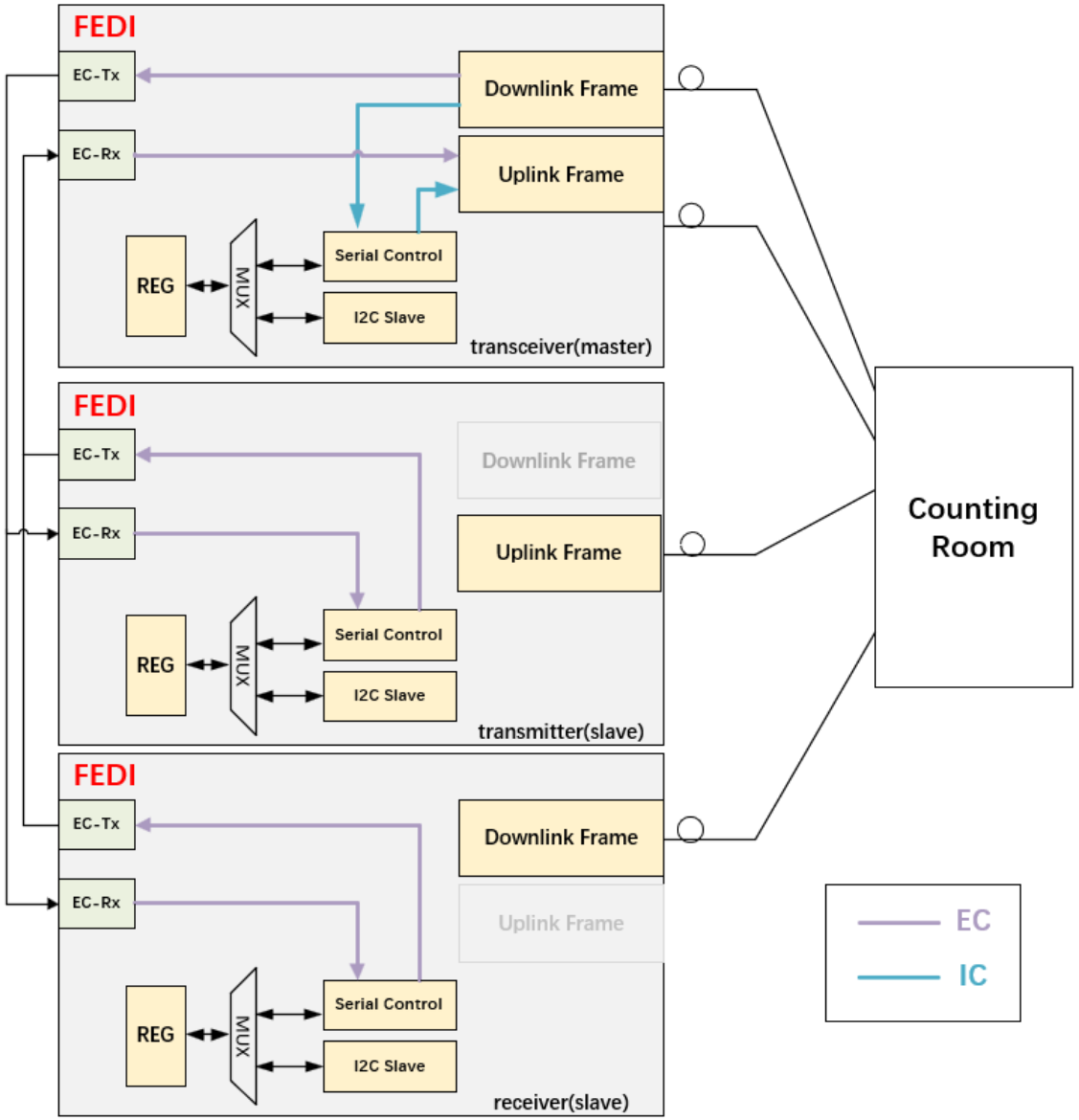
- Two blocks can modify writable registers: I2C Slave and Serial Control.

Serial Control:

- In transceiver mode, the Frame's IC[1:0] field controls the local chip, whereas EC[1:0] field controls external chips (such as those in simplex mode).

I2C Slave:

- It can configure registers in all operating modes.

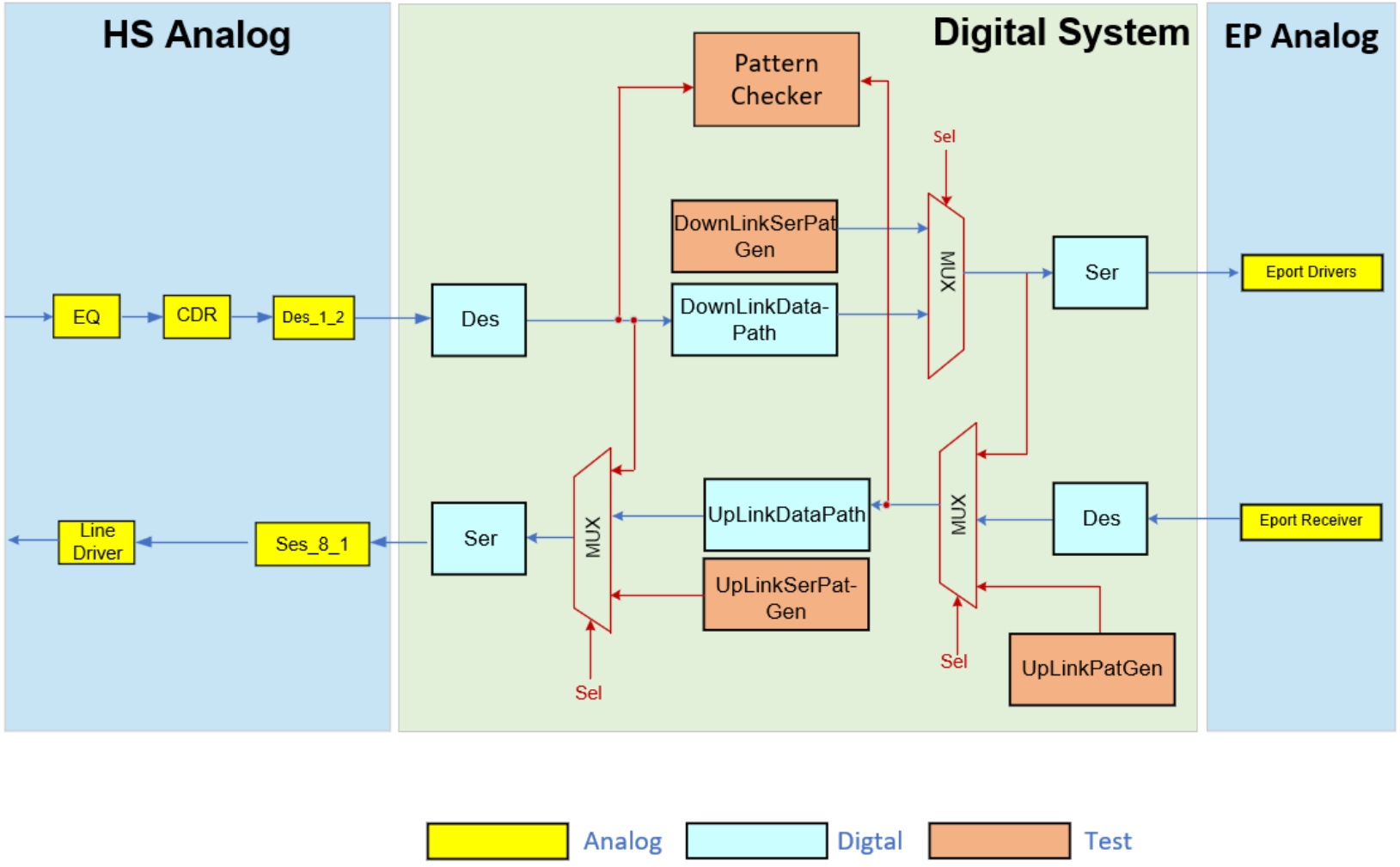


Built-in Self Test (BIST) of Datapath

- BIST is designed for the uplink and down link Datapath for highly efficient chip debug and test.

The BIST architecture includes:

- Test Pattern Generators
  Inject defined data sequences into various points of the data path for debugging.
- Test Pattern Checkers
  Check the data stream for errors against a known sequence
- Loopbacks
  Isolate and test specific data paths (e.g., Digital System, SerDes).



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Verification Method of FEDI

- **We utilize UVM in our verification for the following reasons:**

1. Modularity and Reusability will speed up future verification work.

Standard, component-based testbenches (UVCs) that are easy to plug-and-play. This modular design allows for quick integration of new features or subsystems.

2. It is efficient and suitable for FEDI's architecture.

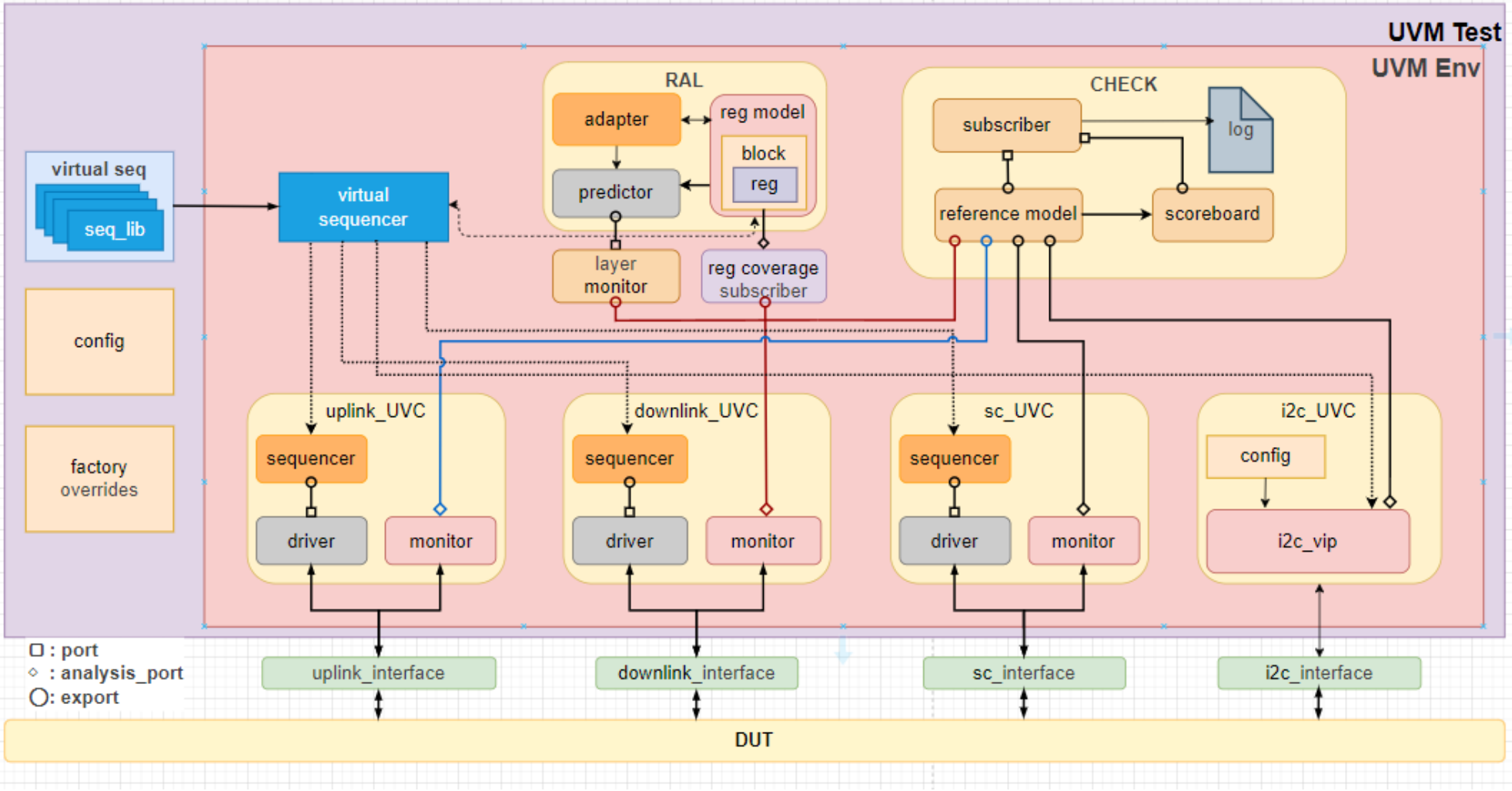
- Constrained-random stimulus reduces manual test case creation effort;
- Coverage-driven verification ensures comprehensive validation;
- The register model simplifies register-level testing.

All contributing to high verification efficiency aligned with FEDI's architecture.

3. Adherence to Industry Standards mitigates the development risks, as it

- Ensures compatibility with mainstream vendor tools;
- Facilitates smoother collaboration across multi-functional teams.

UVM Architecture



Core Philosophy:

- **Factory override** mechanism
- **Reusable** sequence
- **Decouple** Test from Env

Key Blocks

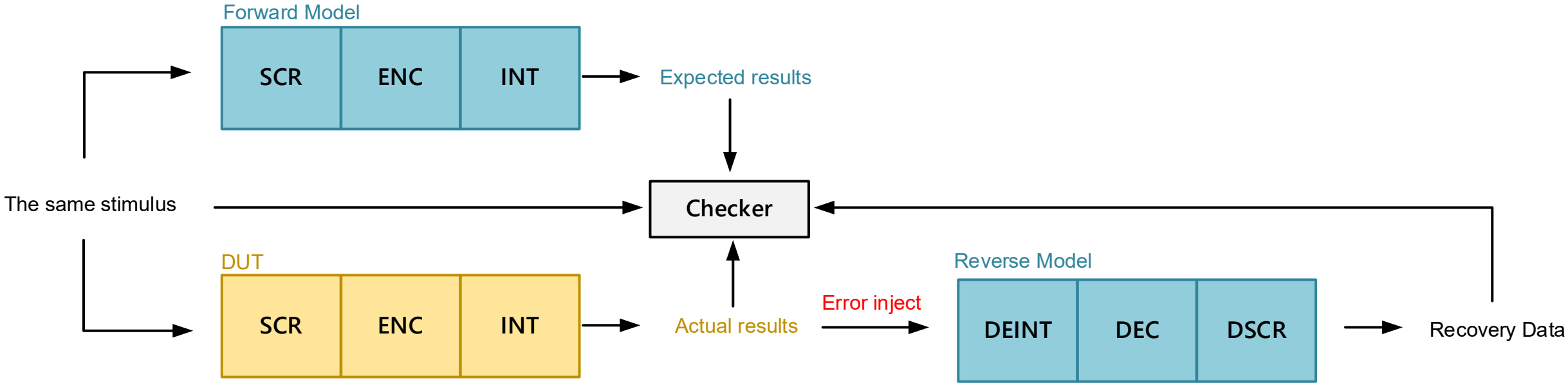
- **Functional UVCs**
- **RAL Model** for DUT Configuration
- Online Validation Engine (**Checker**)
- **Virtual Sequencer**

Key Component: Reference Model

- A functionally accurate, high-level reference model of the design that independently calculates the expected results based on the same stimulus sent to the DUT.
- Objective
  - Provide Expected Results
  - Verify Functional Correctness

Example： Uplink

- Build Forward Model : step-by-step check for fast debugging
- Build Reverse Model : assess uplink recoverability and FEC correction limits.

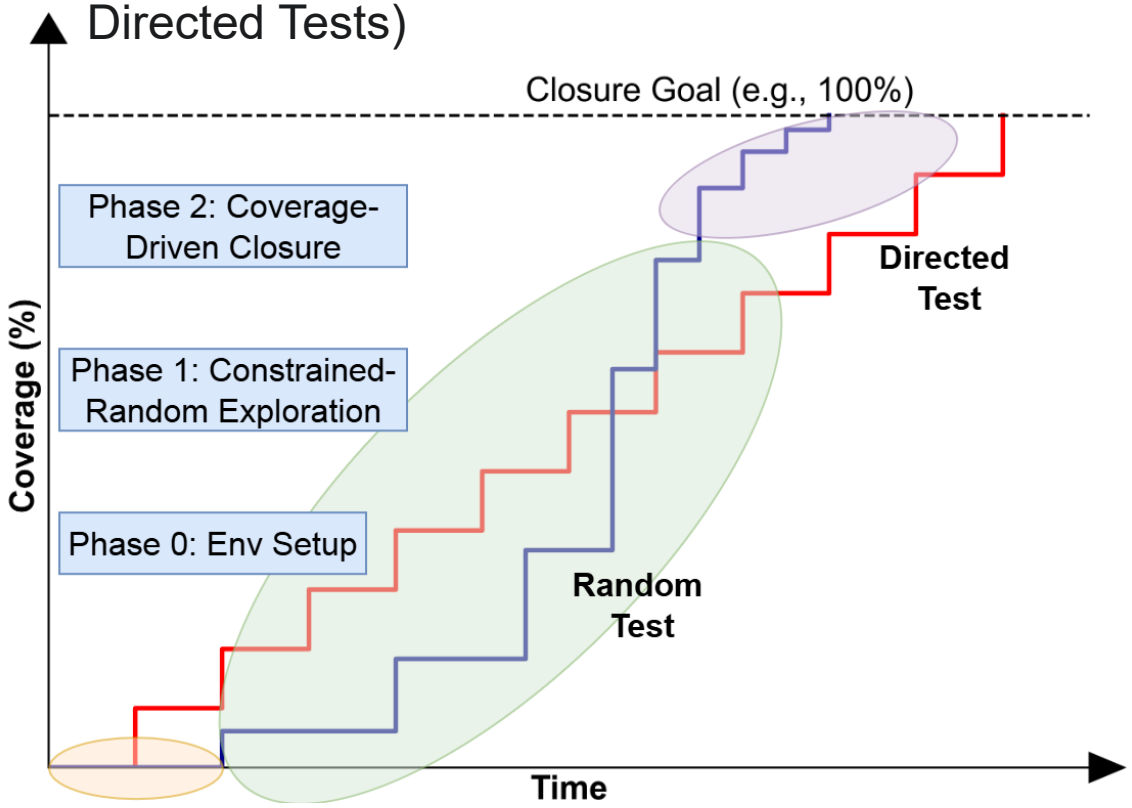


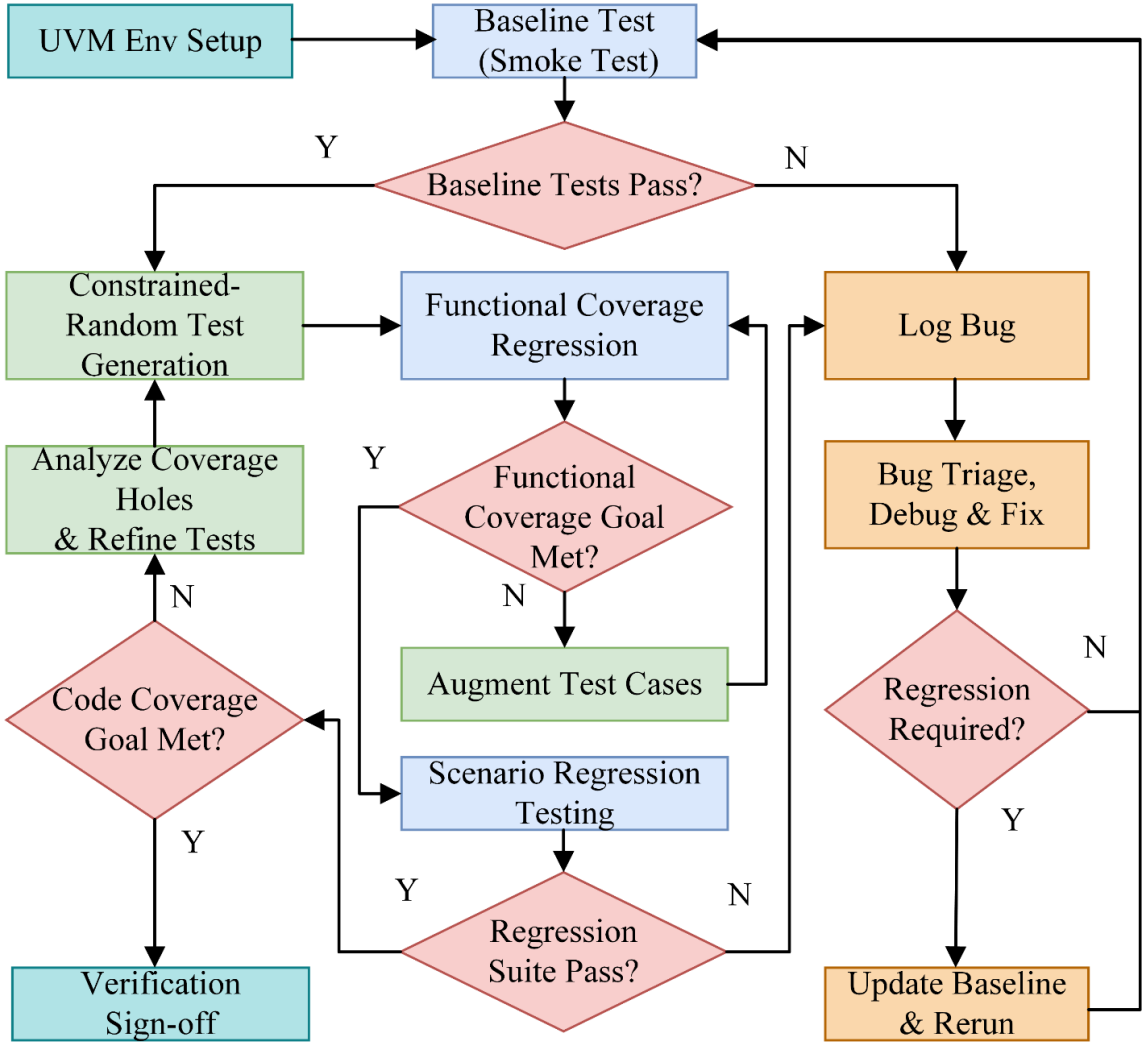
Verification Strategy & Flow

Goal: Systematically achieve **Verification Closure**.

Strategy:

- **Phase 1: Broad Exploration** (Constrained-Random)
- **Phase 2: Deep-Diving & Closure** (Coverage-Driven Directed Tests)





Our Metric-Driven Verification (MDV) Flow

Source: 2025 ICICM Design of a Reusable UVM Verification Framework for Pixel Readout Chips -Zhao,Zhao, Jiao, Wei, Yang, Liu, Hu*

Verification Status

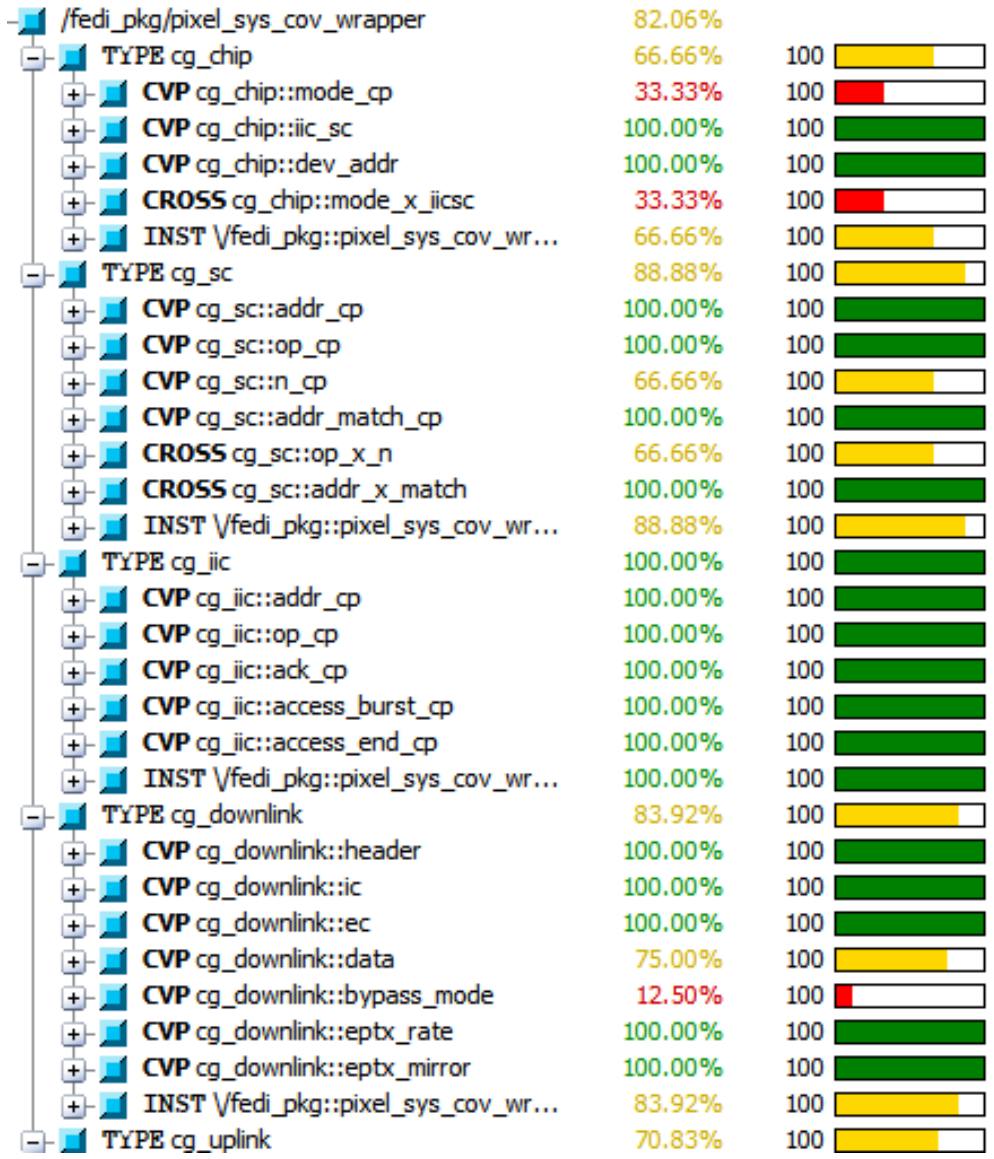
Scope	TOTAL	Statement	Branch	FEC Expression	FEC Condition	Toggle
TOTAL	87.65	97.63	93.89	83.79	86.95	75.97
u_Digital_Core	85.30	100.00	80.00	100.00	--	61.21
u_Clock_Gen	98.86	100.00	100.00	--	100.00	95.45
u_reset_gen	87.17	100.00	100.00	--	--	61.53
u_Debug_Top	68.18	94.36	77.38	71.45	50.00	47.74
u_DownLink_Top	96.37	96.77	94.56	98.42	--	95.75
u_UpLink_Top	97.65	99.35	96.74	100.00	--	94.50
u_System_Core	82.79	98.26	97.45	78.70	85.52	54.00

Current Coverage Metrics:

- **Code Coverage:** 87.65%
- **Functional Coverage:** 82.06%

Next Steps:

- **Coverage Closure:** Augment more test cases.
- **Regression Implementation:** Establish and deploy an automated regular regression flow.



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Completed Design Milestones:

- The core 11.09 Gb/s Uplink and 2.77 Gb/s Downlink data processing paths have been fully designed and implemented.
- Both I2C and SC interfaces are integrated for versatile configuration.
- A comprehensive BIST architecture has been incorporated to ensure chip testability.

Verification Status & Methodology:

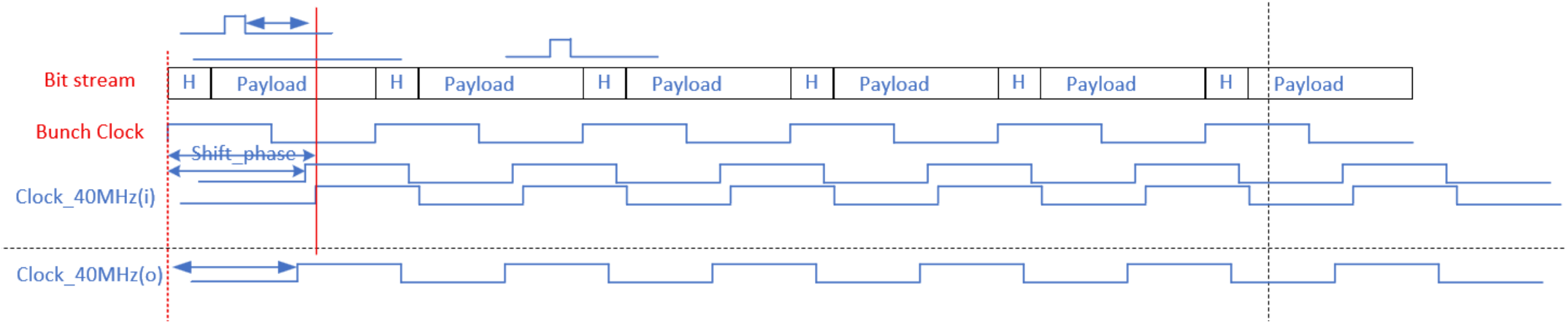
- A UVM-based verification environment is being systematically developed to verify the FEDI ASIC.
- A reference model and scoreboard were developed to verify the functional correctness of the design from end to end.

The FEDI ASIC tape-out is scheduled for Q1 2026

Thank you for your attention!

Backup

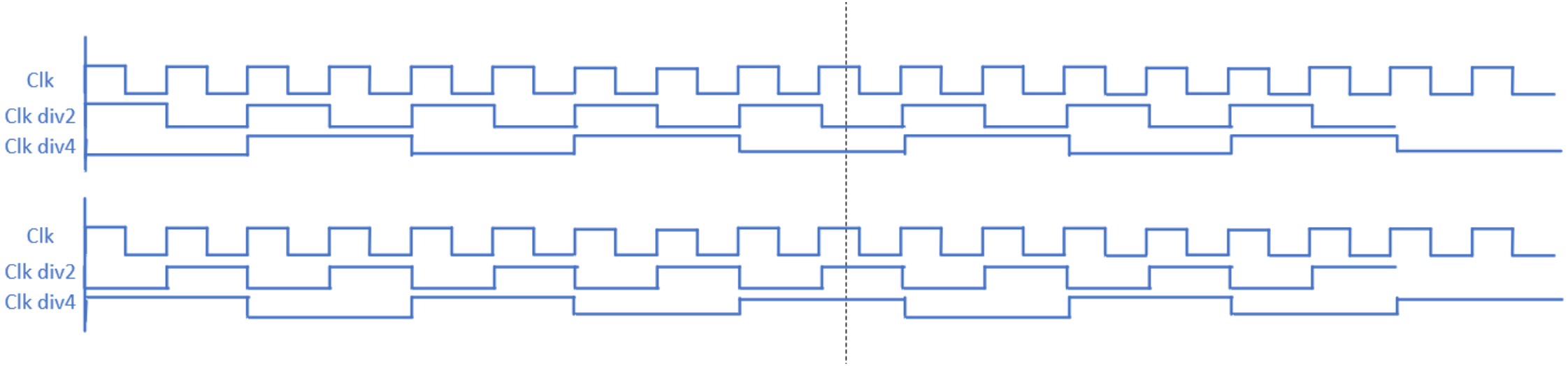
fixed latency



CDR clock & Digital system clock

If we need to phase shift using our phase shift function to align the 40 MHz clock of the CDR, it is necessary to ensure that after reset, the clock behaviors of the two frequencies remain consistent.

Example:



MSB output

We must align the bit order of the digital and analog Ser&Des.