The development of FEDA

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Outline

- Background
- FEDA Chip: Requirements & Overall Block Diagram
- FEDA_v1 Chip : Overall Block Diagram
- FEDA_v1 Chip : Core Module Design
- FEDA_v1 Chip : Layout and Simulation
- Summary and Plan

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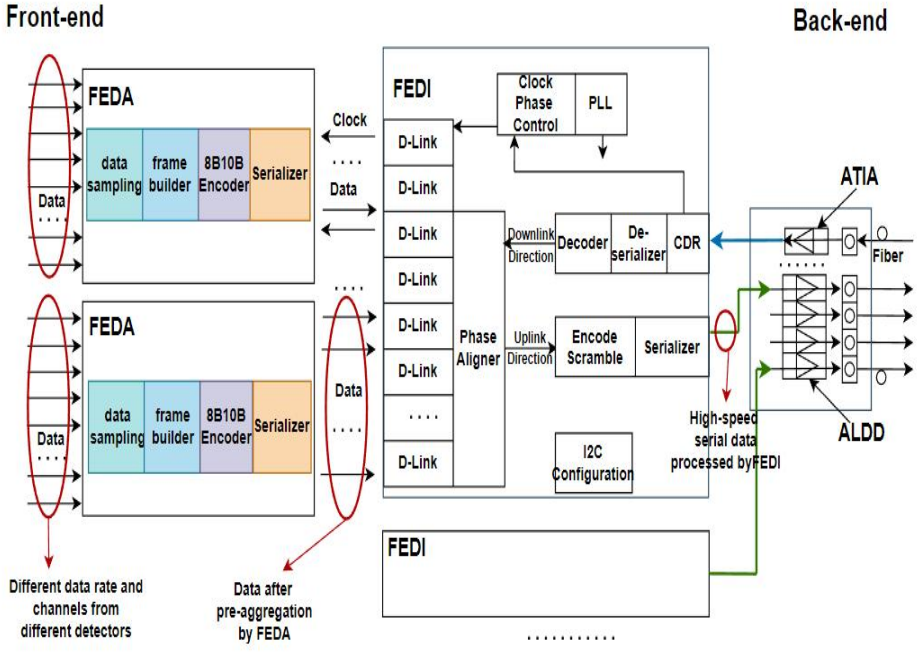
Background



- This project focuses on the requirements of **CEPC (Circular Electron-Positron Collider)** in high-energy physics, developing **a general-purpose bidirectional high-speed data transmission system** to solve the problem of efficient acquisition and transmission of multi-source data in the CEPC detection system.

- Within the system's overall framework, frontend data—with varying rates from different channels—is sent to the backend through this data link system; this is what we call **uplink transmission**. At the same time, clock signals, trigger signals, and configuration signals are also sent to the frontend through this system, which we refer to as **downlink transmission.**

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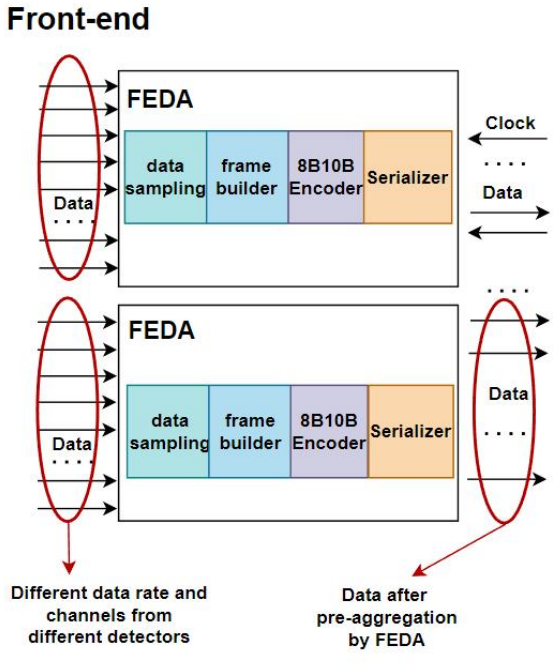
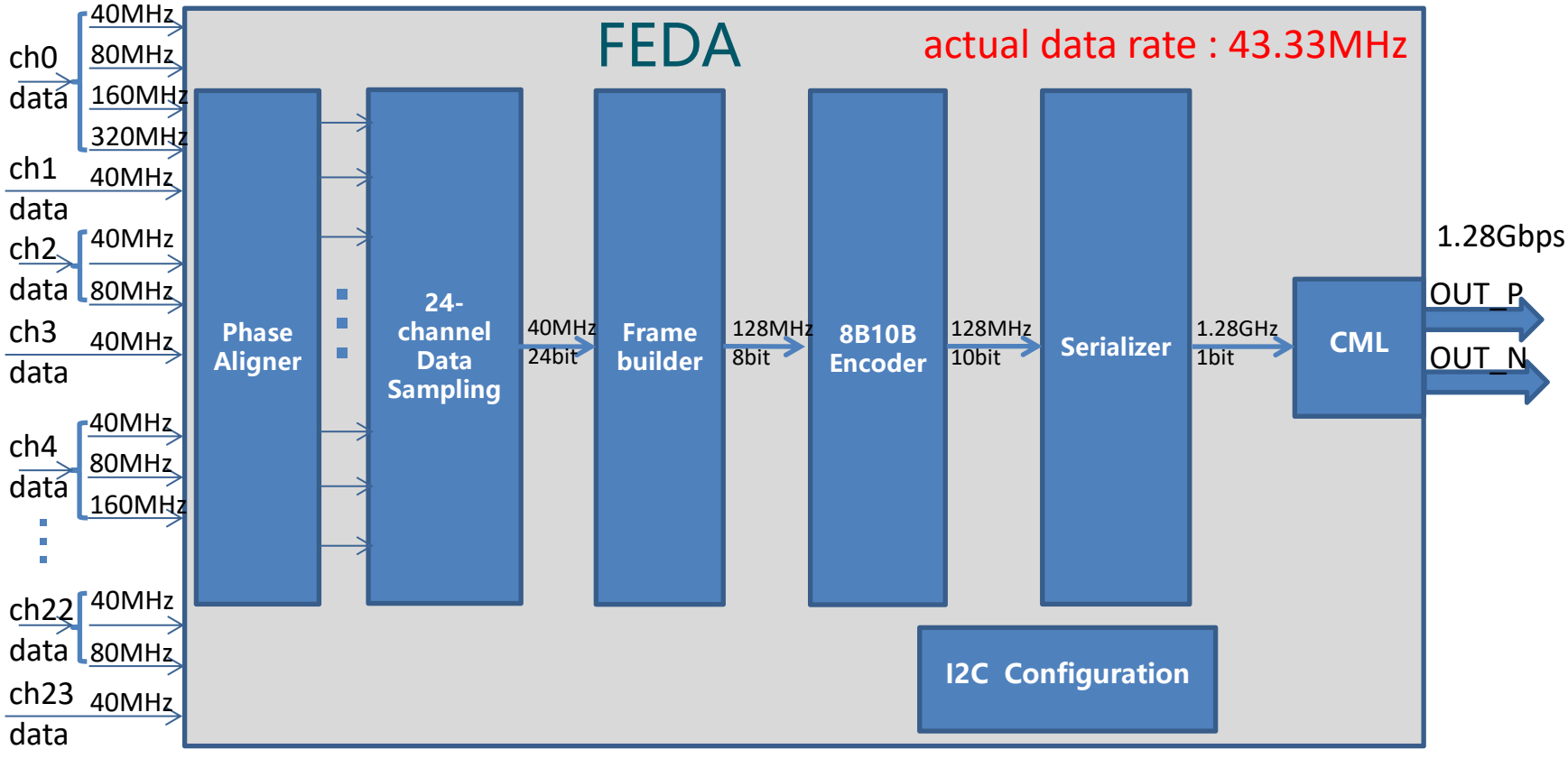
FEDA Chip: Requirements & Overall Block Diagram



- To meet this core need, the Front-End Data Aggregator(FEDA) chip we designed plays an important role in data processing: it collects data of **different rates** (40 MHz, 80 MHz, 160 MHz, 320 MHz) from **various frontend detectors**. After gathering this data, it finally outputs data at a rate of **1.28 Gbps**—providing a stable data stream for the backend's high-speed data transmission link.

FEDA Chip: Requirements & Overall Block Diagram



The FEDA Chip design is mainly composed of seven core modules: Phase aligner,24-channel Data Sampling, Frame Builder, 8B10B Encoder, Serializer,CML Driver and I2C Configuration.

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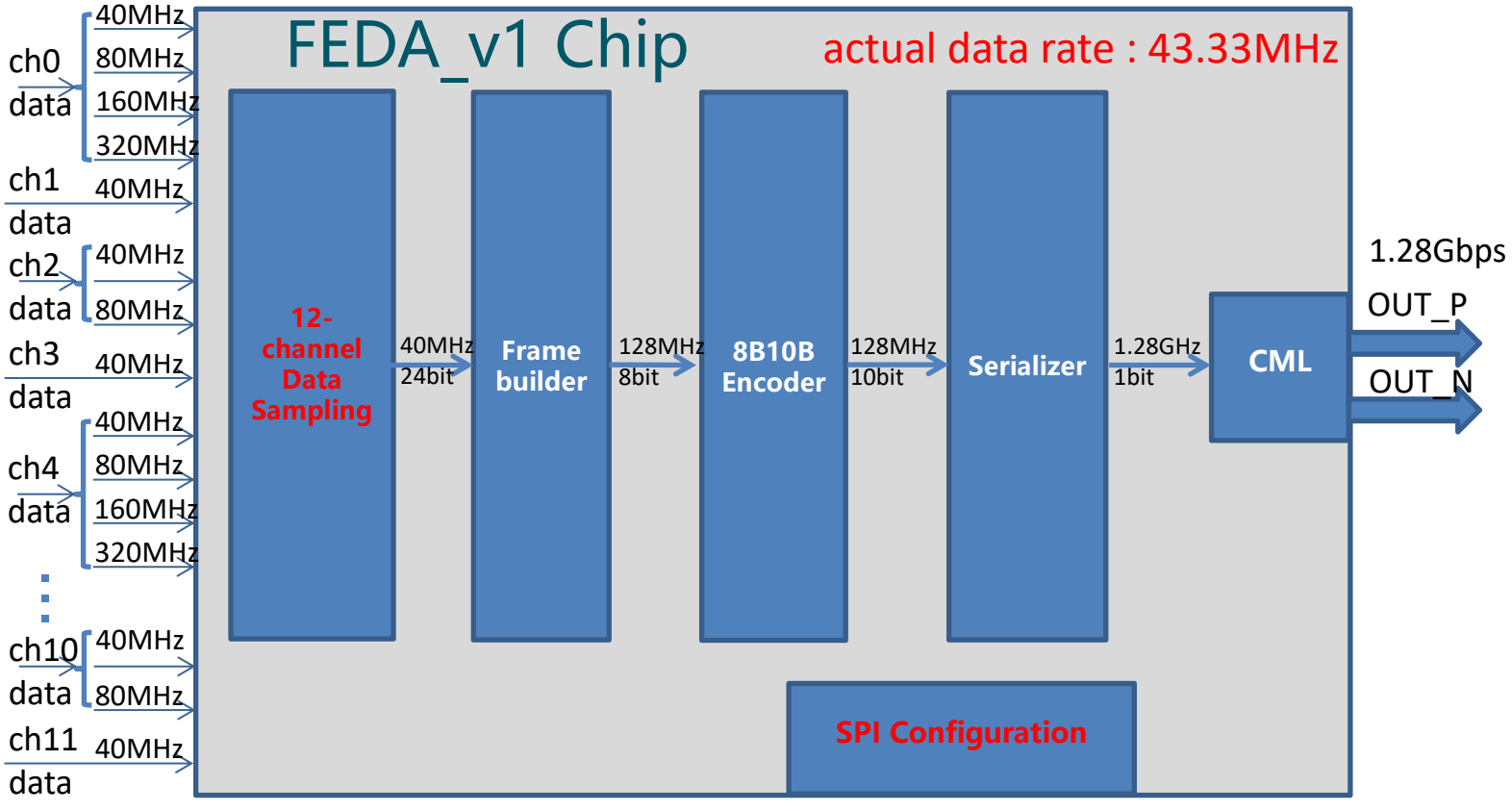
FEDA_v1 Chip : Overall Block Diagram



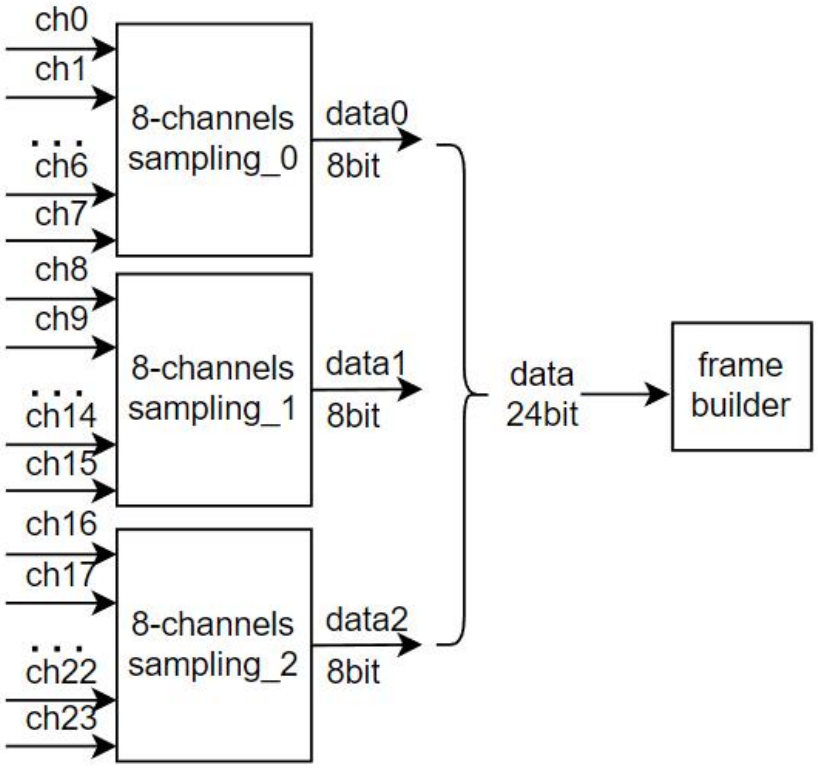
The FEDA_v1 Chip design is mainly composed of **six** core modules: **12-channel Data Sampling**, Frame Builder, 8B10B Encoder,Serializer,CML Driver and **SPI Configuration**.

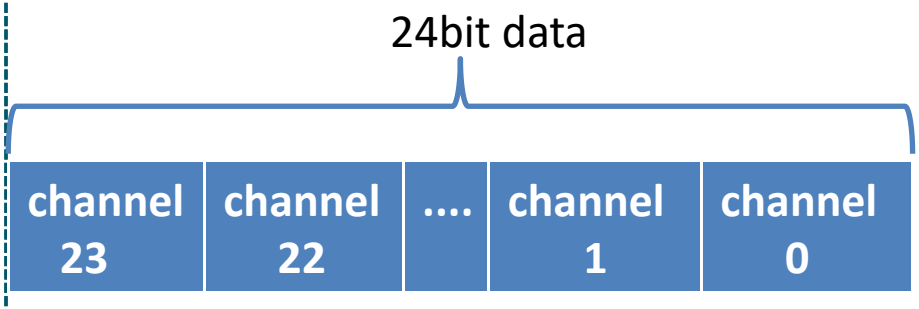
FEDA_v1 Chip : Overall Block Diagram

Differences Between the FEDA_v1 Chip and the Final FEDA Chip:

- **Data Input Channels**: In the first version uses **12 data input channels**, while the final version will have **24 data input channels**.
- **Configuration Interface**: The first version uses **SPI configuration**, while the final version will use **I2C configuration**.
- **Phase Alignment Function**: The FEDA_v1 Chip didn't employ phase alignment; while the final FEDA chip will add **phase alignment** before data sampling.

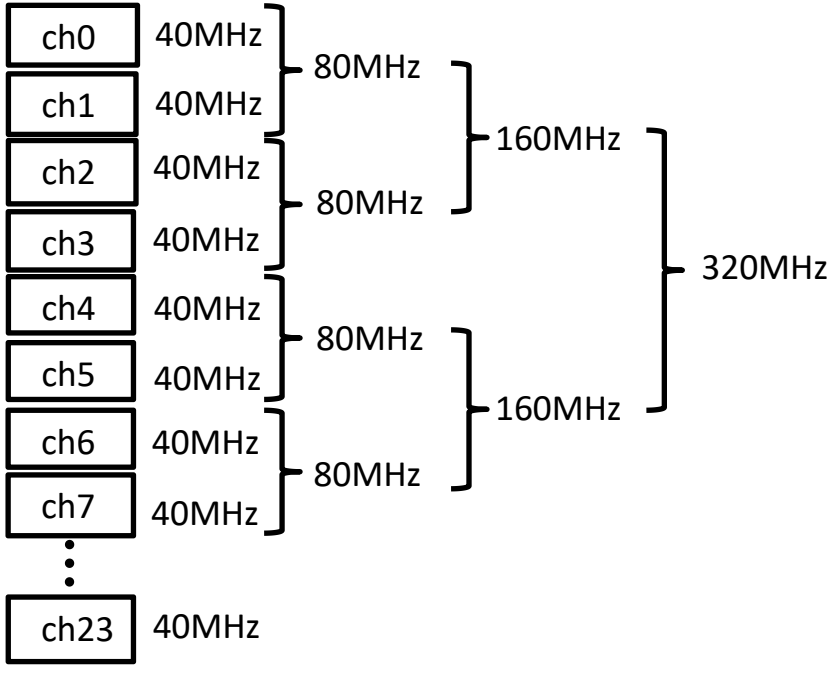
FEDA Chip : 24-channel Data Sampling





As we all know, the FEDA chip has an output rate of **1.28 Gbps** and an input frequency of 40 MHz. Calculations show it can support a maximum of 32 channels; however, we adopted **24-channel input** in the final design to account for **DC balance** and so on. In the sampling module, 24-channel data is sampled every 40 MHz cycle to ensure data integrity and timing consistency.

FEDA Chip : 24-channel Data Sampling



The 24 input channels can be divided into 3 independent 8-channel units (i.e., Channels 0-7, 8-15, 16-23). The input rate analysis of Channels 0-7 can be directly reused for the other two 8-channel units.

the 24-channel input of the FEDA supports multiple channel rate configurations—it works with both single-rate and mixed-rate configurations.

Configuration Type	Specific Configurations
Single-rate Configuration	- 40 MHz x 24 channels
	- 80 MHz x 12 channels
	- 160 MHz x 6 channels
	- 320 MHz x 3 channels
Mixed-rate Configuration	e.g.,320 MHz × 1 channel + 160 MHz × 2 channels + 80 MHz × 2 channels + 40 MHz × 4 channels

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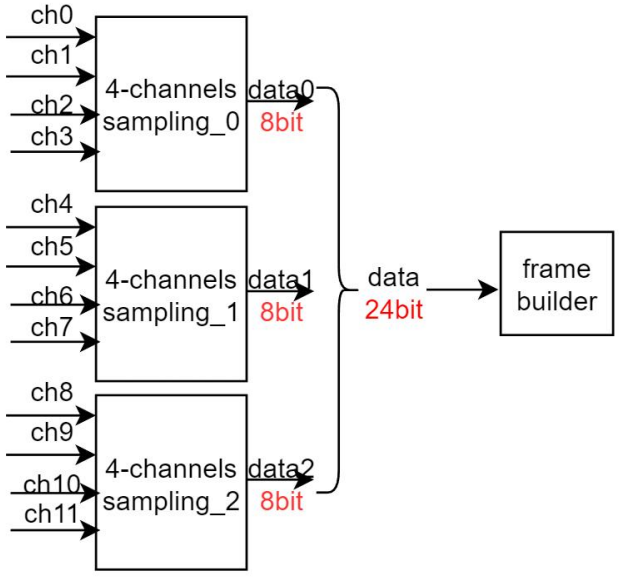
FEDA_v1 Chip : Core Module Design

(1) 12-channel Data Sampling:



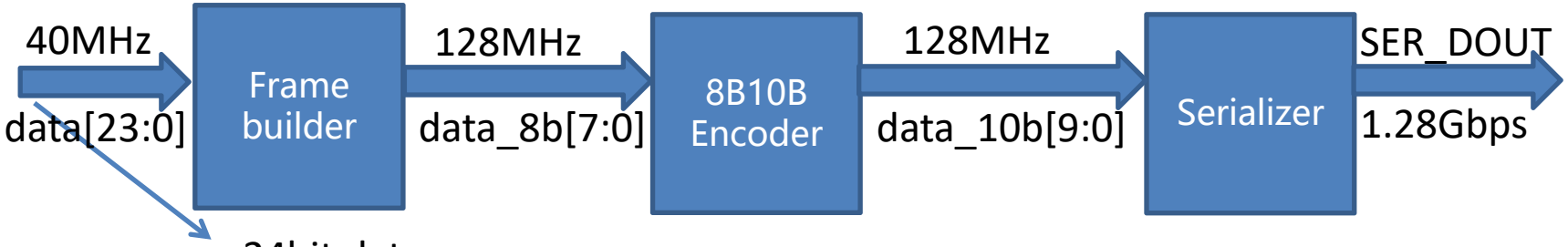
24bit data

4'b10 10	ch 11	ch 10	ch 9	ch 8	...	4'b10 10	ch 3	ch 2	ch 1	ch 0

- The output bit width of both the 12-channel data sampling in the first version (V1) and the 24-channel data sampling is 24 bits, which ensures a consistent frame format. for each 8-bit group, the **upper 4 bits use a fixed input of 4'b1010**, and the **lower 4 bits are channel sampling values**;
- **Advantages**:fewer channels mean **fewer PADs**, a smaller chip area, and lower costs;
- **Compatibility**: **No modification** to the **frame format** is required for the V2 version, enabling direct expansion to 24 channels and reserving good compatibility for project iteration.

FEDA_v1 Chip : Core Module Design

(2) Frame Builder:



channel23	channel22	....	channel1	channel0

The position of 24-channel data in the frame format is **fixed**, eliminating the need to waste 5-bit channel addresses for marking 1-bit data.

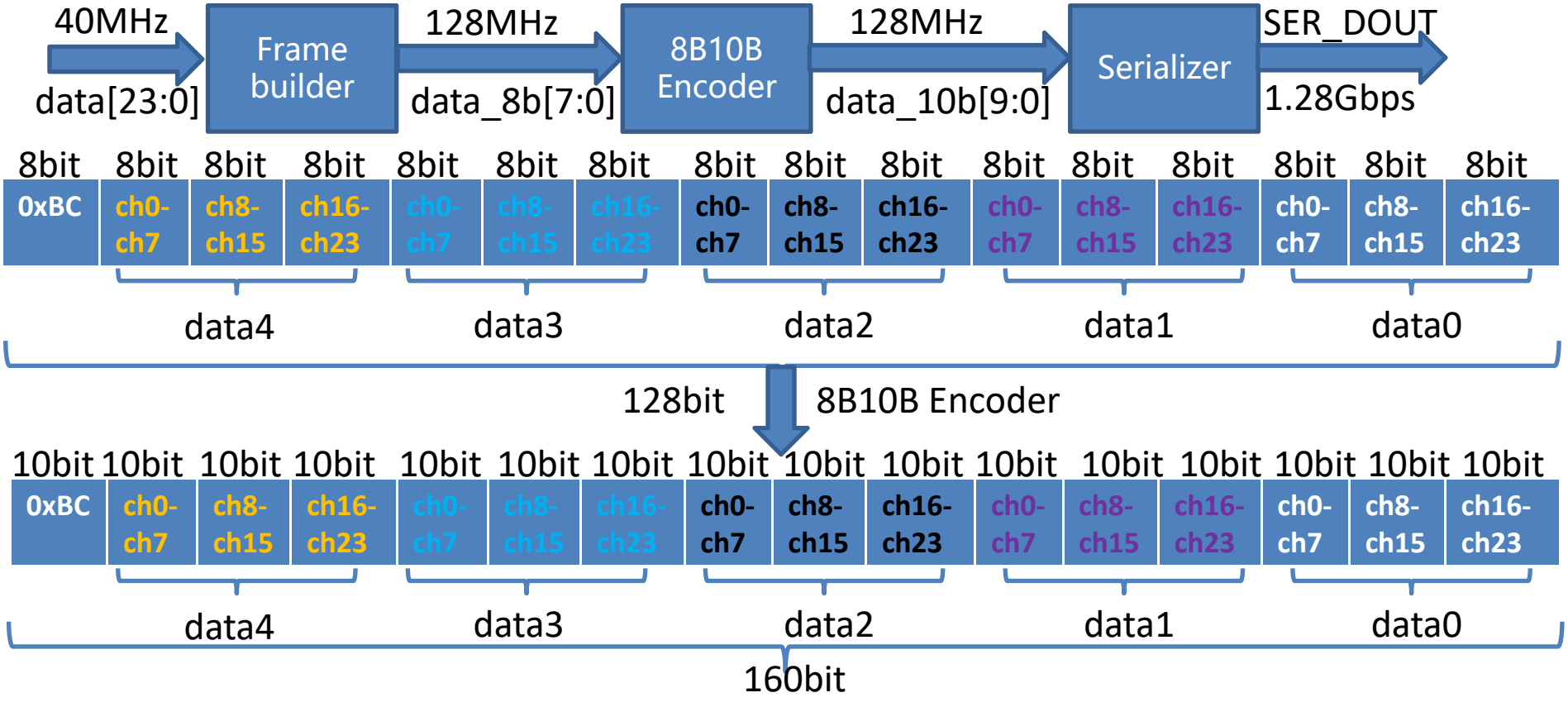
8'hBC	data0	data1	data2	data3	data4
8bit	24bit	24bit	24bit	24bit	24bit

data_8b_0[7:0]	data_8b_1[7:0]	.....	data_8b_14[7:0]	data_8b_15[7:0]

Composition of One Frame: 8-bit frame header + 5 × 24-bit input data (din) = 128 bits = 8 bits × 16.

FEDA_v1 Chip : Core Module Design

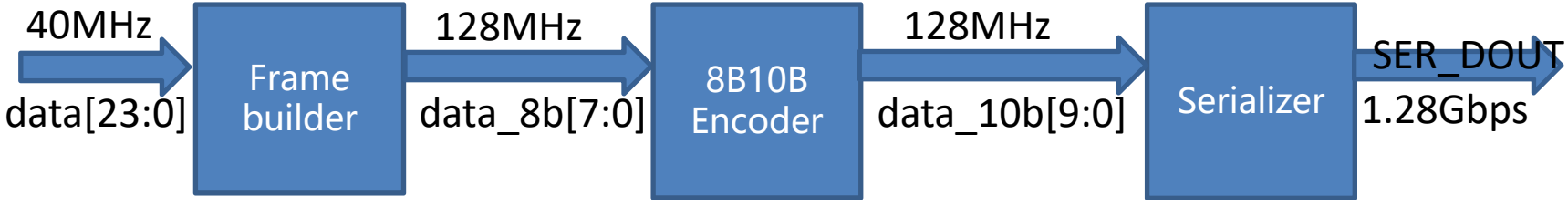
(3) 8B10B Encoder:

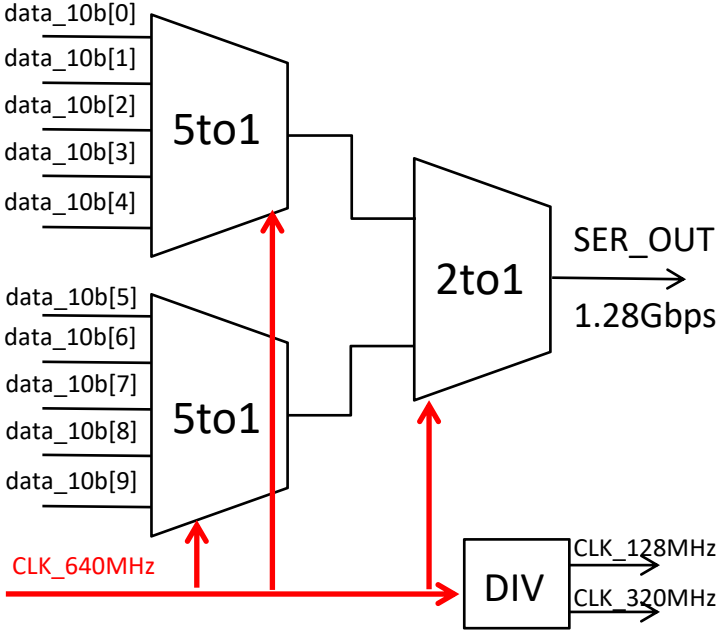


Purpose: We use 8B10B encoding mainly to ensure **DC balance**—this keeps the number of "0"s and "1"s in the signal balanced over the long run, which is key for stable transmission.

FEDA_v1 Chip : Core Module Design

(4) Serializer:





Core Functions:

①it serializes the frontend 10-bit parallel data, achieving a final output rate of 1.28 Gbps with **LSB first**;

②it performs frequency division on the 640 MHz clock to generate **128 MHz** and **320 MHz** clocks for the frontend modules, ensuring that all clocks in the system are in-phase.

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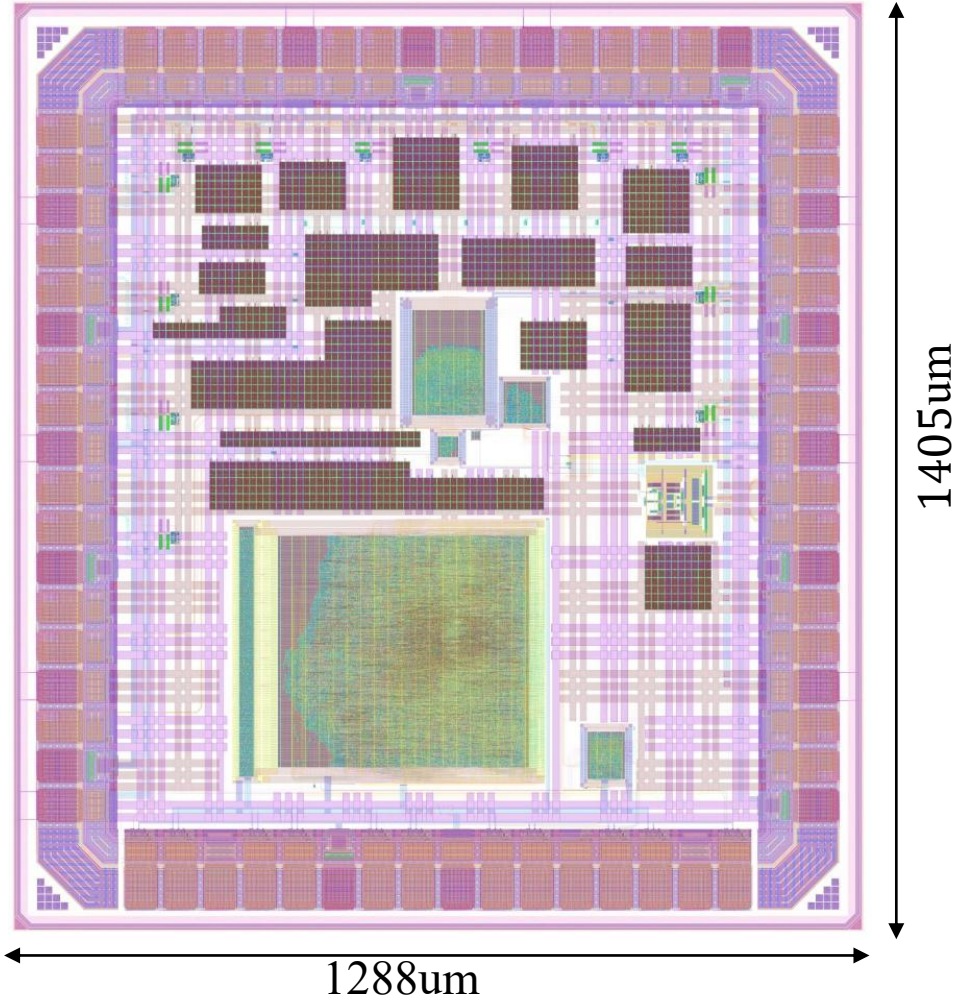


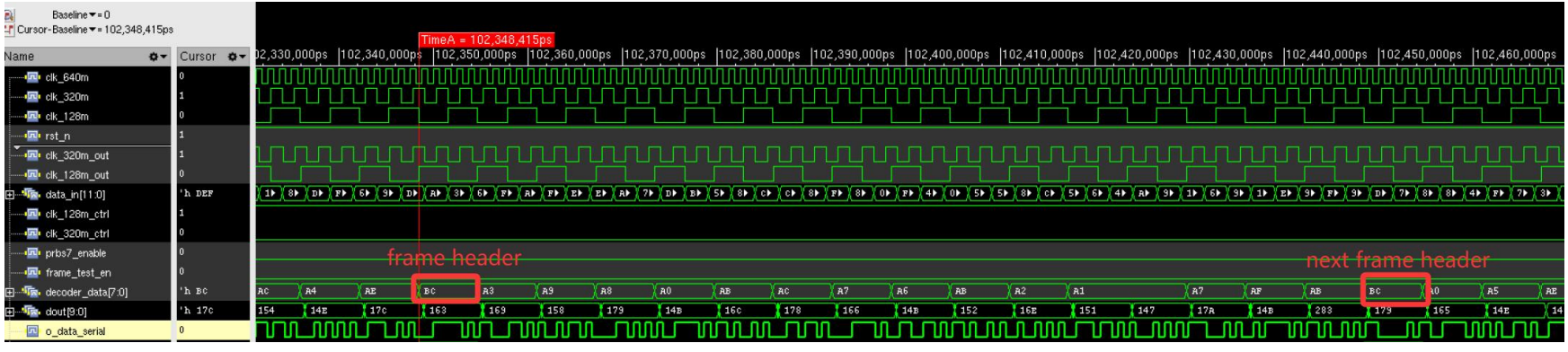
Key Chip Specifications:

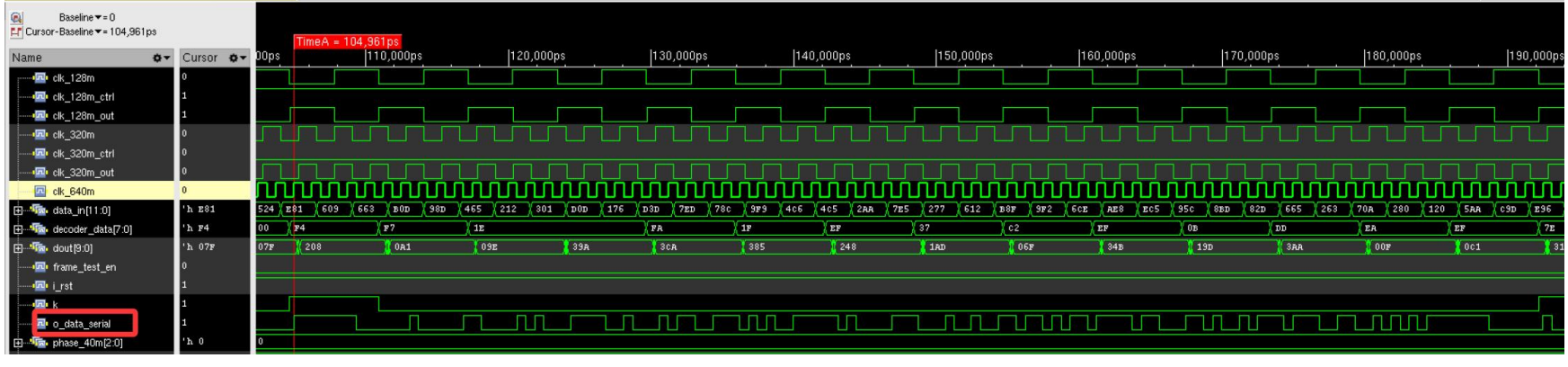
- **Process：** SMIC55nm
- **Chip Area：** 1288um×1405um
- **Voltage：** 1.2V

FEDA_v1 Chip : Layout and Simulation

simulation①: Post-Layout Digital Post-Simulation

- Tool: Nclaunch
- Process: By feeding the encoded output into a decoder, we successfully got the **right frame format**.



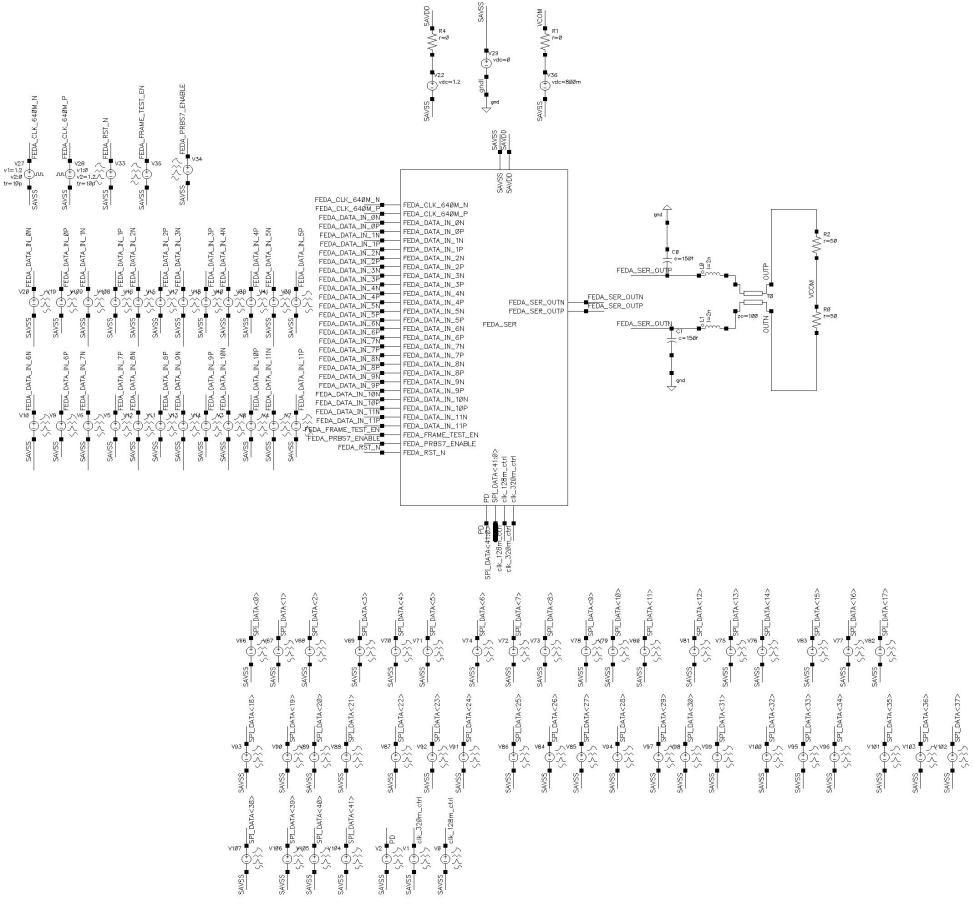


We also checked the serial data output under **PRBS7 pseudo-random numbers**—and it matched the XOR relationship of pseudo-random numbers.

FEDA_v1 Chip : Layout and Simulation

simulation②:Post-Simulation with Transmission Line Model

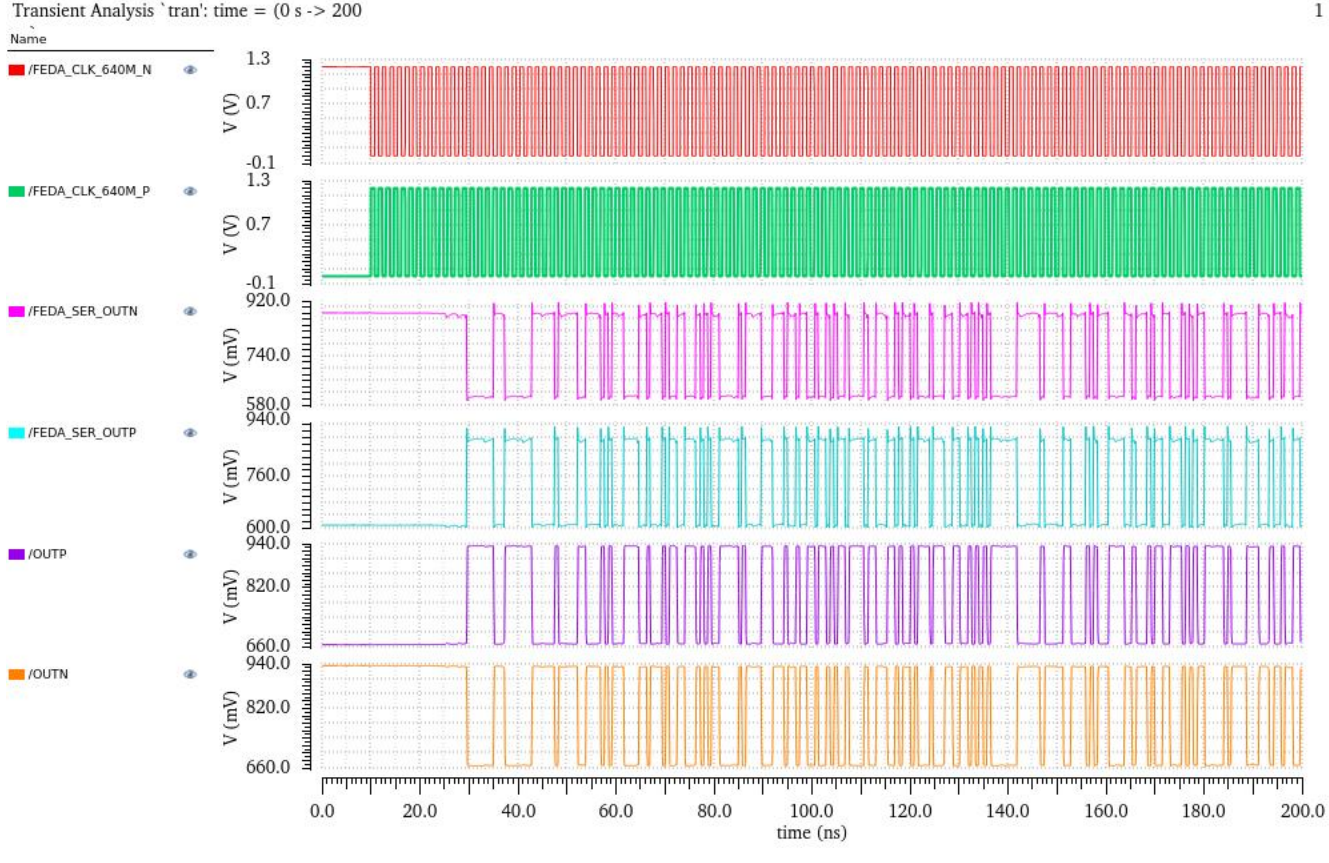
- Tool: Virtuoso
- Process: added a transmission line model to the Test Bench for the simulation.



FEDA_v1 Chip : Layout and Simulation

simulation②:Post-Simulation with Transmission Line Model

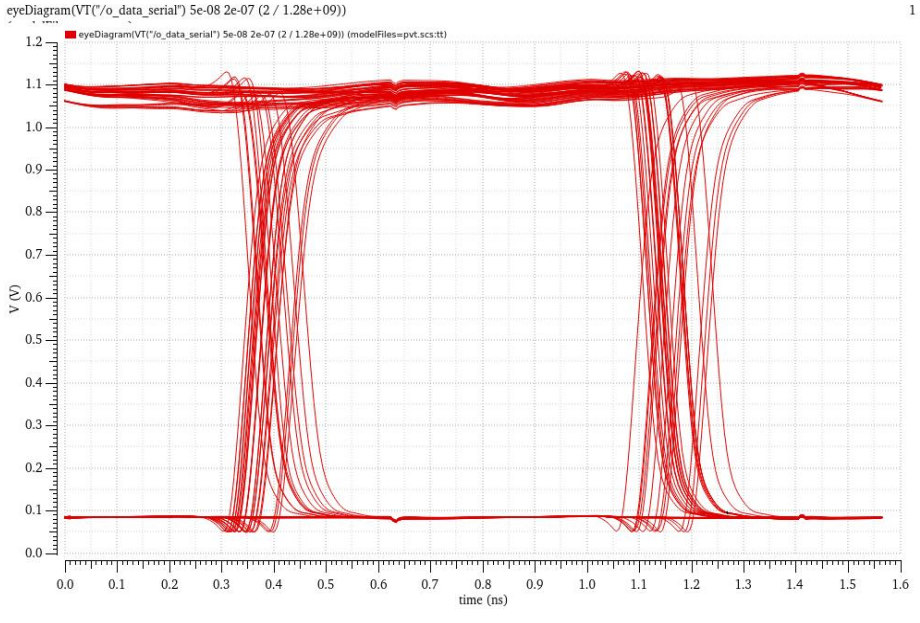
- Output Signals: Under PRBS7 pseudo-random number mode, The output waveforms of the chip and the transmission line model are as follows.



FEDA_v1 Chip : Layout and Simulation

simulation②:Post-Simulation with Transmission Line Model

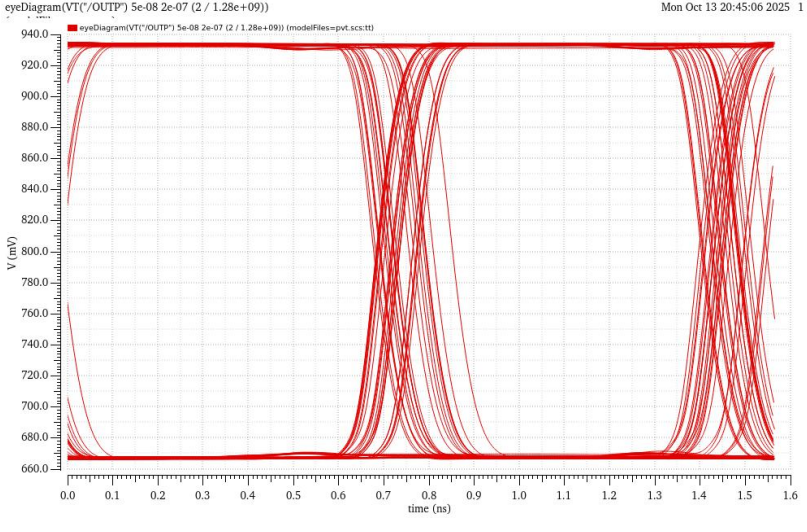
Eye Diagrams: Eye diagrams of the "o_data_serial" signal output by the Serializer in the design:



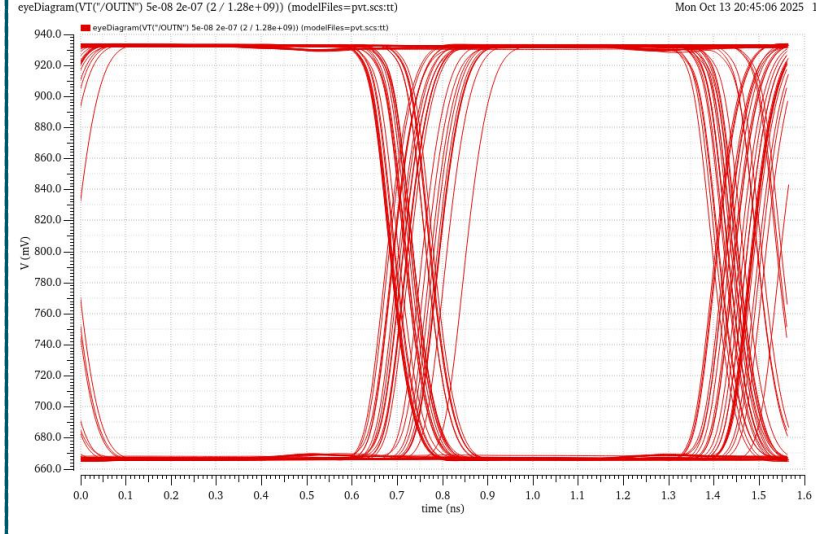
o_data_serial eye diagram

FEDA_v1 Chip : Layout and Simulation

simulation②:Post-Simulation with Transmission Line Model
Eye Diagrams: Eye diagrams of the "OUTP" and “OUTN” signal output by the Transmission Line Model:



OUTP eye diagram



OUTN eye diagram

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Summary

- The first version (V1) of the FEDA chip has completed design and been submitted to the foundry for **tape-out**.

Future Plans

- **Before chip return**: Complete the design of the test PCB board and firmware configuration of the test system.
- **After chip return**: Immediately initiate chip testing to verify key performance indicators (e.g., data rate, transmission stability).
- **Looking ahead**: The current first version uses 12 data input channels. The second version will focus on **expanding the channel count to 24**, improving the stability of the data sampling module, and making targeted improvements based on V1 test results.

Ending

Thanks for your attention!