The Development of High-Speed TIA and VCSEL Driver ASICs for Optical Data Transmission in HEP

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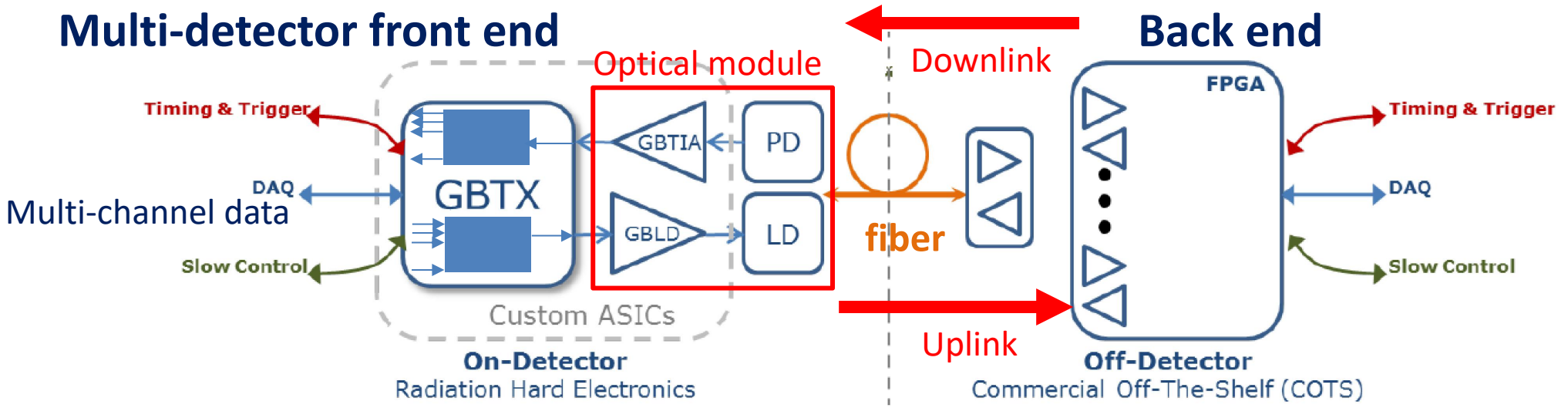
1、Project Background

2、ATIA (Array Transimpedance Amplifier ASIC)

3、ALDD (Array Laser Driver ASIC)

4、Summary

A typical optical data transmission system by CERN for HEP

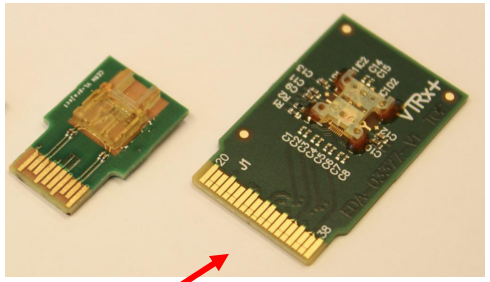


Optical Data Transmission System (Versatile Link) by CERN

- Versatile Link: A high-speed bi-directional optical data transmission system developed by CERN for the HEP applications.

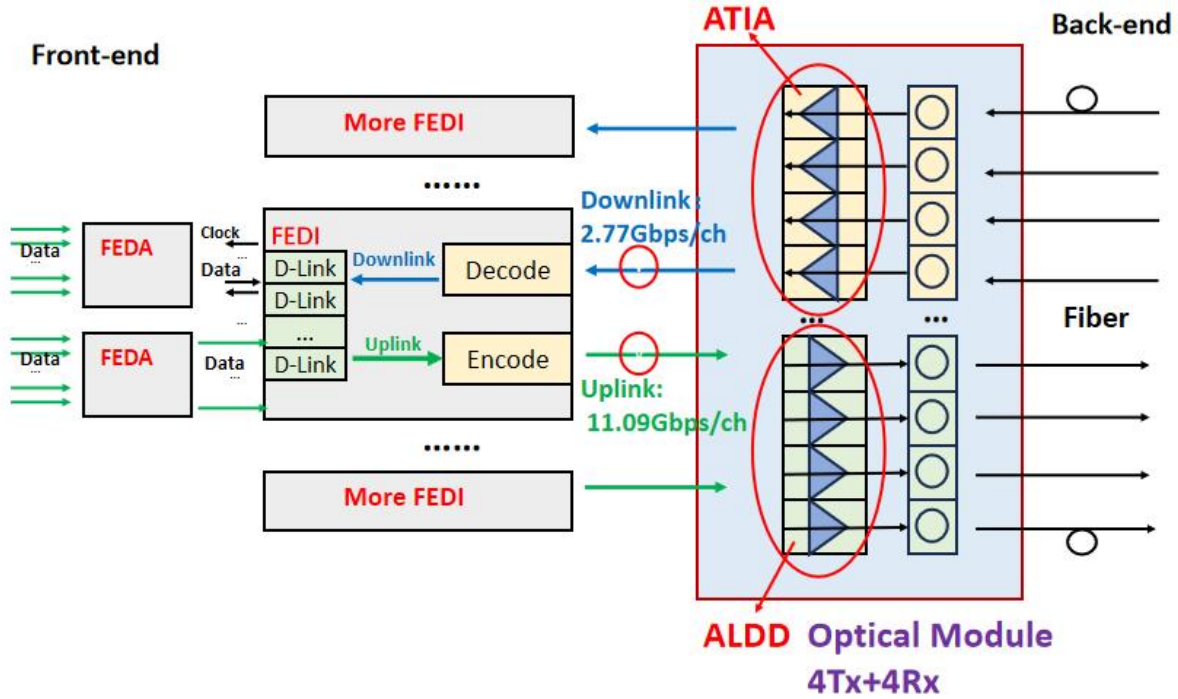
  It includes the following key ASICs:

  - GBTx： Bidirectional data interface chip
  - GBTIA: **Transimpedance Amplifier ASIC**
  - GBLD： **Laser Driver ASIC**



Integrated in the optical module

The optical data transmission system in CEPC



Optical Data Transmission System for CEPC

- The optical data transmission system for CEPC is under development. This system includes the following key ASICS:
- FEDA and FEDI: Data processing ASICs
- ATIA： **4 x 2.77 Gbps/ch Array Transimpedance Amplifier ASIC**
- ALDD: **4 x 11.09 Gbps/chArray Laser Driver ASIC**

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3、ALDD (Array Laser Driver ASIC)

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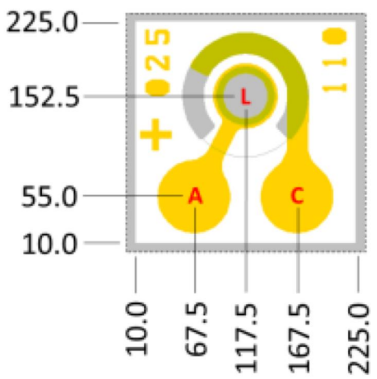
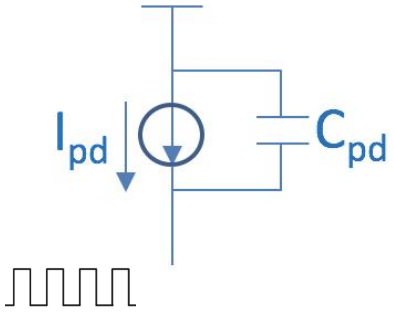
The principle of Photodiode (PD) and ATIA ASIC

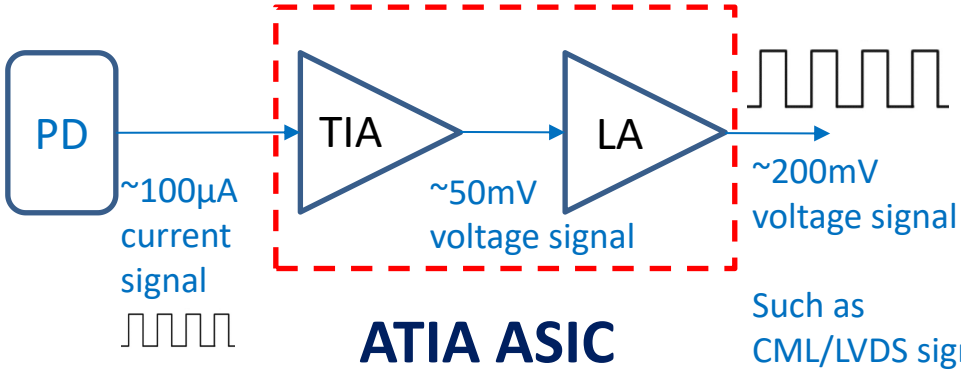


Photodiode chip



The electrical model of PD

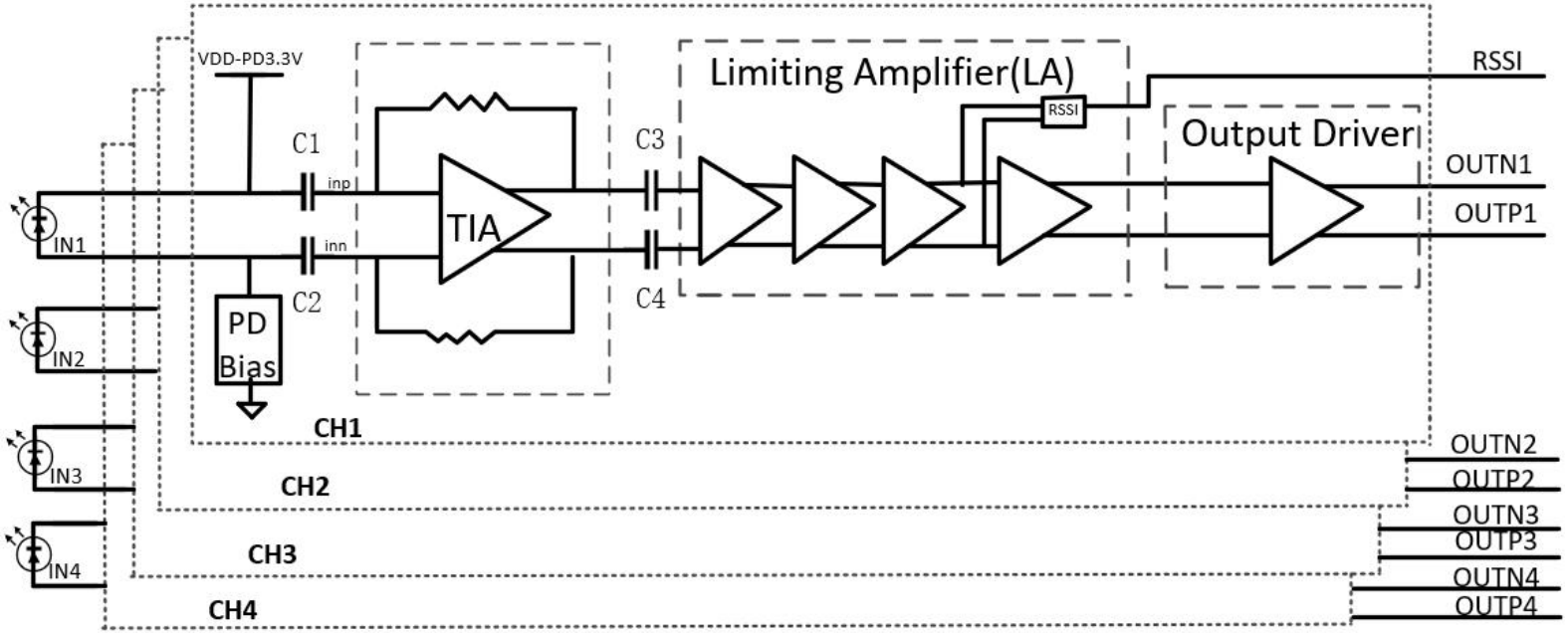
- Photoelectric Diode (PD) chip:
  - Receives optical signal, outputs corresponding current signal.
  - Electrical model of the PD
  - Commercially available



ATIA ASIC

- ATIA: Receives and amplifies the current signal from the PD
  - Input: ~100 uA amplitude , 2.77 Gbps current signal
  - Output: Diff p-p 400mV signals (CML)
  - Includes two core parts: TIA + LA

Overall block diagram of ATIA ASIC



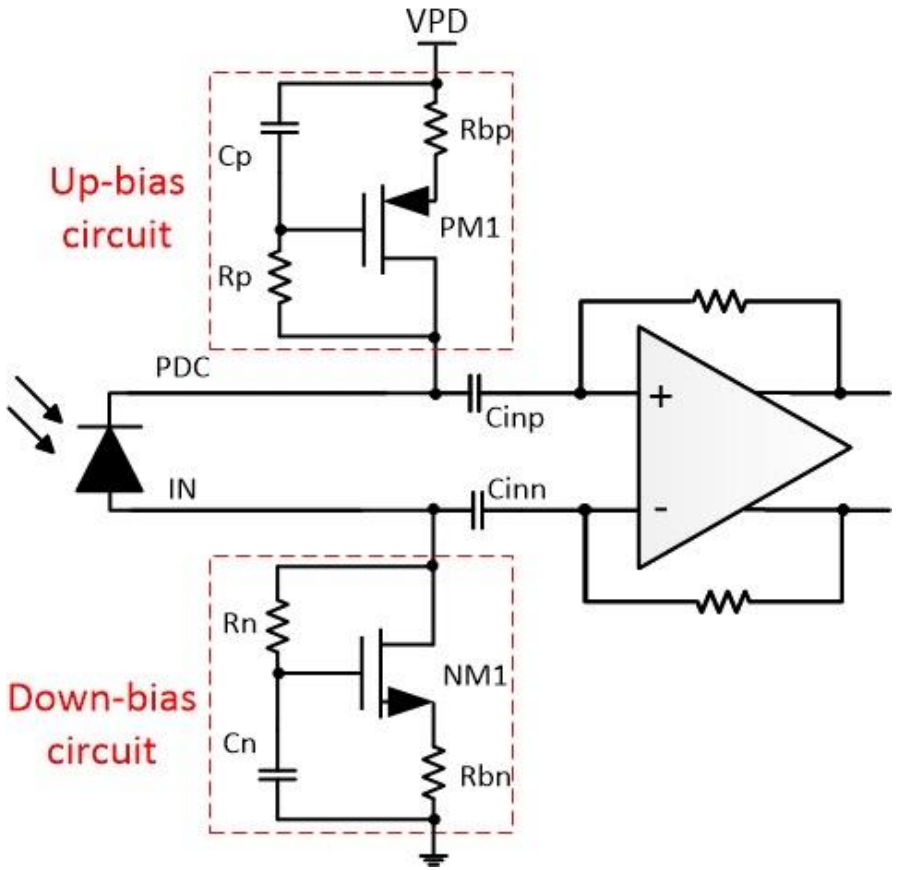
Block Diagram of ATIA ASIC

- ATIA is a 4 x 2.77 Gbps/ch transimpedance amplifier AISC, including:
  - PD Bias
  - ATIA core and LA stages
  - Output Driver
- Overall gain: 75 dB ohm
- Output differential p-p 400 mV signals with configurable pre-emphasis.

Parameter	Design indicators
Bit rate	2.77 Gbps
Photodiode capacitance	200fF to 2pF
High cut-off frequency	2 GHz
Low cut-off frequency	<1 MHz
Sensitivity for BER=10-12	20 uA p-p(-17dBm)
Transimpedance gain	75 dB ohm
Output differential p-p voltage	≥400 mV(50 ohm)
PD bias supply voltage	3.3V
Circuit supply voltage	1.2V
Power consumption	<100 mW/ch
Total jitter	0.085 UI(<34ps@2.77Gbps)

ATIA Specification

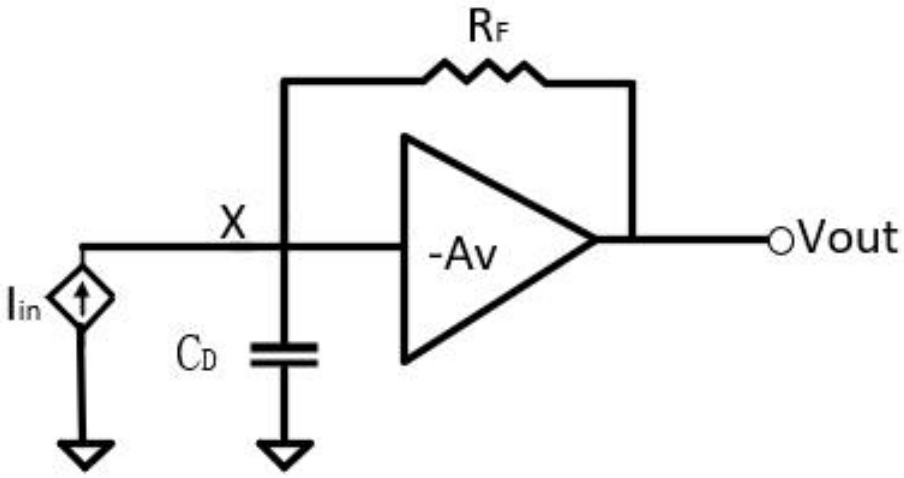
PD Bias structure and principle



PD Bias structure

- AC coupling connects to PD for the differential ATIA core.
- Larger AC impedance of RBIAS :
  - Increase the transconductance of ATIA.
  - Decrease the low cut-off frequency.
- Smaller DC impedance of RBIAS:
  - Keep the voltage across the PD.
  - Make sure high speed, low noise.
- RBIAS is designed by active devices (PMOS and NMOS with source degeneration) and can be much large and adjustable by frequency.

ATIA core requirements



ATIA core

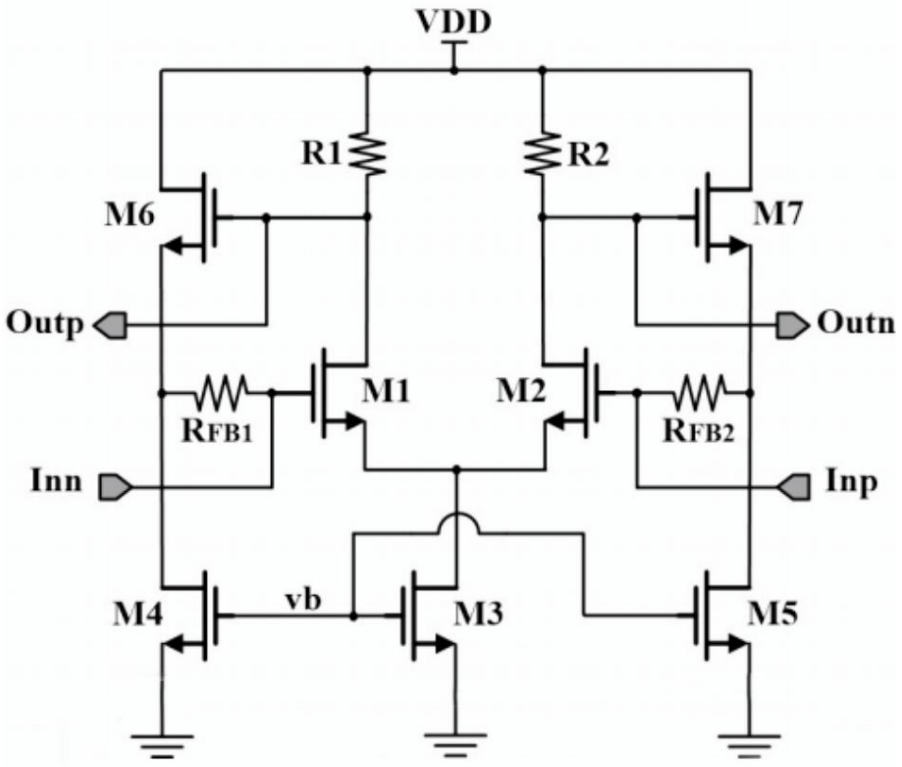
$$R_{in(s)-TIA} = -\frac{R_F}{A_V+1}\cdot\frac{1}{1+s\frac{R_F C_D}{1+A_V}}$$

$$BW = \frac{1}{2\pi}\cdot\frac{1+A_V}{R_F C_D}$$

$$i_{n,in}^2 = \frac{4kT}{R_F} + \frac{4kT\Gamma}{R_F^2}\left(\frac{1}{g_m} + \frac{(2\pi R_F C_D)^2}{g_m} f^2\right)$$

- Feedback ATIA core.
- Low noise requires:
  - Large feedback resistor.
  - Large amplifier transconductance.
  - Small input node capacitance.
- High bandwidth requires:
  - Small feedback resistor.
  - Large amplifier open loop gain.
  - Small input node capacitance.

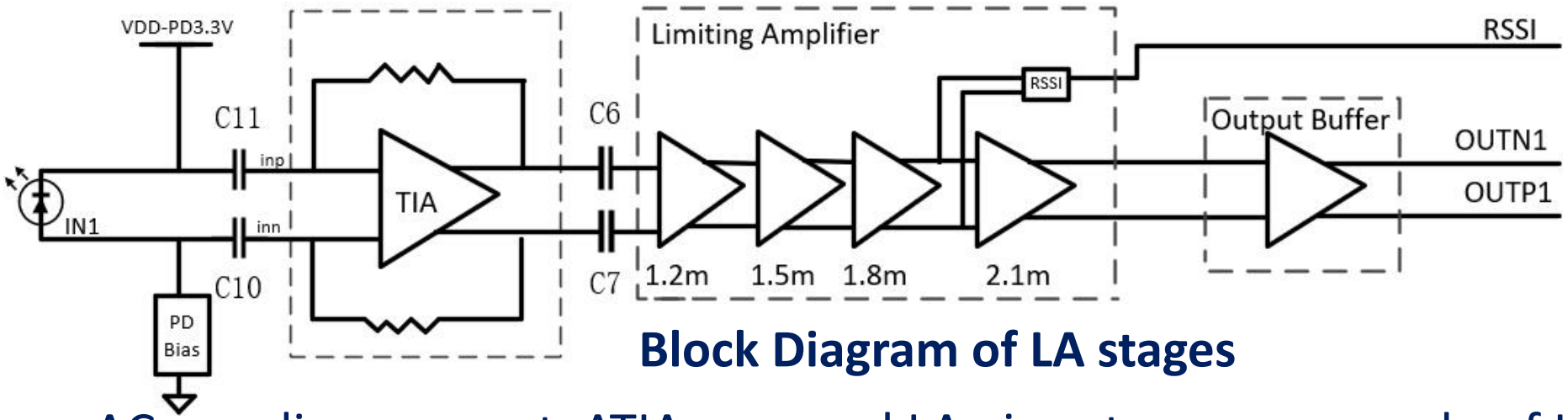
ATIA core



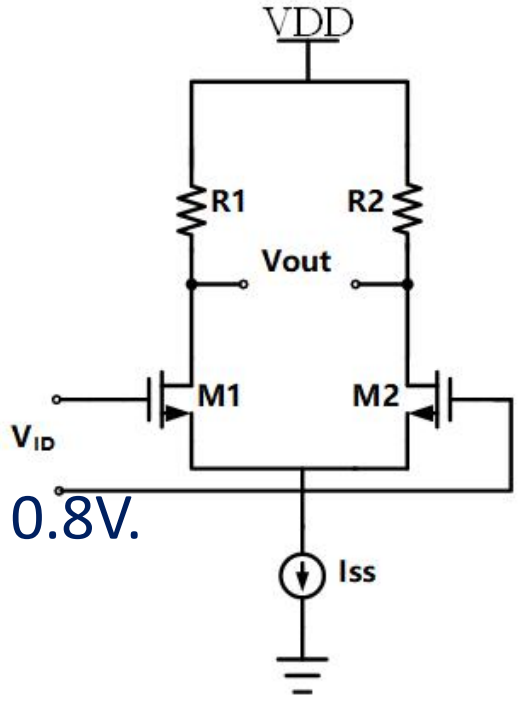
ATIA core structure

- Fully differential, common-source structure
- Feedback resistors (R_{FB}): adjust the transimpedance gain and bandwidth.
- The open loop gain of the first stage: ~ 3 (9 dB).
- 1.2 V supply required.

LA stages



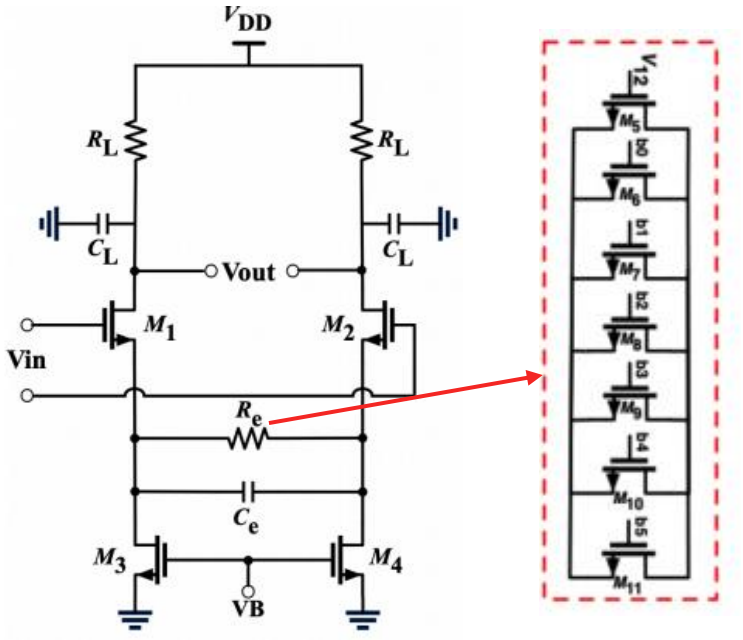
Block Diagram of LA stages



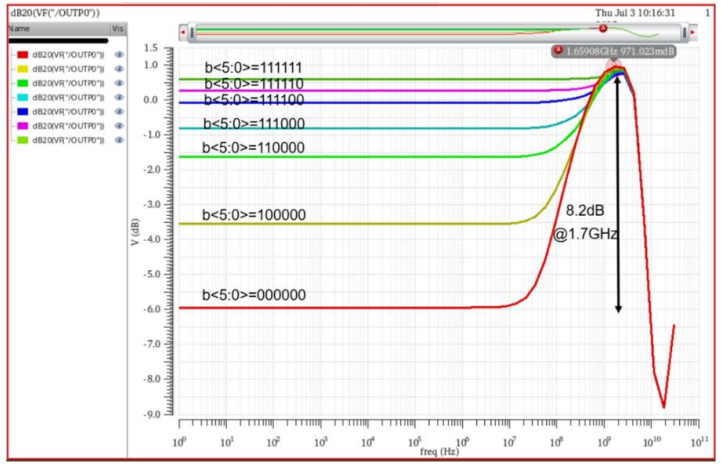
LA structure

- AC coupling connect ATIA core and LA, input common mode of LA is 0.8V.
- The bias current of the LA increases proportionally.
- The overall bandwidth of LA can reach 4 GHz and its gain is 30 ~ 40 dB.
- SMIC 55nm CMOS technology is enough to meet the LA bandwidth requirement of 2.77Gbps,so we did not design a complex circuit structure.

Output Driver



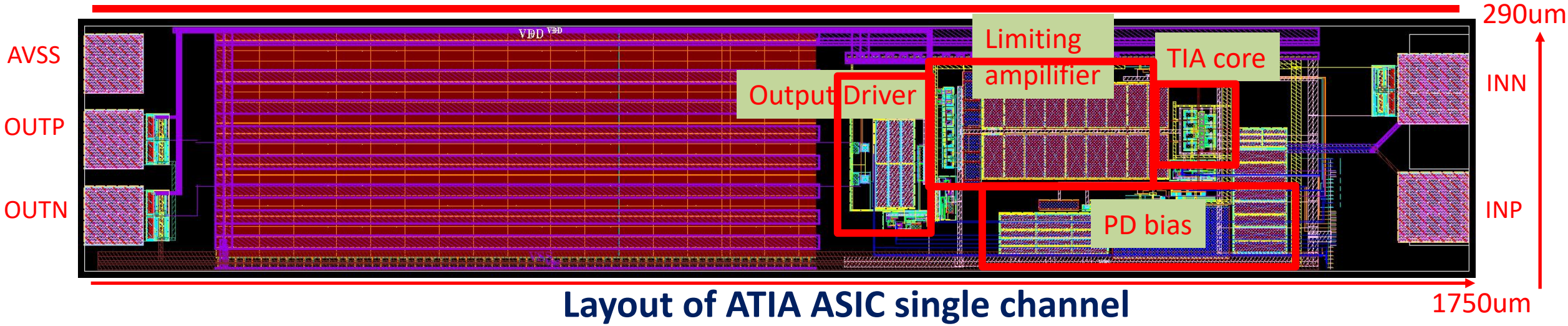
Output Driver structure



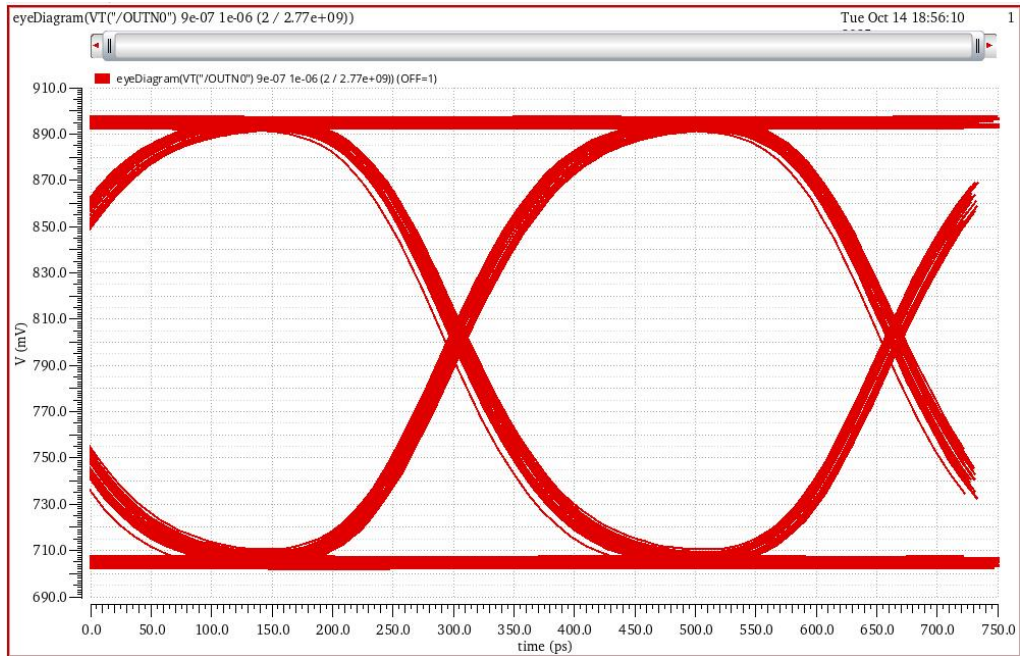
Peaking Strength

- Output driver is a CML driver with CTLE (Continuous-Time Linear Equalizer) structure to give configurable pre-emphasis function .
  - Configurable R implemented with 6 NMOS controlled by SPI
  - Peaking Strength: 0~8.2 dB @1.7 GHz
- The Output amplitude can be adjusted by the programmable biasing current.
  - Output amplitude: dif p-p 140 mV ~ 600mV
- Output impedance 50Ω for impedance match.

Layout of the ATIA ASIC single channel



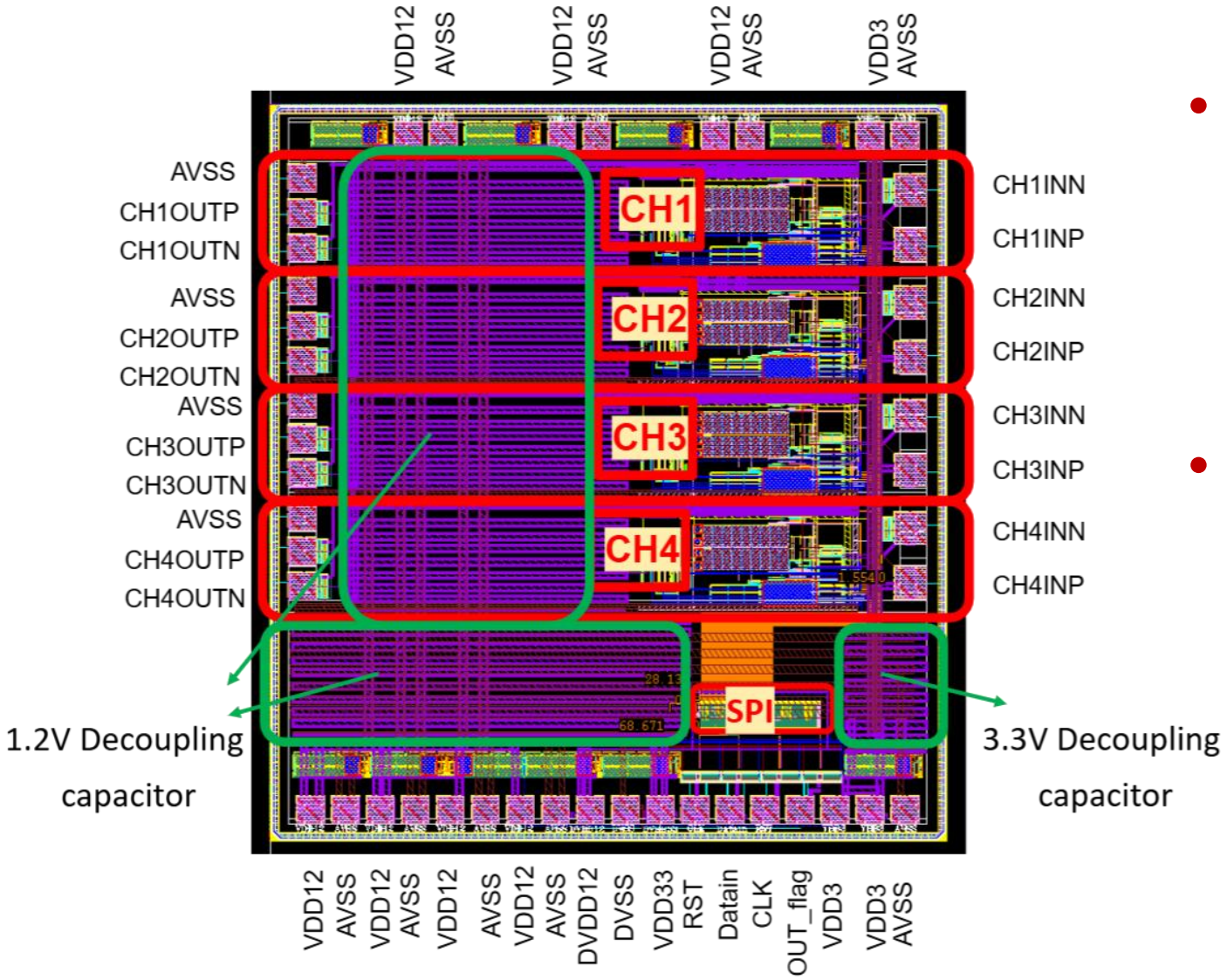
Layout of ATIA ASIC single channel



eye diagram of ATIA ASIC single channel

- Based on SMIC 55nm CMOS technology
- The size of the single channel is 1750 × 290 um.
- The left figure shows the post-simulation eye diagram of a single channel @ 2.77 Gbps

ATIA ASIC overall layout



Overall layout of 4 x 2.77 Gbps/ch ATIA ASIC

- The size of the ATIA ASIC is 1750×1900 um.
- This ASIC has been taped out in Oct 2025 and is expected to be returned for testing in Jan 2026.

1、Project Background

2、ATIA (Array Transimpedance Amplifier ASIC)

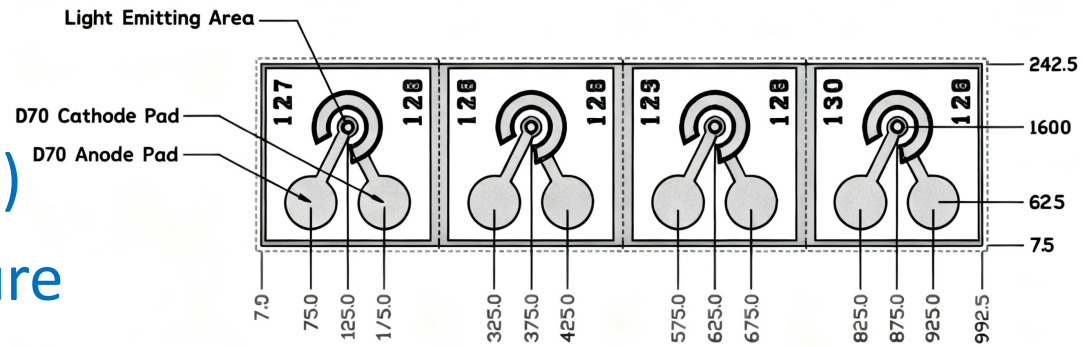
3、ALDD (Array Laser Driver ASIC)

4、Summary

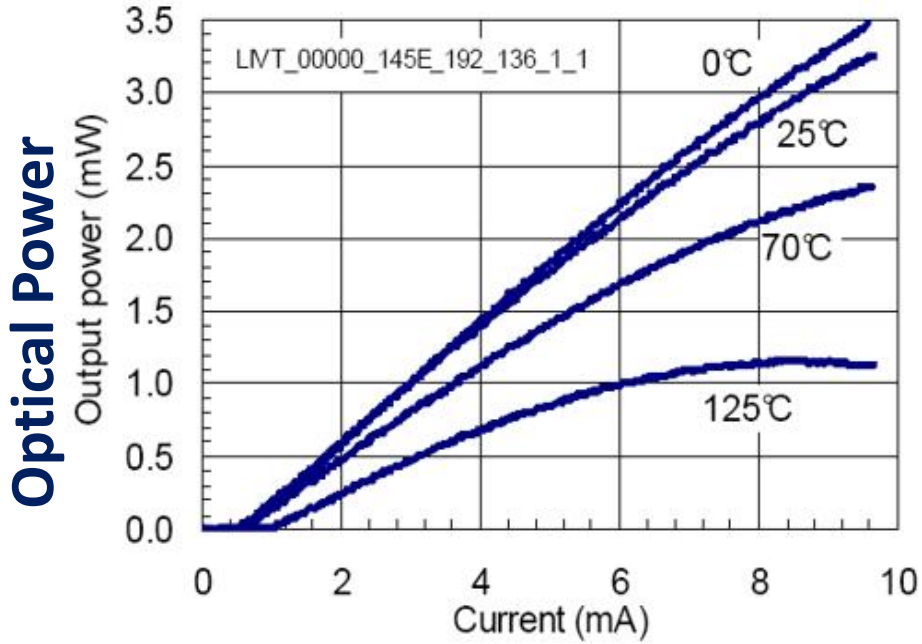
The principle of VCSEL Laser and ALDD ASIC

- VCSEL Laser (850 nm)
  - VCSEL (Vertical-Cavity Surface-Emitting Laser)
  - Anode , Cathode and Optical emitting aperture
  - Input: High-speed modulated current (typical 2 ~ 8 mA)
  - Output: High-speed modulate optical signal

- ALDD ASIC (Laser Driver)
  - Input: High-speed differential signals (CML signals for example)
  - Output: High-speed modulate current signal (to driver laser)

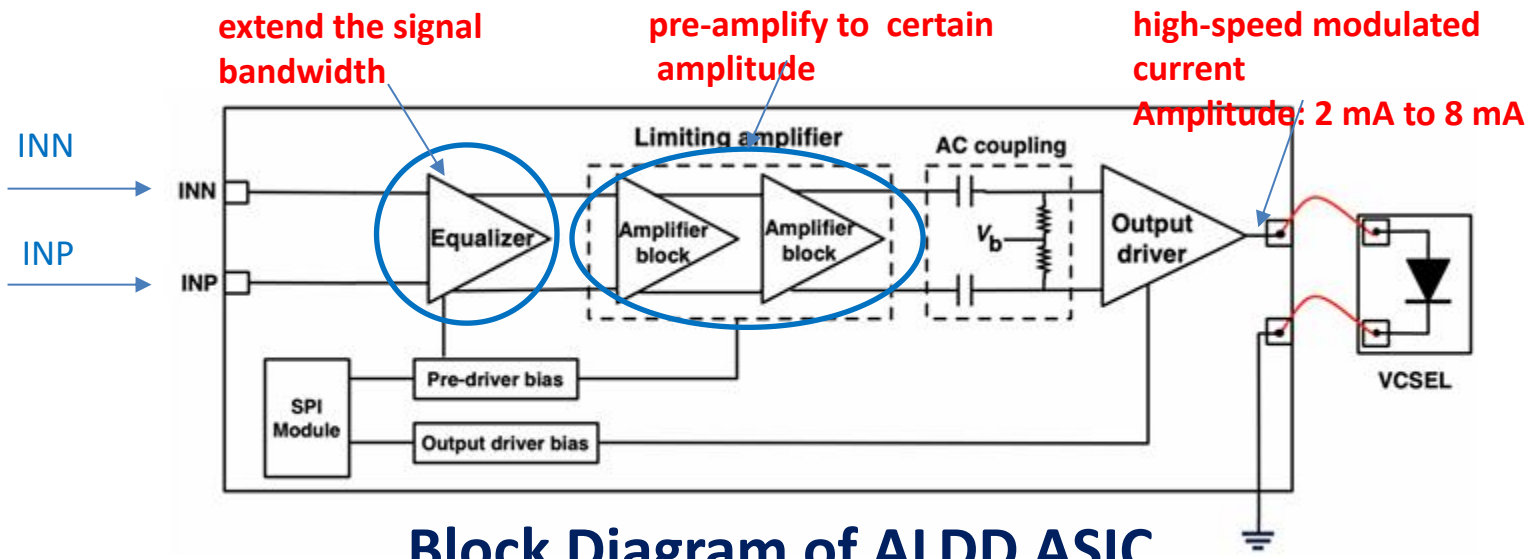


Four channel VCSEL Laser



Output Optical Power ---Input current of the 850 nm VCSEL

Overall block diagram of ALDD Laser Driver ASIC



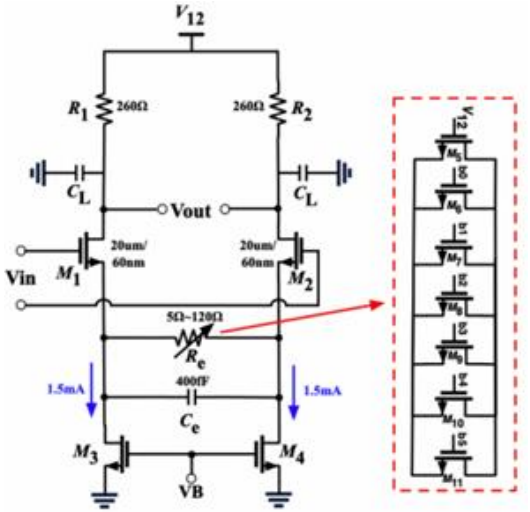
Block Diagram of ALDD ASIC

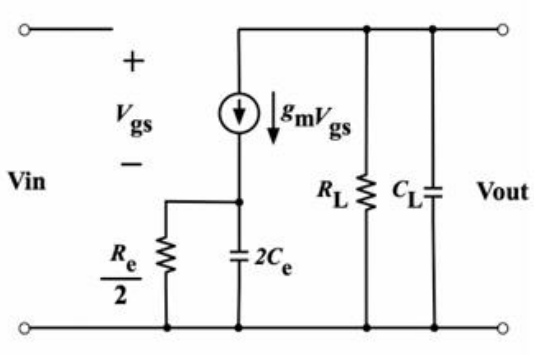
- The structure of ALDD ASIC mainly consists of three parts:
  - Equalizer
  - Limiting Amplifier(LA)
  - Output driver

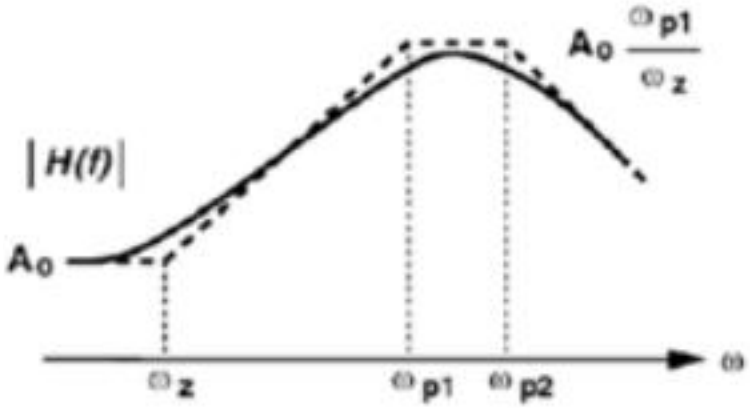
parameter	Design indicators
power supply voltage	1.2 V and 3.3 V
Power consumption	typical 50 mW/ch 200 mW when working at 4 ch x11.1 Gbps/ch
Bit rate	11.1 Gbps/ch
Differential input signal amplitude	Minimum differential peak-to-peak 200 mV
differential input impedance	100Ω
Maximum equalizer equilibrium strength	>7dB
Limiting amplification stage gain	>12dB@typical
Limiting amplification level bandwidth	>9.8GHZ@typical
Output current amplitude	5mA@typical
Maximum pre emphasis strength	>2.5dB
Simulate ISI jitter	<15ps

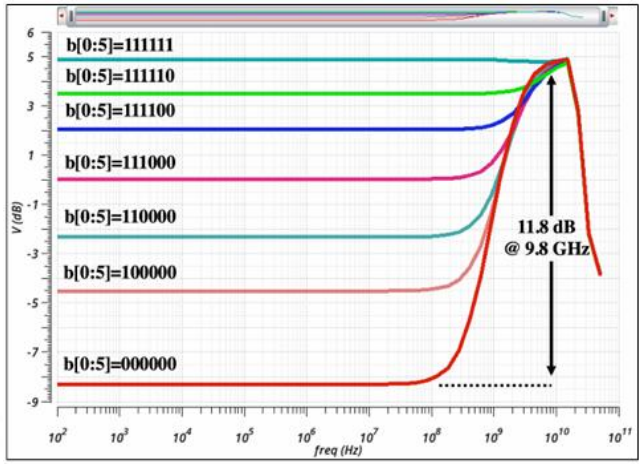
General specifications of the ALDD

Equalizer









CTLE structure **Small-Signal Model of CTLE** **frequency response** **frequency response of differerential Re value**

$$H(s)=\frac{g_m}{C_p}\frac{s+\frac{1}{R_S C_S}}{\left(s+\frac{1+g_m R_S/2}{R_S C_S}\right)\left(s+\frac{1}{R_D C_p}\right)}$$

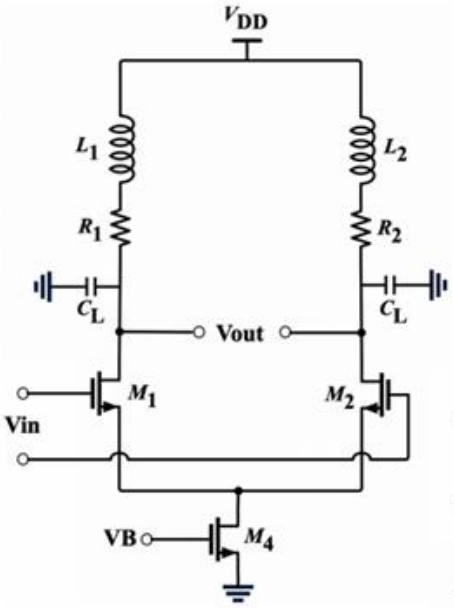
$$\omega_z=\frac{1}{R_S C_S},\quad \omega_{p1}=\frac{1+g_m R_S/2}{R_S C_S},\quad \omega_{p2}=\frac{1}{R_D C_p}$$

$$\text{DC gain}=\frac{g_m R_D}{1+g_m R_S/2},\quad \text{Ideal peak gain}=g_m R_D$$

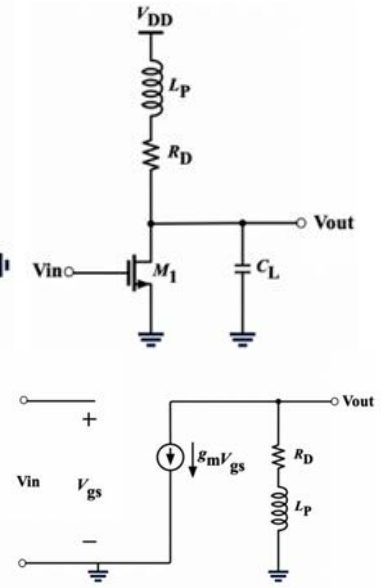
$$\text{Ideal Peaking}=\frac{\text{Ideal peak gain}}{\text{DC gain}}=\frac{\omega_{p1}}{\omega_z}=1+g_m R_S/2$$

- Similar configurable CTLE structure is used here as the input stage of the ALDD.
- Peaking Strength: 0~11.8 dB @9.8 GHz

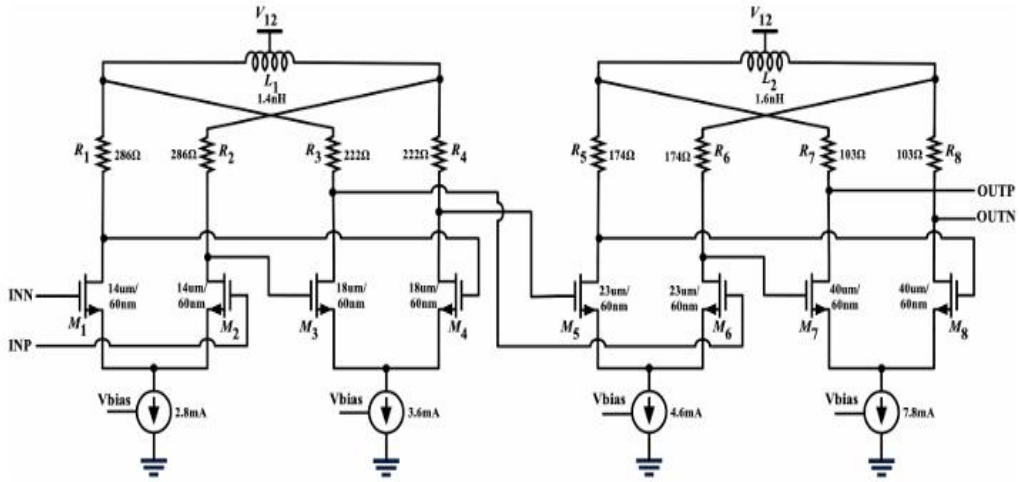
Limiting amplifier



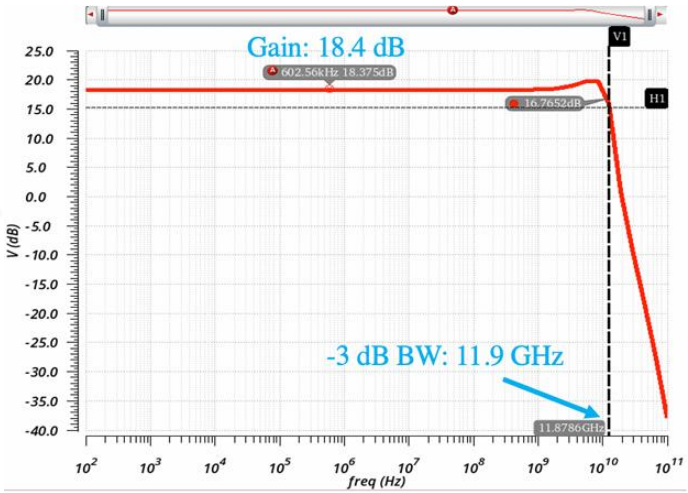
Inductive Peaking



Small-Signal Model



Limiting amplifier circut



Frequency response of LA stages

$$V_{out}C_L s + \frac{V_{out}}{L_P s + R_D} = -g_m V_{in}$$

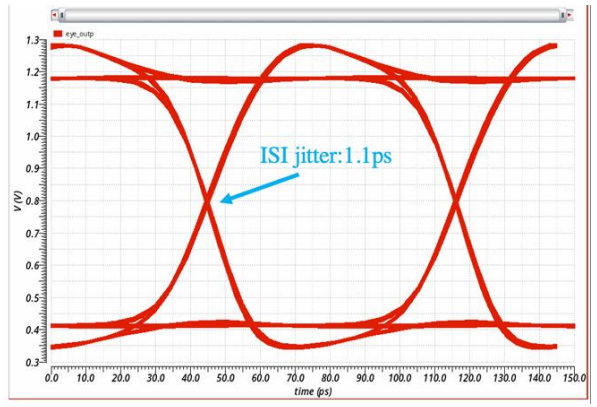
$$\frac{V_{out}}{V_{in}} = -g_m \frac{L_P s + R_D}{L_P C_L s^2 + R_D C_L s + 1}$$

$$= -g_m R_D * \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} * \frac{\omega_n}{2\zeta}$$

$$\zeta = \frac{R_D}{2}\sqrt{\frac{C_L}{L_P}} \qquad \omega_{-3\,dB} = \omega_n = \frac{\sqrt{2}}{R_D C_L}$$

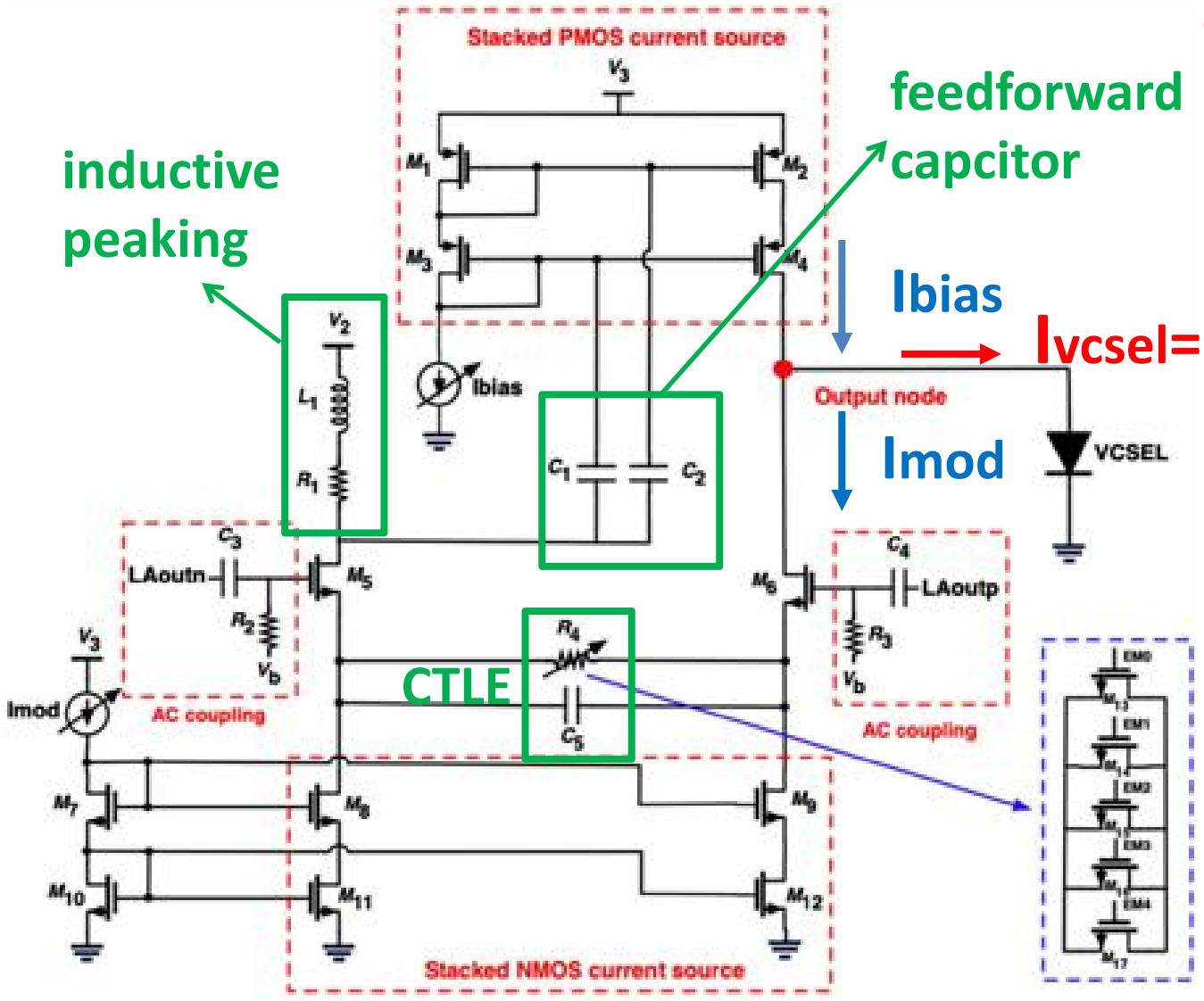
$$\omega_n^2 = \frac{1}{L_P C_L}$$

- Limiting amplifier in ALDD:
  - Including four differential stages with an overall 18.4 dB gain and 11.9 GHz BW.
  - Inductive peaking
  - Sharing inductor technology used for every two stages.



eye diagram of Limiting amplifier

Output Driver



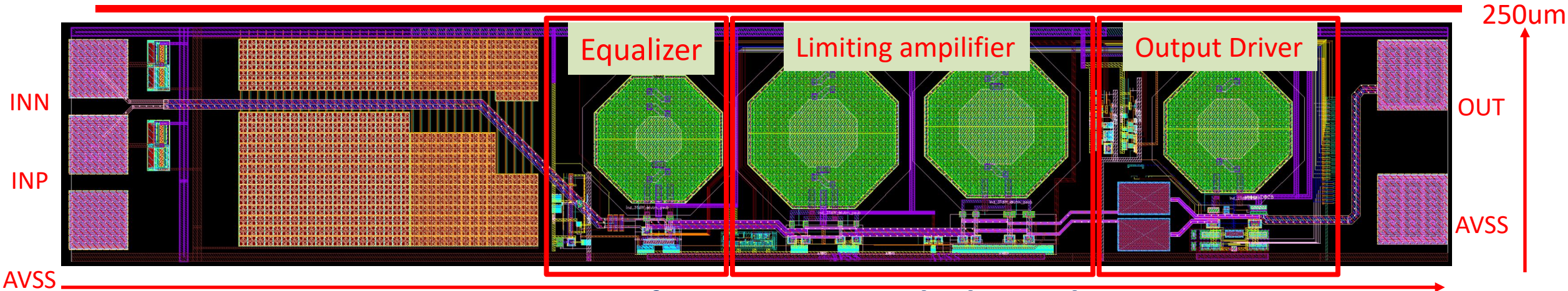
Output Driver structure

- Design of Output Driver Stage
  - Convert high-speed differential voltage into a high-speed current to drive the laser.

$I_{vcsel} = I_{bias} - I_{mod}$

- Output current : $I_{vcsel} = I_{bias} - I_{mod}$
- Inductive peaking + Cofigurable CTLE structure + Feed-forward Capacitor to improve bandwidth of the output driver.

Layout of the ALDD ASIC single channel



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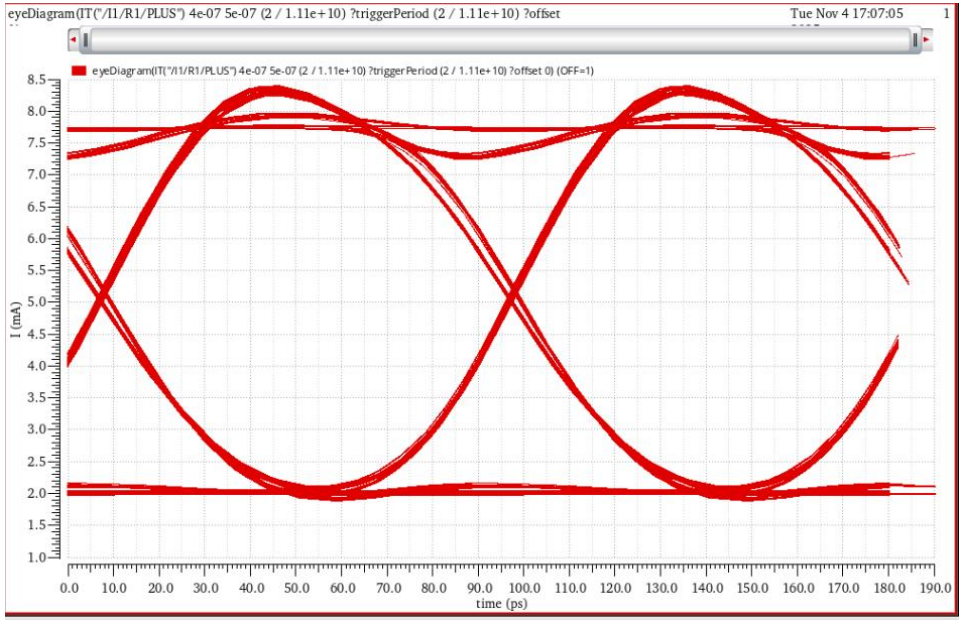
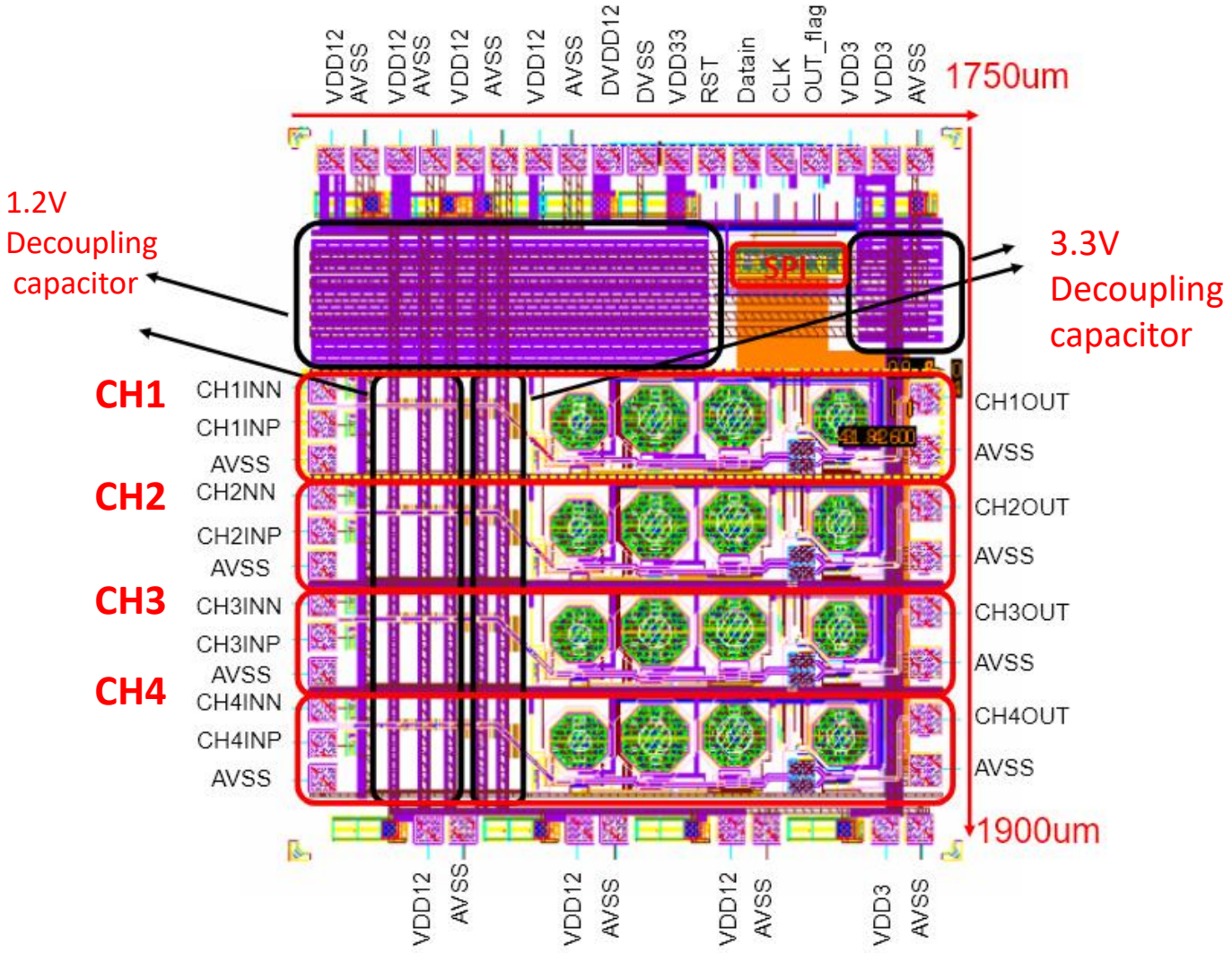


eye diagram of ALDD ASIC single channel

- Based on SMIC 55nm CMOS technology
- The size of the single channel is 1750 × 290 um.
- The left figure shows the post-simulation eye diagram of a single channel @ 11.09 Gbps

ALDD ASIC overall layout



Overall layout of 4 x 11.09 Gbps/ch ALDD ASIC

- The size of the ALDD ASIC is 1750×1900 um.
- This chip has been taped out in Oct 2025 and is expected to be returned for testing in Jan 2026.

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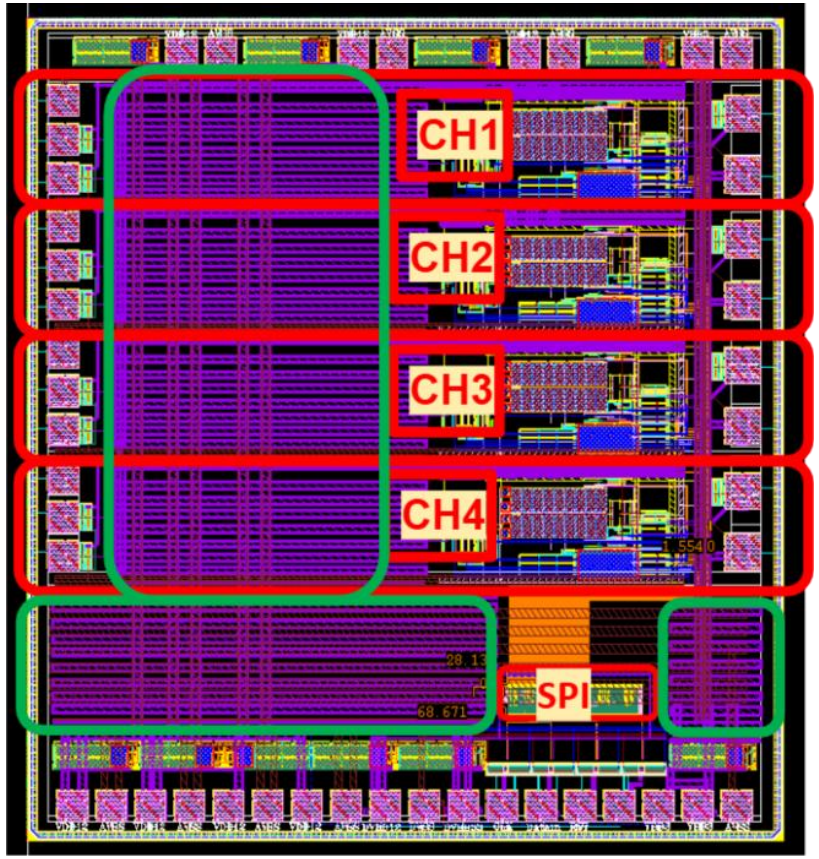
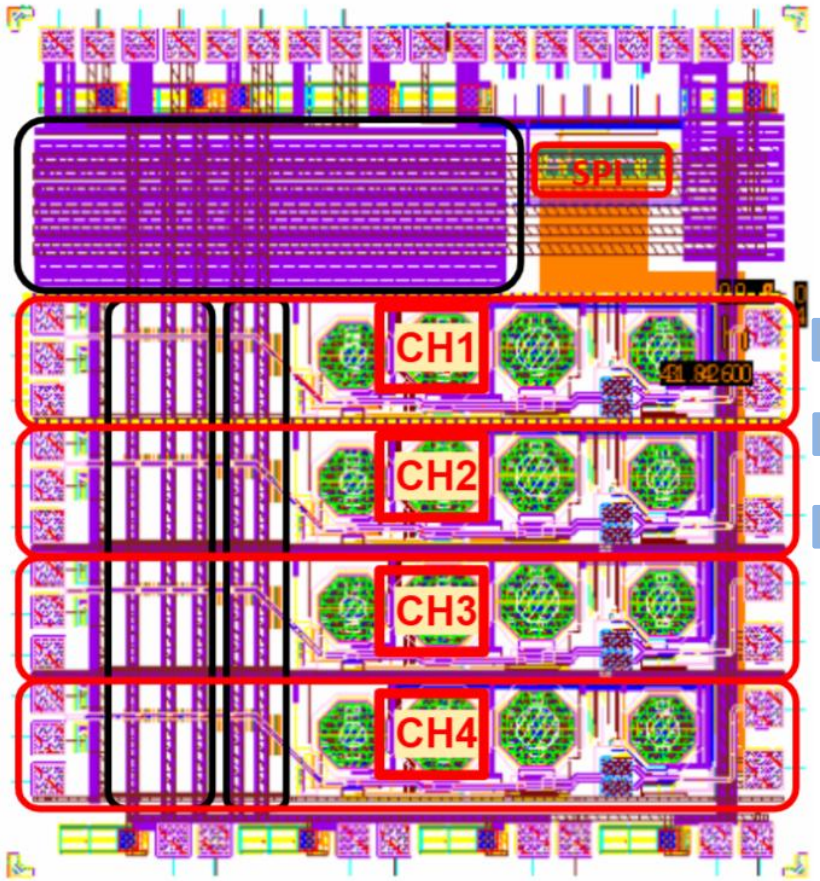


4 x 2.77 Gbps/ch
ATIA ASIC



4 x 11.09 Gbps/ch
ALDD ASIC

- Based on domestic technology (SMIC 55nm CMOS), we have designed ATIA and ALDD.
- Two ASICs have been taped out in Oct 2025 and is expected to be returned for testing in Jan 2026.

Thank you for your attention !