
# Development of the FEE-Powering: DC/DC

Xiayu Wang, Weiming Yang, **Jia Wang**

Institute of microelectronics, Northwestern Polytechnical University

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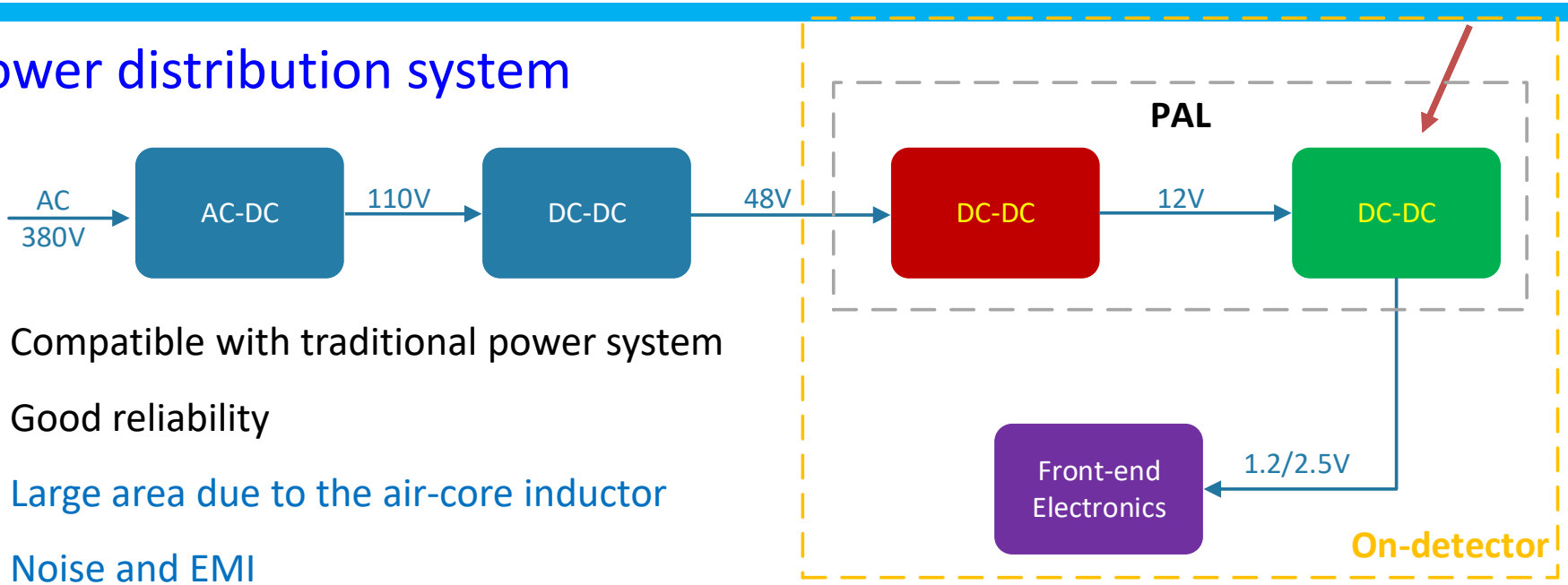
- Design of DC/DC buck converter
- Measurement results
- Summary and future work

# Introduction

## Power distribution system




- Compatible with traditional power system
- Good reliability
- Large area due to the air-core inductor
- Noise and EMI

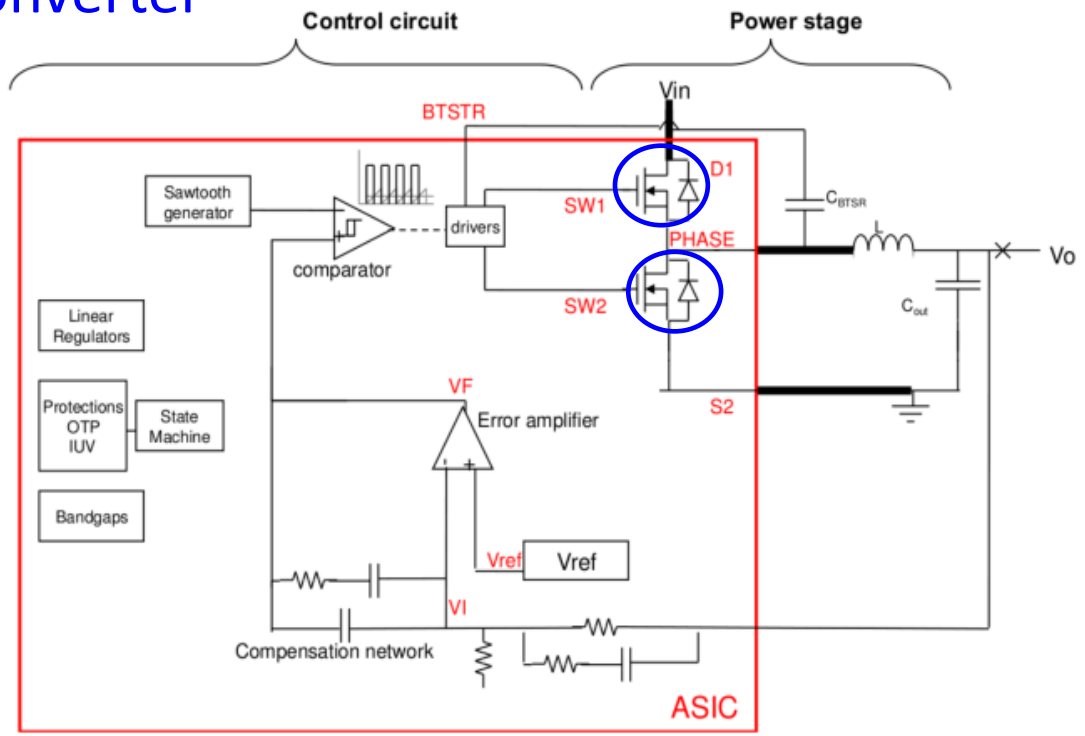
## Harsh working environment

- High magnetic field (Up to 3T in CEPC)
- High level of radiation will be reached inside the detectors (0.6 Mrad/y)

# Design of DC/DC buck converter

## Design specification of the DC/DC converter

| Parameter | Value |
|---|---|
| Input voltage | 12-10 V |
| Output voltage | 1.8/1.2 V |
| Output current | <10 A |
| Output ripple voltage | <10 mV |
| power efficiency | >80% |
| Power module size | <30x20x6.7mm$^3$ |
| TID | 0.6 Mrad/year |
| Magnetic field | 3T |
| Switching frequency | 1-3 MHz |



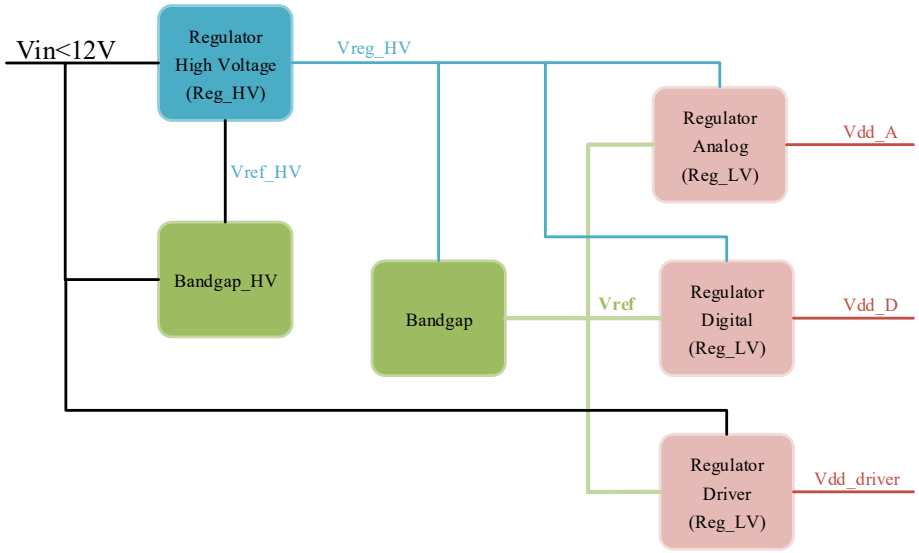

GaN power transistors are also considered to be used.

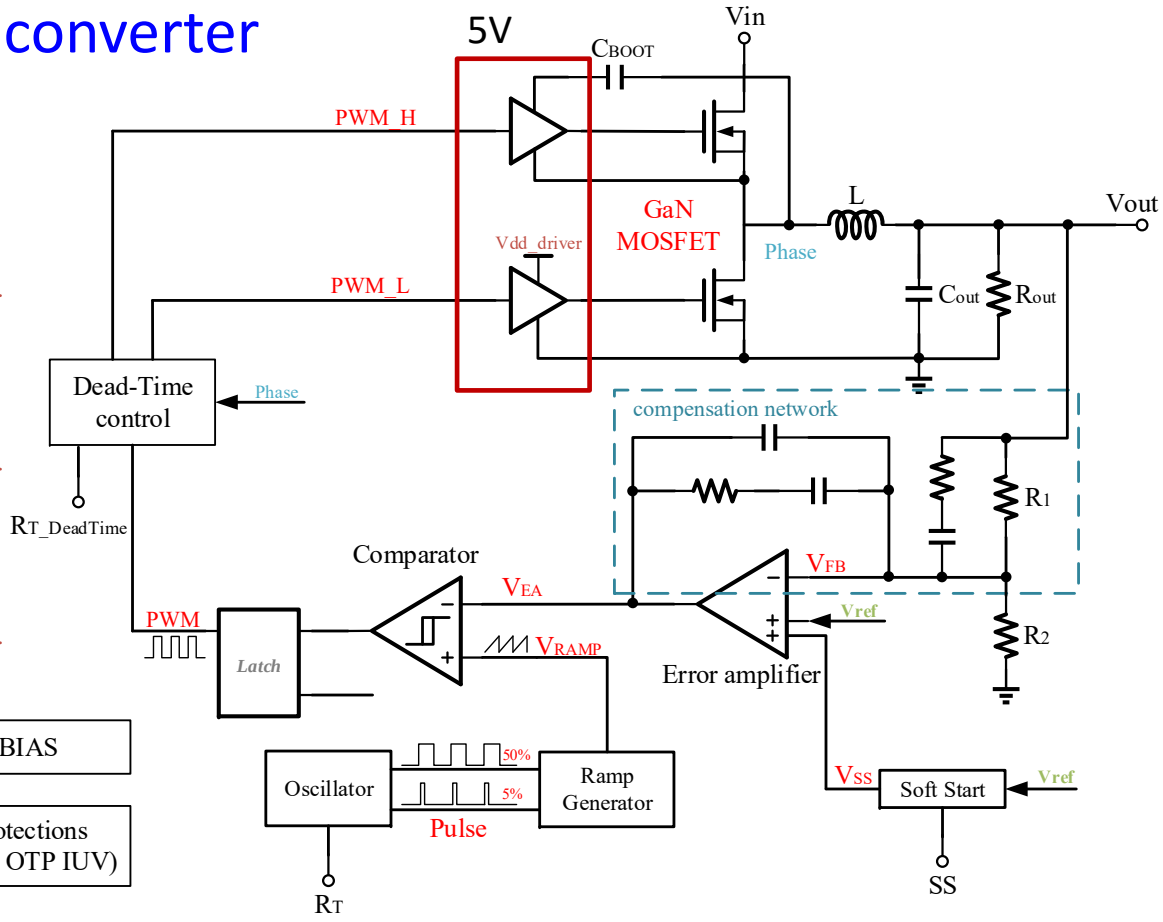
- fast switching speed
- low power loss
- high radiation tolerance
- low on-resistance

High current

# Design of DC/DC buck converter

- Diagram of the proposed DC/DC converter




- Smaller process node technology can resist TID.
  → Most of transistors are 0.18 um CMOS
- Built-in LDOs for different voltage domains

Controlling loop: Voltage mode PWM

# Design of DC/DC buck converter

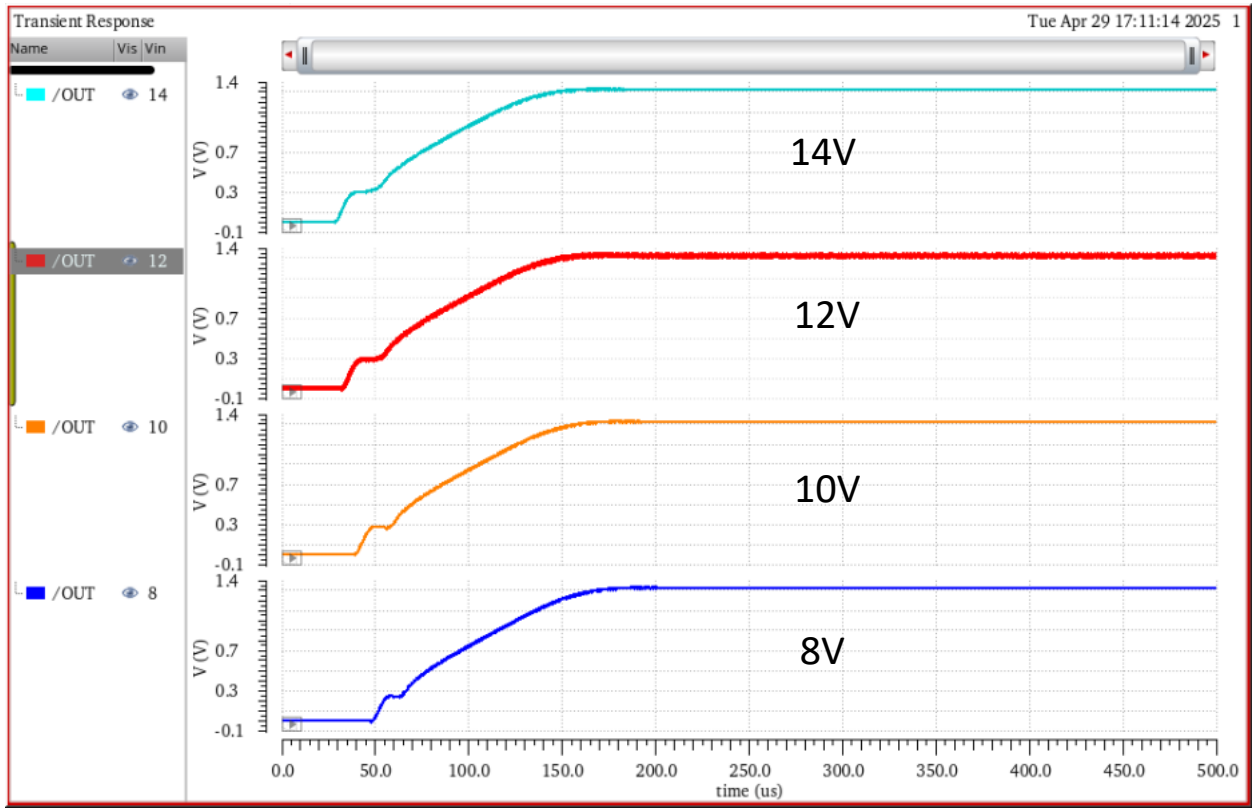
- Simulated ripple voltage of the proposed DC/DC converter @ Io=10A

| Corner | VBG (mV) | RT(Ω) | $f_{sw}$(Hz) | Ripple current (A) | Vo(V) | Ripple voltage 1st(V) | Ripple voltage 2nd(V) | Efficiency (%) |
|---|---|---|---|---|---|---|---|---|
| SS | 920 | 50k | 3.72M | 2.1 | 1.517 | 4.18m | 425.6u | 75.2 |
| | | 100k | 2.008M | 3.6 | | 9.618m | 1.385m | 81.6 |
| | | 200k | 1.085M | 6.15 | | 26.76m | 4.594m | 83.7 |
| | | 400k | 587.7K | 11.2 | | 92.3m | 39.6m | 84.3 |
| | | floating | 1.892M | 3.7 | | 13.15m | 835.6u | 79.8 |
| TT | 835 | 50k | 4.203M | 1.75 | 1.332 | 3.785m | 295.4u | 72 |
| | | 100k | 2.281M | 3.2 | | 8.157m | 627.1u | 79 |
| | | 200k | 1.237M | 5.9 | | 20.93m | 2.233m | 83 |
| | | 400k | 672.4K | 10.8 | | 64.88m | 17.87m | 84.9 |
| | | floating | 2.43M | 3 | | 7.417m | 555.4u | 78.4 |
| FF | 750 | 50k | 4.762M | 1.44 | 1.237 | 3.11m | 277.3u | 69.4 |
| | | 100k | 2.595M | 2.63 | | 6.427m | 530.7u | 77.3 |
| | | 200k | 1.415M | 4.8 | | 16.57m | 2.433m | 82.2 |
| | | 400k | 773.3K | 8.8 | | 45.47m | 8.803m | 84.9 |
| | | floating | 3.164M | 2.16 | | 4.959m | 435.7u | 75.1 |

Ripple voltage can be decreased by increasing the switching frequency, while the power efficiency decreases.

# Design of DC/DC buck converter

- Start-up simulation @ VIN:14,12,10,8,6V



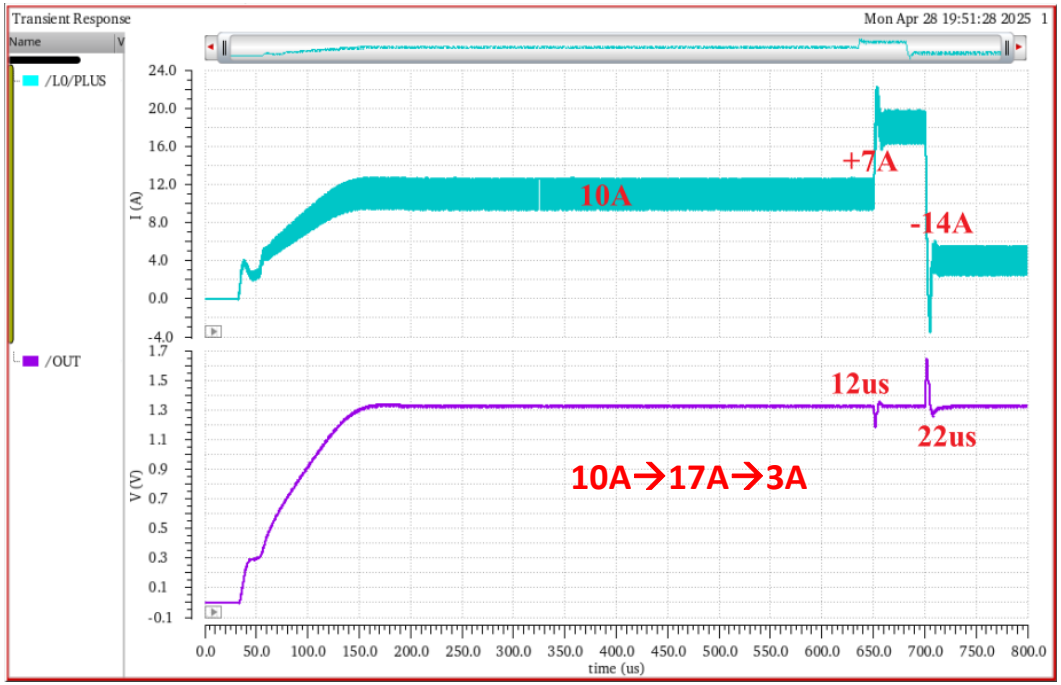

| Vin (V) | 14 | 12 | 10 | 8 | 6 |
|---|---|---|---|---|---|
| Efficiency (%) | 77.28 | 78.93 | 80.73 | 82.1 | / |
| Switching Frequency | 2.283 MHz | | | | |
| Vo（V） | 1.331 | | | | / |
| Vorip1st (mV) | 8.365 | 8.159 | 8.03 | 7.121 | / |
| Vorip2nd (uV) | 686 | 705.1 | 840 | 314.5 | / |

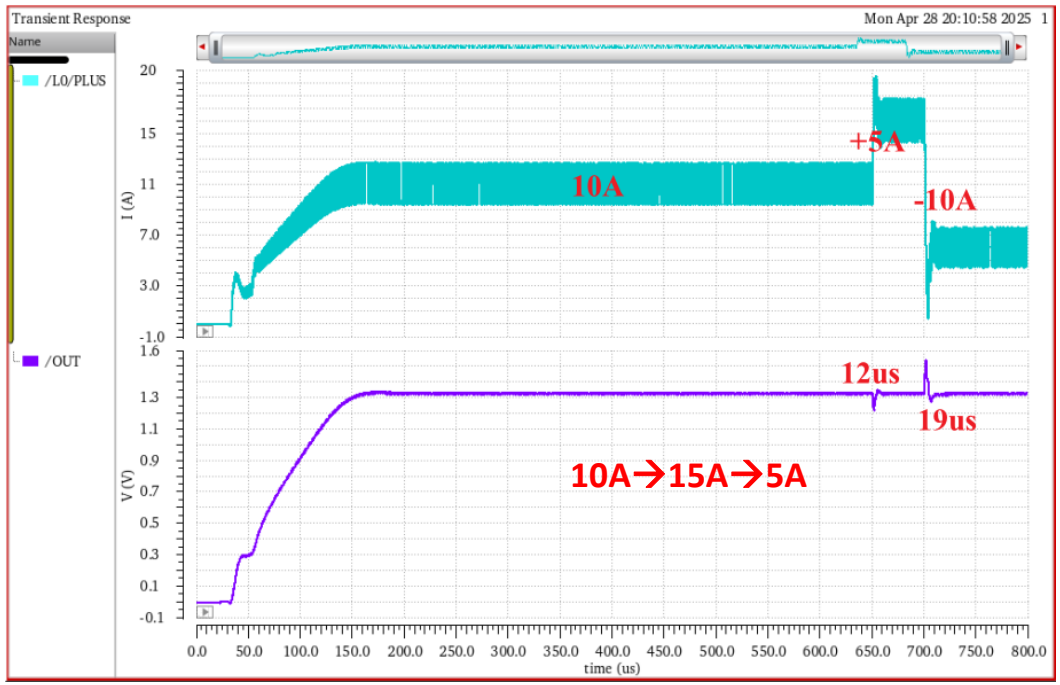
The efficiency increases and ripple voltage decreases with input voltage decreasing, owing to the increase of duty cycle.

The converter can work well, except at vin of 6V. ←The under-voltage lockout (UVLO) works

# Design of DC/DC buck converter

- Transient response with load current step

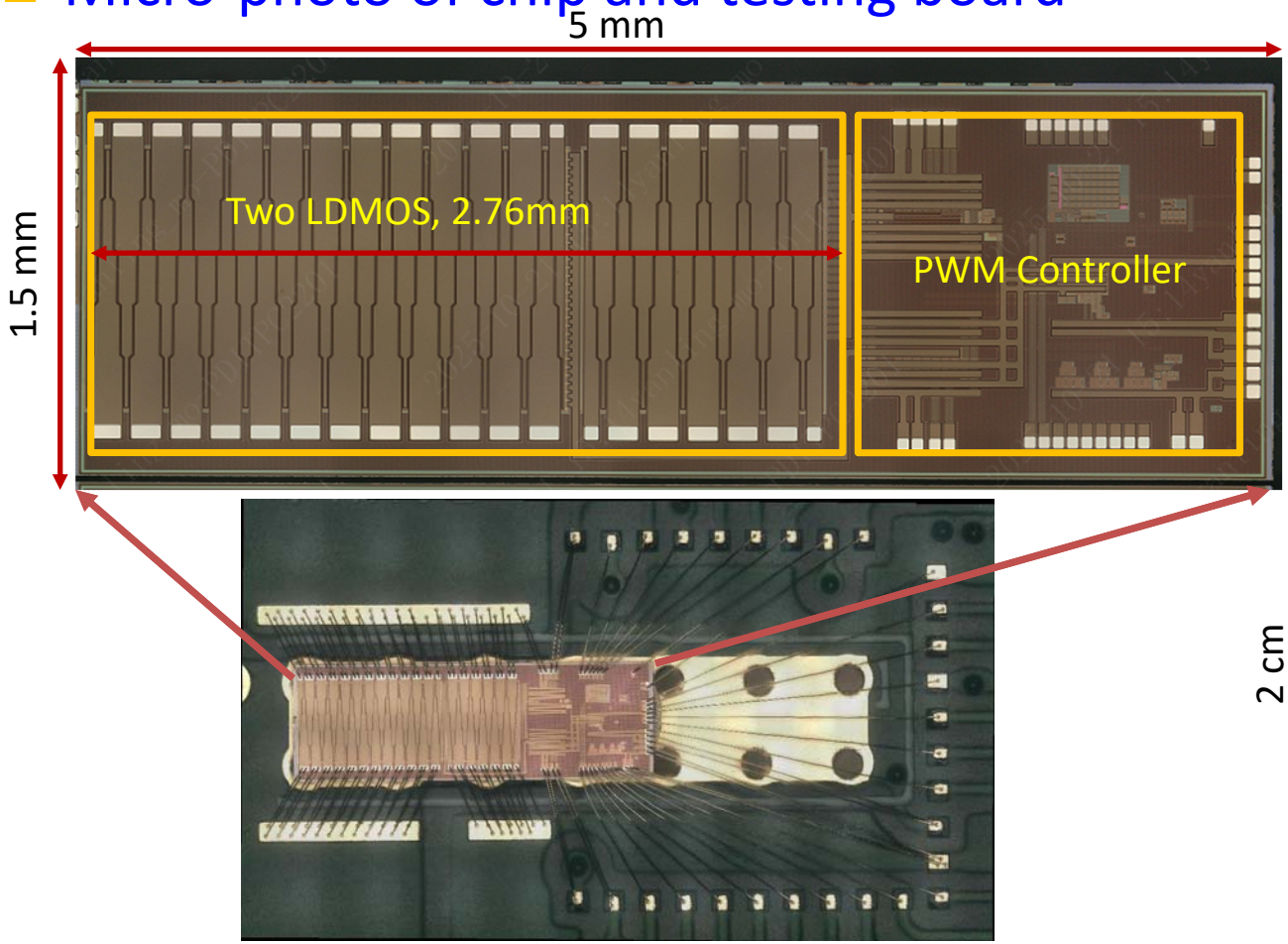



- The output voltage can recover after 22us.
- No oscillation is observed.

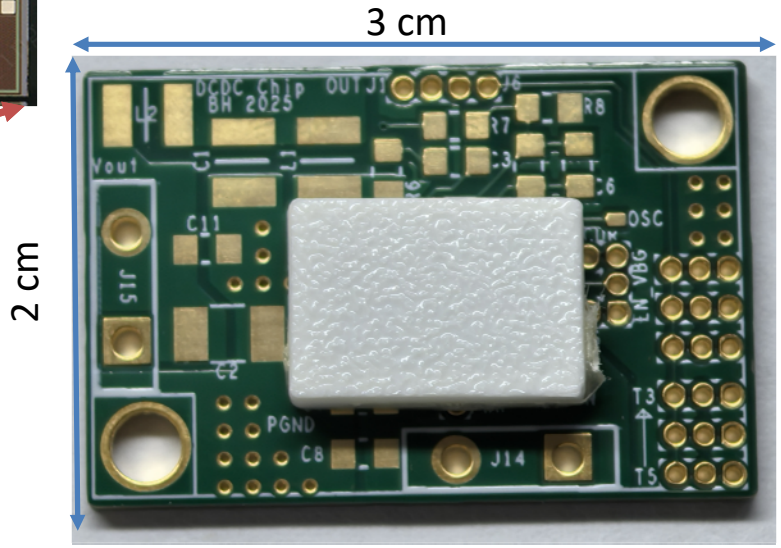
# Primary measurement results

- Micro-photo of chip and testing board




Assambled with Wire-bonding

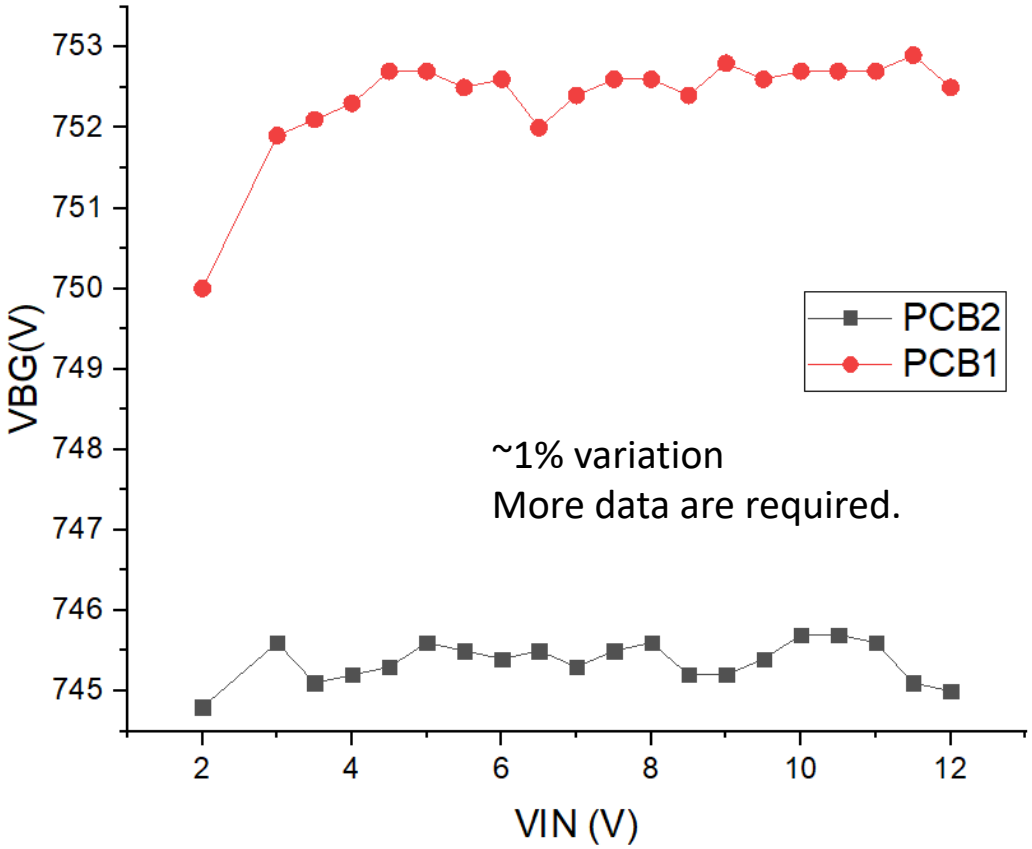
- 180nm BCD process
- 1.8V, 5V, 12V MOS devices
- Large area PADs → high current
- Fabricated at the end of October
- Measurement is ongoing



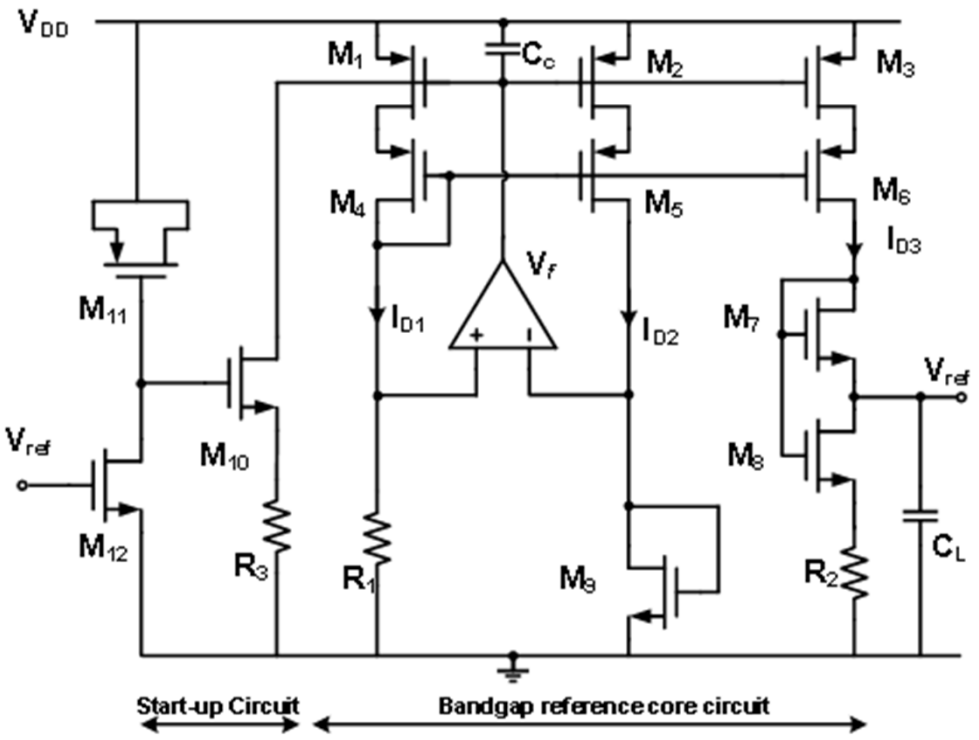

The photo of the testing board

# Primary measurement results

- Bandgap Voltage VS VIN



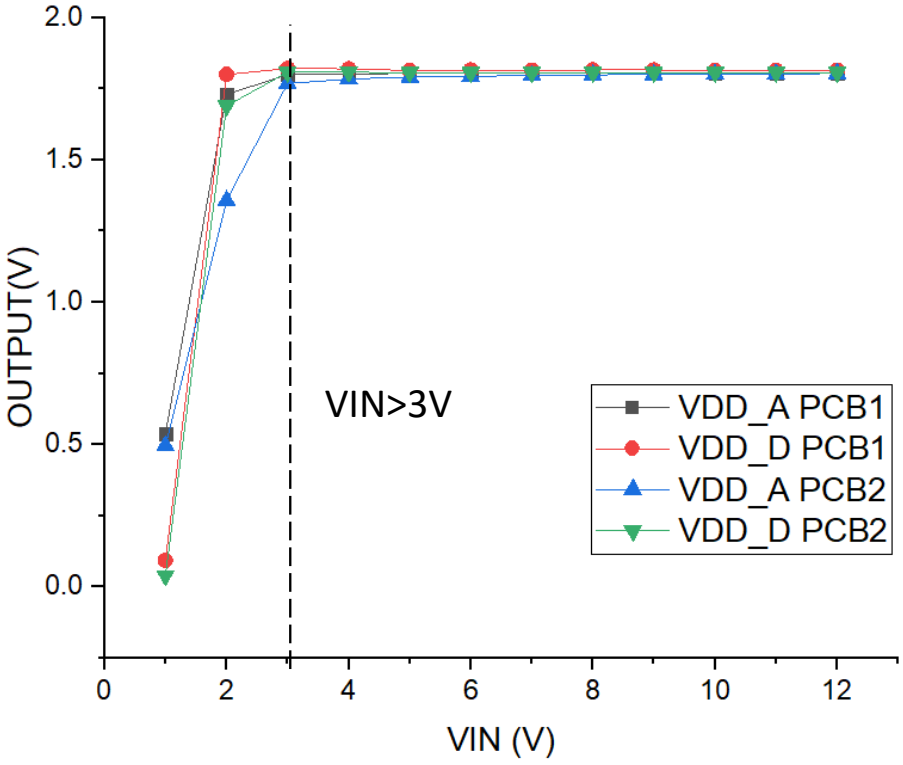

The full CMOS bandgap output can be unvaried with VIN



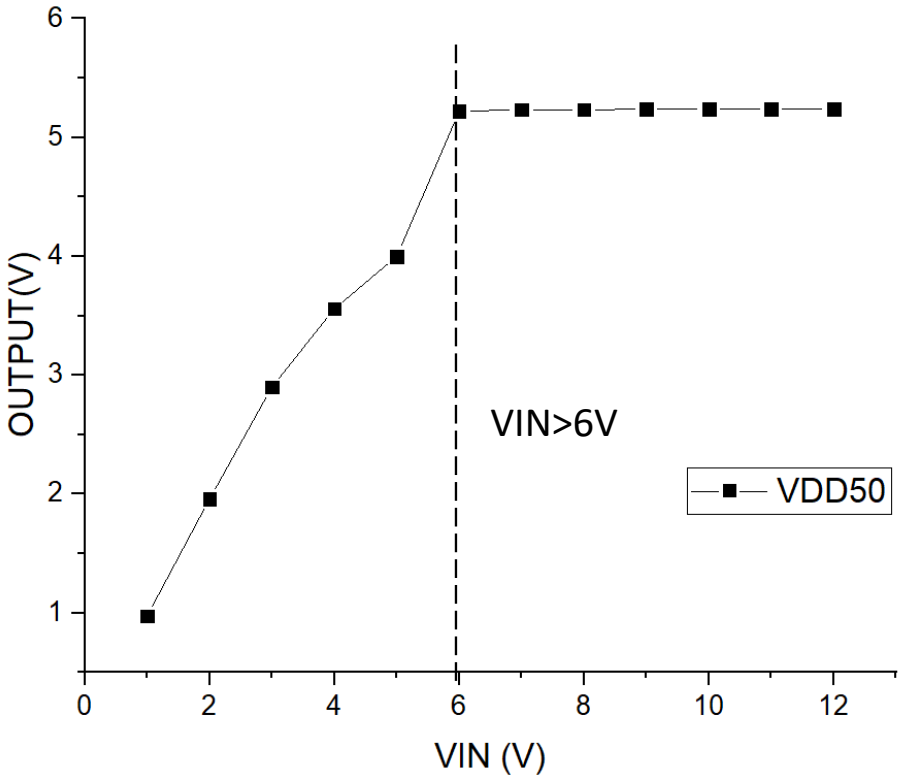

Schematic of the bandgap

# Primary measurement results

- Measurement results of the built-in regulators



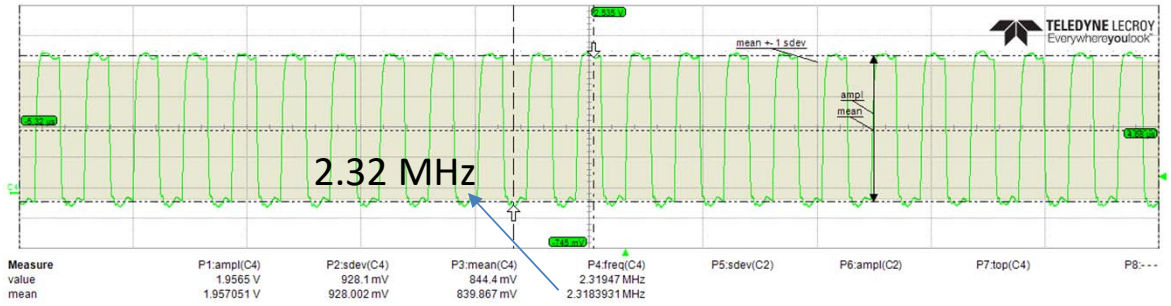

Supply analogue/digital power for controller (1.8V)



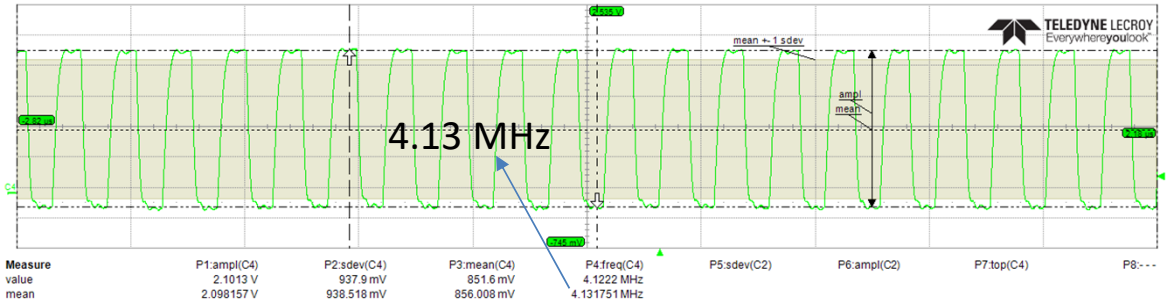

Supply power for the LDMOS driver (5V)

# Layout and measurement results

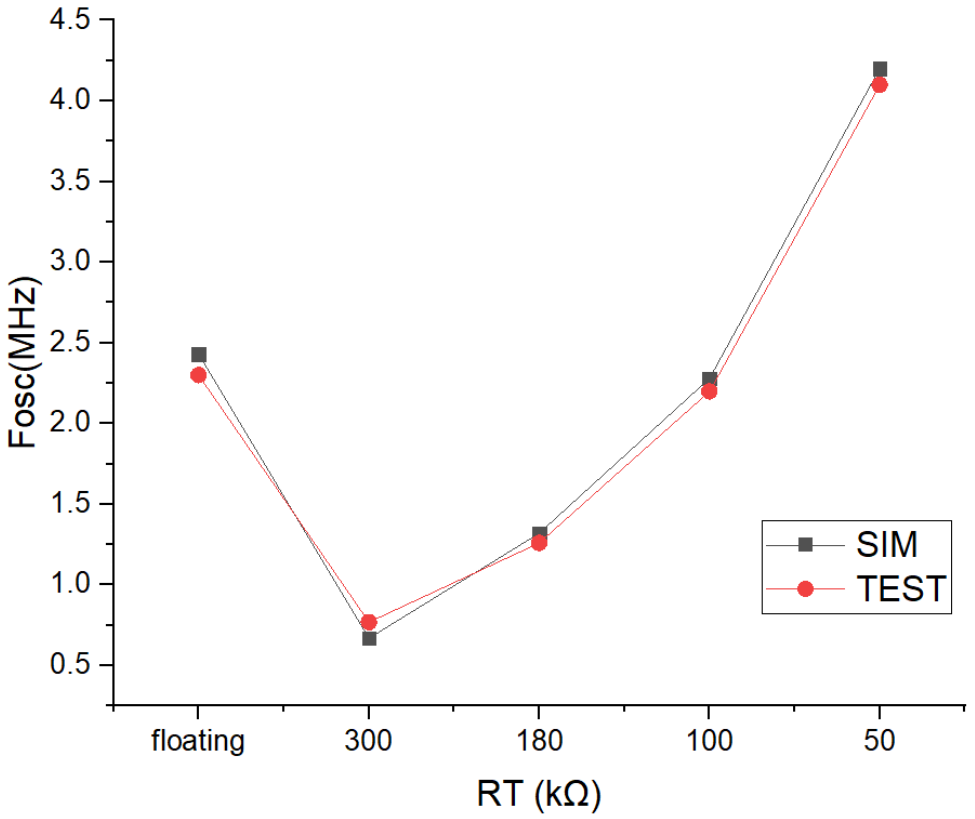
- Measured frequency of oscillator




Works with internal current source, when RT is floating.




Works with external current source, when RT is 50kΩ




- Frequency changes linearly with the value of RT(0.5-4MHz)
- Test results are consistent with simulation results

# Summary and working plan

## Conclusion

- A radiation tolerance 12V-1.2V DC/DC converter has been designed and fabricated.
- Simulation results demonstrate low ripple voltage can be achieved by higher switching frequency and larger inductor.
- Measured results demonstrate the built-in bandgap, regulators and oscillator can work well.

## Future work

- Continue to test the prototype chip (with GaN power transistors)
- The irradiation experiment will be completed.


# Thanks for your attention!

Xiayu Wang, Weiming Yang, **Jia Wang**

Institute of microelectronics, Northwestern Polytechnical University

NSFC

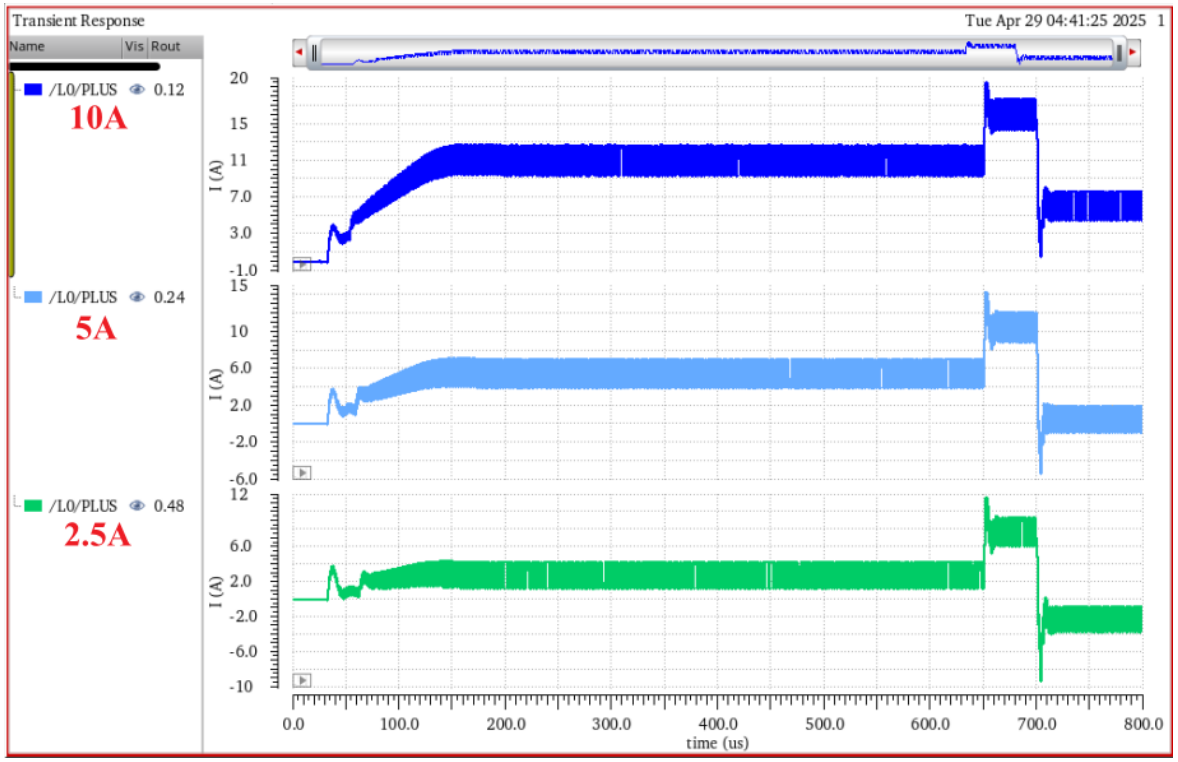
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

西北工业大学
NORTHWESTERN POLYTECHNICAL UNIVERSITY

中国科学技术大学
University of Science and Technology of China

# Design of DC/DC buck converter

## 不同负载情况启动过程仿真




| Load current(A) | 10 | 5 | 3.3 | 2.5 |
|---|---|---|---|---|
| Efficiency(%) | 83.14 | 83.15 | 83.16 | / |
| Frequency(Hz) | 2.283M | | | |
| Output voltage(V) | 1.331 | | | |
| Ripple voltage 1st(V) | 8.594m | 7.845m | 7.504m | 7.54m |
| Ripple voltage 2nd(V) | 1.173m | 705.1u | 354.2u | 574.4u |

- 负载为10A、5A、2.5A情况下，电路均可以正常启动，输出稳定的电压信号

# Design of DC/DC buck converter

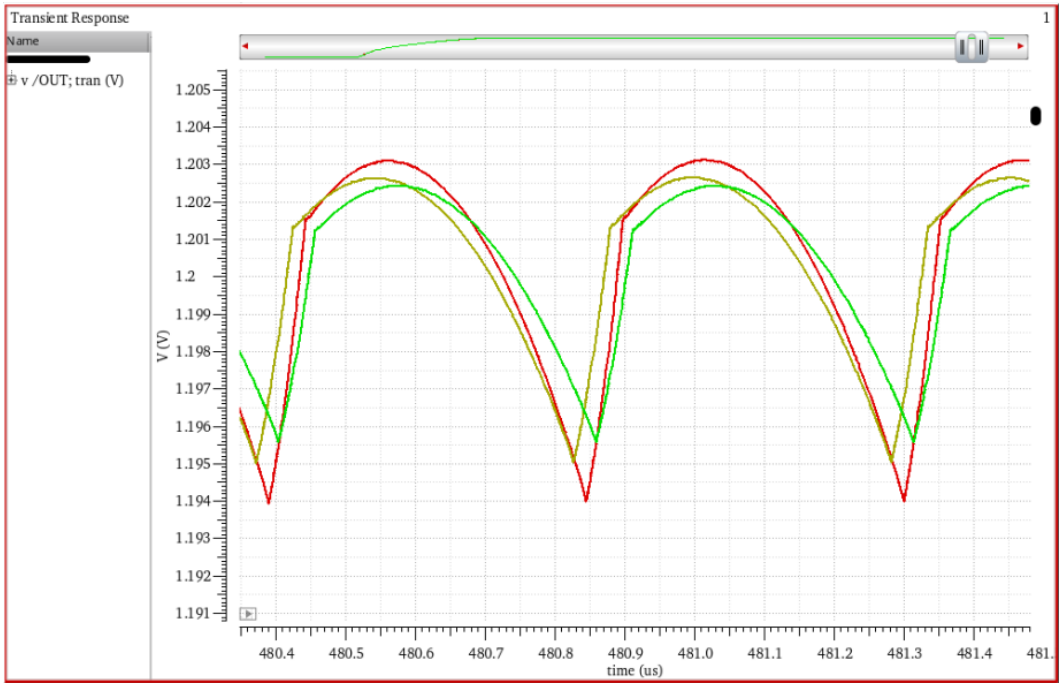
## 电压纹波受电感值影响仿真

①受振荡器频率控制，芯片工作频率保持不变

②输出纹波与感值成反比

③不同电感值下，输出信号有一定的相位差

| 电感感值(nH) | 150 | 180 | 200 |
|---|---|---|---|
| 电源效率(%) | 83.14 | 83.15 | 83.16 |
| 工作频率(Hz) | 2.162M | 2.164M | 2.16M |
| 第一级输出纹波(V) | 9.477m | 7.859m | 7.046m |
| 第二级输出纹波(V) | 452.9u | 442.8u | 382.1u |



# Design of DC/DC buck converter

## Simulation Results

| / | Corner | $f_{sw}$(HZ) | VBG(V) | Output voltage (V) | Ripple current (A) | Ripple voltage(V) | | Efficiency(%) |
|---|---|---|---|---|---|---|---|---|
| | | | | | | (1st) | (2nd) | |
| PRE-SIM | SS | 2.008M | 920 | 1.517 | 3.6 | 9.618m | 1.385m | 81.6 |
| | TT | 2.281M | 835 | 1.332 | 3.2 | 8.157m | 627.1u | 79.4 |
| | FF | 2.595M | 750 | 1.237 | 2.63 | 6.427m | 530.7u | 77.4 |
| POST-SIM | SS | 1.979M | 761 | 1.179 | 3.19 | 8.397m | 631.8u | 79.0 |
| | TT | 2.283M | 765 | 1.127 | 2.83 | 6.895m | 359.5u | 80.1 |
| | FF | 2.696 | 763 | 1.261 | 2.47 | 5.715m | 306.2u | 79.6 |

对各工艺角下带隙进行了修调：

| Corners | Nominal | ss | ff | tt |
|---|---|---|---|---|
| Temperature | | 125 | -40 | 27 |
| Design Variables | | | | |
| T5 | | 1.8 | 0 | 1.8 |
| T4 | | 1.8 | 0 | 0 |
| T3 | | 1.8 | 0 | 0 |
| T2 | | 0 | 0 | 0 |
| T1 | | 1.8 | 0 | 0 |
| T0 | | 0 | 1.8 | 0 |

不同工艺角下电路启动过程后仿真：