# FPGA-based front end electronics for AC-LGAD detector

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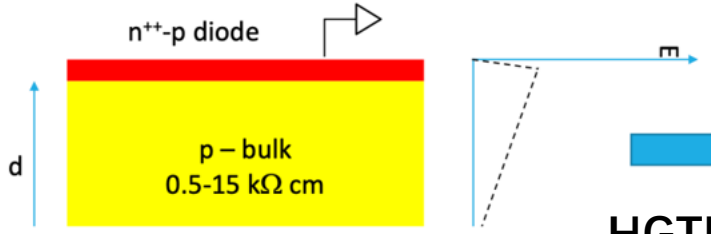
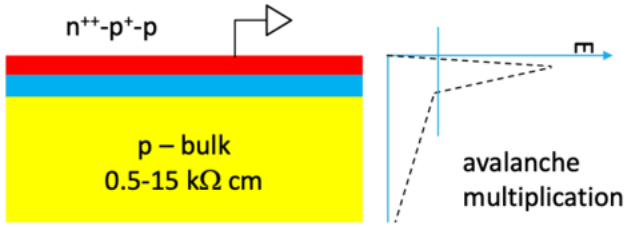
# Capacitively-coupled Low Gain Avalanche Detectors (AC-LGAD) 低增益雪崩硅传感器

一般的 PiN结传感器




低增益雪崩硅传感器

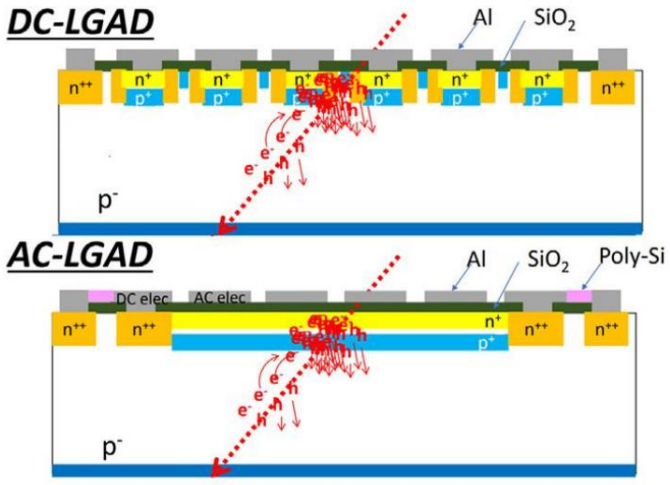
P+ gain layer on top of PIN diode




LGAD Advantages:

1. Large S/N;
2. Thin PN junction;
3. Good irradiation hardness
4. Fast rise time (~500 ps);
5. Modest gain (~50);

**HGTD project** in ATLAS phase-II upgrade

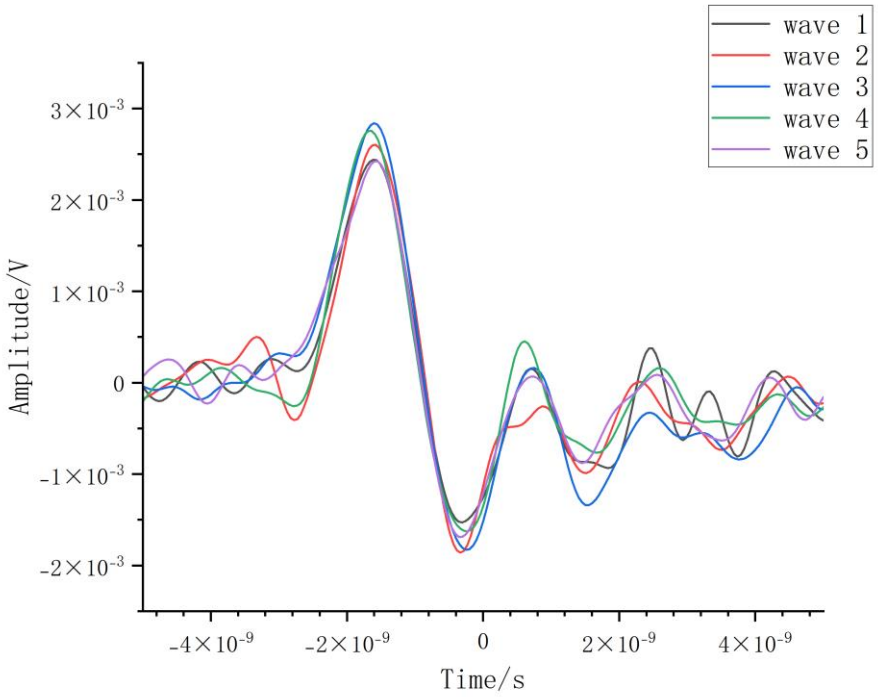



Improved LGAD design

DC-LGAD: large insensitive region

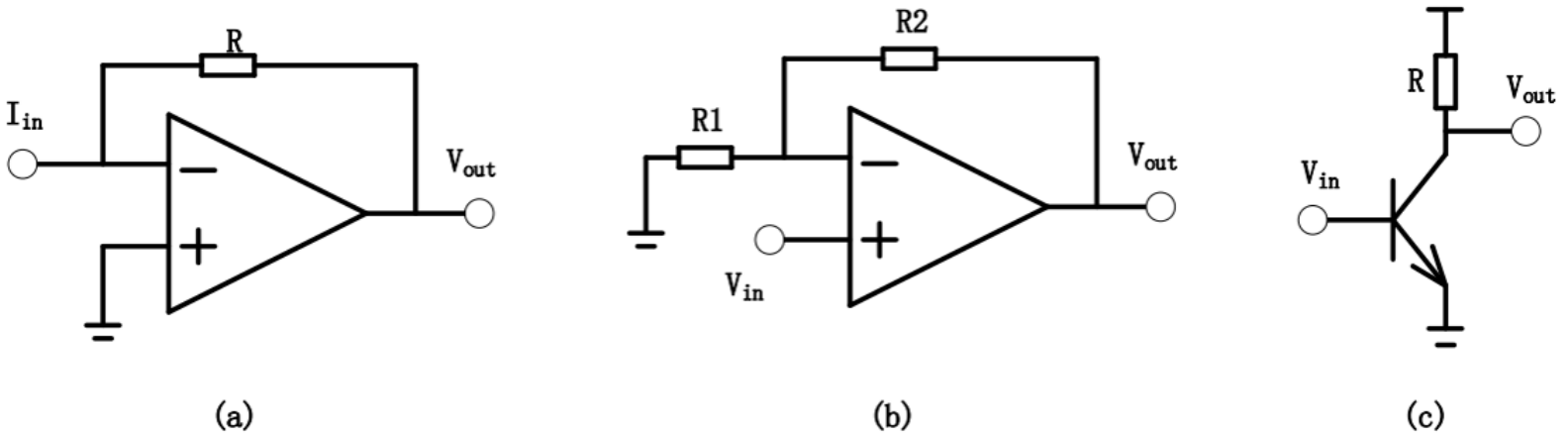
AC-LGAD: Capacitive coupled technology to decrease the insensitive region.

# Characteristics of AC-LGAD signal




| Characteristics of AC-LGAD output signal | | Characteristics of Front End Electronics (FEE) |
|---|---|---|
| 1. Short pulse (~2 ns); | → | 1. Fast response |
| 2. Fast rise time (~500 ps); | → | 2. High bandwidth of amplification circuit |
| 3. Small amplitude (<10 mV); | → | 3. Large gain |

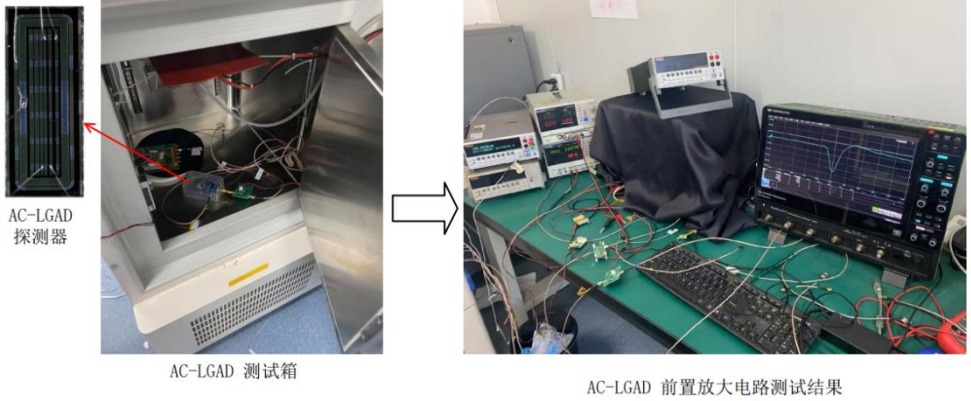
# Front-End Readout electronics




Transimpedance Amplifier (**TIA**): Vout=$I_{in}$* R ; → (HGTD-Altiroc);
Voltage Amplifier (**VA**): Vout = (1+$R_2$/$R_1$)Vin;
Wideband Radio-Frequency Amplifier (**RF**): fixed gain.

# RF Amplifier test in IHEP

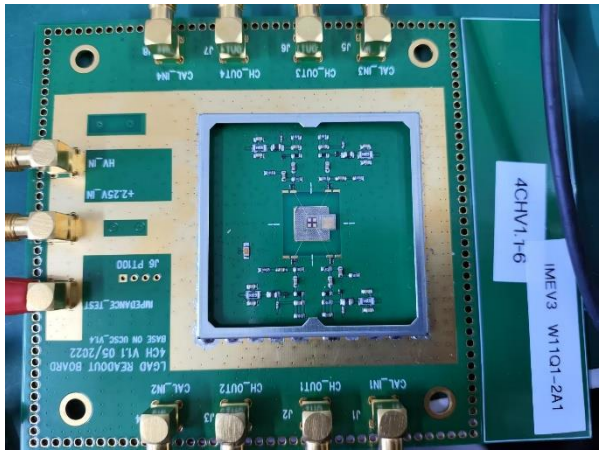
**PGA-103+ :** BandWidth 4GHz, rise time 600ps-800ps;
**BGA420 :** BandWidth 3GHz, rise time 500-600ps;
**BGA427 :** BandWidth 3GHz, rise time **400-500ps**;
**PHA-23LN+ :** BandWidth 2GHz, rise time 600ps;
**ADL 5536 :** BandWidth 1GHz, rise time 700ps-900ps;
**MAR-6+/ADL5545 :** BandWidth 6GHz, rise time **550ps，pulse width<2ns.**

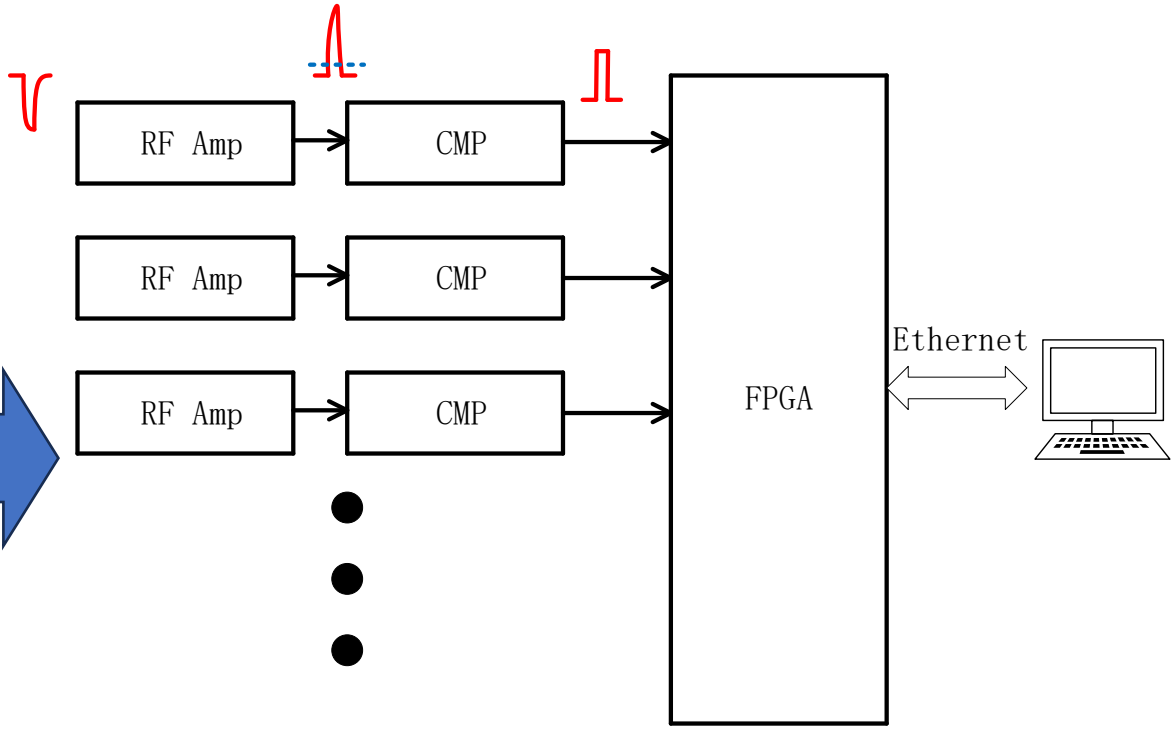



Experimental setup in IHEP.


More than 100 mV after two-stage RF Amp.

# Framework of the FEE



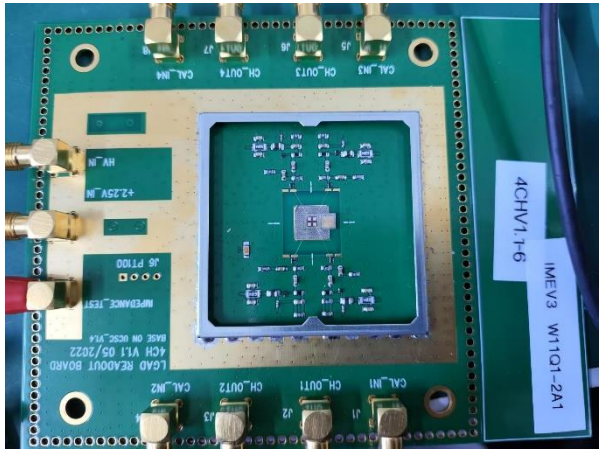




LGAD detector & adapter board

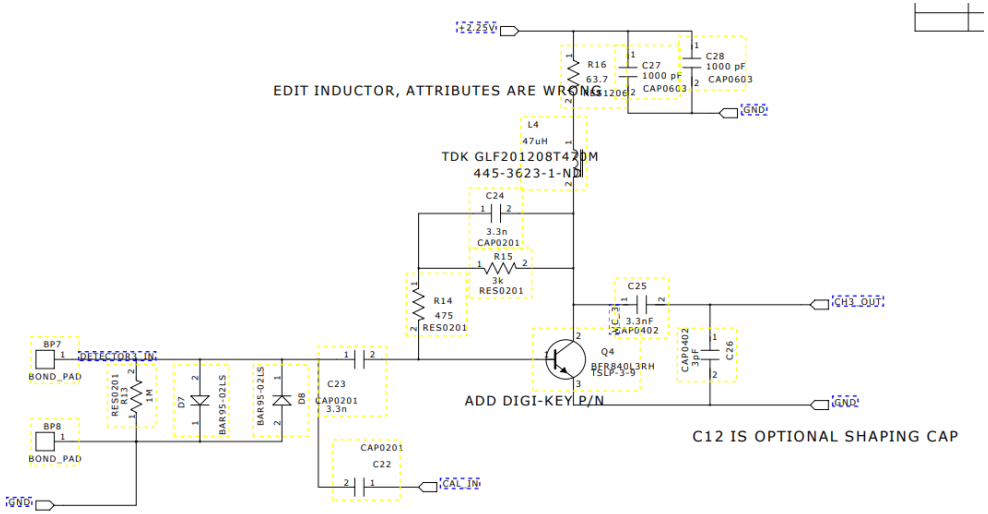
LGAD front-end electronics (FEE)

PC

# Adapter board

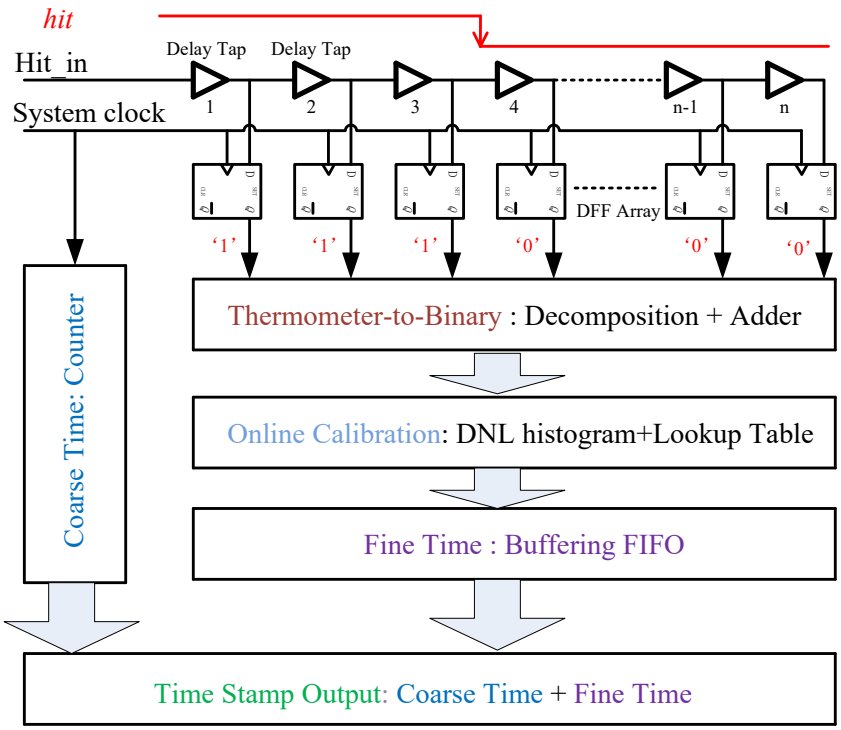



LGAD detector & adapter board




One-stage or two-stage amplifier

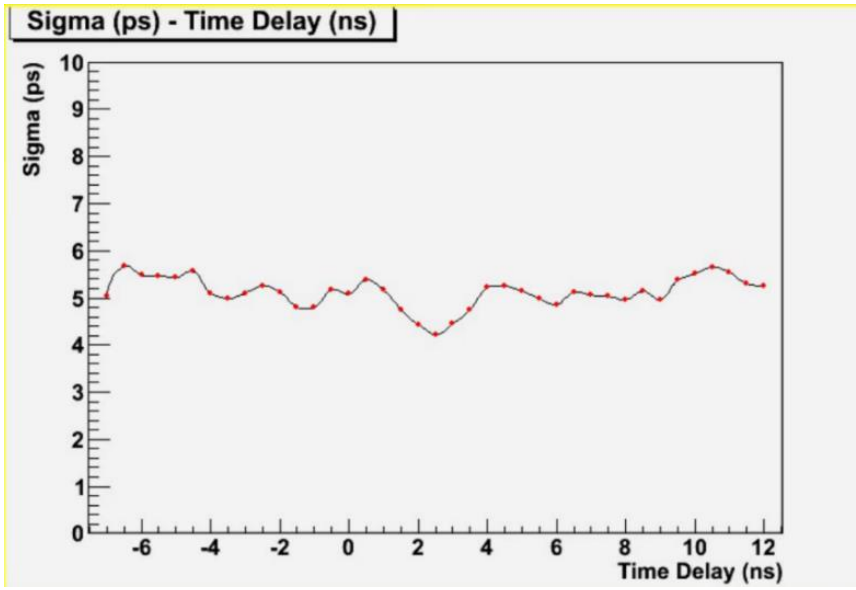
# TDL-TDC in FPGA




**FPGA-TDC (Tapped Delay Line,)**

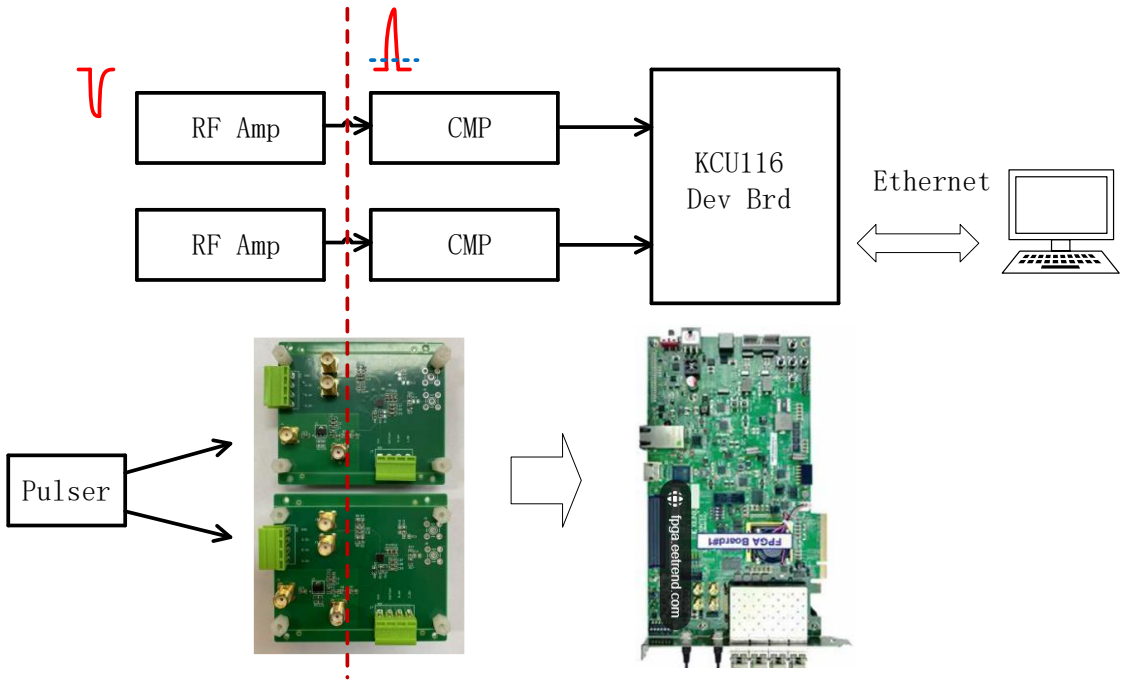
1.Coase time：16-bit counter；

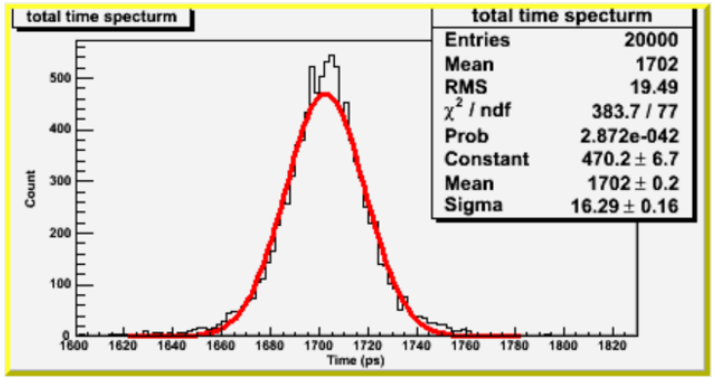
2.Fine time：Time delay line is implemented CARRY8 primitive.




The resolution of FPGA-based Tappled Delay Line (TDL) TDC in Kintex Ultrascale family is ~6 ps .

# Two-ch FEE Verification



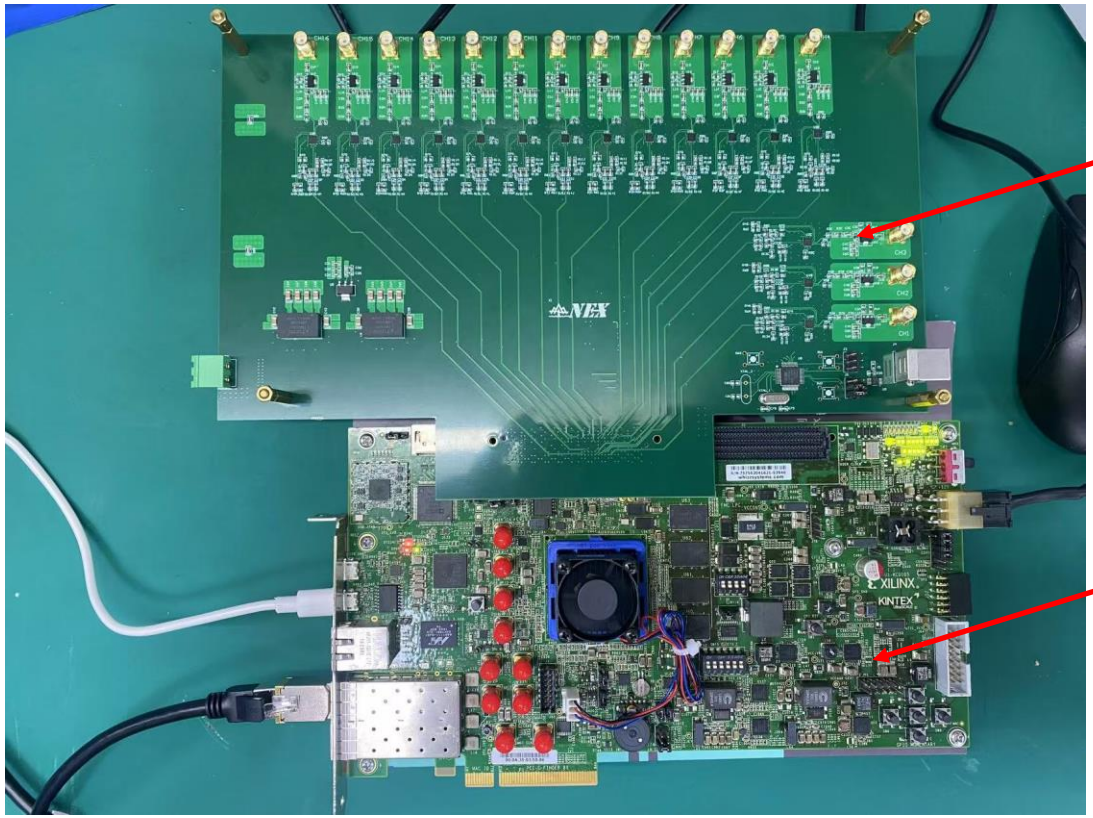

~16 ps

**2-ch test system** to validate the time resolution measurement:

1. RF: ADL5545->6 GHz with integrated bias control circuit;
2. Ultrafast comparator: ADCMP572 with differential output;
3. Time-to-Digital Converter (TDC): KCU116 Dev-> Tapped delay line (TDL) technology in the FPGA.

Due to analog electronics, the time resolution of one-ch TDC decrease to ~11 ps.

# 16-ch FEE prototype

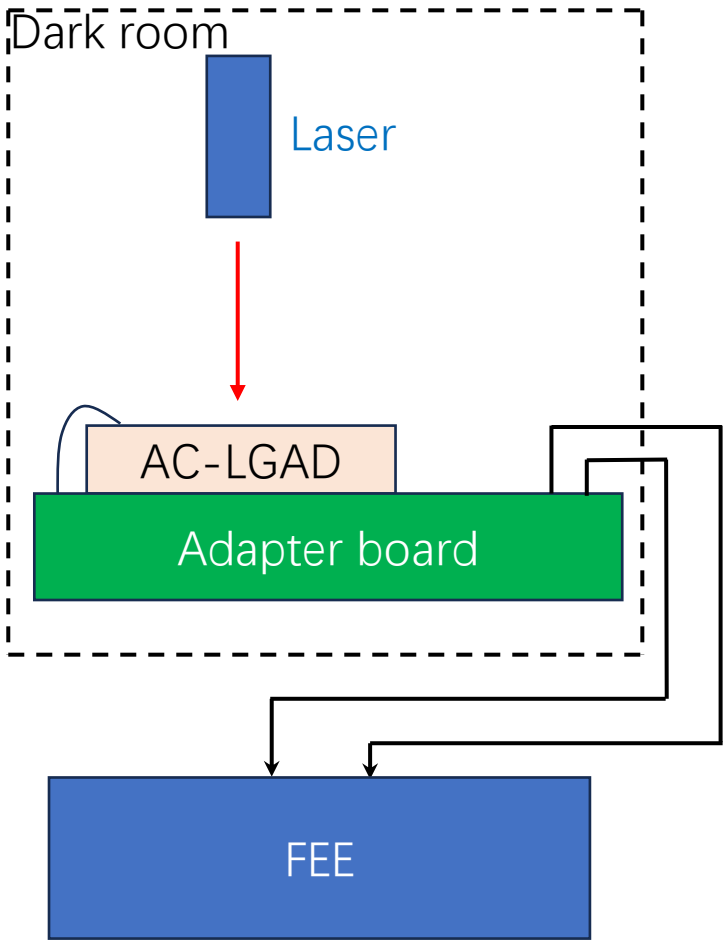



**16-ch front-end board** :

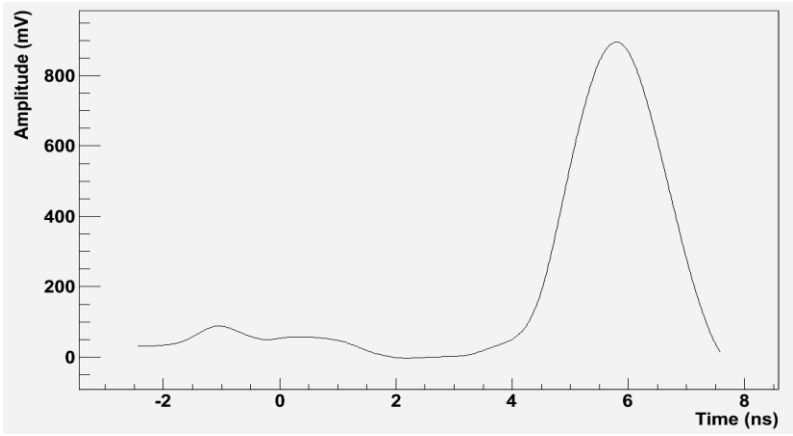
1. RF: ADL5545->6 GHz with integrated bias control circuit
2. Comparator: ADCMP572 with differential output;

**KCU116 dev :** TOT & TOA measurement

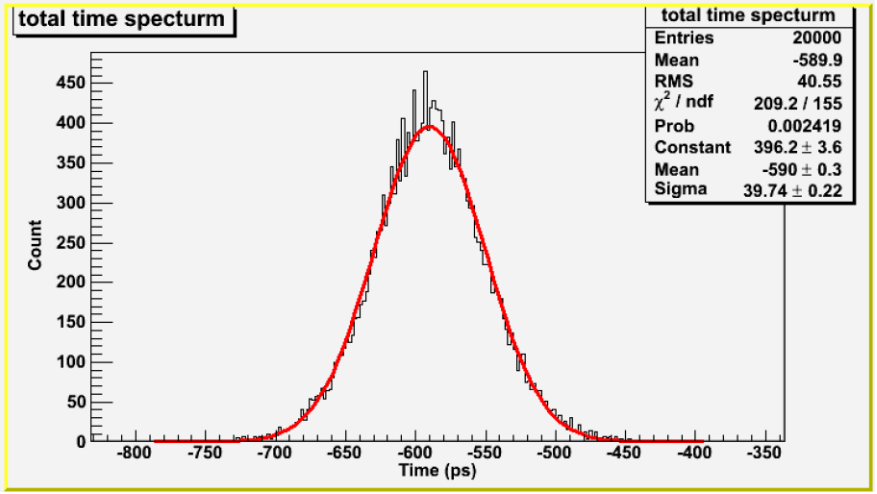
# Detector Test




Experimental setup



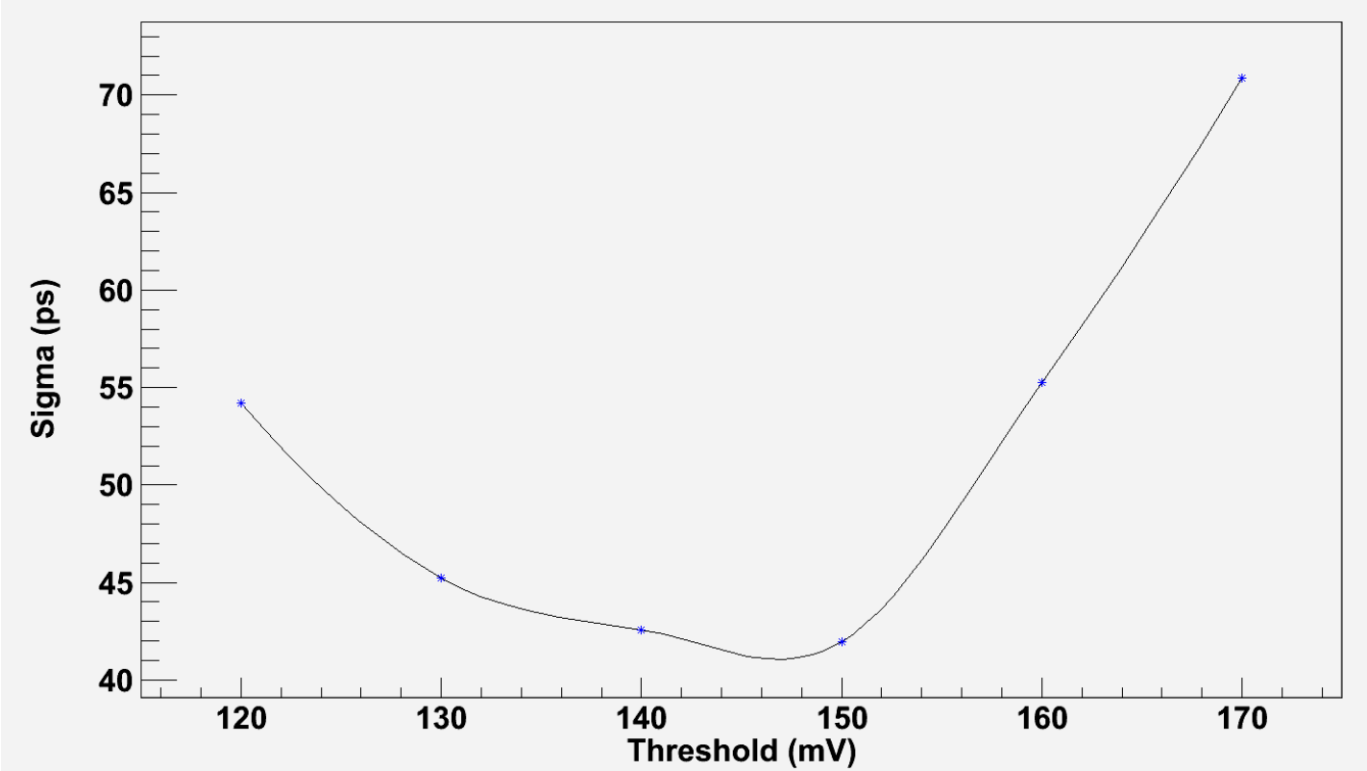

AC-LGAD signal after three-stage amplifiers (~900mV), pulse width ~3 ns




~40 ps at threshold of 145mV

# Detector Test

Rise time ~750ps




Resolution vs Threshold

# Summary

1. 16-ch FEE was implemented. Some works are ongoing:
   - Improve the measurement precision of the TOA;
   - Add the TOT measurement;
   - Try other types of amps with high BW.
2. Preliminary test results of AC-LGAD detector shows a good time resolution (~40/sqrt(2) for one channel), it could be improved after the TOT calibration in the future.

*Thanks for your listening!*