Test results of sensing diode, PLL, NMOS comparator and readout circuit of COFFEE3 pixel MAPS prototype for CEPC

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CMOS SENSOR IN FIFTY-FIVE NM PROCESS

Introduction

COFFEE3 prototype chip is fabricated with 55-nm HV-CMOS process designed to meet the requirements of CEPC inner tracker. COFFEE3 is consists of 4 sectors: 1) passive sensing diode array; 2) standalone PLL block; 3) right pixel matrix with in-pixel CSA and half part of discriminator, while other circuits at the end of column (EOC); 4) left pixel matrix with full in-pixel CSA, discriminator, TDC, while readout circuit at the end of column.

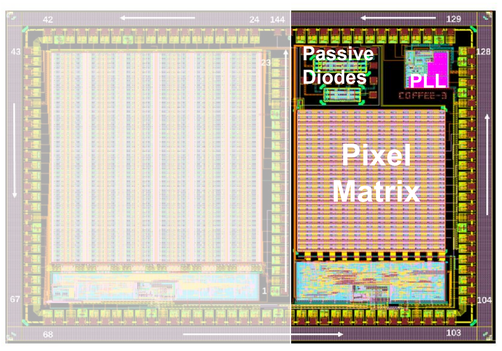

Fig1. Layout of COFFEE3 chip. Test results of the right sector are reported in this poster.

The readout out architecture of sect.3 has less cross-talk effect between digital and analog circuit, which is more suitable with the current triple-well HV-CMOS process. The sect.4 could handle higher hit density rate, while need more R&D effector. The current testing results of the first 3 sectors are presented in this poster.

COFFEE3 Test System

IV & CV test system

PC + Source Meter + homemade HV bias adapter + bare chip

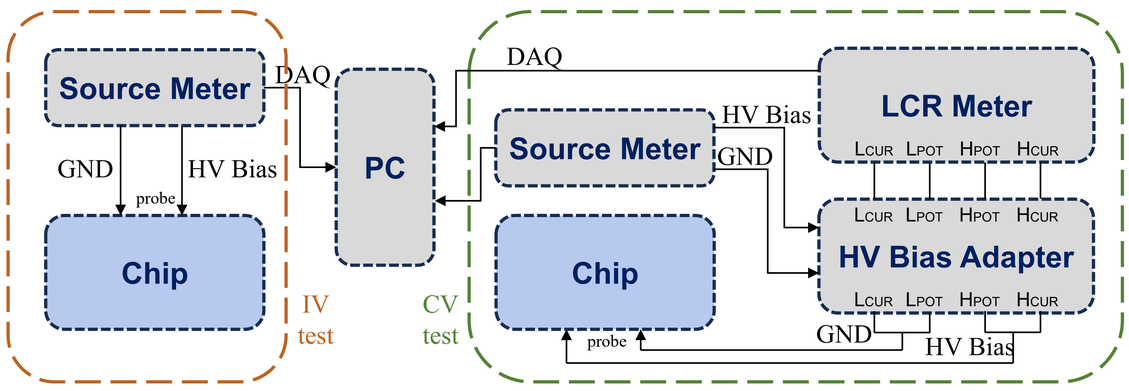

Fig2. Sketch of IV & CV test system

PLL test system

PC + power & signal supply + dedicated chip test board

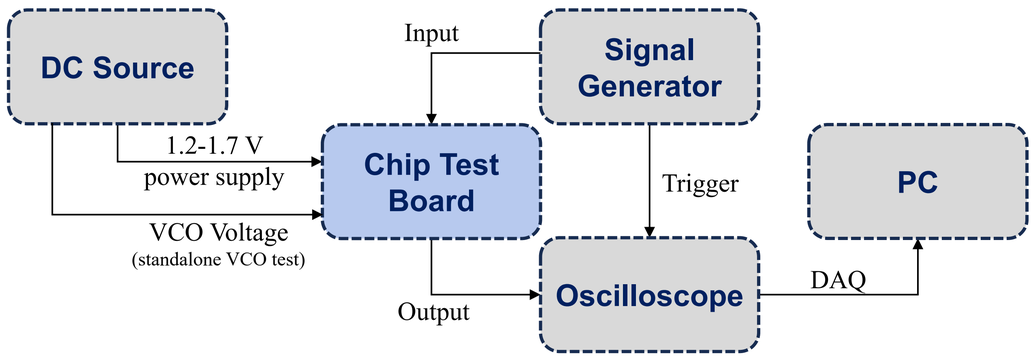

Fig3. Sketch of PLL test system

Pixel Matrix test system

PC + FPGA Board + Caribou Board + Dedicated Chip Carrier Board

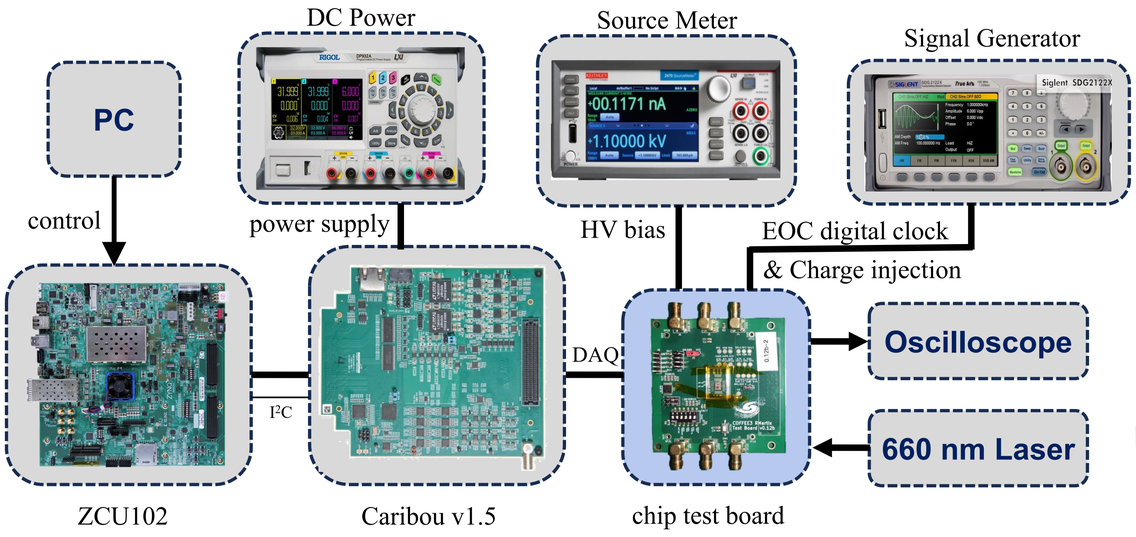

Fig4. Sketch of pixel matrix test system

- H. Liu et al., *Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade*, Journal of Instrumentation 12 (2017) P01008.
- https://caribou-project.docs.cern.ch/

Caribou is a versatile and modular DAQ system designed for prototyping silicon pixel detectors.

Main Results

Passive sensor diode IV & CV results

The passive diode array consists of two 3×3 sub-arrays, featuring pixel size of 45×145 μm² and 40×100 μm², corresponding to left and right pixel matrix, respectively. The results from 40×100 μm² sub-array 2 are presented, with its CV curve offset by a parasitic capacitance of ~247 fF.

- IV test: breakdown at ~ –70 V. Leakage current is ~140 pA at –70 V, as expected for a regular resisitivity (10 Ω · cm) wafer.
- CV test: single pixel has capacitance of ~50 fF at –70 V due to depletion. The involement of deep-p-well significantly increases pixel capacitance by ~100 fF.

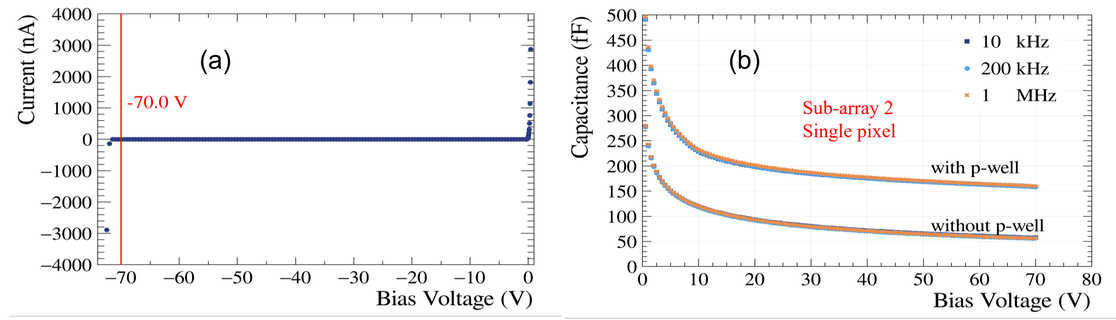

Fig5. IV test results. (a) and CV test (b) of single pixel in sub-array 2, which includes both with- and without-p-well design

PLL test results

PLL on COFFEE3 is designed for synchronization between the clock and data, as well as between multiple chips. It was designed to supply output clock with frequency of up to 640 MHz at working voltage of 1.2 V.

- Standalone VCO: with analogue power reaches 1.7 V exclusively, stable 640 MHz output can be obtained.
- Frequency multiplication: 4×, 8× and 16× at 40 MHz input clock.

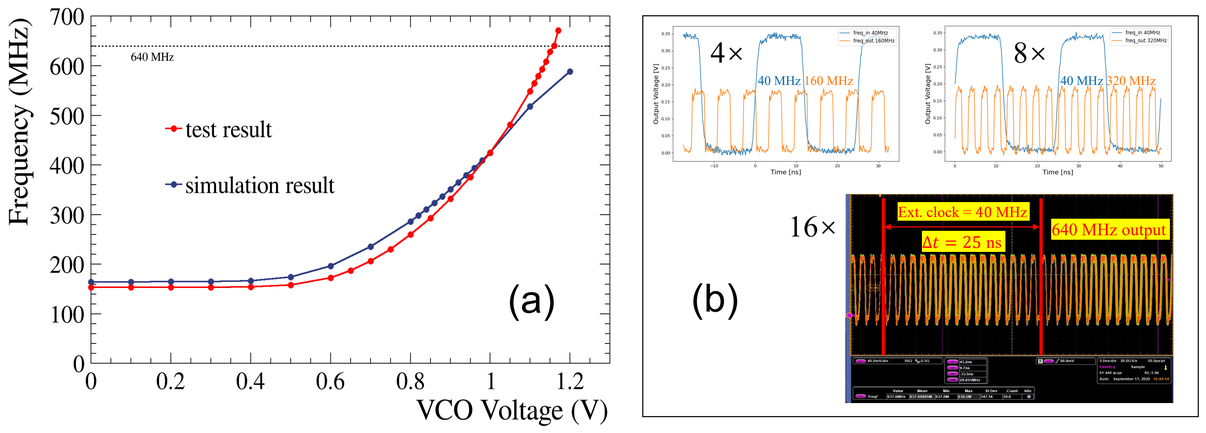

Fig5. PLL test results. (a) Standalone VCO test, frequency-voltage curve of VCO; (b) 4, 8 and 16 times frequency multiplication with 40 MHz square wave as input.

Pixel matrix test results

COFFEE3 right pixel matrix uses NMOS for in-pixel comparator only, and CMOS process for other front-end electronics. Comparator is consist of two half parts, NMOS half in pixel and CMOS half in EOC.

- Charge Sensitive Amplifier (CSA): CSA is working as expected with both charge injection and laser. Observed TOT is ~5 μs for injection and ~2.5 μs for laser.
- Laser & EOC readout test: In-pixel part of comparator works as expected, and induced EOC digital readout with pixel address can be successfully decoded.

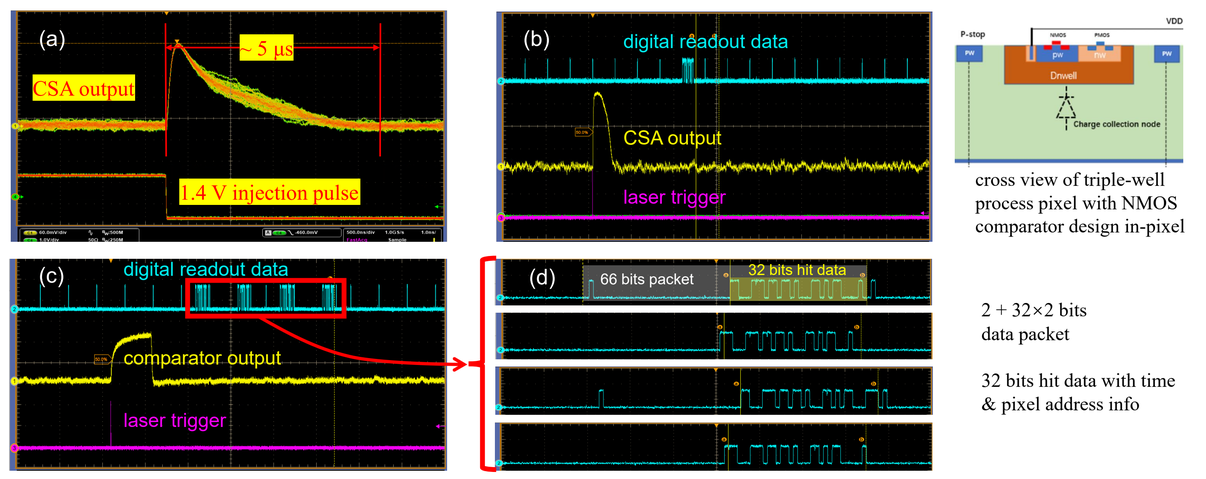

Fig5. Function verification of right pixel matrix of COFFEE3. (a) CSA response to charge injection; (b) CSA response to laser hit; (c) comparator response and digital readout of laser hit; (d) maginified digital readout waveform and data format.

Summary & Outlook

Preliminary tests using charge injection and laser confirmed that all core functions are performing as designed. COFFEE3 is dedicated to verifying the readout circuit and the core performance of a 55nm HV-CMOS technology for high-energy physics detectors. Upcoming tests will include TDAC, irradiation, and refined performance evaluations.

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