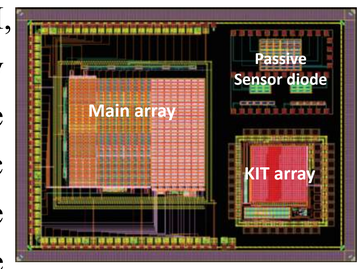
Irradiation study of COFFEE2, the first 55nm High Voltage CMOS sensor prototype

Tianyu Shi[1,2], Mingjie Feng[1,2], Yiming Li[1], Jianchun Wang[1], Zhiyu Xiang[3], Zijun Xu[1], Xuhao Yuan[1], Cheng Zeng[1,2], Hui Zhang[1]

[1]Institute of High Energy Physics, CAS, Beijing, China [2]University of Chinese Academy of Sciences [3]Central South University

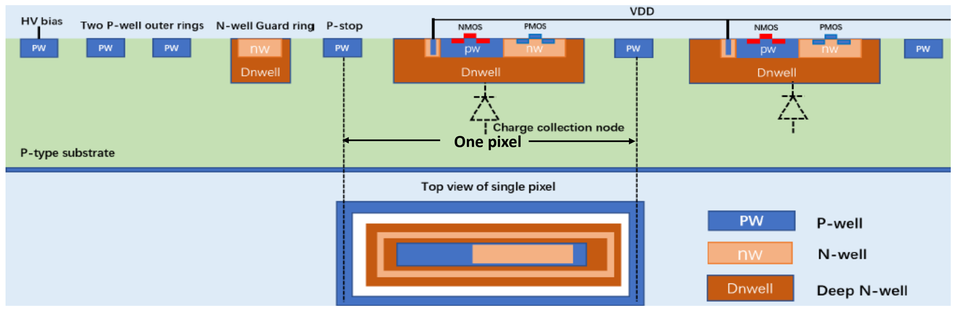
Introduction

To meet the increasingly demanding requirements of future tracking detectors for the CEPC and LHCb Upgrade II, advanced detector technologies with enhanced hit density processing capabilities and enhanced radiation tolerance are essential. To study the sensor performance and electronic response in the next generation process of High Voltage CMOS (HV-CMOS), the sensor chip called COFFEE2, the first prototype for process and circuit module in a 55 nm High-Voltage Technology, is designed and tested. A comprehensive irradiation tolerance testing campaign was conducted on the COFFEE2 chip. Utilizing the KIT pixel array, which boasts a fully integrated readout system, this work presents the first irradiation tolerance study of the 55 nm High-Voltage CMOS process.



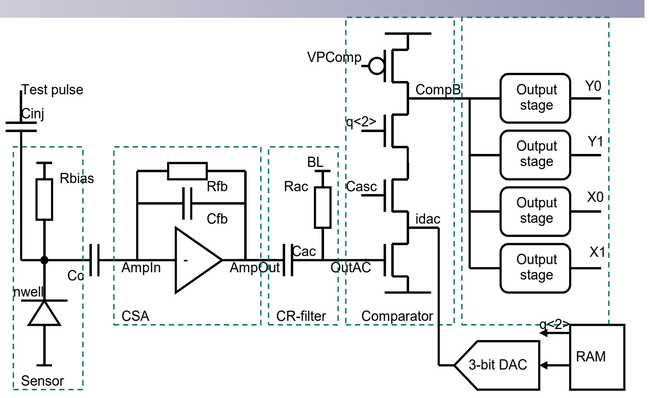
Process Features

- Deep n-well - P substrate junction as collection electrode
- Triple-well process: N-well/P-well/Deep n-well
- P-type substrate resistivity: 10 Ω·cm
- Guard ring: one inner N-well ring, with two P-well outer rings
- Substrate breakdown Voltage > 70V with frontside HV bias
- More design details:
  - Z. Chen et al., *Feasibility study of CMOS sensors in 55 nm process for tracking*, Nuclear Instruments and Methods in Physics Research A 1069 (2024) 169905.
  - H. Zhang, et al., *High voltage monolithic pixel sensor in 55 nm technology*, JINST 20 (2025) 03, C03023



KIT Pixel Electronics

- Pixel electronics (25 μm × 25 μm)
  - ✓ Sensor diode
  - ✓ Charge Sensitive Amplifier (CSA)
  - ✓ CR filter
  - ✓ Comparator
  - ✓ RAM and tune DAC
  - ✓ Output stages



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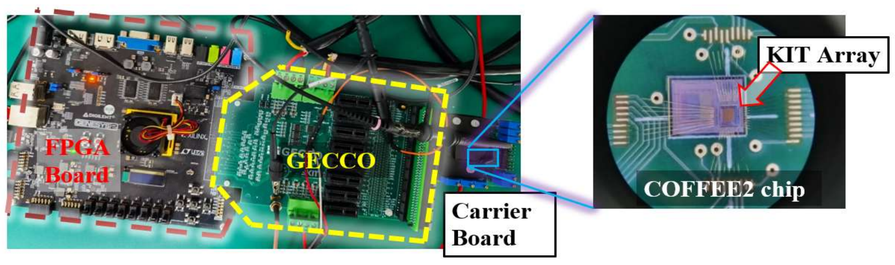
- Work principle
  - ✓ Charge collected by pixel n-well
  - ✓ Converted to voltage signal by Charge Sensitive Amplifier
  - ✓ Analog voltage pulse shaped and converted to digital signal by comparator
  - ✓ Output stage generates current
  - ✓ Current is sent via address line to the transimpedance amplifier outside matrix
  - ✓ Address lines have constant potential – no cross-talk

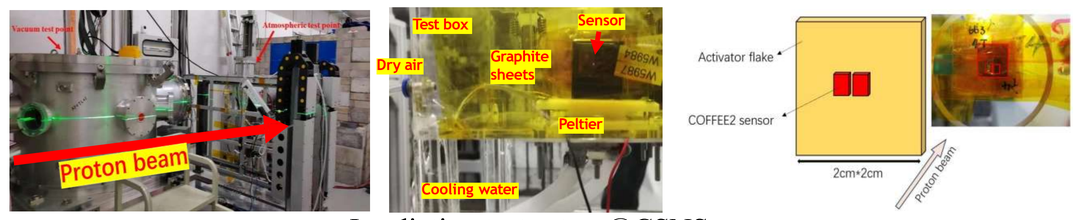
Bench test setup



- Genesys2 FPGA Board
  - ✓ Translates commands from the PC into the precise low-level digital protocol
- GECCO Control Readout Board
  - ✓ It integrates power delivery and controls and supplies all required electrical potentials for testing the chip
- Carrier Board (with wire-bonded COFFEE2 chip)
- Signal Generator
  - ✓ Provide charge injection to the chip through the GECCO board

Irradiation Test

Fluence [n_{eq}/cm^2]	3.2×10^{11}	4.9×10^{12}	5.7×10^{13}	1.6×10^{14}	1.3×10^{15}
Temperature	Room temperature				-28°C



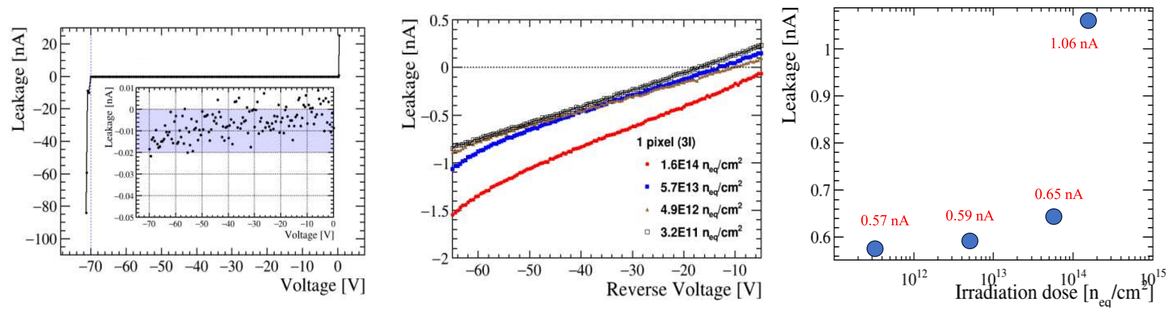
Irradiation test setup @CSNS

- Irradiated in 80 MeV proton beam at China Spallation Neutron Source (CSNS) in April 2024
- 2 sensors placed at each test point
  - ✓ 1 IV/CV tested + 1 new
- Aluminum foil pieces placed at each point to calibrate irradiation fluence

Main results

Irradiated IV change

With bias of -50V, leakage current increases from ~ 10 pA to ~ 1nA after irradiated. The magnitude of leakage current is proportional to the irradiation fluence



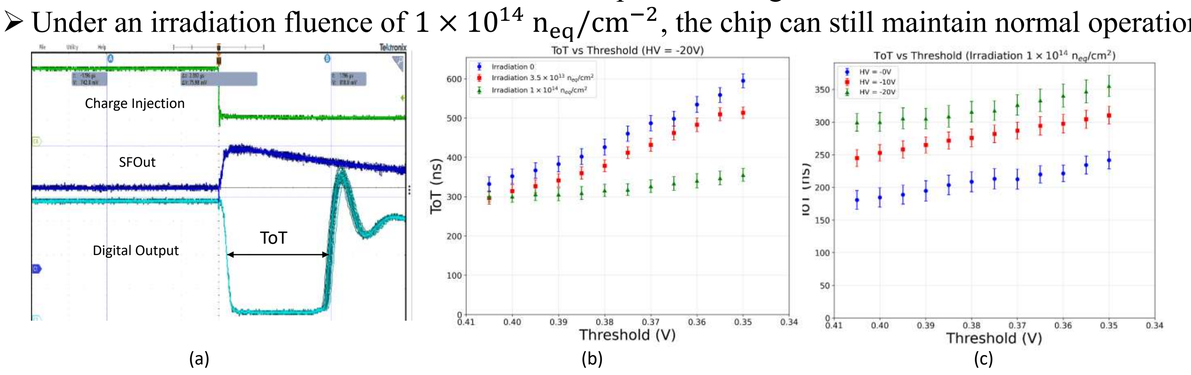
IV test results of COFFEE2 in different irradiation fluence

Irradiation Tolerance Evaluation

Time over Threshold (ToT) versus Threshold

ToT and noise rate as a function of the threshold reference for all tested samples different voltages and irradiation fluence. Results are shown for chips settings at room temperature.

- ➢ Time over Threshold (ToT) is correlated with the energy of a signal
- ➢ An increase in ToT leads to an increase in the depletion voltage
- ➢ Under an irradiation fluence of 1×10^{14} n_{eq}/cm^{-2}, the chip can still maintain normal operation.



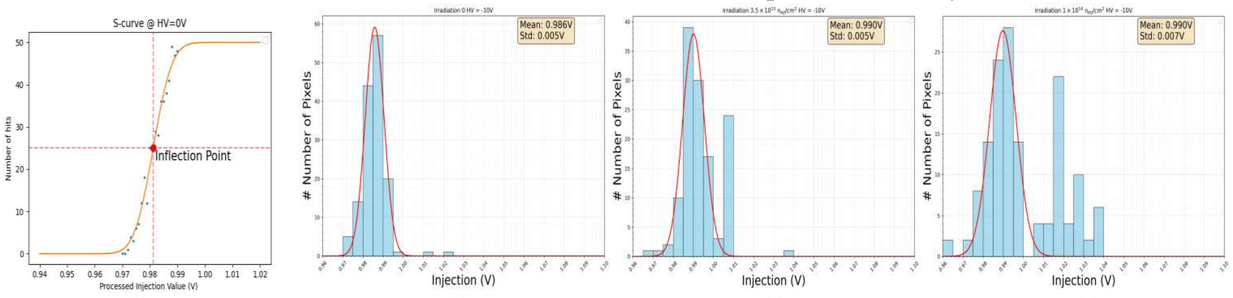
(a) (b) (c)

Chip Response to Charge Injection(a); ToT vs. Thershold in different Irradiation fluence (b); ToT vs. Threshold in different bias voltage(c)

Inflection Point of S-curve for pixels

Inflection point of the S-curve as a function of charge injection for different irradiated chips. Results are shown for HV = -10V settings at room temperature

- ➢Show the noise level of the pixel
- ➢Systematic right-shift of inflection point distribution with increased fluence
- ➢An increase in the irradiation fluence leads to a reduction in pixel uniformity



(a) (b) (c) (d)

The inflection Point of S-curve (a); The distribution of inflection point in bias voltage of -10V(b),-20V(c),-30V(d);

Summary & Outlook

The COFFEE2 chip demonstrated excellent irradiation tolerance, confirming the resilience of the 55 nm HV-CMOS process. It remained fully functional with only minor performance degradation up to an accumulated fluence of 10^{14} n_{eq}/cm^2. The observed degradation primarily manifested as a slight shift in the S-curve inflection point and a minor broadening of its distribution; nevertheless, the overall performance was well maintained. Furthermore, it was found that applying a higher bias voltage improved charge collection efficiency and increased the depletion depth, which consequently helped recover performance parameters.

Future work involves more detailed test including radioactive source test and test beam measurement.

Email: shity@ihep.ac.cn