Testing Results of the In-Pixel CSA, Discriminator, TDC, and Readout Circuit of COFFEE3 Pixel MAPS Prototype for CEPC

Yuman Cai[1], Mengke Cai[1], Leyi Li[1,3], Yiming Li[1], Weiguo Lu[1], Dexing Miao[1], Boxin Wang[1], Jianchun Wang[1], Xiaomin Wei[2], Zhiyu Xiang[1,5], Zijun Xu[1], Cheng Zeng[1], Xiaoxu Zhang[1,4], Yang Zhou[1]

[1]Institute of High Energy Physics, CAS, Beijing 100049, China [2]Northwestern Polytechnical University, Xi'an 710129, China
[3]Shandong University, Qingdao, Shandong 266237, China [4]Nanjing University, Nanjing 210093, China [5]Central South University, Changsha 410083 China

CEPC 2025

COFFEE: CMOS sensOr in FIFTY-FIvE nm proceSs

Introduction

To address the requirements of CEPC inner-tracker, the COFFEE3 chip was developed using an advanced 55 nm High Voltage CMOS (HV-CMOS) process for high spatial and time resolution and low power consumption,COFFEE3 is designed to validate two distinct readout architectures integrated on a single chip, focusing on verifying circuit functionality and core performance. This poster presents the preliminary test results for the left-side array, which features a more complex in-pixel design incorporating a full CMOS-based CSA, discriminator, TDC, and priority-based readout, targeting higher hit-rate environments. Bench tests utilizing laser and radiation sources successfully demonstrate the basic functionality of the in-pixel circuits and the full readout chain at digital peripheral which also including the serializer and LVDS transceivers.

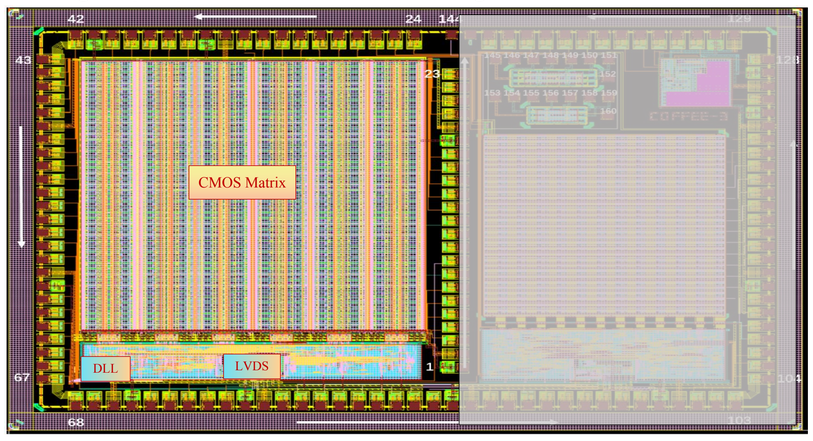


Fig 1 Layout of COFFEE3 chip for the left-side array

Left-side Array Design

Chip OVerview

- ✓ Chip Size: 4000 μm × 3000 μm
- ✓ Core Array: 48 (Rows) × 12 (Columns)
- ✓ Pixel Pitch: 40 μm (Column) × 145 μm (Row)

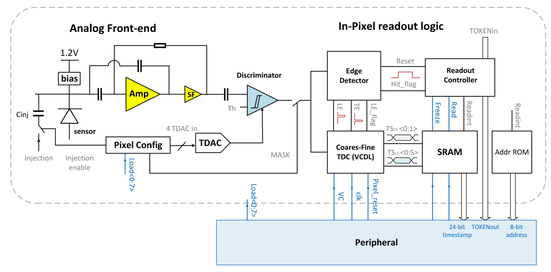


Fig 2 Functional schematic of the in-pixel circuitry

Pixel Array

- ● Analog Front-End
  - ✓ 4 Types of Charge-Sensitive Amplifiers (CSA)
  - ✓ CMOS Discriminator with Threshold Adjustment TDAC
- ● Readout Circuit & In-pixel Memory
  - ✓ Time-to-Digital Converter (TDC)
  - ✓ In-Pixel RAM & Address ROM

Innovative CSA

A unique "Double-Column" unit groups pixels for testing four CSA variants side-by-side:

- ✓ Double-Column 1: Cascode CSA
- ✓ Double-Column 2-3: Sensor-Isolated Cascode CSA
- ✓ Double-Column 4: Folded Cascode CSA
- ✓ Double-Column 5-6: Sensor-Isolated Folded Cascode CSA

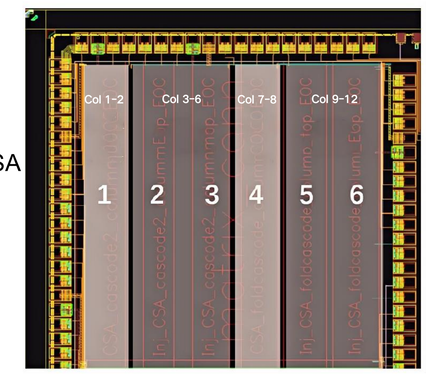
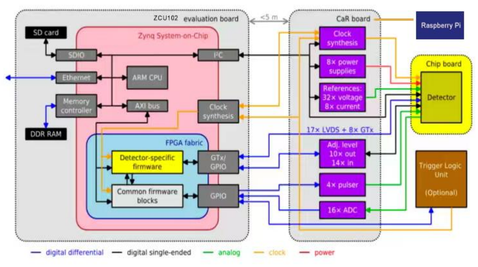


Fig 3 Left-side CMOS pixel array layout

Test Setup



Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Resources for various target applications

Fig 4 Caribou test system architecture & feature of CaR board

Pixel Matrix Test System

Test platform is based on Caribou system

- ✓ PC + ZCU102 + Caribou board + chip carrier board
- ✓ ZCU102 evaluation board from AMD/Xilinx
- ✓ CaR board DAQ framework from Caribou Project
- ✓ ASIC specific SW and FW by IHEP

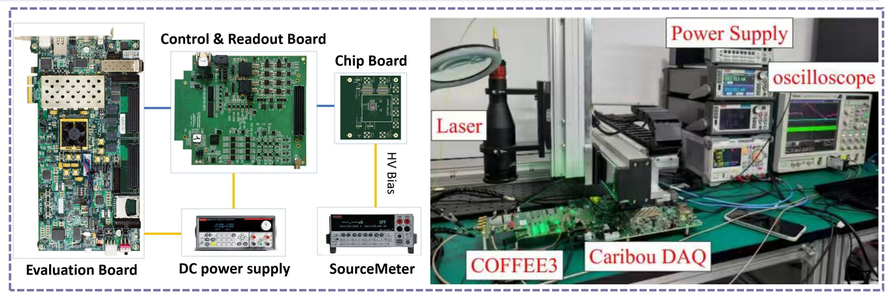


Fig 5 Photograph of the implemented test setup

Test Results

Pixel Matrix Test System

- ● Low-Voltage Differential Signaling (LVDS)

At 640 MHz supporting to 1.28 Gbps high speed data transmission, to reduce common mode noise.

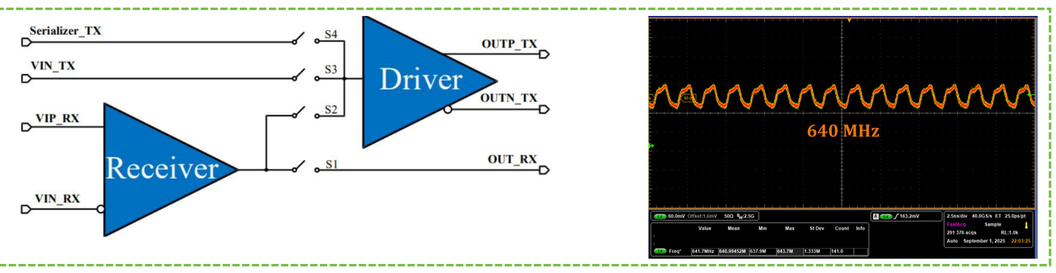


Fig 6 LVDS Overview & Functional Verification

- ● Delay-Locked Loop (DLL)

The phase difference matches expectations, to achieve a finer binning in time (~4 ns) than the main clock (23 ns).

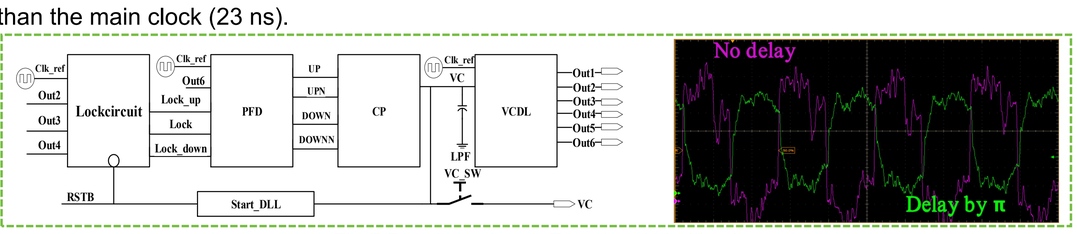


Fig 7 DLL Overview & Functional Verification

- ● Empty Packet Test

The expected Empty Packet was successfully read out.

- ● Pixel Mask Test
  - ✓ Successfully verified by enabling only a single pixel.
  - ✓ Data stream correctly switched between Empty Packet and Valid Hit Packet, confirming proper self-triggered readout logic and per-pixel control.

Fig 8 Empty Packet Output

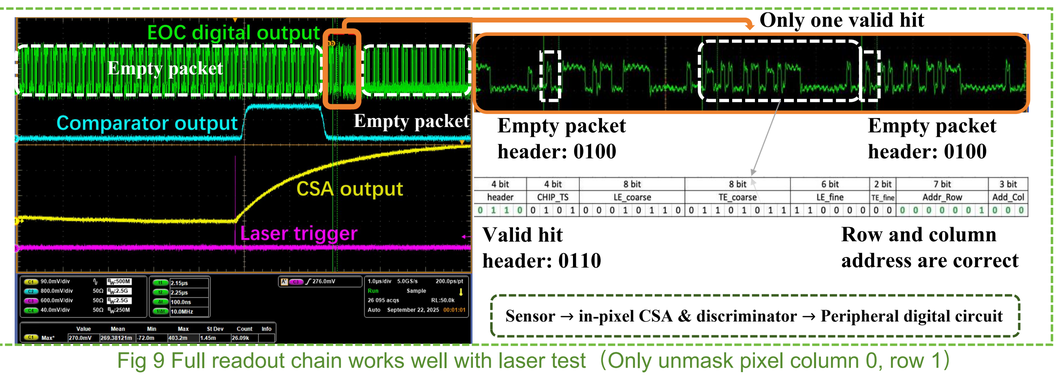


Fig 9 Full readout chain works well with laser test (Only unmask pixel column 0, row 1)

In-pixel Analog Test

- ● Charge Injection Test
  - ✓ Four types of CSA demonstrated correct functionality through direct charge injection.
  - ✓ Clear linear response to injected charge confirms predictable analog chain performance.

Reference Voltage	Set Value (V)	Default Value (V)
A1	0.45	0.447 (range: 0.1–0.7)
A2	0.94	0.910 (range: 0.7–1.2)
A3	0.97	0.759 (range: 0.6–1.2)
B1	0.93	0.930 (range: 0.7–1.2)
B2	0.80	0.547 (range: 0.1–0.8)
B3	0.75	0.746 (range: 0.6–1.2)
B4	0.60	0.500 (range: 0.1–0.7)

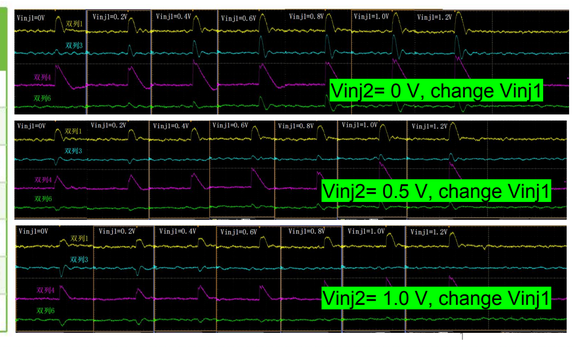


Fig 10 Peripheral digital circuit readout for charge injection test

- ● Laser Test

Pixel can response to laser signal, CSA and comparator work as expected and typical time over threshold (TOT) of laser signal is consistent with simulation.

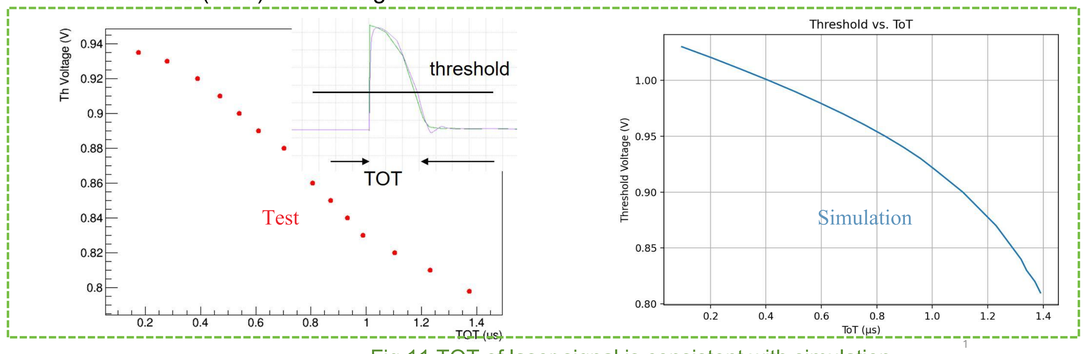


Fig 11 TOT of laser signal is consistent with simulation

- ● ^{55}Fe Radioactive Source Test

Pixel can also response to ^{55}Fe signal (x-ray).

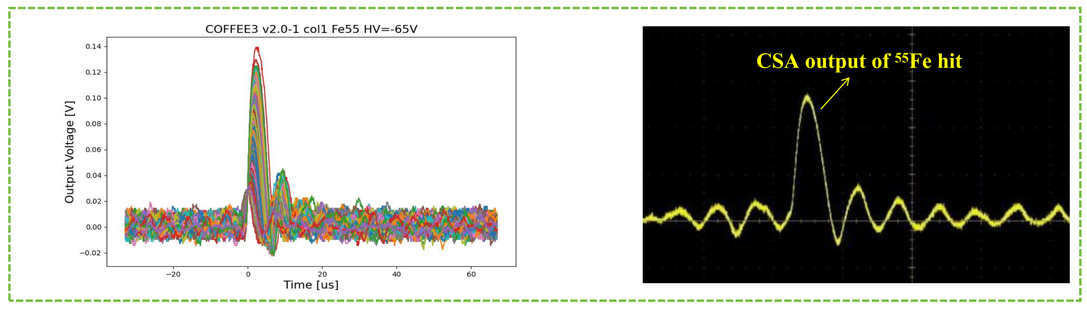


Fig 12 ^{55}Fe Radioactive Source test results

Summary & Outlook

- ● **Summary**

COFFEE3 left-side array preliminary testing results validates the basic functional design:

- ✓ Full Chain Operational: In-pixel circuits (CSA, discriminator, TDC) and peripheral logic are correct.
- ✓ Performance Verified: Achieved Gbps LVDS output, precise DLL clocking.
- ✓ Detection Confirmed: Clear response to charge injection, laser, and ^{55}Fe source demonstrated.

- ● **Outlook**

Future work will focus on detailed performance characterization and design optimization:

- ✓ Perform energy spectrum analysis on the collected ^{55}Fe data to quantify the energy resolution.
- ✓ Conduct beam tests with high-energy particles to evaluate spatial resolution, detection efficiency.
- ✓ Utilize the feedback from these tests to inform the optimization of the next-generation chip design.