

Capacitance Optimization of AC-LGAD Sensors through Novel Structure Design and TCAD Simulation



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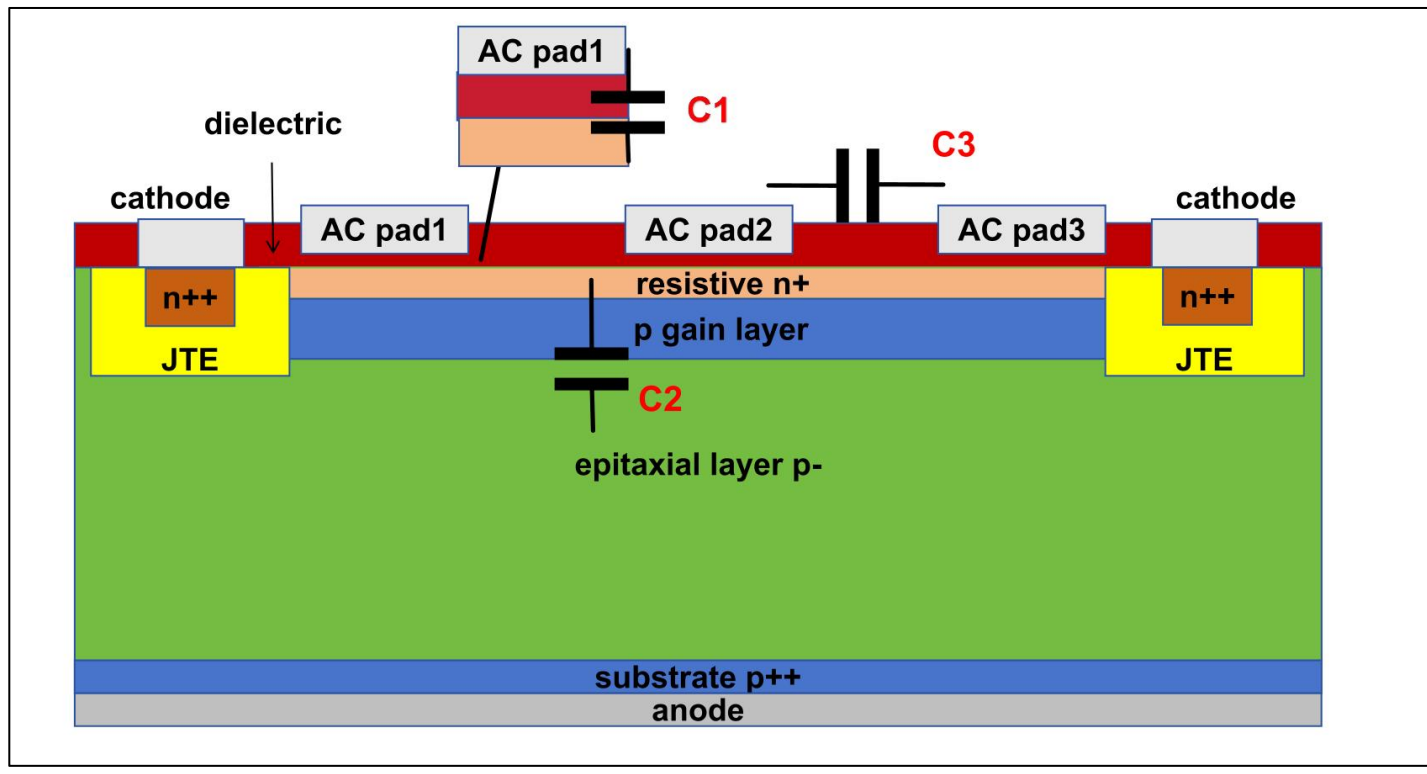
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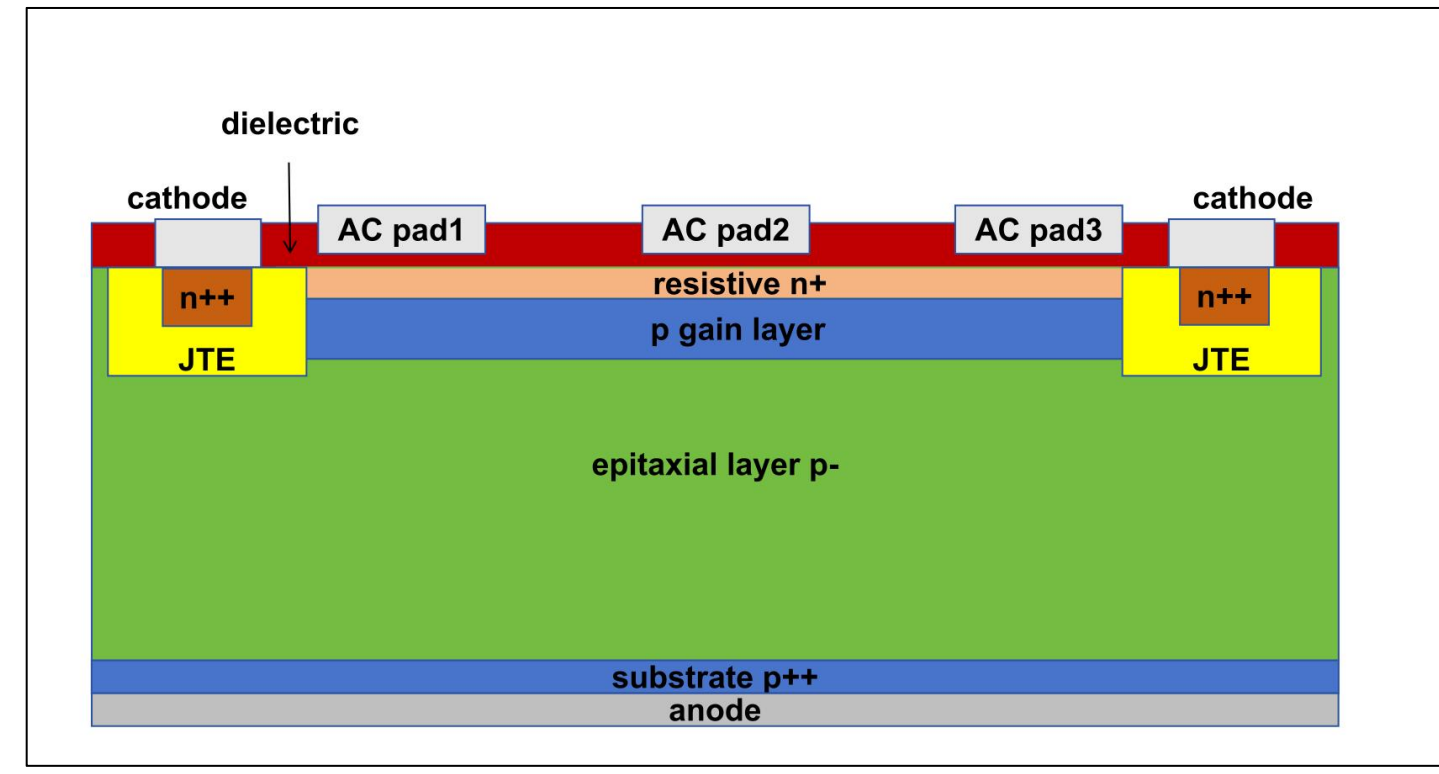
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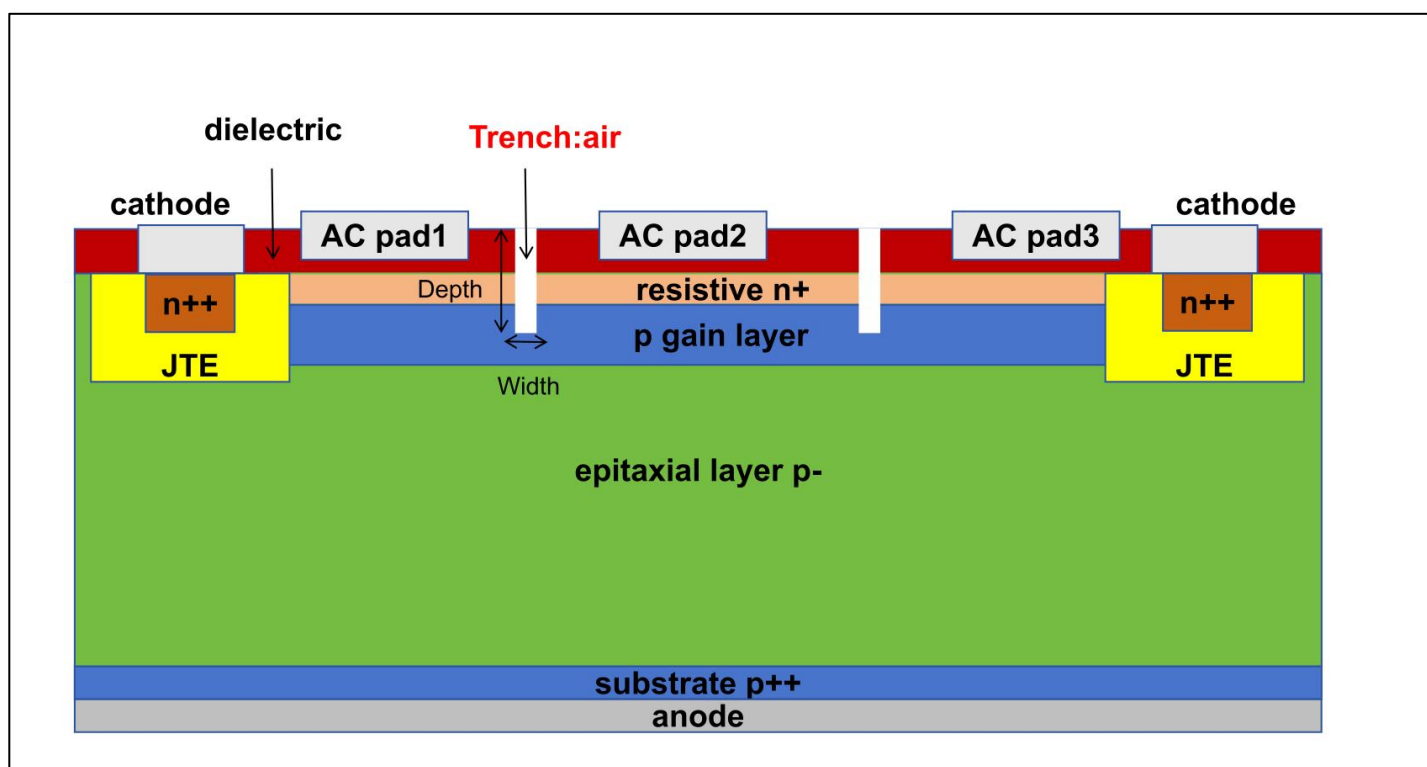
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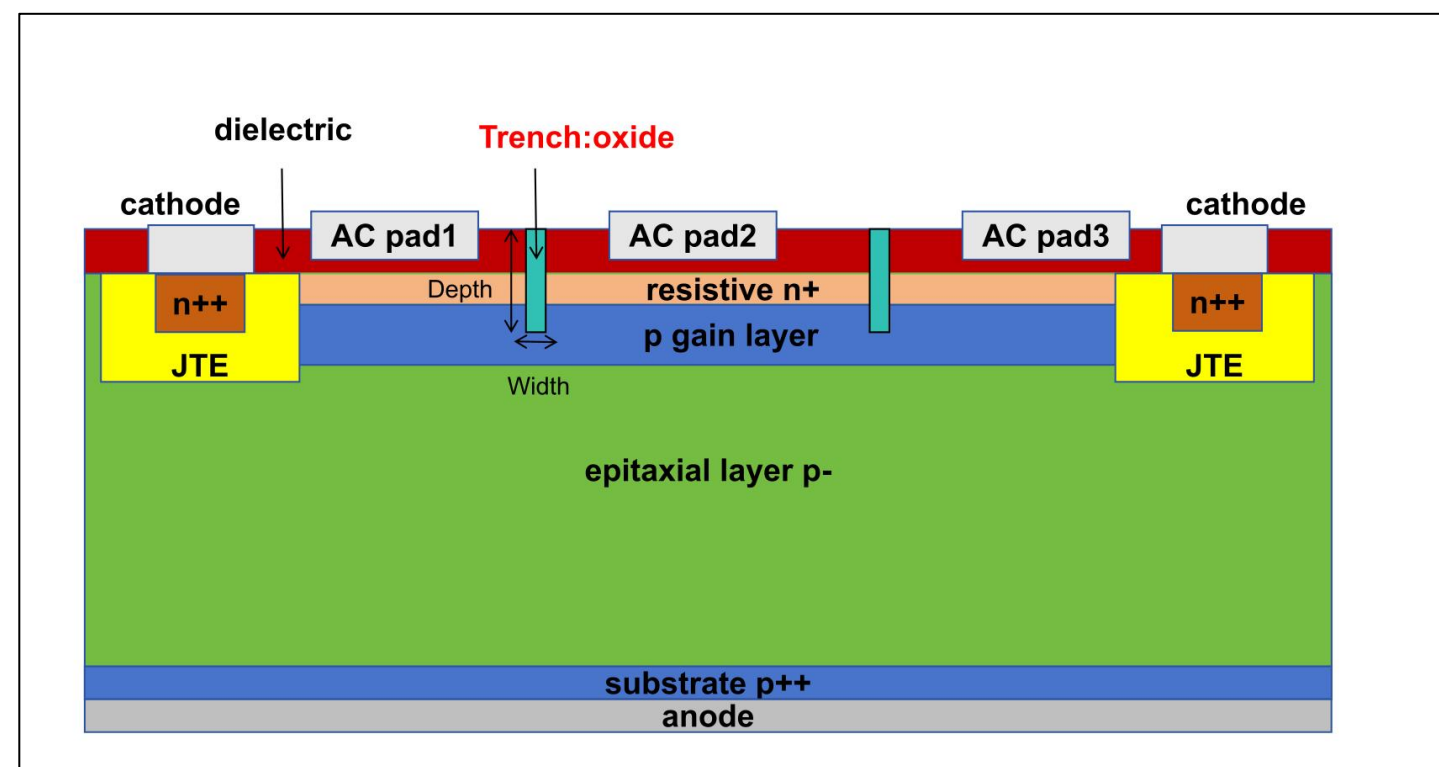
(a) Capacitance schematic of AC-LGAD with 3 AC pads



(b) Sketch of AC-LGADs with 3 AC pads



(c) Schematic of AC-LGADs with 3 AC pads and oxide-gap isolation



(d) Schematic of AC-LGADs with 3 AC pads and air-gap isolation

Fig. 1 Schematic diagrams of AC-LGAD structures: (a) Capacitance schematic (b) traditional structure, (c) with air-gap isolation, and (d) with oxide-gap isolation

Novel Low-Capacitance AC-LGAD Design: Core Innovations

- **Low-k Dielectric Isolation**
 - ◆ Method: Add trenches (filled with SiO₂ or air) between resistive electrodes.
 - ◆ Effect: Low-k materials cut electric field coupling, reducing $C_{\text{inter-pad}}$ by decreases by more than three orders of magnitude.
 - ◆ Outcome: Minimizes crosstalk, enhances spatial resolution.
- **Optimized Isolation Geometry**
 - ◆ Method: Tune isolation structure depth/width via simulations.
 - ◆ Effect: Deeper trenches concentrate electric fields; optimized width balances isolation & compactness.
 - ◆ Outcome: Ideal capacitance reduction, maintains practical sensor dimensions.

Electric Field Distribution Analysis

- Setup: 4 μm Depth, 0–10 μm Widths for Electric Field Distribution Study
- For the isolation width, both 1 μm and 3 μm are fully depleted

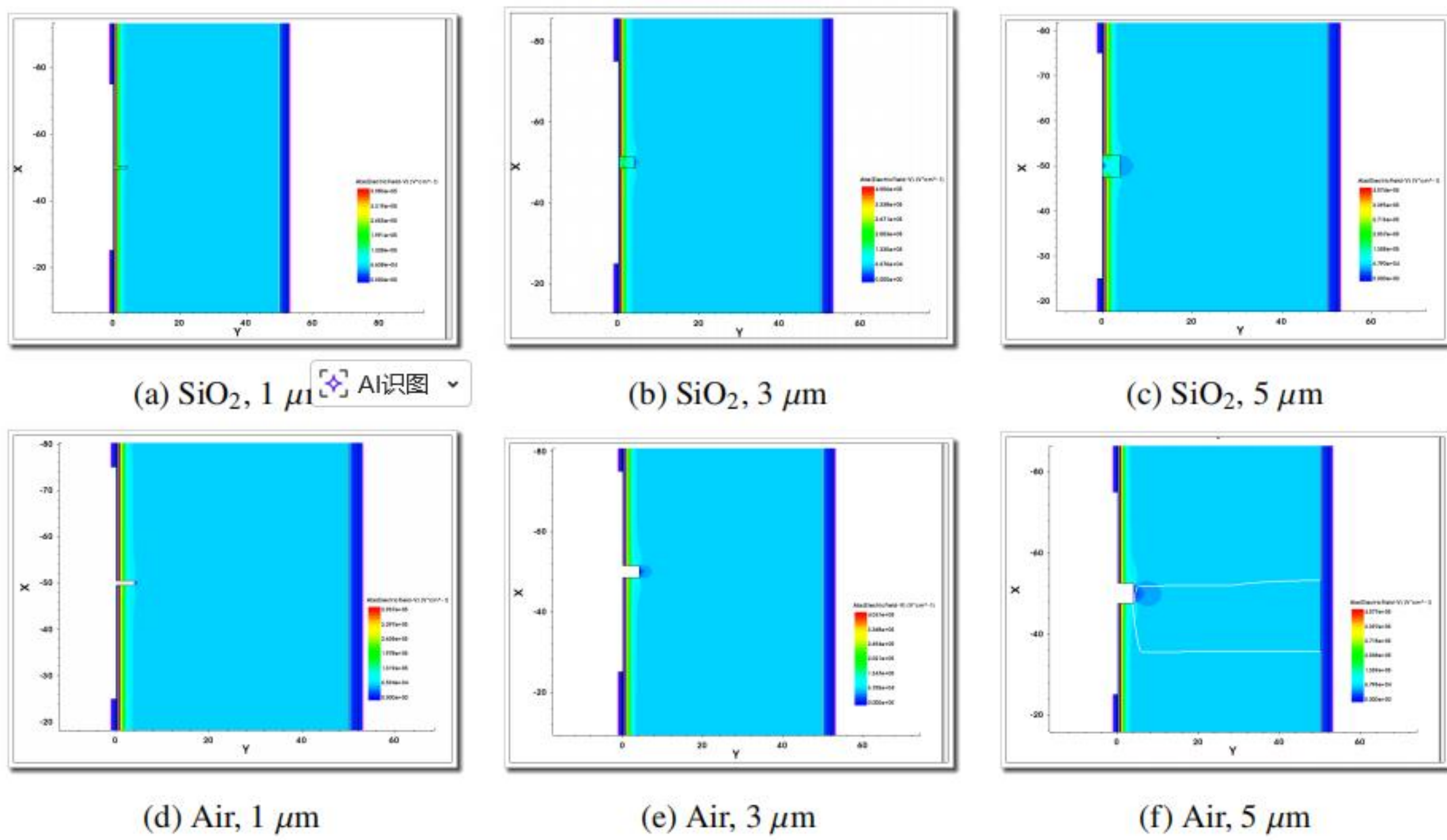


Fig. 4 Electric Field Distributions: Isolation Structures' Effect

Summary

This work presents a Isolated-Structure low-capacitance AC-LGAD structure utilizing low-k dielectric isolation and optimized geometry. TCAD simulations demonstrate significant capacitance reduction: Bulk capacitance decreased to one strip capacitance, while inter-pad capacitance decreases by over three orders of magnitude with increasing isolation width (0-10 μm). For same trench size parameters, Air isolation outperforms SiO₂, providing 30% additional reduction in inter-pad capacitance.

Key Parasitic Capacitances in AC-LGAD Sensors

- **C1 (Coupling Capacitance, C_{coupling})**
 - Location: Metal readout strips $\leftrightarrow$ semiconductor gain layer (across dielectric)
 - Impact: Weakens signal, slows rise time, distorts waveform
 - Dependence: Dielectric thickness, permittivity, effective area
- **C2 (Bulk Capacitance, C_{bulk})**
 - Location: p–n junction (n gain layer $\leftrightarrow$ p+ gain layer with the p- epitaxial layer; space charge region as capacitor)
 - Impact: Forms low-pass filter (with front-end capacitance) $\rightarrow$ attenuates high-frequency signals, degrades timing precision
 - Dependence: Follows $C = \frac{\epsilon S}{d}$; relies on gain layer/backplane area, separation, medium permittivity
- **C3 (Inter-Pad Capacitance, $C_{\text{inter-pad}}$)**
 - Location: Adjacent resistive electrodes (via semiconductor bulk, from inter-electrode electric fields)
 - Impact: Causes crosstalk $\rightarrow$ interferes with position reconstruction, limits spatial resolution
 - Dependence: Electrode spacing, semiconductor permittivity, thickness under electrodes

TCAD Simulation of Different Isolation Structure Parameters

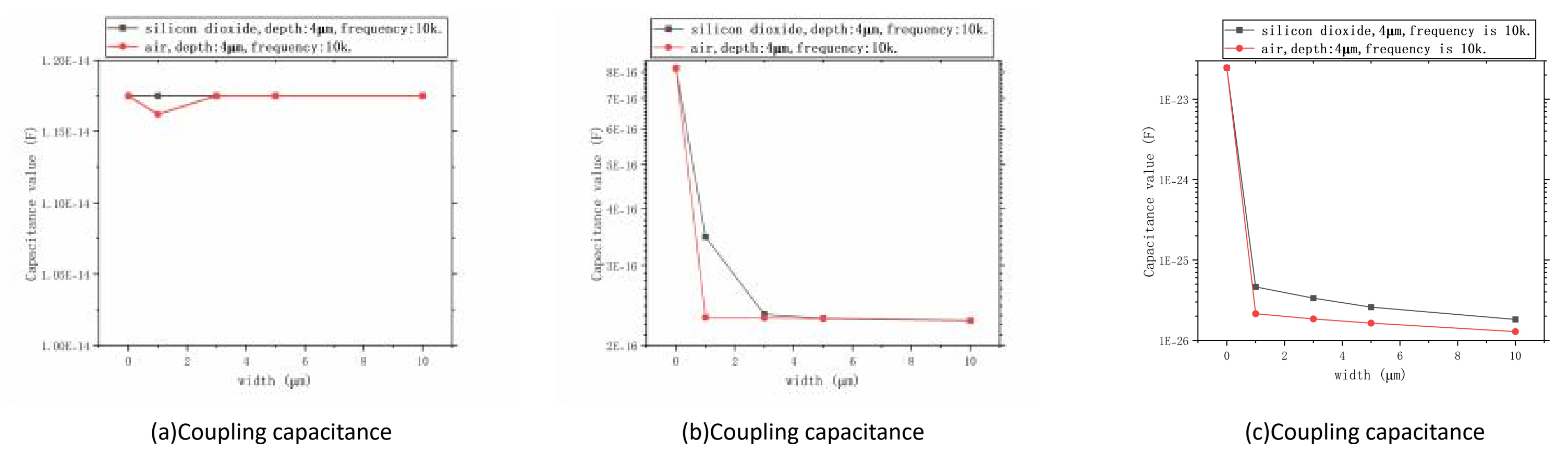


Fig. 2 Effect of different isolation widths on capacitance parameters at a fixed depth of 4 μm .

- Setup: Fixed isolation depth (4 μm), tested isolation widths (0–10 μm) to study capacitance changes.
- Key Trends:
 - $C_{\text{inter-pad}}$: Drops by >3 orders of magnitude (width 1 $\rightarrow$ 10 μm), Fig. 2(b).
 - C_{bulk} : with theoretical calculations yielding $\sim 3 \times 10^{-16}$ F that matches Figure 3(b) experimental data. ($\epsilon = 3 \times 10^{-11}$ F/m, $S = 5 \times 10^{-11}$ m², $d = 50$ μm)
- Minor Impact: Isolation width has little effect on C_{coupling} .

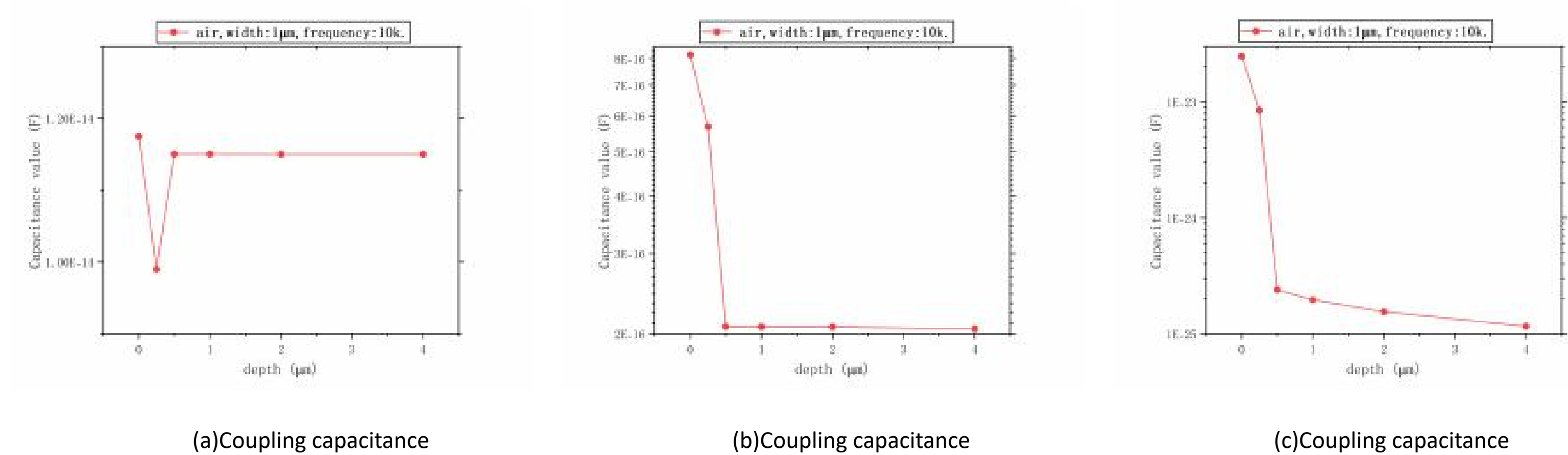


Fig. 3 Isolation Depth vs. Capacitance (Air, 1 μm Width, 10 kHz)

- Setup: Fixed isolation width (1 μm), tested isolation depths (0–4 μm) to study capacitance changes.
- Observe:
 - The capacitance reduction at a depth of 0.25 μm is far less effective than that at other depths.