Prototype assembly and tests for CEPC VerTeX detector

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1. Introduction

The first four layers of the CEPC (Circular Electron Positron Collider) VTXD (VerTeX Detector) are designed using wafer-scale sensors based on stitching technology. To ensure the inner most layer is as close as possible to the central beam pipe, the design radius is set at 11.1 mm, posing significant challenges for the development of bent detector modules. In this study, a complete prototype module is designed and developed to validate bent chip bonding techniques. Additionally, to verify the performance of silicon pixel sensors after bending, a small-area bent detector module with a radius of 20 mm was fabricated using 50 μm-thick MAPS (Monolithic Active Pixel Sensors) chips.

■Vertex detector design from CEPC TDR

The VTX is designed as six concentric cylindrical pixel layers covering a radius of 11.1 mm to 47.9 mm around the beam pipe, with a polar angle coverage of $|\cos\theta| < 0.99$.

➢ Inner layers (1-4 layers) with stitching design
➢ Outer layer (layers 5 and 6) with double-sided ladders design

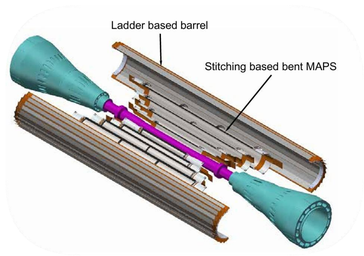

Fig.1 CEPC Vertex detector

$$\sigma_{r\varphi} = a \oplus \frac{b}{p(GeV)sin^{3/2}\theta}\ \mu m$$

a = 5 μm and b = 10 μm·GeV

Parameter	Design
Spatial Resolution	~5 μm
Material budget	~0.8% X_0
First layer radius	11.1 mm
Mechanical Support	Ultralight structures
Angular Coverage	$\|\cos\theta\| < 0.99$
…	…

Table.1 Vertex detector design parameter

■R&D of the inner layer VTXD prototype

➢ Producing a full-sized vertex detector's first four layers using ultra-thin curved stitched chips is highly challenging, and the process development is crucial
➢ As the first four layers of CEPC VTXD, the radius are 11.1 mm, 16.6 mm, 22.1 mm, and 27.6 mm respectively
➢ This study can validate the processes for the minimum bending radius, full-sized bent detection module (long-readout FPC), and the assembly processes to accumulate valuable experience for CEPC VTXD

2.Prototype module design

■Prototype module design

The full-sized prototype model consists of the FPCs (Flexible Printed Circuits), thinned dummy sensors, Cylindrical support (including the chip supports and FPC supports structure).

Layer	Chip Length mm	FPC Length mm	Chip width/arc length mm
Layer1	161.4	145.2	34.54
Layer2	121.1	104.8	51.81
Layer3	161.5	64.4	69.08
Layer4	134.6	24	86.35

Table.2 ¼ VTXD prototype module design parameter

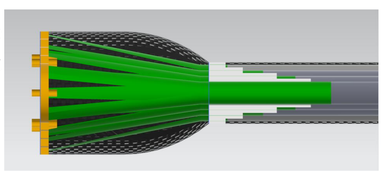

Fig.2 ¼ VTXD prototype module

➢ **Dummy sensors.** The thickness is thinned to 30-40 μm. The Layer1-3 are cut from 8-inch wafers, and the Layer4 is cut from a 12-inch wafer
➢ **Chip supports.** Select PMI foam (~0.075 g/cm^3), which offers high structural strength and low material budget. To ensure the strength of the support structure, holes are drilled in the foam to enhance airflow for better heat dissipation, while further reducing material budget
➢ **FPCs.** The composite FPC consists of three layers of 37.5 μm thick Cover layer, 18 μm thick signals (Copper), and 50 μm Core FR4

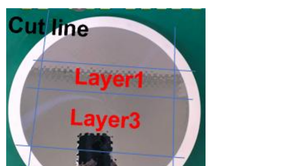

Fig.3 8-inch dummy wafer

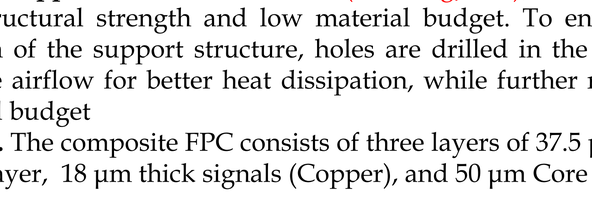

Fig.5 FPC structure

Fig.4 Chip support

➢ **FPC supports.** Using 3D printing, positioned outside the polar angle θ between the chip and FPC, and fix and support the FPCs. Protecting the lower chips from contact with the upper FPCs

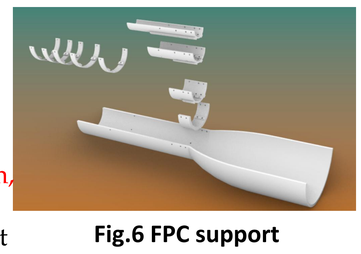

Fig.6 FPC support

■Material budget

➢ Gray represents the PMI support position, the rings width is 10 mm, and red indicates the detector position
➢ Average material budget per sensitive layer **: ~0.1068 %X_0,** The next step is to optimize the structure and minimize the material budget

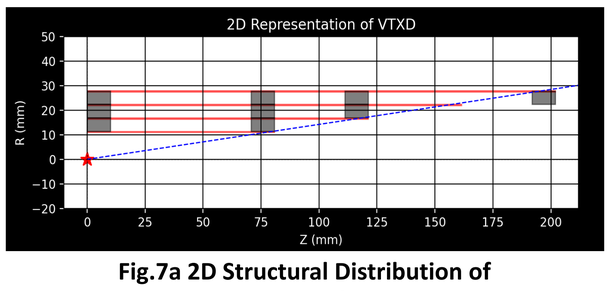

Fig.7a 2D Structural Distribution of VTXD prototype in the Z Direction

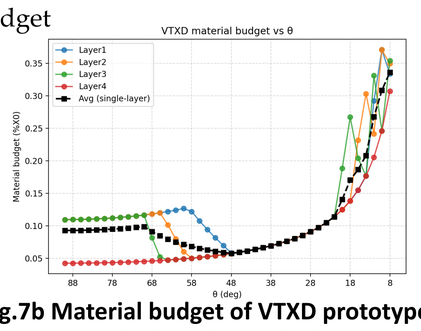

Fig.7b Material budget of VTXD prototype with the polar angle θ

3. Prototype module assembly

Validation and successful of a bent dummy wafer with an 11 mm radius without wire bonding.

■ Assembly

First wire bonding, then bending together.

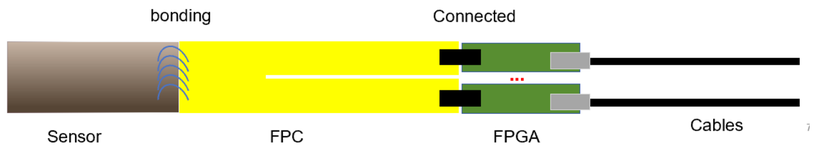

Fig.9 Full-sized Prototype module structure

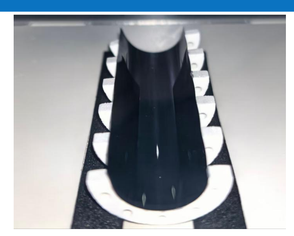

Fig.8 11 mm radius bending Without damage

➢ **Glued.** The non-sensitive area of the chip is glued to the edge of the FPC (2 mm margin) using liquid insulating adhesive. The adhesive thickness is controlled at 50 μm
➢ **Wire bonding.** The chip is bonded to the FPC and electrically connected through bonding
➢ **Bending.** After bonding, the detector module is fixed onto the spool and slowly curled together
➢ **Support.** four layers, with reasonable screw holes designed based on practical experience, secured with screws

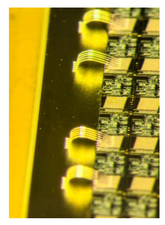

Fig.10a Wire bonding

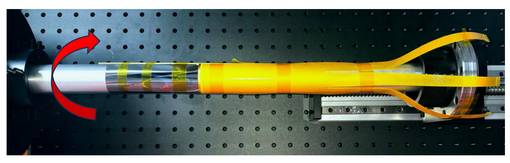

Fig.10b Bending

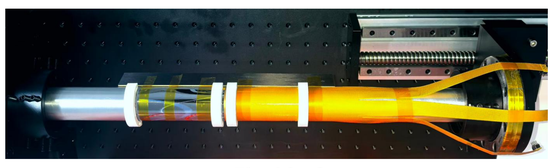

Fig.10c Support

■Pull Test

➢ The tensile results before and after bending are consistent
➢ all tensile results ranging from 4-8 g, which is related to the quality of the pads on the dummy chip

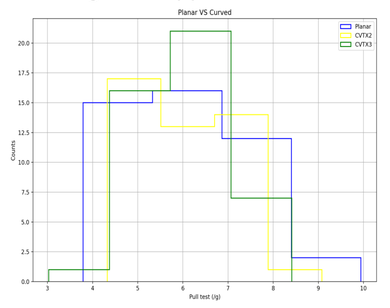

Fig.11 The pull test before and after bending

4. Performance tests after bending

■Small bent detector

To verify the performance of the chip after curling, a small-area curled detection module was designed and tested.

➢ The bent detector module based on MAPS primarily comprises a bending support frame, a test readout board, and a chip
➢ The bending radius is 20 mm

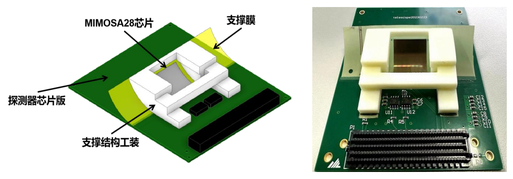

Fig.12 A small bent detector module

■Test Results

➢ The noise level tests on the same chip before and after bending remain consistent.
➢ The test beam was conducted at IHEP, and the residual distribution is consistent before and after bending.

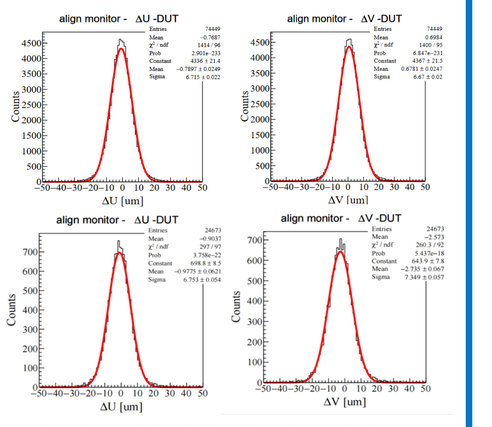

Fig.13 Residual distribution of Planar detector and bent detector

■Next plan

➢ Using a small-area MAPS chip, performance tests were conducted on the full-sized detector (including the long readout FPC) after bending.

Fig.14 full-sized bent detector design

5. Summary

- From the requirements of CEPC TDR, the vertex detector consists of six layers, with the innermost four layers using stitched chip.
- A full-sized VTXD prototype model was designed, with a low material budget of about 0.1068% X_0 per layer.
- Key components were designed and produced, optimizing the VTXD assembly process.
- The tensile results before and after bending are consistent.
- The performance of the bent detector is consistent with that of the planar detector. The next step is to enhance the performance testing of the long-readout bent module.