



HV-MAPS for the Mighty-Tracker of the upgraded LHCb detector

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5 November 2025





LHCb - a forward spectrometer at the LHC

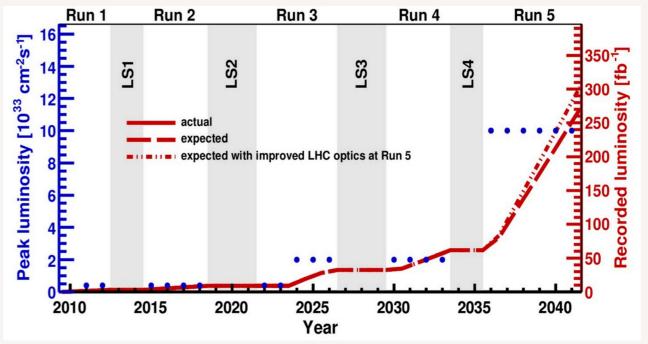
 Designed to explore large cross section for bb, cc production in the forward region

> Integrated luminosity:

today: 31.7 fb⁻¹

end of Run 4: ~50 fb⁻¹

end of Run 5: $\sim 300 \text{fb}^{-1}$



Very broad physics program: flavor physics, rare decay & CP-vioalation, EW physics, QCD, exoctic particles, fixed target, heavy ion physics

The LHCb Upgrade II

RICH 1&2:

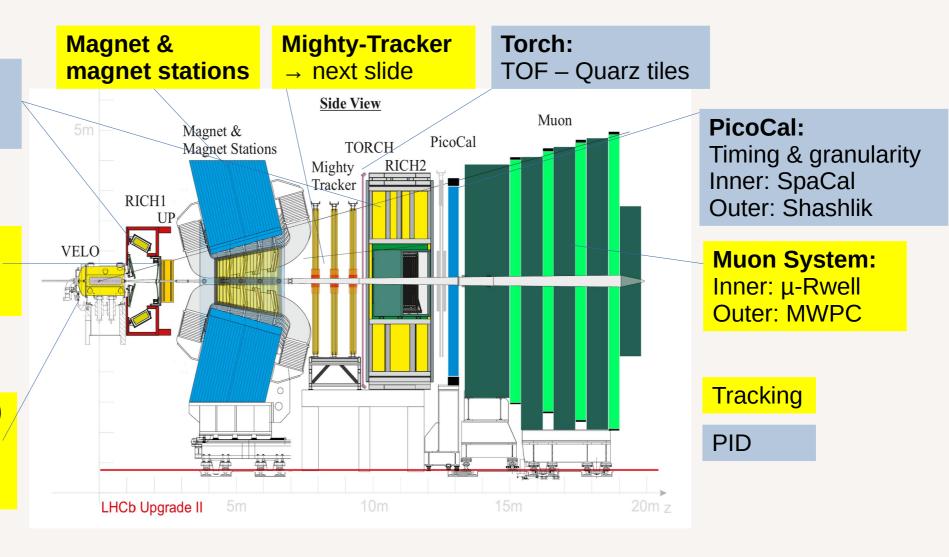
Increased granularity
Time measurement

UP:

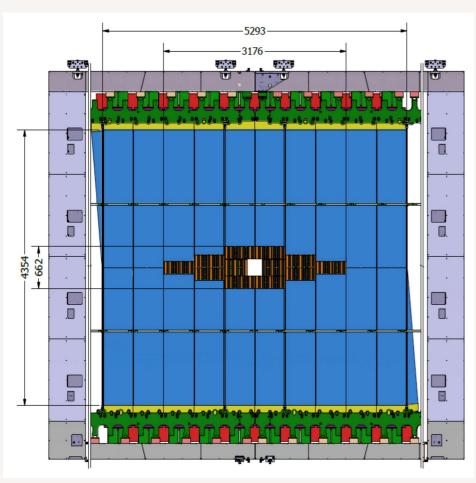
Pixels in DMAPS technology

Vertex locator: (VELO)

Pixels
Timining 50ps
New RF foil



The Mighty-Tracker



Outer region (Mighty-SciFi):

- > 3 stations à 4 layers \rightarrow ~300m² detector area
- scintillating fibres with SiPM readout
- > 250µm fibres
- > SiPM operated at liquid N₂ temperatures

Inner region (Mighty-Pixel):

- Silicon pixels in HV-MAPS technology
- > 6 layers à 1.3m²
- Options for Mighty-Pixel sensor:

MightyPix ← this talk

RadPix ← DRD3 development

Challenges for the MightyPixel:

Environment:

> Particle rate: 13MHz/cm² *

> NIEL: $2.5 \times 10^{14} \, n_{eq}/cm^2 *$

> TID: 40 MRad *

> Bunch crossing spacing: 25 ns

Material budget:

> Per layer: 1-2% X0

* numbers do not include safety factors

Powering & power consumption:

> Power consumption <150

 $<150 \text{mW/cm}^2$

Serial powering

Slow control:

Large system :

~22k sensors

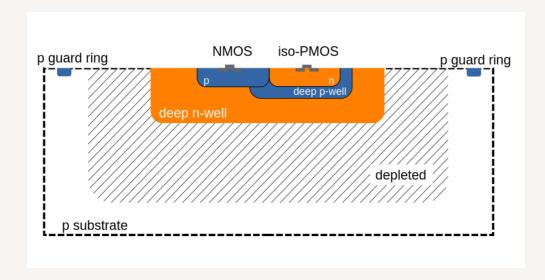
O(10⁹) channels

SPECIFICATIONS IN A NUTSHELL

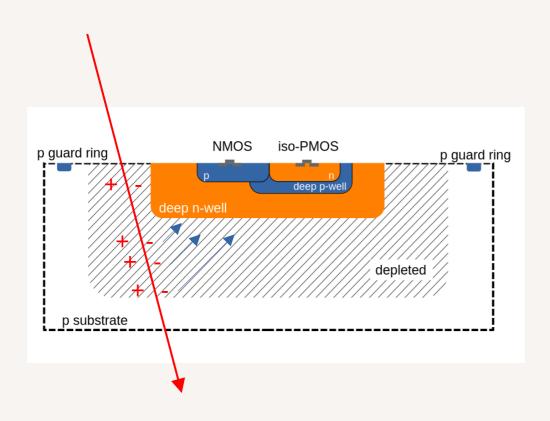
- The sensors have to guarantee an in-time efficiency* of >99% over the entire lifetime of the experiment at a power consumption < 150mW/cm².
- Spatial resolution is given by the binary resolution of pixels

(*i.e. an hit efficiency > 99% with correct bunch crossing identification, corresponding to ~3ns time resolution for a 25ns bunch crossing spacing)

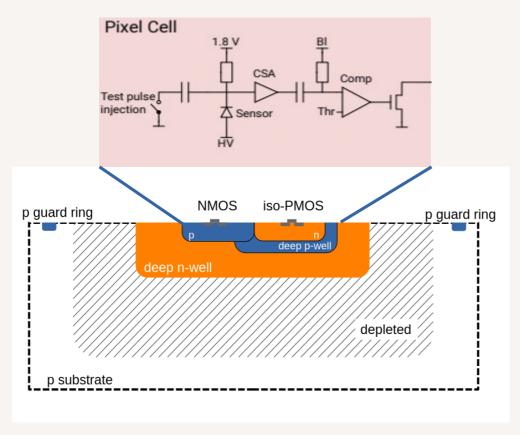
I. Peric, Nucl.Instrum.Meth. A582 (2007) 876-885



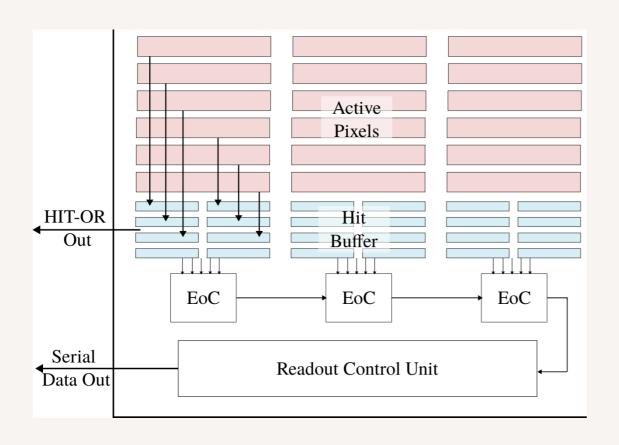
- produced in commercial HV-CMOS processes
- pn junction formed by reverse biased deep n-well and p substrate



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- pn junction formed by reverse biased deep n-well and p substrate
- fast charge collection via drift



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- pn junction formed by reverse biased deep n-well and p substrate
- fast charge collection via drift
- every pixel houses tuneable amplifier & comparator



- produced in commercial HV-CMOS processes
- pn junction formed by reverse biased deep n-well and p substrate
- fast charge collection via drift
- every pixel houses tuneable amplifier & comparator
- hit information (ToA, ToT) stored in periphery
- hit driven readout controlled by FSM

The MightyPix Family

MightyPix1



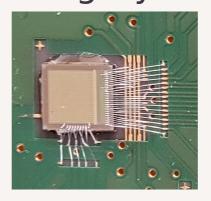
TSI 180nm

Area: 5 mm x 20 mm

Pixel size:

50 μm x 165 μm

LF-MightyPix



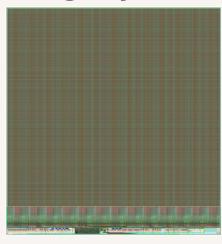
LFoundry LF15

Area: 3.5 mm x 4 mm

Pixel size:

 $100 \mu m \times 100 \mu m$

MightyPix2



AMS ah18

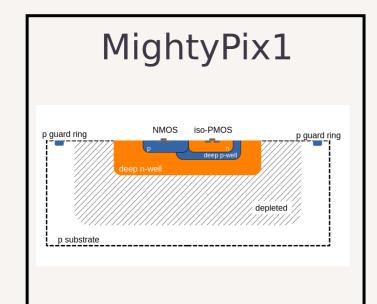
Area: 21mm x 19mm

Pixel size:

84 μm x 84μm

submitted 06/2022 submitted 05/2024 submitted 10/2025

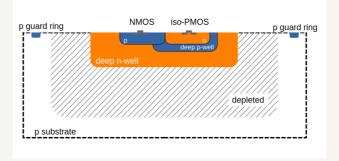
The MightyPix Family



TSI 180nm

Amplifier-type: CMOS Comparator: CMOS

LF-MightyPix

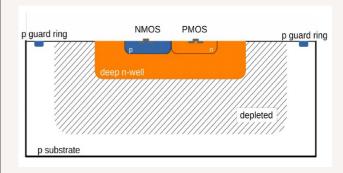


Similar to MightyPix1, but different chip guard ring design.

LFoundry LF15

Amplifier-type: NMOS Comparator: CMOS

MightyPix2



AMS ah18

Amplifier: CMOS Comparator: NMOS

MightyPix: Specific features for LHCb

TFC (fast commands@320Mbit/s)

ECS (configuration@10Mbit/s)

1280 / 640 / 320 Mb data link

Mulitplexer 4:2, 4:1

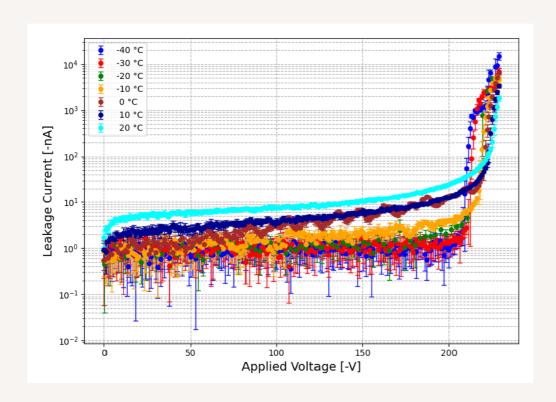
Serial powering

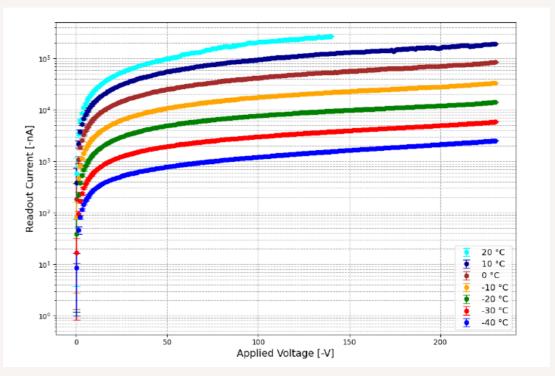
- → shunt LDO's on chip
- → DC balancing for all communication links (data, TFC, & ECS)

Hadronic environment \rightarrow SEE

→ triple redundant configuration & power on, glitch filter, hamming-2 encoded state variables to protect FSM implemented on MightyPix2

MightyPix1: IV curves

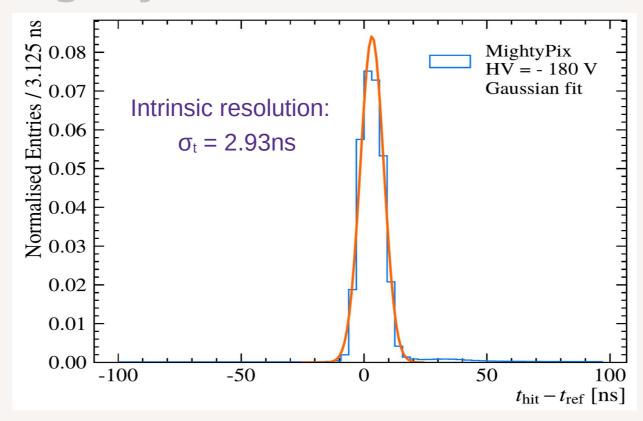




before irradiation

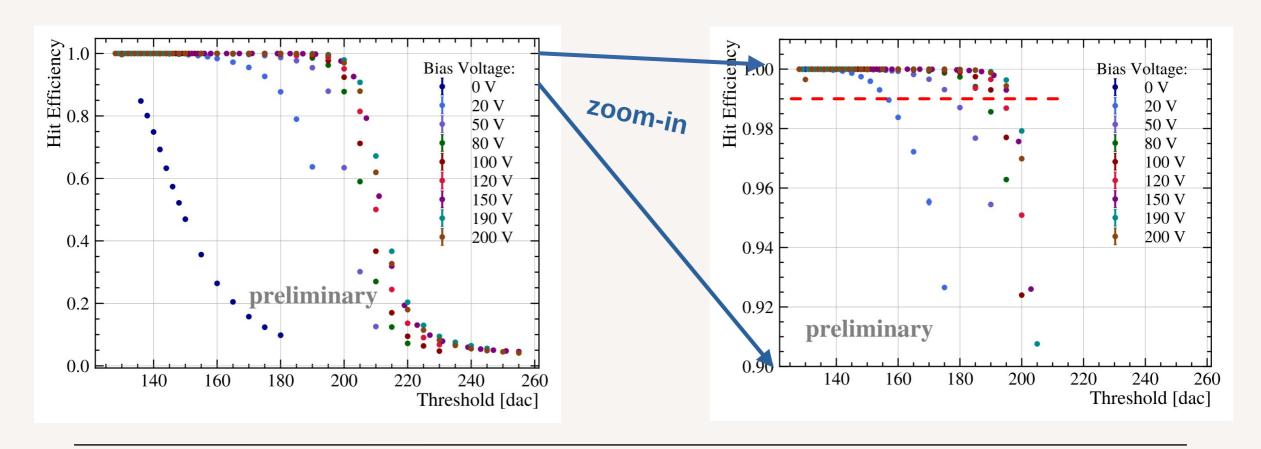
after $1x10^{15}n_{eq}/cm^2$

MightyPix1: Time resolution

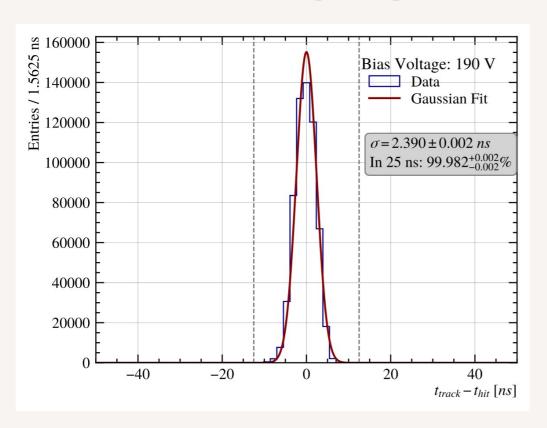


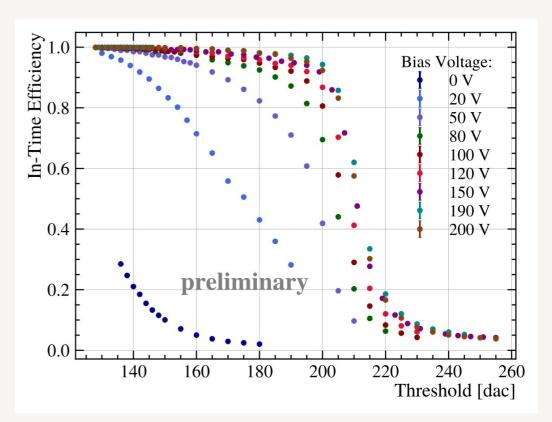
Only operational after FIB repair, but with very good performance demonstrated in lab with 90Sr.

LF-MightyPix: Efficiency



LF-MightyPix: In-time efficiency

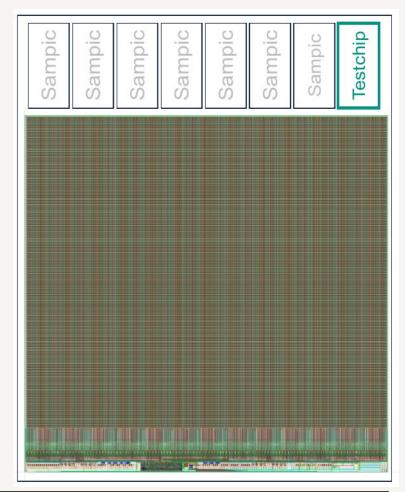




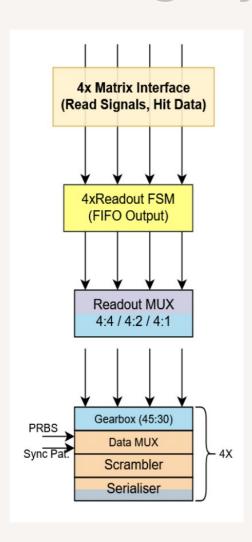
In_Time Efficiency = In-Time Fraction * Efficiency

MightyPix2: Overview

- AMS ah18 engineering run
- Features:
 - 244 x 194 pixel (full size: 244 x 240)
 - pixel size 84 μm x 84 μm
 - 21 x 19 mm²
 - fully compatibility to LHCb (TFC, ECS, readout architecture, serial powering...)
- Dedicated chip with test-structures
 -> allow systematic studies on TID damage, SEU & serial powering



MightyPix2: readout & rate simulation



Rate simulation:

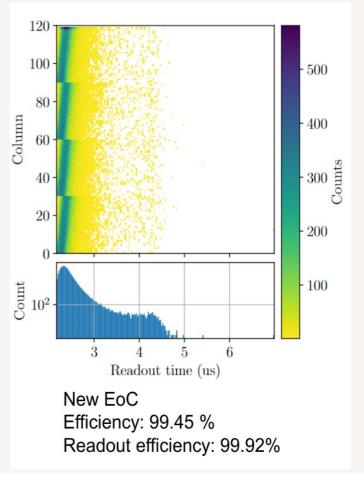
Dedicated software tool* to verify hit rate capability.

Set-up:

- full pixel matrix
- actual MP2 readout design
- p-p run conditions
- Hit rate of 35MHz²

Result:

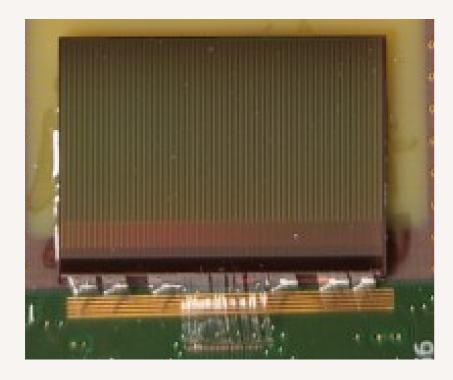
- Very high readout efficiency from improved EOC
- Speed limited by links



* MightyPix at the LHCb Mighty Tracker — verification of an HV-CMOS pixel chip's digital readout

S. Scherl (Liverpool U. and KIT, Karlsruhe, IPE) et.al. DOI: 10.1088/1748-0221/19/04/C04045

Radiation hardness of HV-MAPS: TelePix2 as a primer for MightyPix



* arXiv:2503.08177

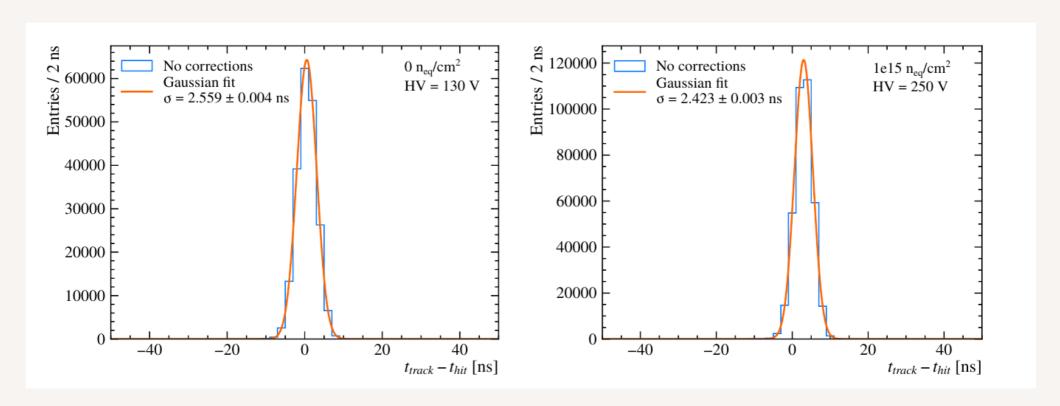
- developed as time reference for DESY test beam telescope *
- foundry, substrate and design of pixel array same as MightyPix1, except pixel size:
 165 μm x 25 μm for TelePix2
 165 μm x 50μm for MightyPix1
- several irradiaton campaigns:

NIEL: up to $1x10^{15}$ n_{eq}/cm^2

TID: high dose/high rate up to 40 MRad

low dose/low rate up to 1-2 MRad

Time resolution after neutron irradiation



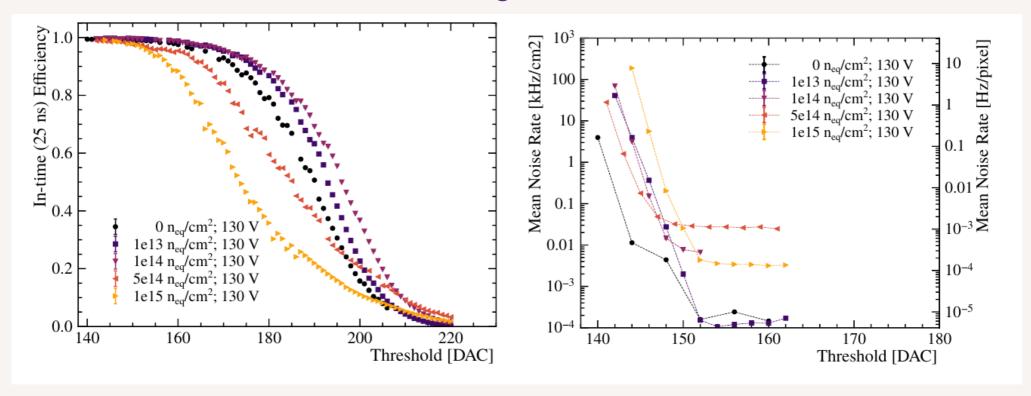
before irradiation

after $1x10^{15}n_{eq}/cm^2$

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In-time efficiency & noise after neutron irradiation

Constant voltage for all fluences

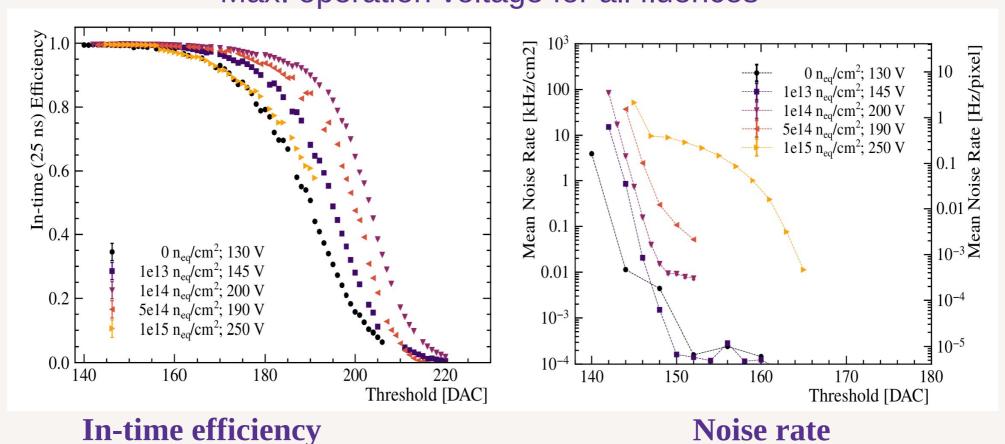


In-time efficiency

Noise rate

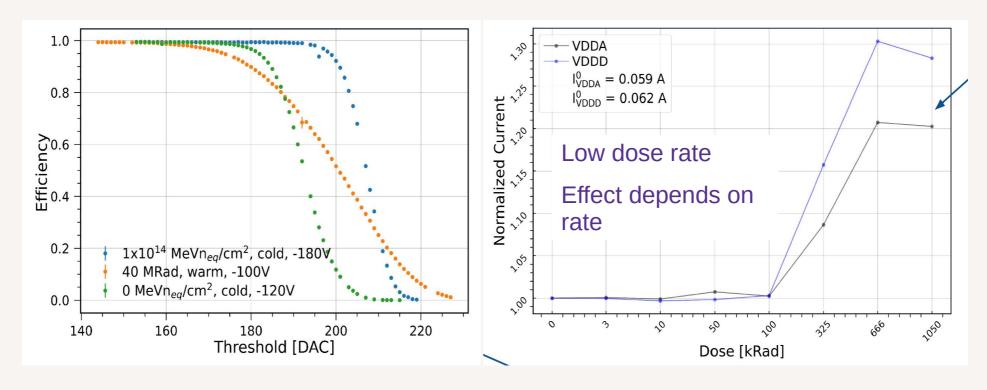
In-time efficiency & noise after neutron irradiation

Max. operation voltage for all fluences



23

Efficiency & power consumption after TID irradiation



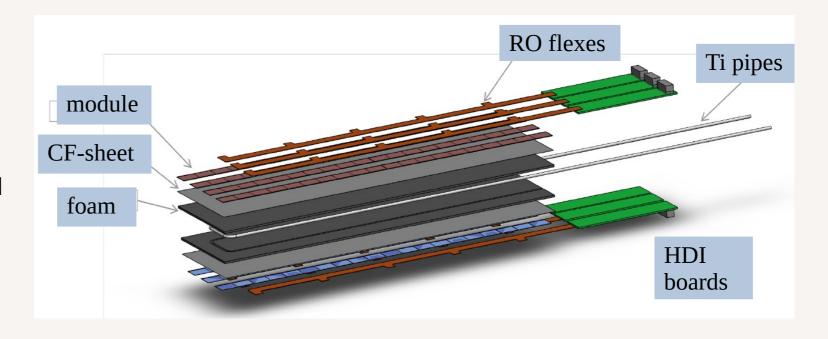
Acceptable performance after irradiation with protons and X-rays, but spurious increase of low voltage currents. Dose rate dependent effect, under investigation.

Sebastian Bachmann - CEPC 2025 11/05/25

FULL STAVE

Assembly:

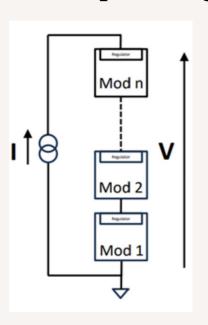
- 6 columns, each housing
 6 modules a 5 sensors
 i.e. 180 sensors per stave
- Core:
 CF sandwich panel with heat conducting foam and Titanium cooling pipe
- Readout flex: Length depends on position of HDI



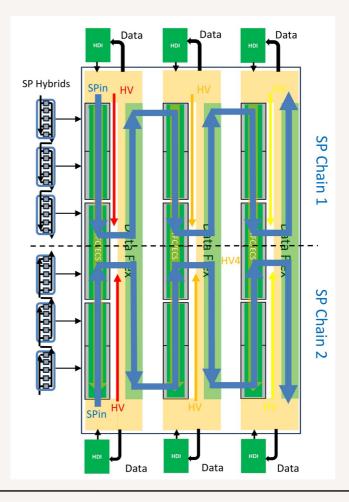
Sebastian Bachmann - CEPC 2025

POWERING SCHEME

Serial powering:



- To minimize material budget serial powering of MightyPix sensors is foreseen
- A module contains 5 sensors which are powered in parallel
- Two serial power chains per full stave containing 30 modules / 180 sensors



26

SUMMARY & CONCLUSION

- LHCb aims for an Upgrade for LHC Run 5 to cope an increase in luminosity by a factor of 5
- Inner region of current downstream tracker (scintillating fibre tracker) has to be replaced by a pixel detector
- The HV-MAPS based MightyPix sensor is currently developed for the Mighty-Tracker with MightyPix2 being the first sensor fully compatible for the application in LHCb
- Radiation hardness of the technology has been demonstrated
- We aim for a TDR in autumn 2026

27

11/05/25

Backup

SPECIFICATIONS

MightyTracker-Pix

EDMS no. 3207186

Parameter	MP Specification
Pixel size (bending plane)	$\leq 100 \mu \mathrm{m}$
Pixel size (non bending plane)	$\leq 200 \mu \mathrm{m}$
Substrate thickness	<200 μm
Pixel orientation	X
Max. Particle Rate	$17~\mathrm{MHz/cm^2}$
Max. Hit Rate	$34 \mathrm{MHz} \ \mathrm{cm}^{-2}$
Max. length of data word	32
Overall efficiency	>96%
In-time efficiency	>99% within 25 ns
Noise rate (End of life)	$\leq 400 \mathrm{kHz/cm^2}$
Transmission rate	4 links of 1.28Gbit/s each
NIEL	$3 \times 10^{14} n_{\rm eq}/{\rm cm}^2$
TID	40 MRad
Power Consumption	$\leq 150 \text{ mW/cm}^2$

Upstream Pixel

Yiming's slide from LHCC ASIC review

Darametera	UP Specification	Remarks
Parameters	Specification	Remarks
Sensor size	~ 2×2 cm²	Common with MT
Pixel size, square	≤ 85×85 µm²	
Pixel size, rectangular	≤ 50×200 µm²	
Substrate thickness	< 200 µm	
Pixel orientation	x	bending plane
Max. Particle Rate	50 MHz/cm²	from Geant 4 + Pythia, @ 4 cm radius previously 74 MHz/cm ² @ \mathcal{L} = 1.5x10 ³⁴ cm ⁻² s ⁻¹
Max. Hit Rate	100 Mhit/cm²	at 4 cm radius, 100 % margin
Max. length of data word	32	
Overall efficiency	> 96 %	Including dead area
In-time efficiency	> 99 % with in 25 ns	
Noise rate (End of life)	≤ 400 kHz/cm²	@ max. 1% masked channels
Transmission rate	N × 1.28 Gbit/s	N ≤ 7 for matching with 1 LpGBT
NIEL	4 ×10 ¹⁵ N _{eq} /cm ²	from Fluka, safety margin 4
TID	250 Mrad	from Fluka, safety margin 4
Power Consumption	≤ 200mW/cm²	no margin, budget ~ 10 μA/pixel (85×85 μm² pixel)

MP2 status and timeline:

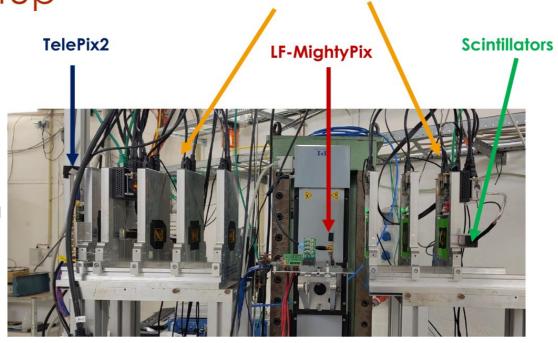
- MightyPix2 is designed for full compliance to the LHCb specifications.
- MightyPix2 has undergone a thorough review process with fruitful discussions. Recommendations have been implemented since then, especially on protection against single event effects (SEE).

Critical issues to be demonstrated with MightyPix2 are tolerance wrt TID damage and SEE's.

DESY Testbeam (13/10 - 2/11/2025)



- DESY Testbeam Area 22
 - 4 GeV electrons
 - Alpide Telescope
 - TelePix2 Time Reference
- Running parasitically to Mu3e/P2
- LF-MightyPix readout using Gecco
- Data Analysis in Corryvreckan

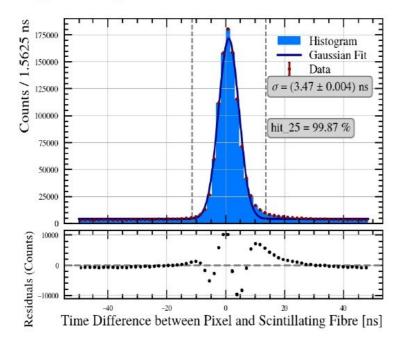


Alpide Telescope

22.10.2025 Celina Welschoff

LF-MightyPix: Lab measurements (Sr-90)

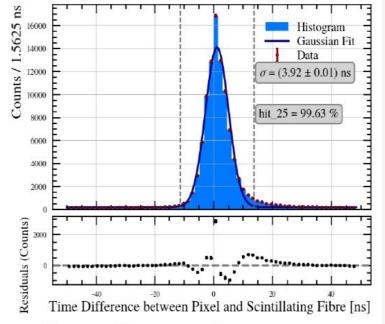
Digital Optimum DACs



Power Consumption:

 $20.65 \,\mu W/Pixel \ or \ 201 \, mW/cm^2$

Analogue Optimum DACs



Power Consumption:

 $19.25 \,\mu W/Pixel \, or \, 193 \, mW/cm^2$

Excellent time resolution at reasonable low power consumption.

Definition of hit_25:

In-Time-Fraction =

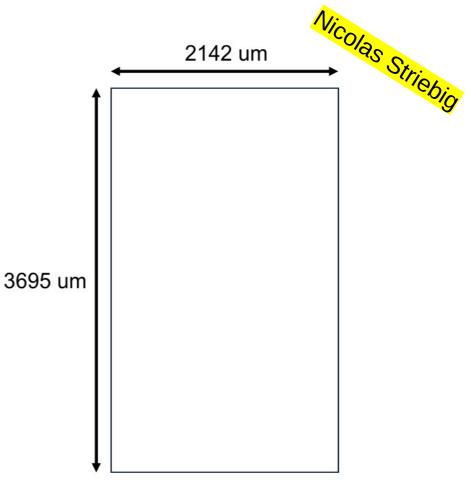
Number of hits in 25 ns
Total number of hits

Conservative estimate
Of power consumption

Dedicated Chip for Teststructures



- TID measurements
 - NMOS/PMOS
 - Rectangular long/short W/L
 - ELT
 - DRAM: Evaluate data retention time
 - SRAM: Evaluate static noise margin
- SEU/SET cross section measurements
 - DRAM
 - SRAM
 - TMR Configuration Registers
- Serial Powering
 - 2 SLDOs for serial/parallel configuration





SEU/SET Improvements



Glitch Filter

- SET glitch filter for async reset input
- Reset syncronizers TMR protected

Hamming 2-encoded state variables

- 1 additional FF to detected single bit errors
- Reduced risk of incorrectly jumping into invalid state
- Allows monitoring -> Error output connected to Counter

TMR

TFC

- Slow clock domain part TMR protected
- Deserializer part unprotected, but all single bit errors can be detected due to 6b8b encoding -> SEE can cause bitslip -> Receiver unlock
- Clock tree is not triplicated, SET could cause bitslip -> Receiver unlock

Registers

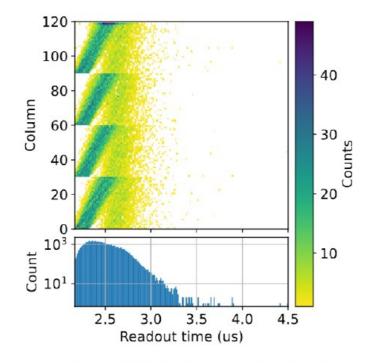
Registerfile partially and chip configuration completely TMR protected



Rate Simulation – Heavy Ion



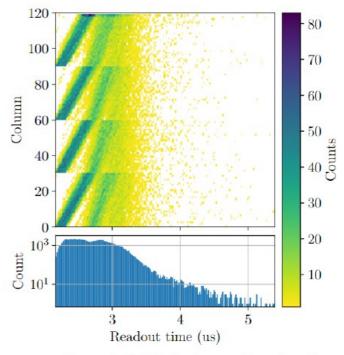
- Heavy Ion run conditions
- 50 ns bunches
- 0.25 % interaction propability
- Much higher peak hitrate



Avg. 20 hits/interaction/cm²

Efficiency: 99.98 %

Readout efficiency: 99.98%



Avg. 40 hits/interaction/cm²

Efficiency: 99.97 %

Readout efficiency: 99.98%

