C01

A 55 nm HV-CMOS Pixel Sensor Design for High-Energy Particle Tracking with High Hit Rate and Precise Time Resolution

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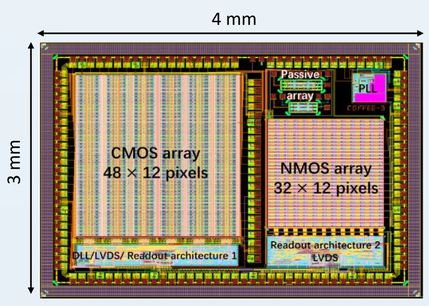
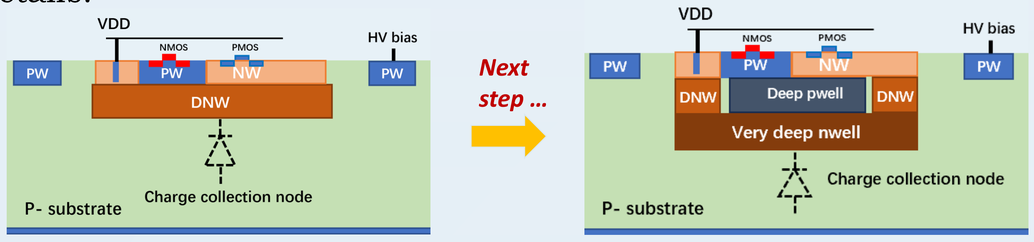
Introduction

This work presents a design framework of a High-Voltage CMOS pixel sensor for high energy particle tracking, which can provide a time resolution of few nanosecond order under the hit rate exceeding 100 MHz/cm^2. The design is based on a **55nm** CMOS process and implemented in the **COFFEE3** prototype. A complete readout architecture has been integrated into a 40 × 145 μm^2 pixel to account for potential process modifications and to prepare for large-scale ASIC development.

Process and Prototype

The COFFEE3 prototype incorporates two architectures: The CMOS array based on modified quintuple-well process , for applications requiring high-precision time resolution under high hit density; The NOMS array based on triple-well process for low power consumption application, please refer to *Bingchen's* poster for more details.





Current process: triple-well, low resistivity ~ 10 Ω•cm (Now)
Large equivalent capacitance
Depletion zone ~ 10 um

Modified process: quintuple-well, high resistivity ~ 1-4k Ω•cm (Future)
↓ Equivalent capacitance ~ 200 fF
↑ Thick depletion zone > 100 um

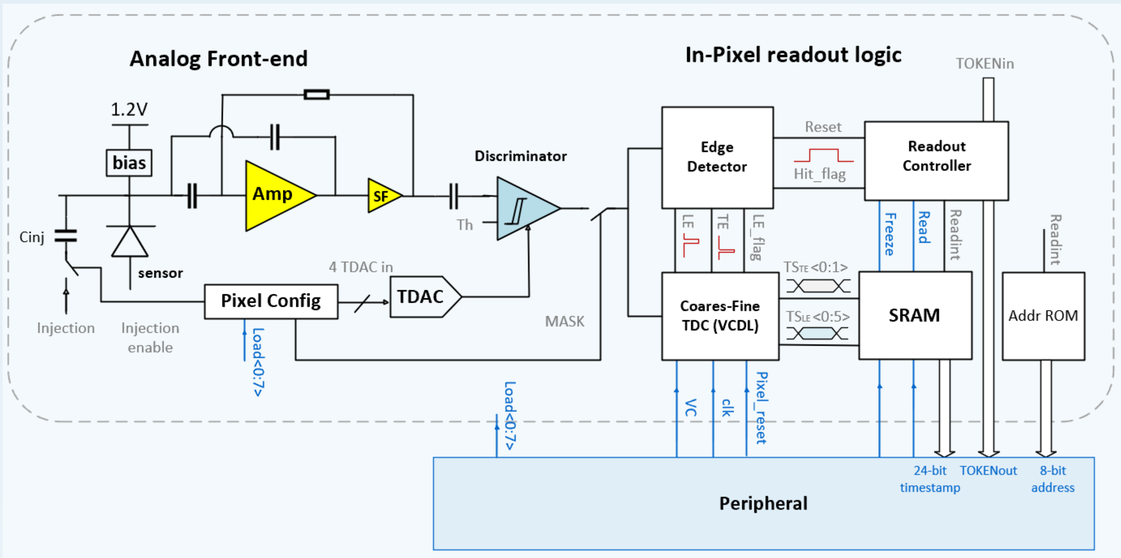


Fig 1. The in-pixel schematic of the CMOS array, including the periphery. Signal collection, amplification, and digitization are all implemented within each individual pixel. Furthermore, a pixel-level coarse-fine **Time-to-Digital Converter (TDC)** is also integrated into each pixel; the **leading edge (LE)** and **trailing edge (TE)** time information of particle hits is first stored locally within the pixel, then transmitted along with the address of the activated pixel to the bottom of the array in priority order.

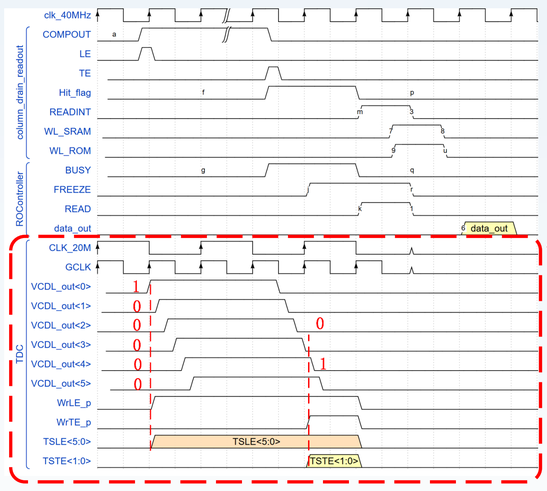


Fig 2. The timing diagram of the in-pixel readout circuitry, illustrating the complete process from the discriminator output to the data packet output and the working principle of in-pixel coarse-fine TDC.

Delay line Coarse-fine TDC

- A 20 MHz Gray-coded clock as input
- A 40 MHz coarse timestamp (25 ns) is internally generated
- Only hit pixels generate fine timestamp from their discriminator output

✓ **Reduce power consumption**

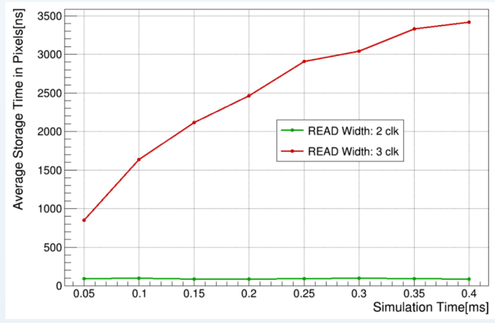
- **Timestamp of LE: 6 bins ~ 4.17 ns**
- Refer to *Yuman's* poster for the related test results

✓ **TDC quantization noise contribution to the time resolution uncertainty is < 2 ns**

Simulation

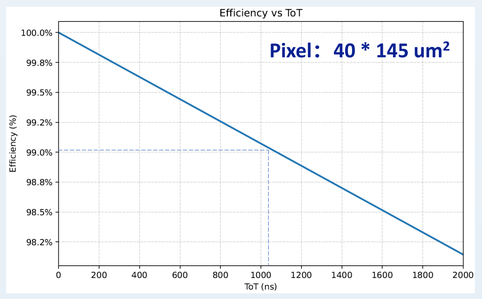
1. Hit Density

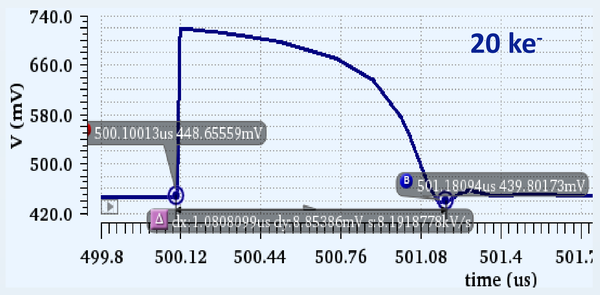
☐ Digital pile-up



- READ = 3 clock cycles → longer in-pixel storage before readout; Causing digital pile-up
- READ = 2 clock cycles → near-zero storage
- In this design, the width of READ signal designed to be adjustable

☐ Analog pile-up

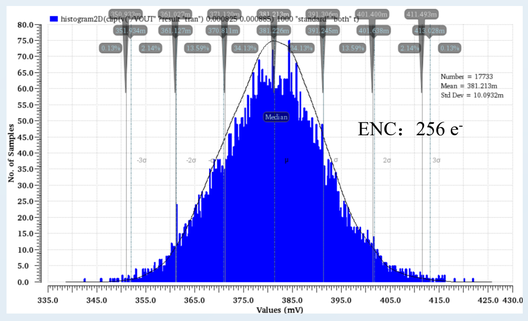




The CSA output waveform width for a 20 ke$^-$ input charge is limited to 1 μs, ensuring a <1% detection efficiency lost due to analogue pile-up while the hit density reach ~100Mhz/cm^2.

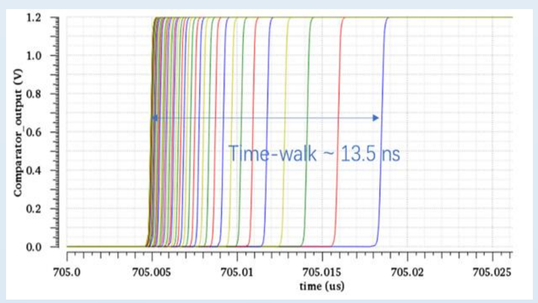
✓ **High hit rate processing capability**

2. Noise



- Based on the modified high resistivity process, **Cd ~ 200 fF**
- ENC ~ 256 e$^-$
- Each pixel integrates a 4-bit DAC for individual threshold configuration

3. Time-walk



- Cd ~ 200 fF
- Signal range: 1.8k - 16 ke$^-$, time-walk ~ 13.5 ns

$$\sigma_{TW}^2 \ contribution < (4\ ns)^2$$

✓ **The time-walk contribution to the time resolution uncertainty is < 4 ns**

Conclusion & outlook

The CMOS array in COFFEE3 prototype for high hit density and time precision was developed in a 55nm CMOS process. We have also achieved the improved column readout and TDC integration within the pixels, laying the research foundation for future expansion to larger chips. The total time accuracy is expected to be less than 5ns, including contributions from signal collection time, time-walk effects, jitter and the quantization noise of the TDC. The testing work for evaluating the readout architecture final performances are still actively in progress.

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Test results of sensing diode, PLL, NMOS comparator and readout circuit of COFFEE3 pixel MAPS prototype for CEPC

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CMOS SENSOR IN FIFTY-FIVE NM PROCESS

Introduction

COFFEE3 prototype chip is fabricated with 55-nm HV-CMOS process designed to meet the requirements of CEPC inner tracker. COFFEE3 is consists of 4 sectors: 1) passive sensing diode array; 2) standalone PLL block; 3) right pixel matrix with in-pixel CSA and half part of discriminator, while other circuits at the end of column (EOC); 4) left pixel matrix with full in-pixel CSA, discriminator, TDC, while readout circuit at the end of column.

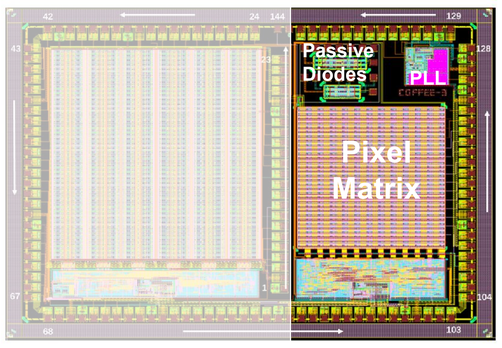

Fig1. Layout of COFFEE3 chip. Test results of the right sector are reported in this poster.

The readout out architecture of sect.3 has less cross-talk effect between digital and analog circuit, which is more suitable with the current triple-well HV-CMOS process. The sect.4 could handle higher hit density rate, while need more R&D effector. The current testing results of the first 3 sectors are presented in this poster.

COFFEE3 Test System

IV & CV test system

PC + Source Meter + homemade HV bias adapter + bare chip

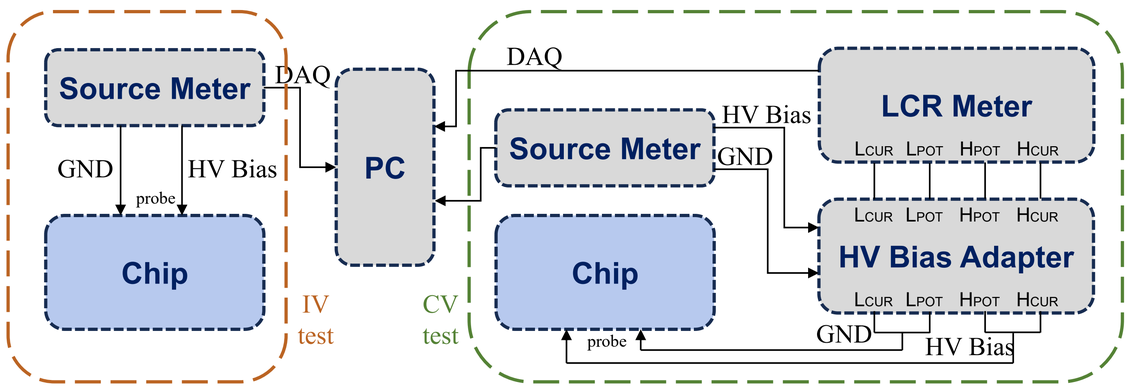

Fig2. Sketch of IV & CV test system

PLL test system

PC + power & signal supply + dedicated chip test board

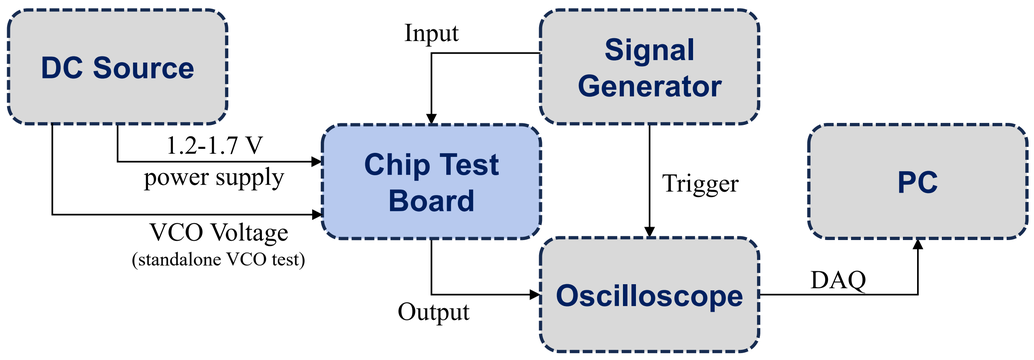

Fig3. Sketch of PLL test system

Pixel Matrix test system

PC + FPGA Board + Caribou Board + Dedicated Chip Carrier Board

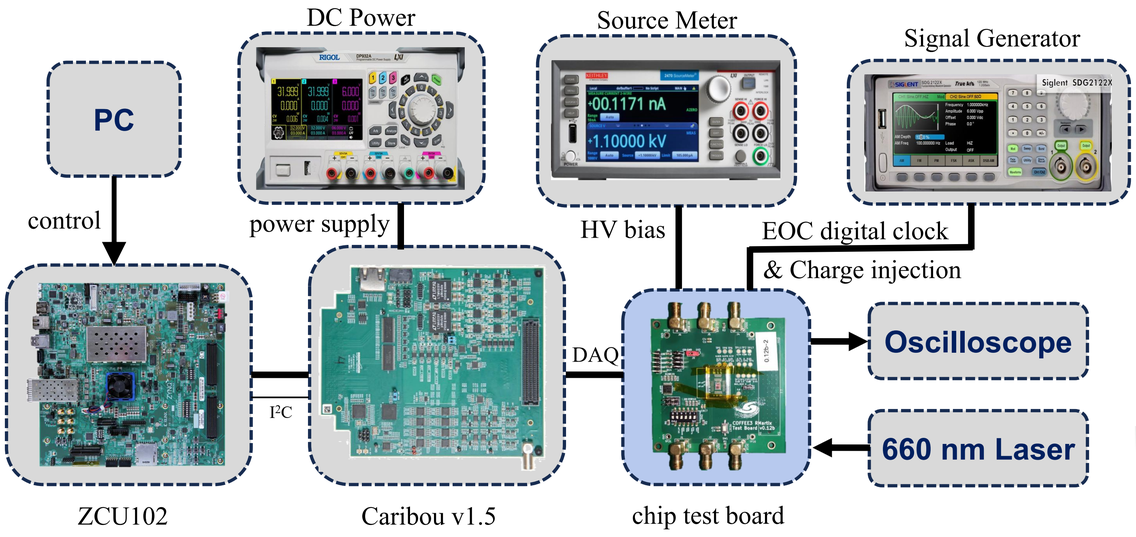

Fig4. Sketch of pixel matrix test system

- H. Liu et al., *Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade*, Journal of Instrumentation 12 (2017) P01008.
- https://caribou-project.docs.cern.ch/

Caribou is a versatile and modular DAQ system designed for prototyping silicon pixel detectors.

Main Results

Passive sensor diode IV & CV results

The passive diode array consists of two 3×3 sub-arrays, featuring pixel size of 45×145 μm² and 40×100 μm², corresponding to left and right pixel matrix, respectively. The results from 40×100 μm² sub-array 2 are presented, with its CV curve offset by a parasitic capacitance of ~247 fF.

- IV test: breakdown at ~ –70 V. Leakage current is ~140 pA at –70 V, as expected for a regular resisitivity (10 Ω · cm) wafer.
- CV test: single pixel has capacitance of ~50 fF at –70 V due to depletion. The involement of deep-p-well significantly increases pixel capacitance by ~100 fF.

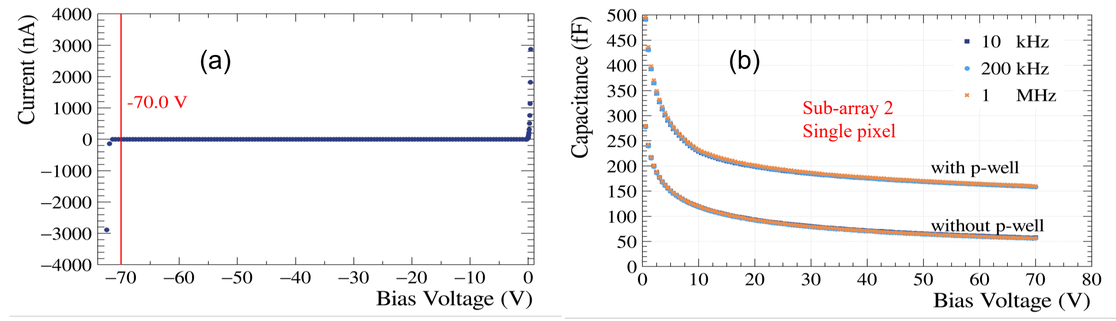

Fig5. IV test results. (a) and CV test (b) of single pixel in sub-array 2, which includes both with- and without-p-well design

PLL test results

PLL on COFFEE3 is designed for synchronization between the clock and data, as well as between multiple chips. It was designed to supply output clock with frequency of up to 640 MHz at working voltage of 1.2 V.

- Standalone VCO: with analogue power reaches 1.7 V exclusively, stable 640 MHz output can be obtained.
- Frequency multiplication: 4×, 8× and 16× at 40 MHz input clock.

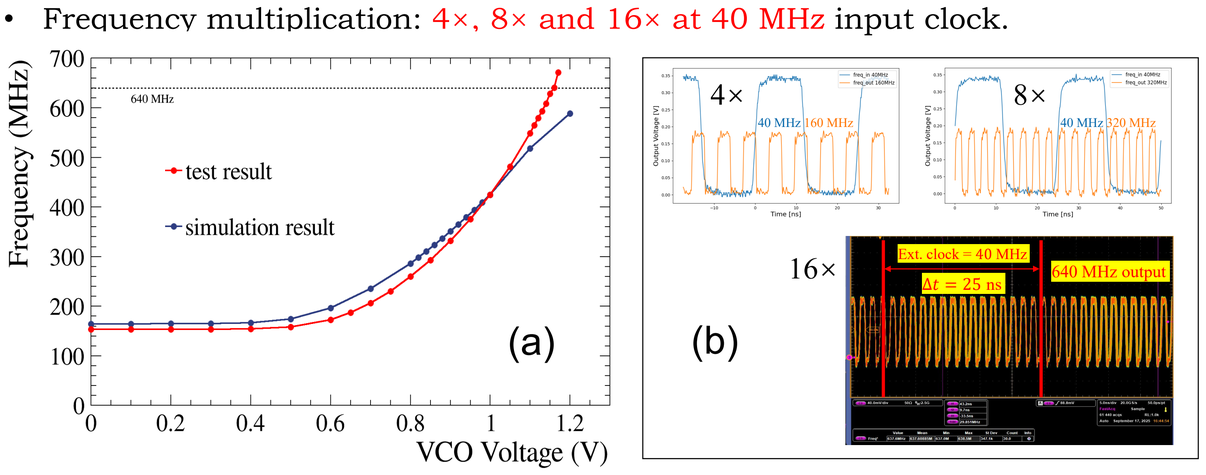

Fig5. PLL test results. (a) Standalone VCO test, frequency-voltage curve of VCO; (b) 4, 8 and 16 times frequency multiplication with 40 MHz square wave as input.

Pixel matrix test results

COFFEE3 right pixel matrix uses NMOS for in-pixel comparator only, and CMOS process for other front-end electronics. Comparator is consist of two half parts, NMOS half in pixel and CMOS half in EOC.

- Charge Sensitive Amplifier (CSA): CSA is working as expected with both charge injection and laser. Observed TOT is ~5 μs for injection and ~2.5 μs for laser.
- Laser & EOC readout test: In-pixel part of comparator works as expected, and induced EOC digital readout with pixel address can be successfully decoded.

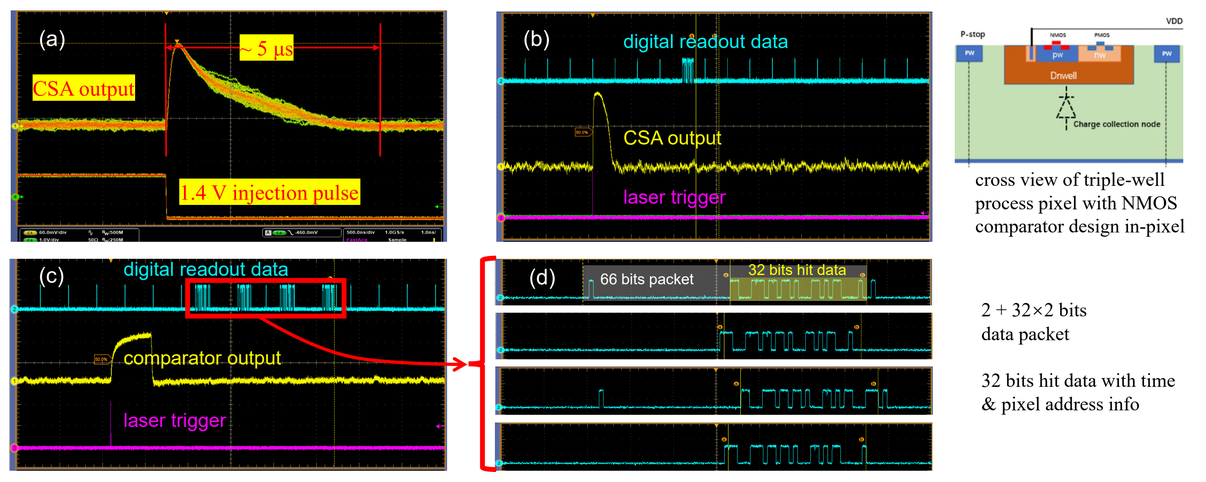

Fig5. Function verification of right pixel matrix of COFFEE3. (a) CSA response to charge injection; (b) CSA response to laser hit; (c) comparator response and digital readout of laser hit; (d) maginified digital readout waveform and data format.

Summary & Outlook

Preliminary tests using charge injection and laser confirmed that all core functions are performing as designed. COFFEE3 is dedicated to verifying the readout circuit and the core performance of a 55nm HV-CMOS technology for high-energy physics detectors. Upcoming tests will include TDAC, irradiation, and refined performance evaluations.

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Irradiation study of COFFEE2, the first 55nm High Voltage CMOS sensor prototype

C03

COFFEE
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

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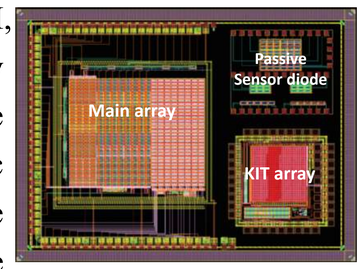
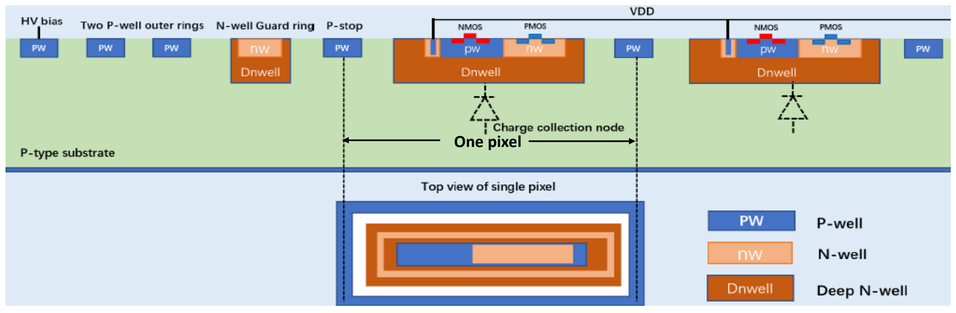
Introduction

To meet the increasingly demanding requirements of future tracking detectors for the CEPC and LHCb Upgrade II, advanced detector technologies with enhanced hit density processing capabilities and enhanced radiation tolerance are essential. To study the sensor performance and electronic response in the next generation process of High Voltage CMOS (HV-CMOS), the sensor chip called COFFEE2, the first prototype for process and circuit module in a 55 nm High-Voltage Technology, is designed and tested. A comprehensive irradiation tolerance testing campaign was conducted on the COFFEE2 chip. Utilizing the KIT pixel array, which boasts a fully integrated readout system, this work presents the first irradiation tolerance study of the 55 nm High-Voltage CMOS process.



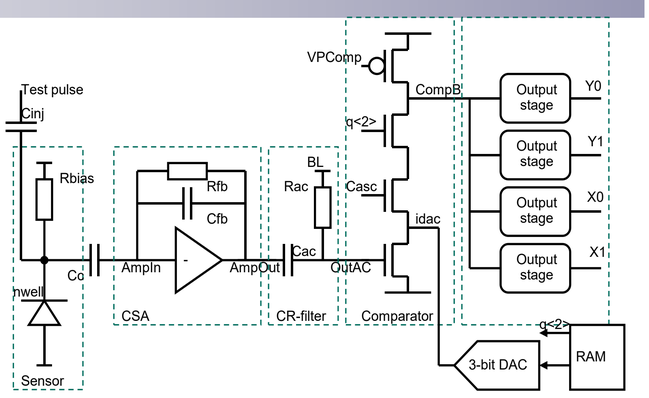
Process Features

- Deep n-well - P substrate junction as collection electrode
- Triple-well process: N-well/P-well/Deep n-well
- P-type substrate resistivity: 10 Ω·cm
- Guard ring: one inner N-well ring, with two P-well outer rings
- Substrate breakdown Voltage > 70V with frontside HV bias
- More design details:
  - Z. Chen et al., *Feasibility study of CMOS sensors in 55 nm process for tracking*, Nuclear Instruments and Methods in Physics Research A 1069 (2024) 169905.
  - H. Zhang, et al., *High voltage monolithic pixel sensor in 55 nm technology*, JINST 20 (2025) 03, C03023



KIT Pixel Electronics

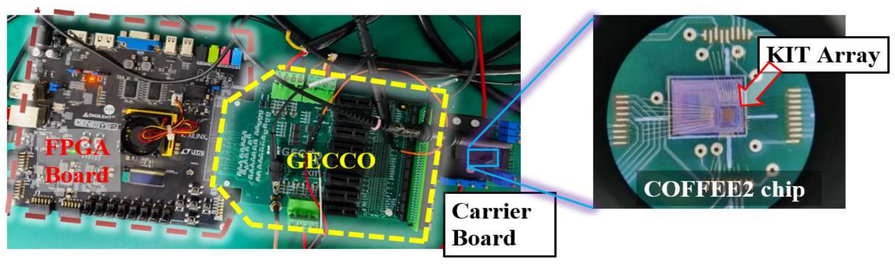
- Pixel electronics (25 μm × 25 μm)
  - ✓ Sensor diode
  - ✓ Charge Sensitive Amplifier (CSA)
  - ✓ CR filter
  - ✓ Comparator
  - ✓ RAM and tune DAC
  - ✓ Output stages



H. Zhang, et al. High voltage monolithic pixel sensor in 55nm technology JINST 20 (2025) 03, C03023

- Work principle
  - ✓ Charge collected by pixel n-well
  - ✓ Converted to voltage signal by Charge Sensitive Amplifier
  - ✓ Analog voltage pulse shaped and converted to digital signal by comparator
  - ✓ Output stage generates current
  - ✓ Current is sent via address line to the transimpedance amplifier outside matrix
  - ✓ Address lines have constant potential – no cross-talk

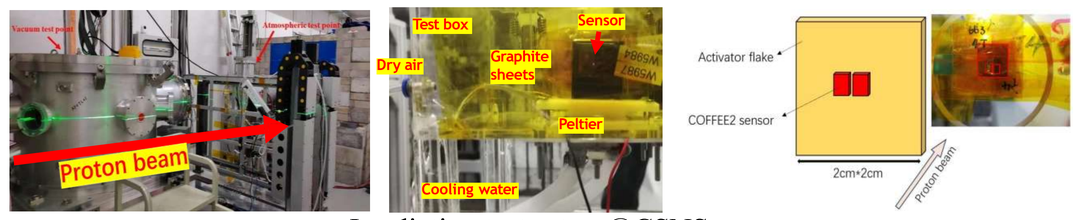
Bench test setup



- Genesys2 FPGA Board
  - ✓ Translates commands from the PC into the precise low-level digital protocol
- GECCO Control Readout Board
  - ✓ It integrates power delivery and controls and supplies all required electrical potentials for testing the chip
- Carrier Board (with wire-bonded COFFEE2 chip)
- Signal Generator
  - ✓ Provide charge injection to the chip through the GECCO board

Irradiation Test

Fluence [n_{eq}/cm^2]	3.2×10^{11}	4.9×10^{12}	5.7×10^{13}	1.6×10^{14}	1.3×10^{15}
Temperature	Room temperature				-28°C



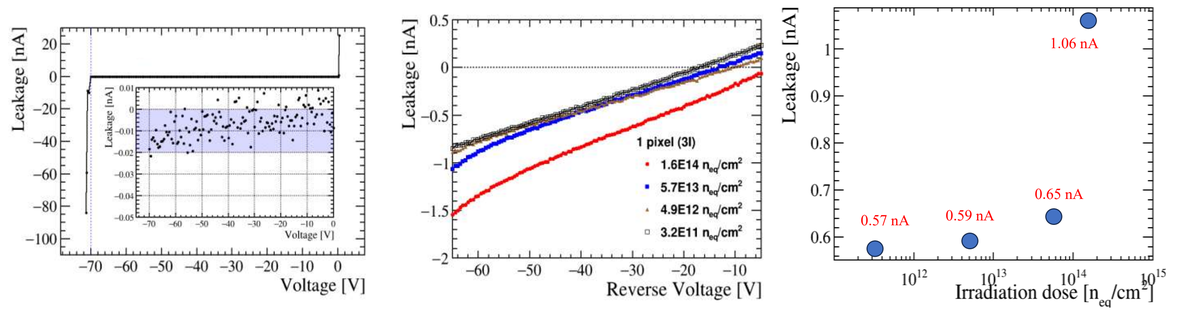
Irradiation test setup @CSNS

- Irradiated in 80 MeV proton beam at China Spallation Neutron Source (CSNS) in April 2024
- 2 sensors placed at each test point
  - ✓ 1 IV/CV tested + 1 new
- Aluminum foil pieces placed at each point to calibrate irradiation fluence

Main results

Irradiated IV change

With bias of -50V, leakage current increases from ~ 10 pA to ~ 1nA after irradiated. The magnitude of leakage current is proportional to the irradiation fluence



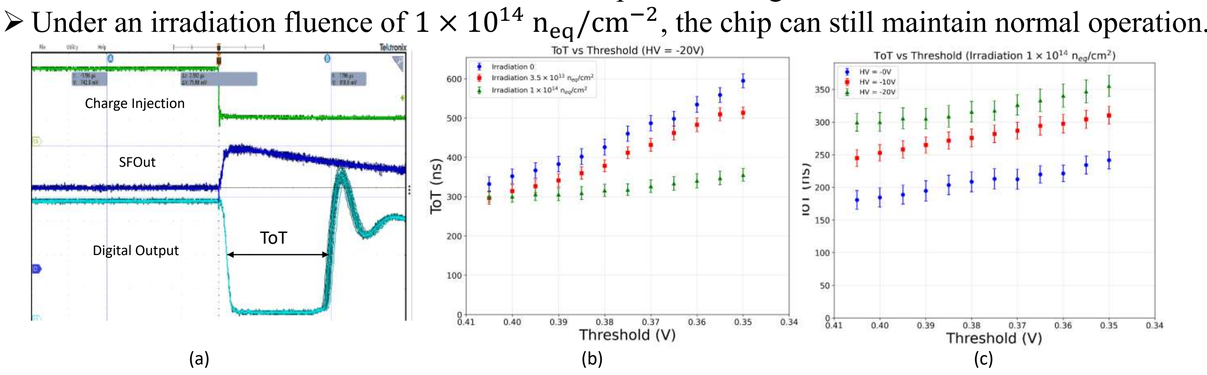
IV test results of COFFEE2 in different irradiation fluence

Irradiation Tolerance Evaluation

Time over Threshold (ToT) versus Threshold

ToT and noise rate as a function of the threshold reference for all tested samples different voltages and irradiation fluence. Results are shown for chips settings at room temperature.

- ➢ Time over Threshold (ToT) is correlated with the energy of a signal
- ➢ An increase in ToT leads to an increase in the depletion voltage
- ➢ Under an irradiation fluence of 1×10^{14} n_{eq}/cm^{-2}, the chip can still maintain normal operation.



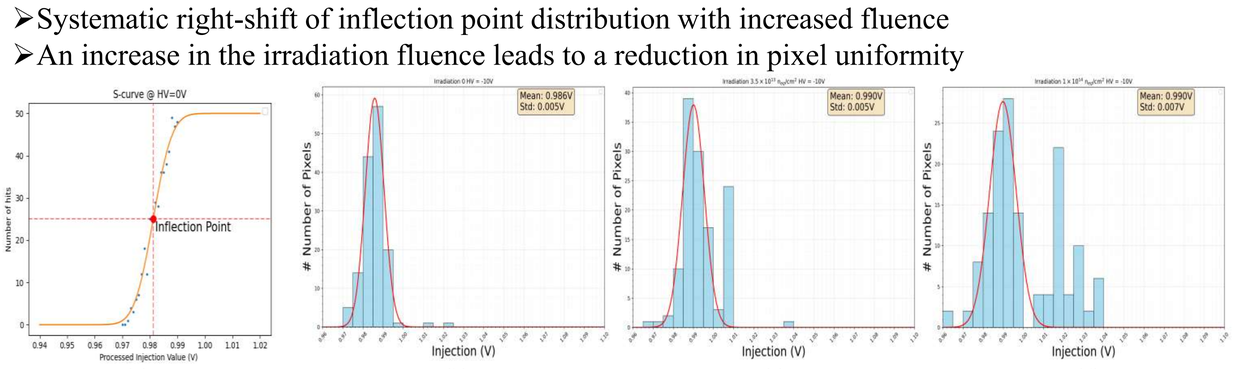
(a) (b) (c)

Chip Response to Charge Injection(a); ToT vs. Thershold in different Irradiation fluence (b); ToT vs. Threshold in different bias voltage(c)

Inflection Point of S-curve for pixels

Inflection point of the S-curve as a function of charge injection for different irradiated chips. Results are shown for HV = -10V settings at room temperature

- ➢Show the noise level of the pixel
- ➢Systematic right-shift of inflection point distribution with increased fluence
- ➢An increase in the irradiation fluence leads to a reduction in pixel uniformity



(a) (b) (c) (d)

The inflection Point of S-curve (a); The distribution of inflection point in bias voltage of -10V(b),-20V(c),-30V(d);

Summary & Outlook

The COFFEE2 chip demonstrated excellent irradiation tolerance, confirming the resilience of the 55 nm HV-CMOS process. It remained fully functional with only minor performance degradation up to an accumulated fluence of 10^{14} n_{eq}/cm^2. The observed degradation primarily manifested as a slight shift in the S-curve inflection point and a minor broadening of its distribution; nevertheless, the overall performance was well maintained. Furthermore, it was found that applying a higher bias voltage improved charge collection efficiency and increased the depletion depth, which consequently helped recover performance parameters.

Future work involves more detailed test including radioactive source test and test beam measurement.

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HVCMOS Pixel Sensor in 55nm Process: Readout Architecture Simulation, Hit Loss Analysis, and Data Transmission Optimization

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C04

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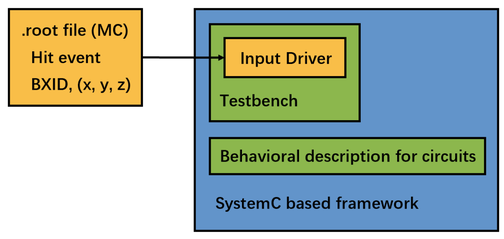
Introduction

Pioneering R&D in HVCMOS pixel sensors at the advanced 55 nm process, the COFFEE series prototypes are currently being developed for the CEPC inner tracker and Upstream Pixel tracker (UP) in the LHCb Upgrade II. COFFEE3, the latest prototype with two distinct readout architecture, was design and fabricated in 2025. Though featuring a small-scale prototype (3×4 mm^2), COFFEE3 is designed to match the final full-scale sensor (~2×2 cm^2), aiming for proof of concept. This poster shows the performance of the preferred readout architecture under the high-hit-density environment of LHCb, especially the efficiency loss. In response to the UP's data compression requirements and the readout link's bandwidth limitations, this poster also shows how simulation can be used to explore and iterate peripheral readout architectures that enable rational scheduling of transmission resources.

SystemC Based Framework using MC Input

By establishing a behavioral-level model of the pixel array and peripheral readout using SystemC, and inputting MC (Monte Carlo) hit data in the testbench, the advantages of this framework are:

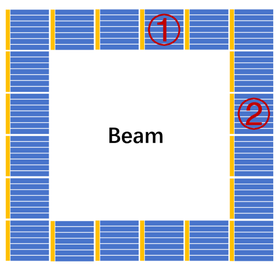


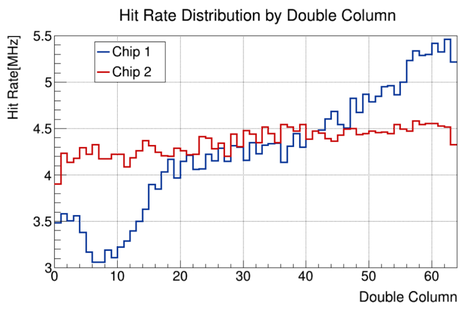
① Using MC data enables the simulation of real experimental environments by capturing hit density fluctuations in spacetime, which produce the non-uniform and bursty data traffic patterns, resulting in detailed and reliable simulation results.

② Compared to RTL-level implementations, behavioral-level models can more rapidly identify transmission bottlenecks for parameter optimization.

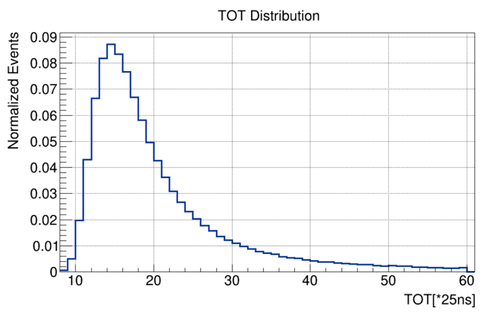
For the chips closest to the beam, two typical examples were selected, with their locations and hit density distributions illustrated below. An event sample of 50,000 BXIDs and a cluster size of 1.5 was used.

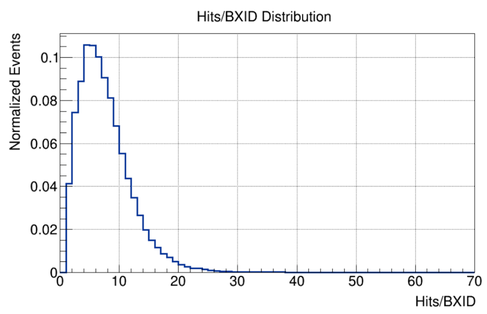
Innermost chip placement





A Landau distribution between 200 and 1500 ns is used for the TOT time. The Hits/BXID distribution shows that most values are below 30, but it has a long tail reaching up to 70.



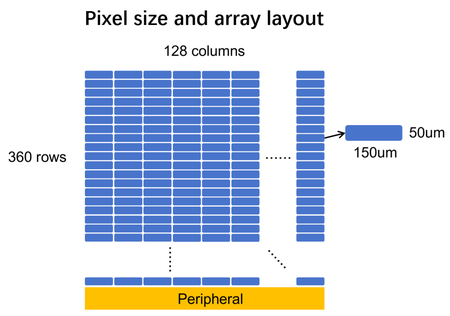


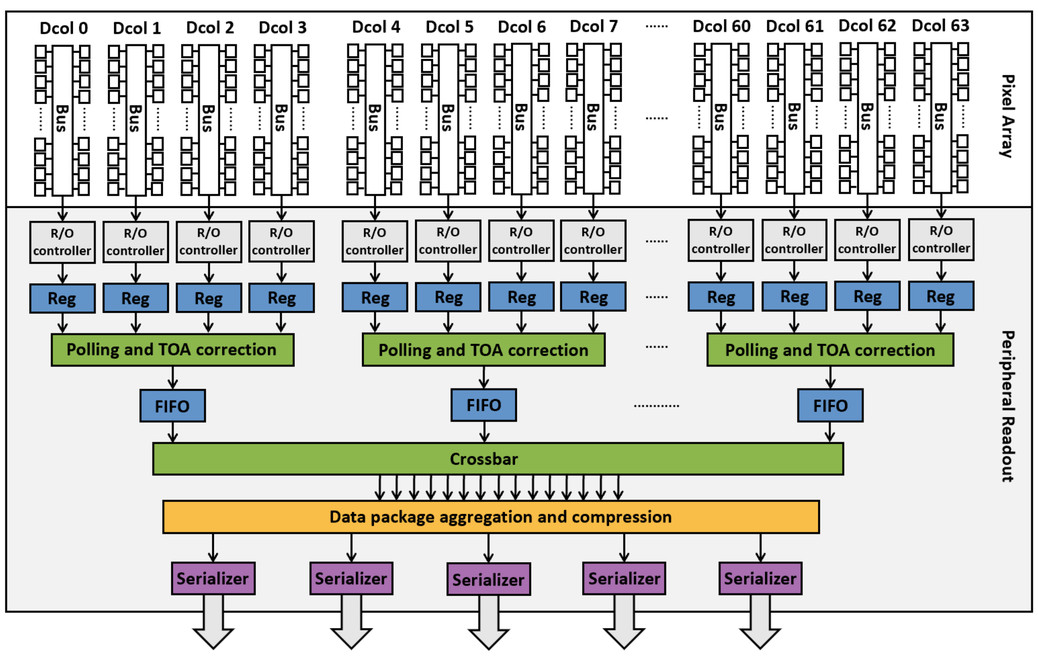
Simulation, Analysis and Optimization

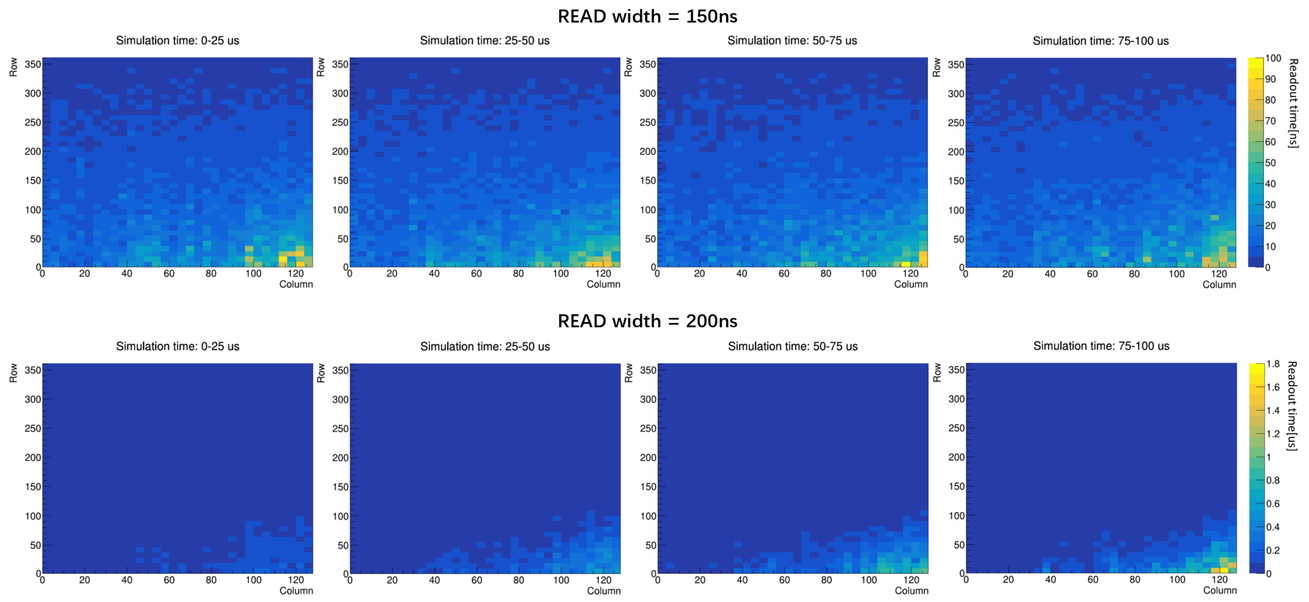
The row-column configuration of pixel array and the architecture of peripheral readout are shown below.

The pixel array uses a column-drain readout architecture. Every two columns serve as a unit sharing one EoC (End of Column). The single read period of EoC (the pulse width of READ signal) and the priority logic determine the readout time required for the process from the generation of hit information within pixel to its readout to EoC. Taking Chip1 as an example, positions with higher hit density or lower priority demonstrate longer readout time. When READ width = 200 ns, the readout time gradually increases as the simulation progresses, indicating that data congestion occurs within the pixel array.

Pixel size and array layout





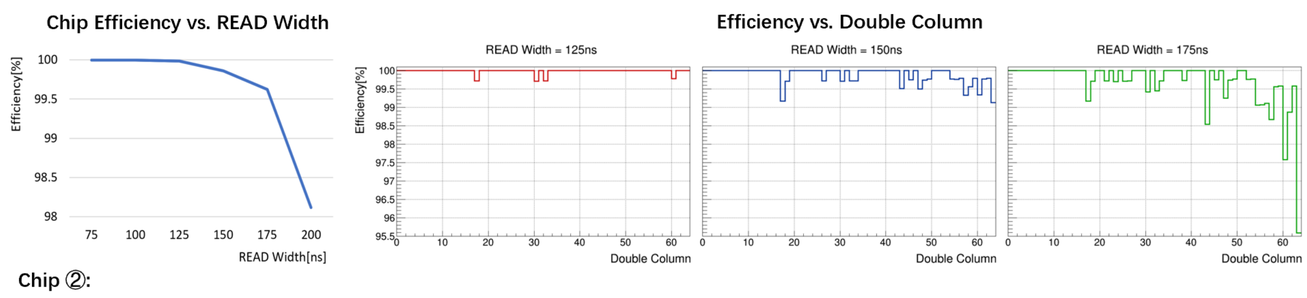


The READ width affects the hit loss as the simulation results indicate:

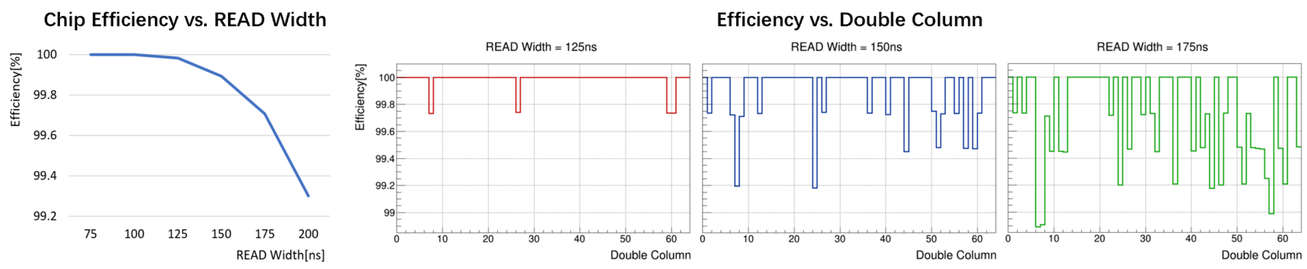
① The chip efficiency remains near 100% for READ width ≤ 125 ns but exhibits a significant decrease for READ widths > 125 ns.

② For READ width > 125 ns, the efficiency of chip1 not only decreases but also exhibits significant variation across different double columns.

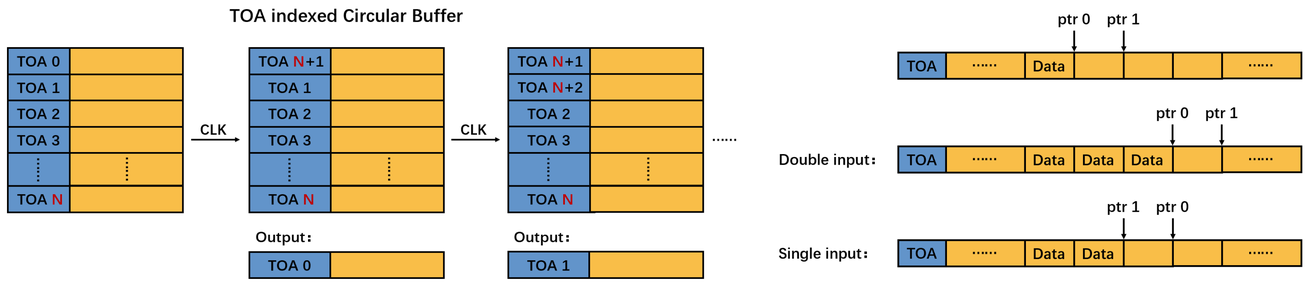
Chip ①:



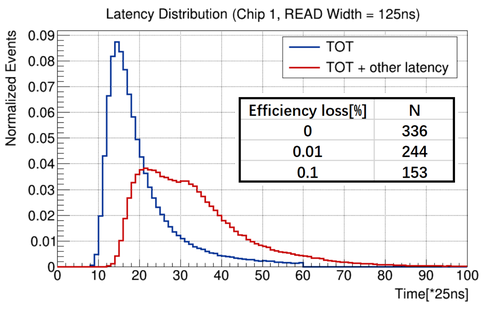
Chip ②:



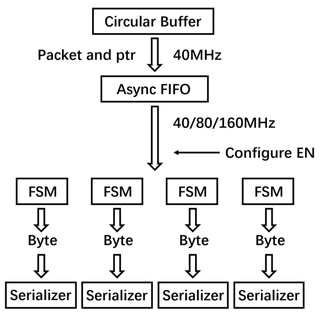
The core of the peripheral readout architecture lies in the data compression format. Aggregating data packets with identical TOA (Time of Arrival) can achieve approximately 30% bit saving. The key to realizing this lies in a globally shared multi-bank circular buffer. Double pointers are used in each bank.



Due to the priority queuing scheme, the latency from hit generation to packet arrival at the circular buffer follows a distribution. The number of banks, N, in the circular buffer is equal to the range of this latency distribution, expressed in units of main clock cycles. Most packets arriving in 11-90 cycles, which primarily influenced by the TOT distribution. However, a few packets suffer from significantly longer latency of up to 346 cycles, creating a long tail in the distribution. Using double pointers in each bank and a CIOQ (Combined Input and Output Queued) queuing strategy in crossbar, the long tail primarily originates from the queuing latency in pixels. The strategy for cutting this tail is driven by the trade-off between silicon area and efficiency loss. The 55nm HVCMOS process is expected to facilitate 100% efficiency in the peripheral readout.



The circuit composition of the circular buffer backend includes an asynchronous FIFO, some FSMs (Finite State Machine) and the same number of 8-bit to 1-bit serializers. The frequency of the final output link can be configured by setting the read clock of the asynchronous FIFO. The number of final output links can be configured by the ENABLE switches before the FSMs. These two configurations enable the chip to be compatible with different hit density. The FSMs split long packets into individual bytes and send them to serializers. The FSMs are designed carefully so that there is no bandwidth waste when FSMs handshake with the asynchronous FIFO. For the condition with four 1.28 GHz output links, the bandwidth utilization was 99.3%, 98.6%, 96.9%, and 95.0% respectively, enabling timely data transmission without congestion. In practical use, as a precautionary measure, the maximum number of output links is set to five.



Conclusion

Using the framework of SystemC behavioral modeling combined with Monte Carlo data, we simulate and analysis the chip performance in the real experimental environments and optimized the peripheral readout architecture to enable rational scheduling of transmission resources, addressing LHCb UP's data compression format requirements and the bandwidth limitations of the chip's readout links. The outcomes of this work are intended to identify bottlenecks in on-chip data processing and transmission under the high hit-density environment, and to further optimize the chip architecture to satisfy the comprehensive performance requirements of applications.

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C05

A low-power 55 nm HV-CMOS pixel sensor readout architecture for the CEPC Inner Tracker

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[3]Zhejiang University [4]Nanjing University, Nanjing, China [5]Dalian Minzu University, Dalian, China [6]Shandong University, Qingdao, China

Introduction

The HV-CMOS pixel sensor has been confirmed as the baseline technical solution for the inner tracking (ITK) detector of the CEPC. It needs to provide ~ns time resolution and <10 μm position under the condition of <200 mW/cm^2 power consumption.

On the basis of meeting the requirements of CEPC, two different readout architectures are proposed. The first one aims to further increase the upper limit of hit density (>100 MHz/cm^2) that HV-CMOS technology can handle (refer to Leyi Li's Poster). The other one target to further reduce the average power consumption of the HV-CMOS pixel sensor to simplify the requirements of the cooling system; this readout concept could also be used to further reduce the position resolution and improve data accuracy. (This Poster)

The power consumption theory

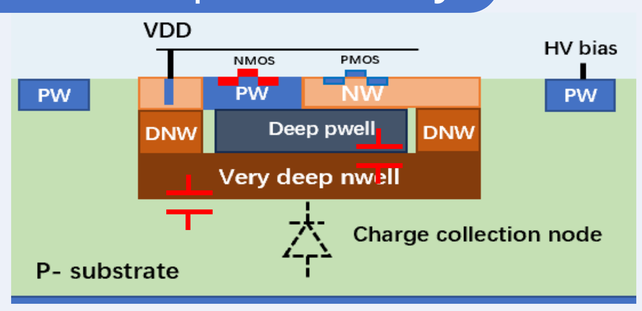


Fig 1. The pixel cross section view of a typical HV-CMOS sensor. The very deep N-well (VDNW) and P-type substrate formed the charge collection electrode. Charge-sensitive amplifiers (CSA) and readout electronics can be integrated nearby within the pixel

Working principle:

- The power consumption of a HV-CMOS pixel sensor (typically contains ~100000 pixel unit) mainly from the in-pixel electronics.
- The response time of a CSA proportional to the capacitance of the sensor diode (C_d) and inversely proportional to the transconductances of the transistor used for the amplifier (g_m), as given by:

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f}$$

- g_m is normally proportional to the consumed current. The relationship is:

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{DS}}$$

- Time walk is the main contributing source to time resolution. It is proportional to the time response of the CSA and the threshold (V_{TH}) of the comparator, and inversely proportional to the minimum signal quantity, which can be expressed as:

$$TW \propto \tau_{CSA}\frac{V_{TH}}{V_{sig,min}}$$

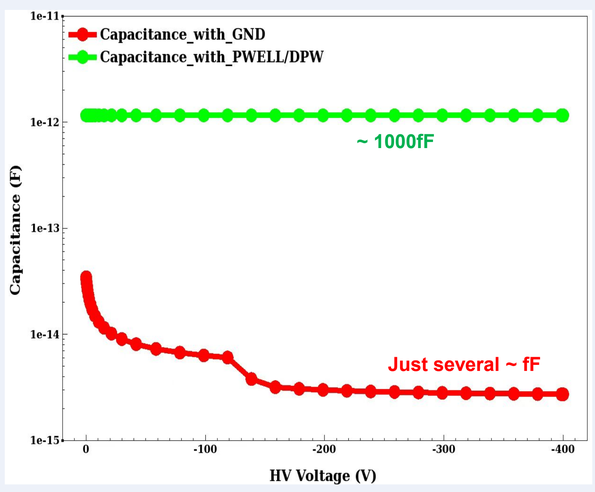
Conclusion:

For a determined temporal response, **a smaller C_d and large signal** are crucial to reduce the power consumption of the pixel sensor.

The C_d theory

The main contributions of C_d:

- **The capacitance between Deep pwell (DPW) and VDNW;**
- The capacitance between the signal collection electrode VDNW and P-sub;



Conclusion:

- Small in-pixel ASIC layout size is most important for less C_d; After the high - voltage reaches 200V, it is also the main source of C_d;
- A simple in-pixel electronic structure is very beneficial for low power consumption.

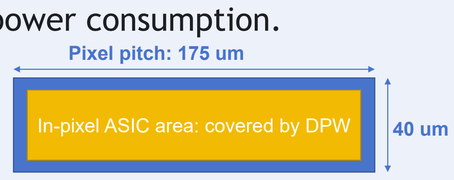
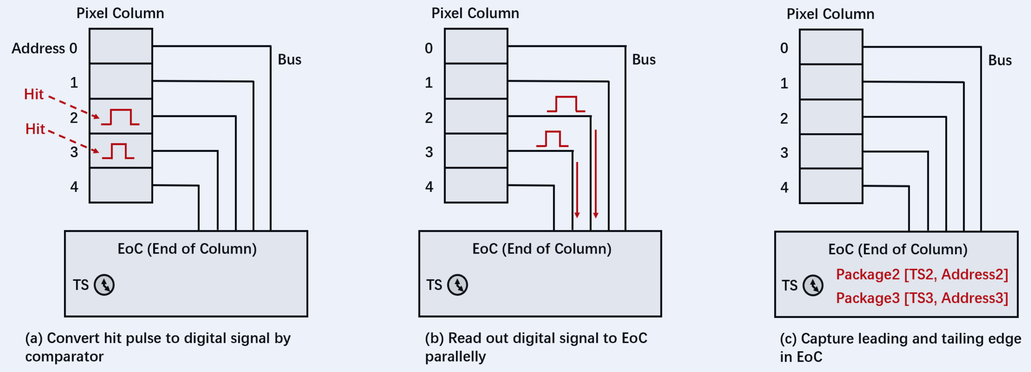


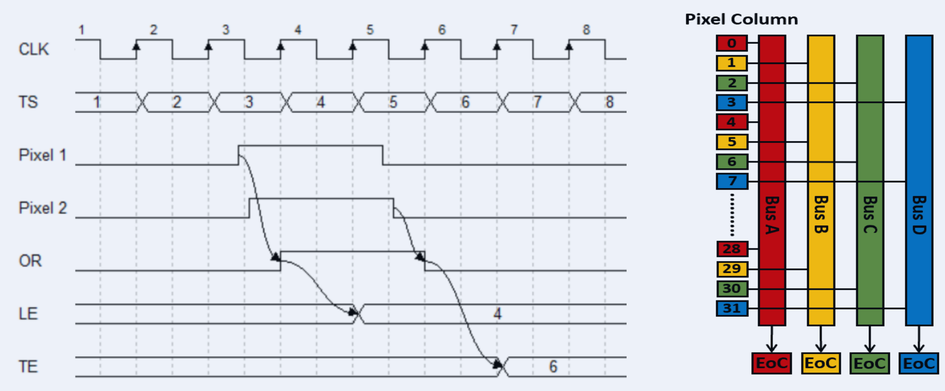
*Fig. TCAD simulation results of the relationship between the Cd value and bias voltage of a typical HV-CMOS pixel. The pixel size is set at 40*175um^2, most of the size is covered by DPW. The doping conditions are derived from speculation. Only the changing trends and proportions of the two capacitance sources are referenced.*

The low-power readout architecture



Read out concept of the pixel matrix: The signal output of each pixel is transmitted in parallel to the bottom of the column for further processing. It is characterized by the fact that the pixel can only contain an amplifier and a comparator, occupying very little area to achieve a smaller Cd value.

Multiple pixels simultaneously fired in a column, may lead to inaccuracies in time stamps.



To overcome such issues. Each column of pixels can be divided into 4 groups, input to 4 distinct EoC modules. Each EoC module contains two separate state machines and time-stamp counters, ensuring accurate time information even when particles hit adjacent pixels (charge sharing effect) or multiple pixels in the same column fired simultaneously.

Implementation of the readout architecture

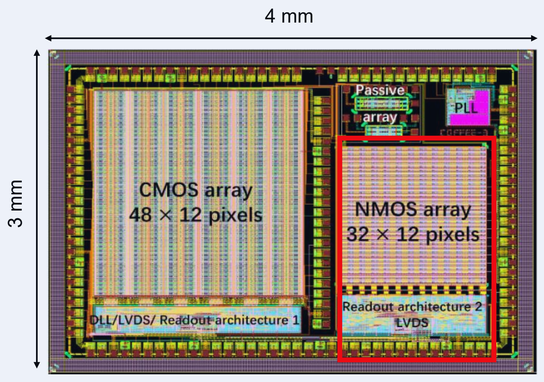


Fig. Layout of the COFFEE3, submitted Jan. 2025. The proposed architecture have implemented in the area circled in red in the above figure. The current process substrate resistivity is 10 Ω·cm, breakdown voltage is ~70V, depletion depth is ~10 μm.

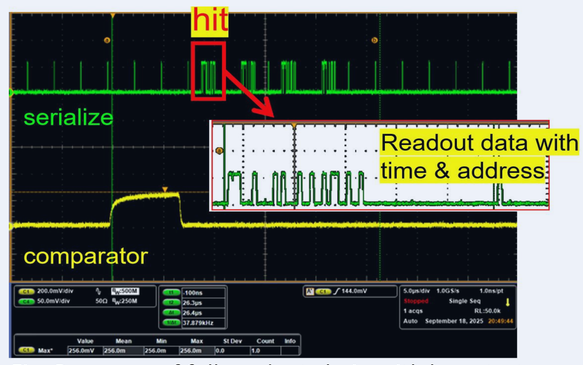


Fig. Response of full readout chain with laser test: Sensing diode → in-pixel (CSA\comparator\TDC) → EOC (digital peripheral) -> data link-> DAQ (refer to Boxin Wang's Poster)

Summary & outlook

On the basis of meeting the requirements of CEPC, we have proposed and preliminarily verified an 55nm HV-CMOS pixel sensor readout architecture on that has the potential to further reduce power consumption or improve position resolution accuracy.

The next step will focus on optimizing the process, increasing the breakdown voltage, and reducing the contribution of VDNW and P-substrate capacitance to C_d. High-resistivity wafers will be adopted to increase the total signal (from the current ~1000e- to ~16000e-), thereby simplifying the design and power consumption of the in-pixel CSA and further reducing the overall chip power consumption.

A simplified in-pixel design could also be used to further reduce the pixel size to improve position resolution, while this requires more discussions starting from the physical requirements to determine.

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Testing Results of the In-Pixel CSA, Discriminator, TDC, and Readout Circuit of COFFEE3 Pixel MAPS Prototype for CEPC

Yuman Cai[1], Mengke Cai[1], Leyi Li[1,3], Yiming Li[1], Weiguo Lu[1], Dexing Miao[1], Boxin Wang[1], Jianchun Wang[1], Xiaomin Wei[2], Zhiyu Xiang[1,5], Zijun Xu[1], Cheng Zeng[1], Xiaoxu Zhang[1,4], Yang Zhou[1]

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[3]Shandong University, Qingdao, Shandong 266237, China [4]Nanjing University, Nanjing 210093, China [5]Central South University, Changsha 410083 China

CEPC 2025 · C06 · COFFEE: CMOS sensOr in FIfty-FivE nm proceSs

Introduction

To address the requirements of CEPC inner-tracker, the COFFEE3 chip was developed using an advanced 55 nm High Voltage CMOS (HV-CMOS) process for high spatial and time resolution and low power consumption,COFFEE3 is designed to validate two distinct readout architectures integrated on a single chip, focusing on verifying circuit functionality and core performance. This poster presents the preliminary test results for the left-side array, which features a more complex in-pixel design incorporating a full CMOS-based CSA, discriminator, TDC, and priority-based readout, targeting higher hit-rate environments. Bench tests utilizing laser and radiation sources successfully demonstrate the basic functionality of the in-pixel circuits and the full readout chain at digital peripheral which also including the serializer and LVDS transceivers.

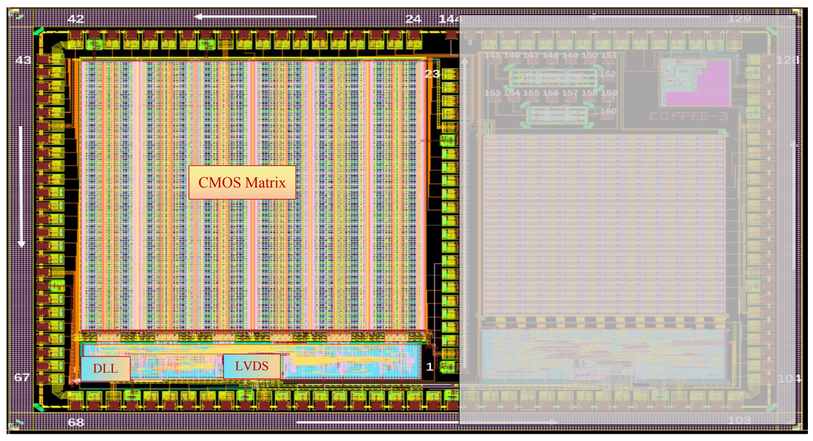


Fig 1 Layout of COFFEE3 chip for the left-side array

Left-side Array Design

Chip OVerview

- ✓ Chip Size: 4000 μm × 3000 μm
- ✓ Core Array: 48 (Rows) × 12 (Columns)
- ✓ Pixel Pitch: 40 μm (Column) × 145 μm (Row)

Pixel Array

- ● Analog Front-End
  - ✓ 4 Types of Charge-Sensitive Amplifiers (CSA)
  - ✓ CMOS Discriminator with Threshold Adjustment TDAC
- ● Readout Circuit & In-pixel Memory
  - ✓ Time-to-Digital Converter (TDC)
  - ✓ In-Pixel RAM & Address ROM

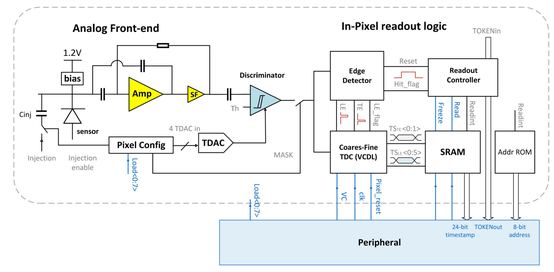


Fig 2 Functional schematic of the in-pixel circuitry

Innovative CSA

A unique "Double-Column" unit groups pixels for testing four CSA variants side-by-side:

- ✓ Double-Column 1: Cascode CSA
- ✓ Double-Column 2-3: Sensor-Isolated Cascode CSA
- ✓ Double-Column 4: Folded Cascode CSA
- ✓ Double-Column 5-6: Sensor-Isolated Folded Cascode CSA

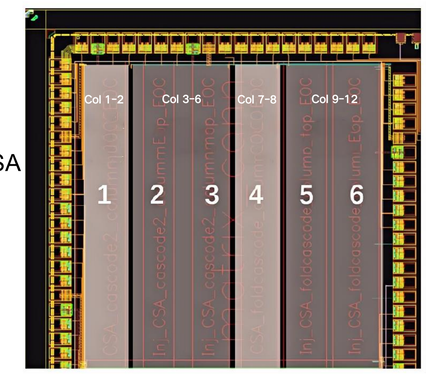
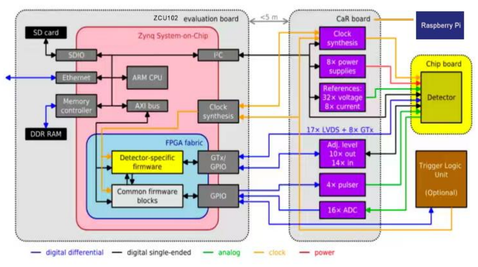


Fig 3 Left-side CMOS pixel array layout

Test Setup



Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Resources for various target applications

Fig 4 Caribou test system architecture & feature of CaR board

Pixel Matrix Test System

Test platform is based on Caribou system

- ✓ PC + ZCU102 + Caribou board + chip carrier board
- ✓ ZCU102 evaluation board from AMD/Xilinx
- ✓ CaR board DAQ framework from Caribou Project
- ✓ ASIC specific SW and FW by IHEP

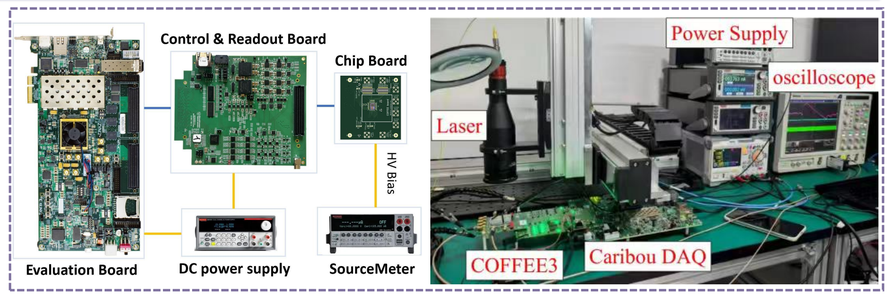


Fig 5 Photograph of the implemented test setup

Test Results

Pixel Matrix Test System

- ● Low-Voltage Differential Signaling (LVDS)

At 640 MHz supporting to 1.28 Gbps high speed data transmission, to reduce common mode noise.

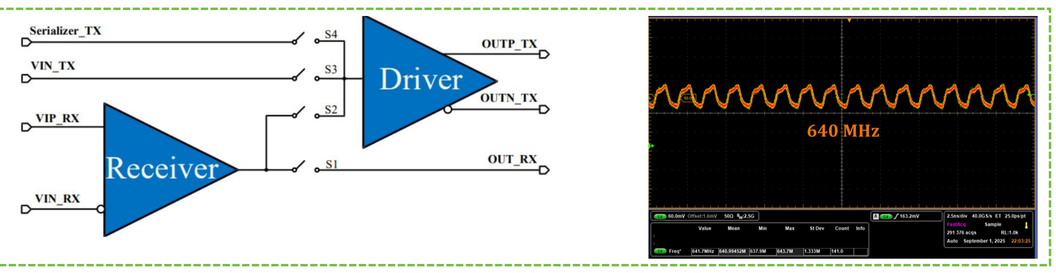


Fig 6 LVDS Overview & Functional Verification

- ● Delay-Locked Loop (DLL)

The phase difference matches expectations, to achieve a finer binning in time (~4 ns) than the main clock (23 ns).

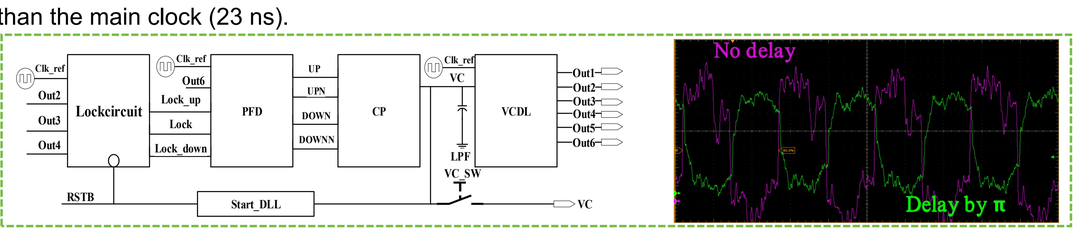


Fig 7 DLL Overview & Functional Verification

- ● Empty Packet Test

The expected Empty Packet was successfully read out.

- ● Pixel Mask Test
  - ✓ Successfully verified by enabling only a single pixel.
  - ✓ Data stream correctly switched between Empty Packet and Valid Hit Packet, confirming proper self-triggered readout logic and per-pixel control.

Fig 8 Empty Packet Output

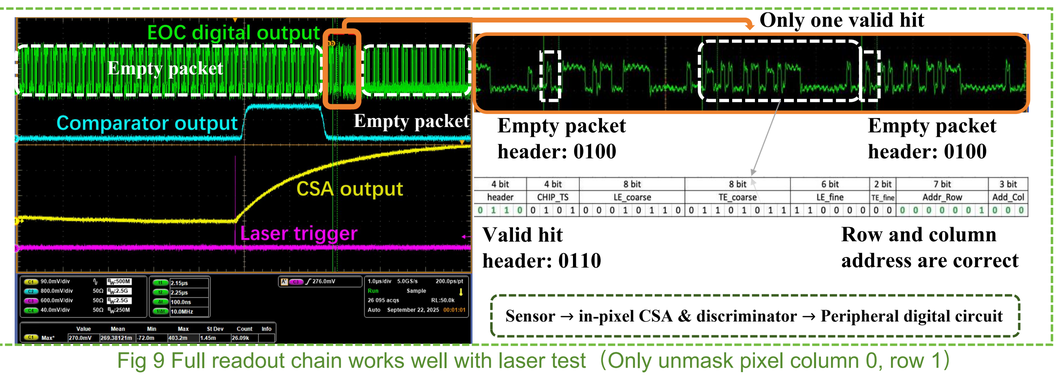


Fig 9 Full readout chain works well with laser test (Only unmask pixel column 0, row 1)

In-pixel Analog Test

- ● Charge Injection Test
  - ✓ Four types of CSA demonstrated correct functionality through direct charge injection.
  - ✓ Clear linear response to injected charge confirms predictable analog chain performance.

Reference Voltage	Set Value (V)	Default Value (V)
A1	0.45	0.447 (range: 0.1–0.7)
A2	0.94	0.910 (range: 0.7–1.2)
A3	0.97	0.759 (range: 0.6–1.2)
B1	0.93	0.930 (range: 0.7–1.2)
B2	0.80	0.547 (range: 0.1–0.8)
B3	0.75	0.746 (range: 0.6–1.2)
B4	0.60	0.500 (range: 0.1–0.7)

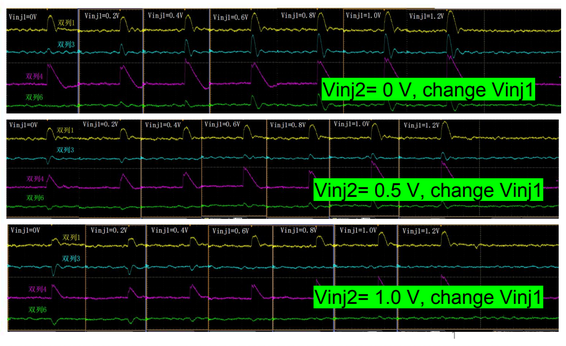


Fig 10 Peripheral digital circuit readout for charge injection test

- ● Laser Test

Pixel can response to laser signal, CSA and comparator work as expected and typical time over threshold (TOT) of laser signal is consistent with simulation.

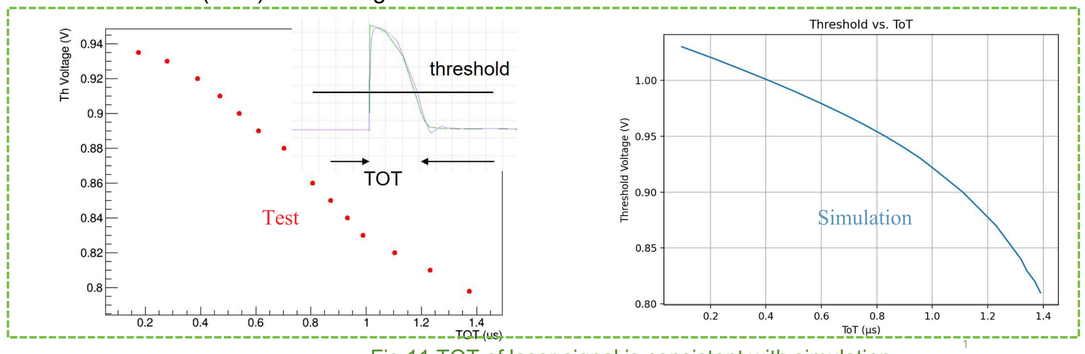


Fig 11 TOT of laser signal is consistent with simulation

- ● ^{55}Fe Radioactive Source Test

Pixel can also response to ^{55}Fe signal (x-ray).

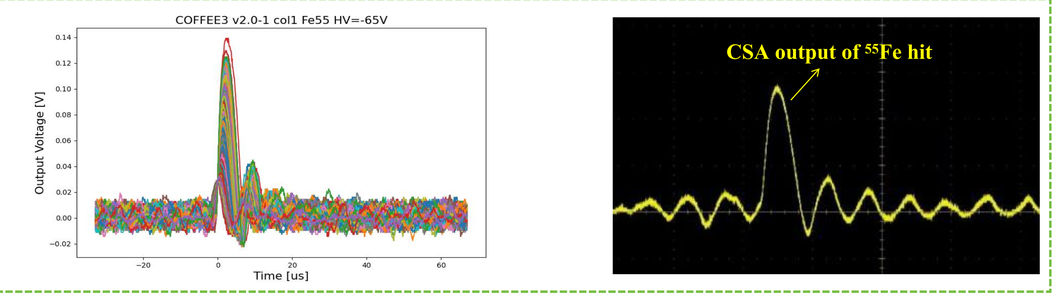


Fig 12 ^{55}Fe Radioactive Source test results

Summary & Outlook

- ● **Summary**

COFFEE3 left-side array preliminary testing results validates the basic functional design:

- ✓ Full Chain Operational: In-pixel circuits (CSA, discriminator, TDC) and peripheral logic are correct.
- ✓ Performance Verified: Achieved Gbps LVDS output, precise DLL clocking.
- ✓ Detection Confirmed: Clear response to charge injection, laser, and ^{55}Fe source demonstrated.

- ● **Outlook**

Future work will focus on detailed performance characterization and design optimization:

- ✓ Perform energy spectrum analysis on the collected ^{55}Fe data to quantify the energy resolution.
- ✓ Conduct beam tests with high-energy particles to evaluate spatial resolution, detection efficiency.
- ✓ Utilize the feedback from these tests to inform the optimization of the next-generation chip design.

Capacitance Optimization of AC-LGAD Sensors through Novel Structure Design and TCAD Simulation

C07

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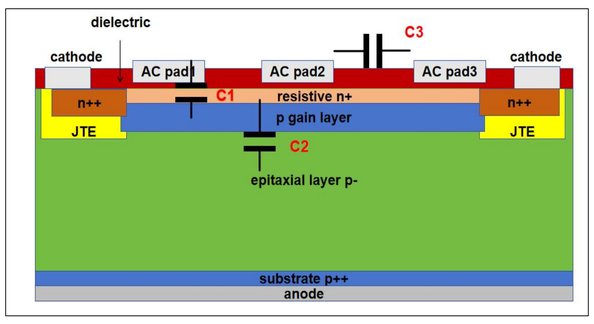
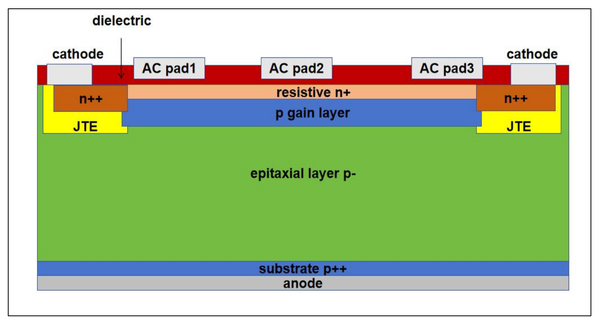
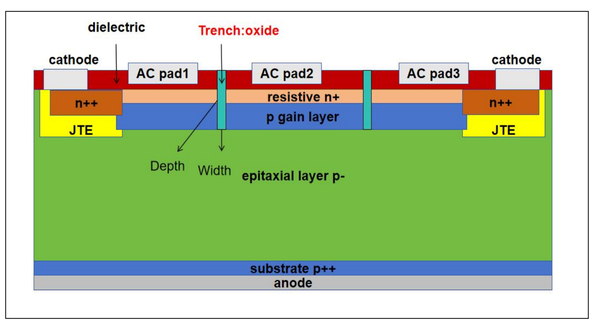


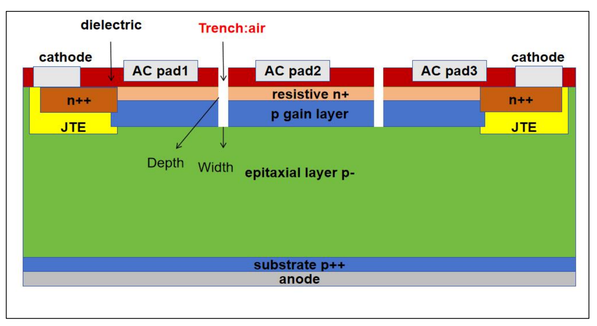
(a)Capacitance schematic of AC-LGAD with 3 AC pads



(b)Sketch of AC-LGADs with 3 AC pads



(c)Schematic of AC-LGADs with 3 AC pads and oxide-gap isolation



(d)Schematic of AC-LGADs with 3 AC pads and air-gap isolation

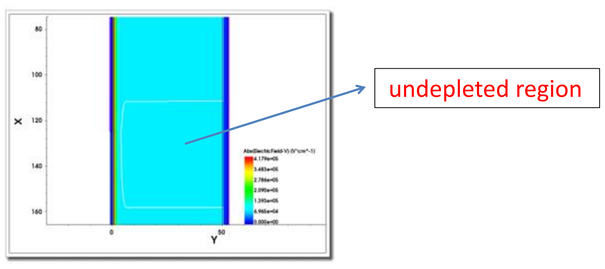
Fig. 1 Schematic diagrams of AC-LGAD structures: (a) Capacitance schematic (b) traditional structure, (c) with air-gap isolation, and (d) with oxide-gap isolation

Novel Low-Capacitance AC-LGAD Design: Core Innovations

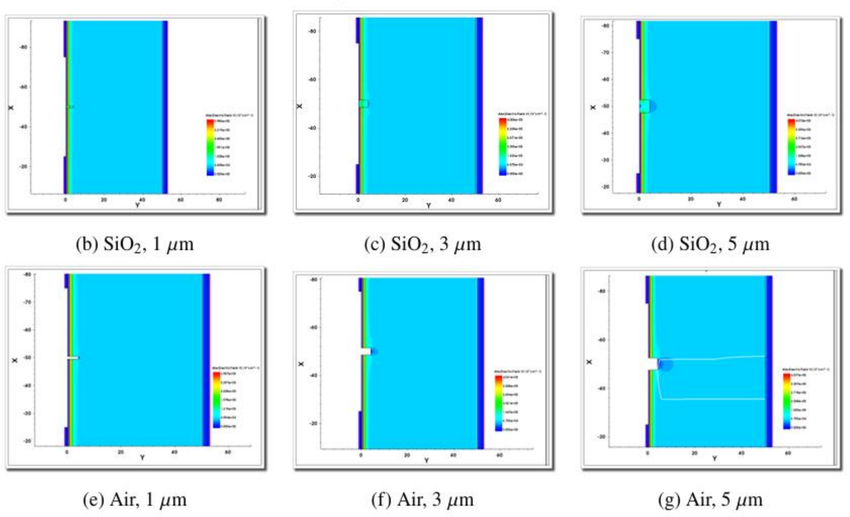
- **Low-k Dielectric Isolation**
  - ◆ Method: Add trenches (filled with SiO_2 or air) between resistive electrodes.
  - ◆ Effect: Low-k materials cut electric field coupling, reducing $C_{\text{inter-pad}}$ by over 1000x.
  - ◆ Outcome: Minimizes crosstalk, enhances spatial resolution.
- **Optimized Isolation Geometry**
  - ◆ Method: Tune isolation structure depth/width via simulations.
  - ◆ Effect: Deeper trenches concentrate electric fields; optimized width balances isolation & compactness.
  - ◆ Outcome: Ideal capacitance reduction, maintains practical sensor dimensions.

Electric Field Distribution Analysis

- ➢ Setup: 4 µm Depth, 0–10 µm Widths for Electric Field Distribution Study
- ➢ For the isolation width, both 1 µm and 3 µm are fully depleted



(a) Traditional structure



(b) SiO_2, 1 μm (c) SiO_2, 3 μm (d) SiO_2, 5 μm

(e) Air, 1 μm (f) Air, 3 μm (g) Air, 5 μm

Fig. 4 Electric Field Distributions: Isolation Structures' Effect

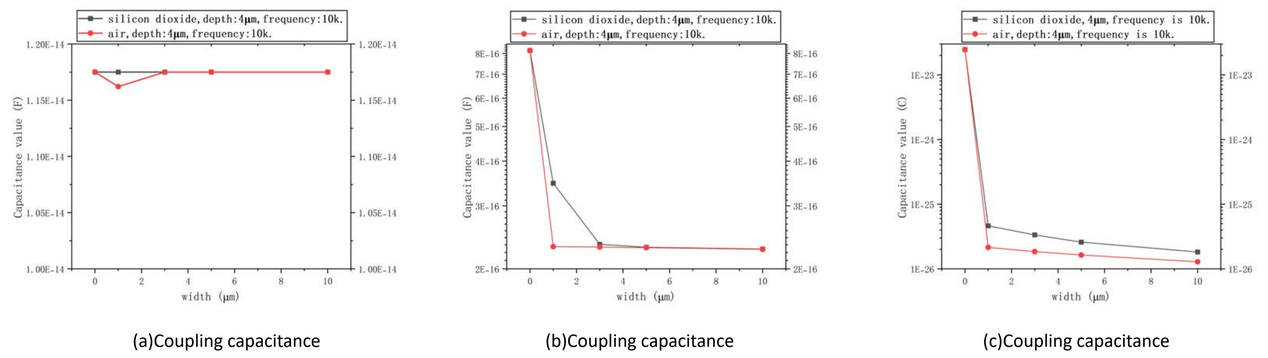
Summary

This poster presents low-capacitance AC-LGAD structure with low-k dielectric isolation is presented. TCAD simulations show inter-pad capacitance reduction over 1000× and bulk capacitance by ~ 70%. Vacuum isolation outperforms SiO_2 with an additional ~ 30% reduction, effectively suppressing parasitic capacitance and guiding future sensor design.

Key Parasitic Capacitances in AC-LGAD Sensors

- **C1 (Coupling Capacitance, C_{coupling})**
  - ☐ Location: Metal readout strips ↔ semiconductor gain layer (across dielectric)
  - ☐ Impact: Weakens signal, slows rise time, distorts waveform
  - ☐ Dependence: Dielectric thickness, permittivity, effective area
- **C2 (Bulk Capacitance, C_{bulk})**
  - ☐ Location: p–n junction (n gain layer ↔ p substrate; space charge region as capacitor)
  - ☐ Impact: Forms low-pass filter (with front-end capacitance) → attenuates high-frequency signals, degrades timing precision
  - ☐ Dependence: Follows $C = \frac{\epsilon S}{d}$; relies on gain layer/backplane area, separation, medium permittivity
- **C3 (Inter-Pad Capacitance, $C_{\text{inter-pad}}$)**
  - ☐ Location: Adjacent resistive electrodes (via semiconductor bulk, from inter-electrode electric fields)
  - ☐ Impact: Causes crosstalk → interferes with position reconstruction, limits spatial resolution
  - ☐ Dependence: Electrode spacing, semiconductor permittivity, thickness under electrodes

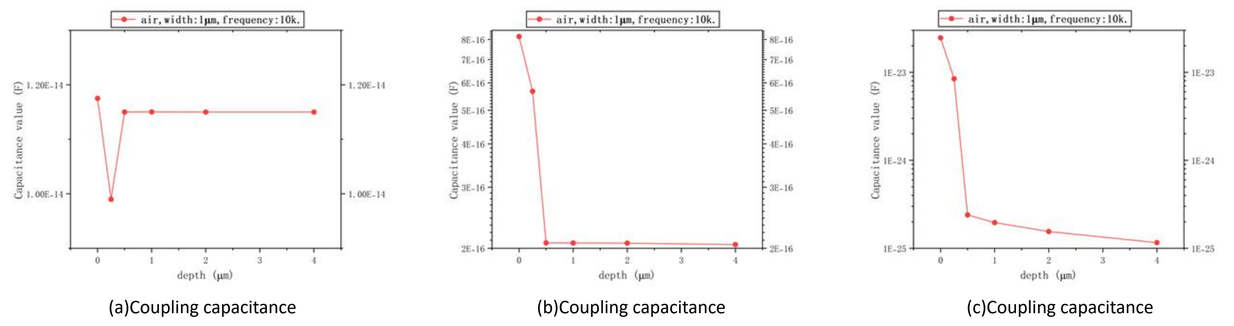
TCAD Simulation of Different Isolation Structure Parameters



(a)Coupling capacitance (b)Coupling capacitance (c)Coupling capacitance

Fig. 2 Effectofdifferentisolationwidthsoncapacitanceparametersatafixeddepthof 4 µm.

- Setup: Fixed isolation depth (4 µm), tested isolation widths (0–10 µm) to study capacitance changes.
- Key Trends:
  - $C_{\text{inter-pad}}$: Drops by >3 orders of magnitude (width 1→10 µm), Fig. 2(b).
  - C_{bulk} : Decreases by ~70% (width 1→10 µm), Fig. 2(c).
- Reason: Larger width lengthens electrode electric field coupling path, weakens field intensity; per $C = \frac{\epsilon S}{d}$, increased d reduces capacitance.
- Minor Impact: Isolation width has little effect on C_{coupling}.



(a)Coupling capacitance (b)Coupling capacitance (c)Coupling capacitance

Fig. 3 Isolation Depth vs. Capacitance (Air, 1 µm Width, 10 kHz)

- Setup: Fixed isolation width(1 µm), tested isolation depths(0–4 µm) to study capacitance changes.
- Observe:
  The capacitance reduction at a depth of 0.25 µm is far less effective than that at other depths.

KNN-Based Position Reconstruction Algorithm for AC-Coupled Low Gain Avalanche Diodes

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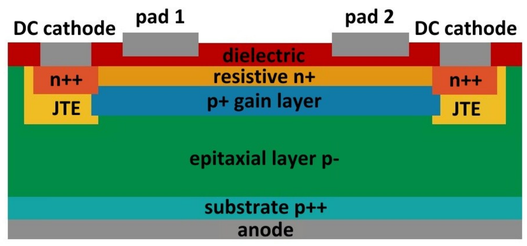
C08

Introduction

To meet the particle detection requirements of next-generation high-energy physics experiments, the AC-Coupled Low Gain Avalanche Diodes (AC-LGADs) have emerged as a breakthrough technology. The figure presents a cross-sectional schematic of an AC-LGAD structure. The intentional resistivity, achieved through deliberate low doping concentration of the n+ layer, causes the path length and direction of electron diffusion to vary with the particle hit position. As a result, the signal amplitudes induced on different metal pads exhibit a spatial dependence, enabling reconstruction of the hit position based on their relative signal strengths.



The complex nonlinear relationship between the signal ratios of metal pads and the particle hit position limits the effectiveness of analysis models, which motivated the adoption of K-Nearest Neighbors (KNN) algorithm for position reconstruction.

Modeling and Simulating Charge Diffusion

Developing reconstruction algorithms requires simulating the charge diffusion and collection process within the resistive readout structure to establish a mapping between particle hit positions and pad signal ratios.

The proposed 2D simplified model preserves the key physics of charge diffusion in the resistive readout structure while significantly reducing computational complexity. Its construction is relied on three fundamental principles (Ohm's law, current conservation and Dirichlet boundary conditions) :

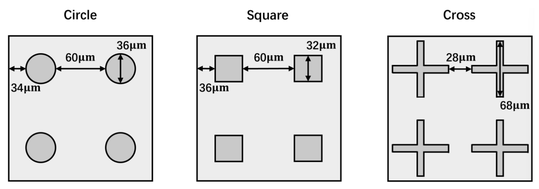
$$\vec{j}(x,y,t) = -\sigma \nabla V(x,y,t) \tag{1}$$

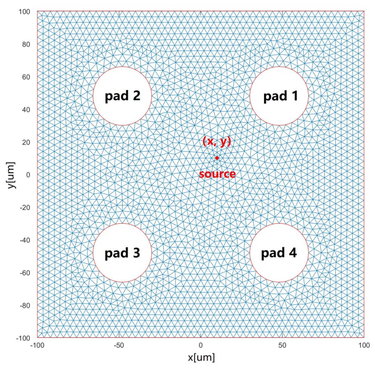
$$\frac{\partial V(x.y.t)}{\partial t} + \frac{1}{c}\nabla \vec{j}(x,y,t) = \frac{1}{c} I(x,y,t) \tag{2}$$

$$V(x,y,t) = 0 \tag{3}$$

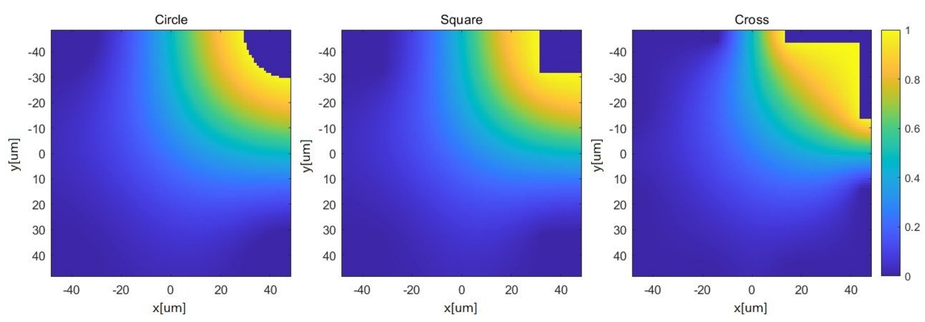
Finite element analysis (FEA) and iterative solvers are employed as the core numerical methods to solve the 2D model. The computational workflow was implemented using MATLAB's PDE Toolbox.

The simulation includes an annular DC cathode enclosing an inner area of 200 μm × 200 μm and four metal pads. Three different metal pad patterns (circle, square and cross), were simulated with equal pad areas and center-to-center spacing. Taking the circle-shaped metal pads as an example, the geometric configuration is illustrated. The n+ layer is defined as the entire square region, subtracted by the four metal pads and a transient source point modeled as a 1 μm-radius circle. The position of the source point is dynamically parameterized by (x,y) to simulate diverse particle hit positions.





By varying the position of the transient source, the particle hit points are scanned across the whole area at 1 μm intervals. The results are shown below, where the x and y axes represent the particle hit position and the color axis indicates the normalized signal proportion of the upper-right metal pad (Pad 1), relative to the total signals from all four pads.



When the particle hit around Pad 1, the signal proportion of this pad exhibits strong positional sensitivity, manifested as a steep gradient of signal proportion across the area. Near the pad edges, where one pad collects nearly all charges, position reconstruction becomes more challenging. This effect is particularly pronounced for cross-shaped pads, whose extended perimeter has larger ambiguous regions than circular or square pads.

KNN Algorithm and Feature Optimization

Let Q_1, Q_2, Q_3, Q_4 denote the normalized charge proportions of the four metal pads. For a test data point in the four-dimensional feature space (Q_1, Q_2, Q_3, Q_4), the KNN algorithm identifies the k closest training samples based on the Euclidean distance defined as:

$$d = \sqrt{\sum_{i=1}^{4} (Q_i^{test} - Q_i^{train})^2} \tag{4}$$

The coordinates of the unknown hit position are then reconstructed as the weighted average of the k neighbors' spatial coordinates, with the weights inversely proportional to their distances:

$$x^{rec} = \frac{\sum_{i=1}^{k} w_i x_i^{train}}{\sum_{i=1}^{k} w_i}, y^{rec} = \frac{\sum_{i=1}^{k} w_i y_i^{train}}{\sum_{i=1}^{k} w_i} \tag{5}$$

The training data are generated using the MATLAB PDE 2D simulation, where particle hit positions were scanned at 1 μm intervals. The test points are randomly generated. Their corresponding charge proportions Q_1, Q_2, Q_3 and Q_4 are also from simulation. These charge proportions serve as input for position reconstruction using the trained KNN algorithm. The positional residual of each test point is defined as the distance between the reconstructed position and the true position as:

$$Residual = \sqrt{(x_{rec} - x_{true})^2 + (y_{rec} - y_{true})^2} \tag{6}$$

The reconstruction accuracy was evaluated using the Root Mean Square Error (RMSE) of N test points as:

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=1}^{N} Residual_i^2} \tag{7}$$

The optimal k-value is determined by the k-curve. Figure (a) (b) (c) show the RMSE as a function of k-value for different pad patterns. Small k-values may overfit noise from individual samples, while large k-values may oversmooth the local geometry and degrade spatial resolution.

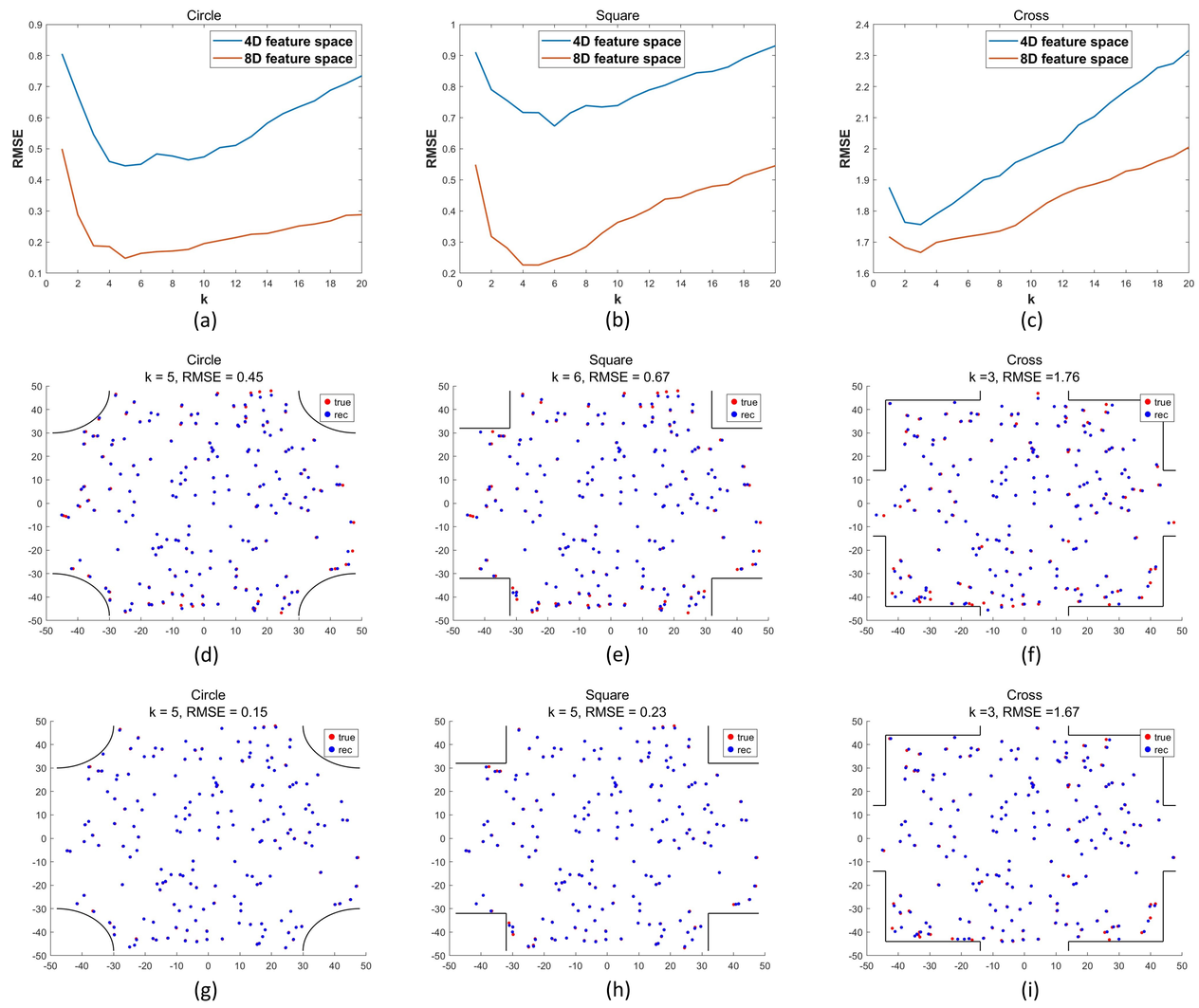
The reconstruction results for different pad patterns are shown in Figure (d) (e) (f). As expected, the reconstruction accuracy degrades significantly near the edges of metal pads, consistent with the locally predominant signal distribution observed in simulation. To correct the non-linearity, four additional features were incorporated:

$$R_1 = \frac{Q_1 + Q_4}{Q_2 + Q_3}, R_2 = \frac{Q_2 + Q_3}{Q_1 + Q_4},$$
$$R_3 = \frac{Q_1 + Q_2}{Q_3 + Q_4}, R_4 = \frac{Q_3 + Q_4}{Q_1 + Q_2} \tag{8}$$

The original four-dimensional feature space was extended to an eight-dimensional feature space (Q_1, Q_2, Q_3, Q_4, R_1, R_2, R_3, R_4) and the Euclidean distance is modified to:

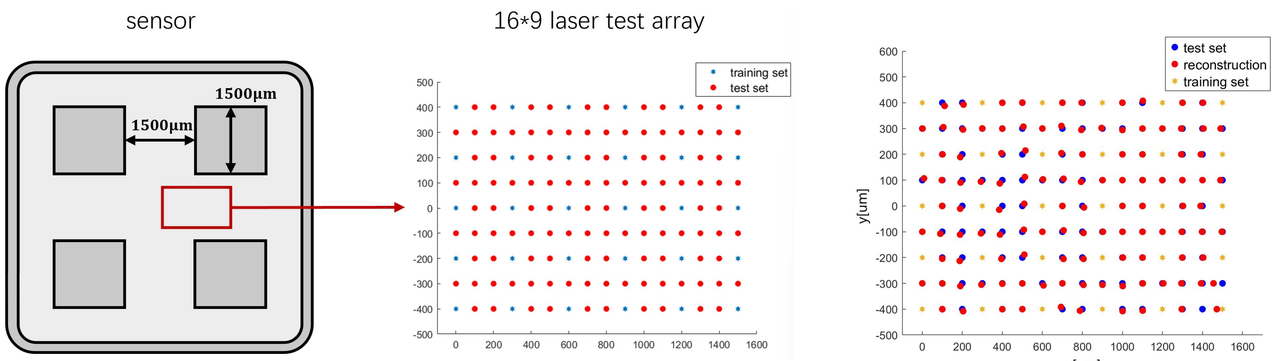
$$d = \sqrt{\sum_{i=1}^{4} (Q_i^{test} - Q_i^{train})^2 + \sum_{i=1}^{4} (1 - \frac{R_i^{train}}{R_i^{test}})^2} \tag{9}$$

This optimized feature space improves performance by combining direct charge proportions and their combinatorial relationships. The improved reconstruction results are shown in Figure (g) (h) (i).



Experimental Validation

The AC-LGAD sensor is fabricated on 8-inch wafers by the Institute of Microelectronics (IME). A 1064 nm laser with a focused spot size of ~10 μm (3σ) was used in conjunction with a three-dimensional translation platform with ~1 μm precision. A 16×9 laser hit array was scanned with 100 μm step between points. At each position, 1000 events were recorded by the oscilloscope and the corresponding signals of four metal pads were averaged for position reconstruction.



To validate the reconstruction algorithm, the 144 scanning points were divided into 30 for training and 114 for testing. Employing the KNN algorithm with the 8-dimensional feature space under the optimal k-value (k=3), the reconstruction results are shown above. As seen, the reconstruction positions match well with actual test positions. With 3000 μm pitch size and 300(x)/200(y) μm training grid intervals, the achieved RMSE is 11.2 μm.

Conclusion

In summary, this work has addressed several key aspects:

① A computationally efficient 2D charge diffusion model for resistive readout structure, grounded in fundamental physical principles, was developed and numerically implemented using MATLAB's PDE Toolbox.

② Comprehensive simulations scanning particle hit position were performed, generating essential datasets that revealed the complex, position-dependent signal distribution characteristics of the pixel-type AC-LGADs for various pad geometries.

③ To address the nonlinear position-signal mapping, a KNN-based algorithm was proposed and optimized. By expanding the feature space and selecting the optimal neighborhood size (k-value), the optimized algorithm significantly improved the reconstruction accuracy, particularly reducing residuals near pad edges for circular and square configurations.

④ The optimized algorithm was validated using experimental data. A polynomial surface fitting and interpolation effectively use sparse training data, enabling the algorithm to achieve a satisfactory positional reconstruction accuracy.

By integrating modeling, simulation, algorithm development and experimental validation, this study establishes a systematic framework for validating AC-LGADs design and optimizing the position reconstruction algorithm, exploiting the potential of AC-LGADs for next-generation high-energy physics experiments.

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Prototype assembly and tests for CEPC VerTeX detector

C09

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1. Introduction

The first four layers of the CEPC (Circular Electron Positron Collider) VTXD (VerTeX Detector) are designed using wafer-scale sensors based on stitching technology. To ensure the inner most layer is as close as possible to the central beam pipe, the design radius is set at 11.1 mm, posing significant challenges for the development of bent detector modules. In this study, a complete prototype module is designed and developed to validate bent chip bonding techniques. Additionally, to verify the performance of silicon pixel sensors after bending, a small-area bent detector module with a radius of 20 mm was fabricated using 50 μm-thick MAPS (Monolithic Active Pixel Sensors) chips.

■Vertex detector design from CEPC TDR

The VTX is designed as six concentric cylindrical pixel layers covering a radius of 11.1 mm to 47.9 mm around the beam pipe, with a polar angle coverage of $|\cos\theta| < 0.99$.

➢ Inner layers (1-4 layers) with stitching design
➢ Outer layer (layers 5 and 6) with double-sided ladders design

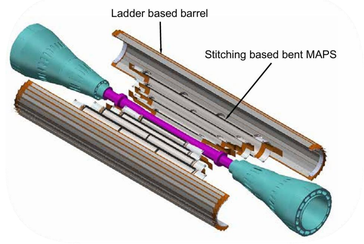

Fig.1 CEPC Vertex detector

$$\sigma_{r\varphi} = a \oplus \frac{b}{p(GeV)sin^{3/2}\theta}\ \mu m$$

a = 5 μm and b = 10 μm·GeV

Parameter	Design
Spatial Resolution	~5 μm
Material budget	~0.8% X_0
First layer radius	11.1 mm
Mechanical Support	Ultralight structures
Angular Coverage	$\|\cos\theta\| < 0.99$
…	…

Table.1 Vertex detector design parameter

■R&D of the inner layer VTXD prototype

➢ Producing a full-sized vertex detector's first four layers using ultra-thin curved stitched chips is highly challenging, and the process development is crucial
➢ As the first four layers of CEPC VTXD, the radius are 11.1 mm, 16.6 mm, 22.1 mm, and 27.6 mm respectively
➢ This study can validate the processes for the minimum bending radius, full-sized bent detection module (long-readout FPC), and the assembly processes to accumulate valuable experience for CEPC VTXD

2.Prototype module design

■Prototype module design

The full-sized prototype model consists of the FPCs (Flexible Printed Circuits), thinned dummy sensors, Cylindrical support (including the chip supports and FPC supports structure).

Layer	Chip Length mm	FPC Length mm	Chip width/arc length mm
Layer1	161.4	145.2	34.54
Layer2	121.1	104.8	51.81
Layer3	161.5	64.4	69.08
Layer4	134.6	24	86.35

Table.2 ¼ VTXD prototype module design parameter

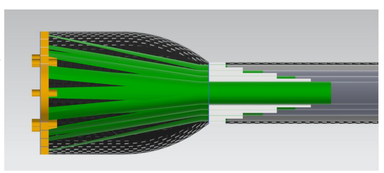

Fig.2 ¼ VTXD prototype module

➢ **Dummy sensors.** The thickness is thinned to 30-40 μm. The Layer1-3 are cut from 8-inch wafers, and the Layer4 is cut from a 12-inch wafer
➢ **Chip supports.** Select PMI foam (~0.075 g/cm^3), which offers high structural strength and low material budget. To ensure the strength of the support structure, holes are drilled in the foam to enhance airflow for better heat dissipation, while further reducing material budget
➢ **FPCs.** The composite FPC consists of three layers of 37.5 μm thick Cover layer, 18 μm thick signals (Copper), and 50 μm Core FR4

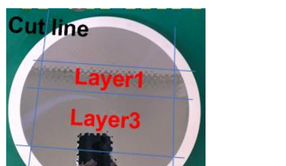

Fig.3 8-inch dummy wafer

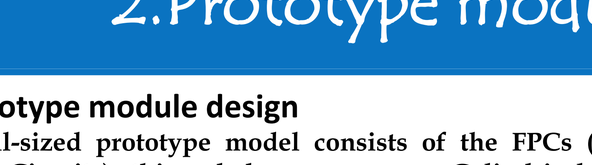

Fig.5 FPC structure

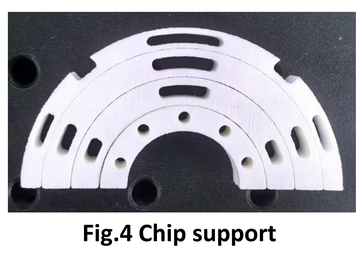

Fig.4 Chip support

➢ **FPC supports.** Using 3D printing, positioned outside the polar angle θ between the chip and FPC, and fix and support the FPCs. Protecting the lower chips from contact with the upper FPCs

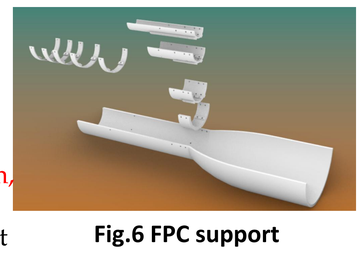

Fig.6 FPC support

■Material budget

➢ Gray represents the PMI support position, the rings width is 10 mm, and red indicates the detector position
➢ Average material budget per sensitive layer **: ~0.1068 %X_0,** The next step is to optimize the structure and minimize the material budget

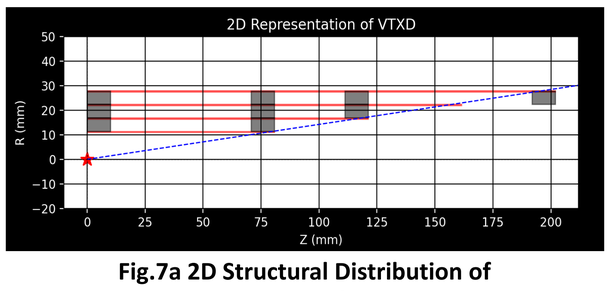

Fig.7a 2D Structural Distribution of VTXD prototype in the Z Direction

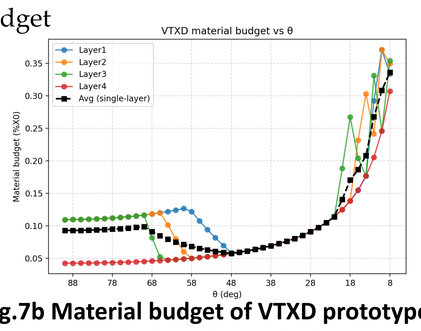

Fig.7b Material budget of VTXD prototype with the polar angle θ

3. Prototype module assembly

Validation and successful of a bent dummy wafer with an 11 mm radius without wire bonding.

■ Assembly

First wire bonding, then bending together.

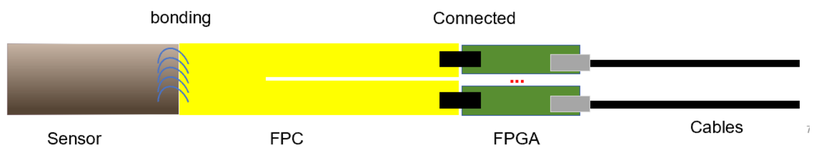

Fig.9 Full-sized Prototype module structure

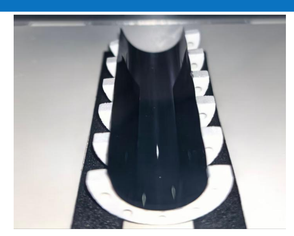

Fig.8 11 mm radius bending Without damage

➢ **Glued.** The non-sensitive area of the chip is glued to the edge of the FPC (2 mm margin) using liquid insulating adhesive. The adhesive thickness is controlled at 50 μm
➢ **Wire bonding.** The chip is bonded to the FPC and electrically connected through bonding
➢ **Bending.** After bonding, the detector module is fixed onto the spool and slowly curled together
➢ **Support.** four layers, with reasonable screw holes designed based on practical experience, secured with screws

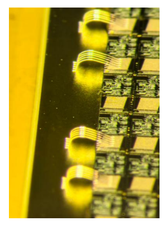

Fig.10a Wire bonding

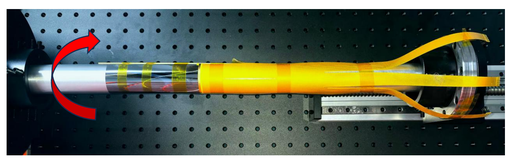

Fig.10b Bending

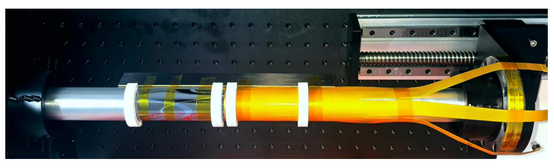

Fig.10c Support

■Pull Test

➢ The tensile results before and after bending are consistent
➢ all tensile results ranging from 4-8 g, which is related to the quality of the pads on the dummy chip

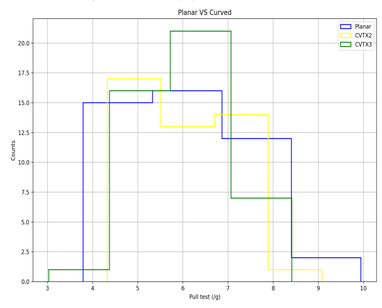

Fig.11 The pull test before and after bending

4. Performance tests after bending

■Small bent detector

To verify the performance of the chip after curling, a small-area curled detection module was designed and tested.

➢ The bent detector module based on MAPS primarily comprises a bending support frame, a test readout board, and a chip
➢ The bending radius is 20 mm

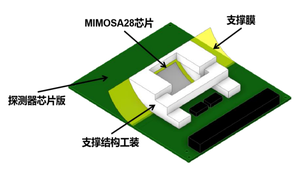

Fig.12 A small bent detector module

■Test Results

➢ The noise level tests on the same chip before and after bending remain consistent.
➢ The test beam was conducted at IHEP, and the residual distribution is consistent before and after bending.

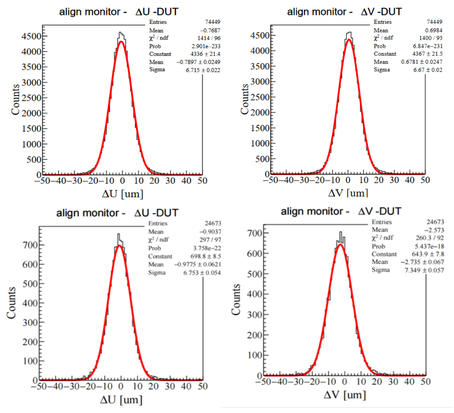

Fig.13 Residual distribution of Planar detector and bent detector

■Next plan

➢ Using a small-area MAPS chip, performance tests were conducted on the full-sized detector (including the long readout FPC) after bending.

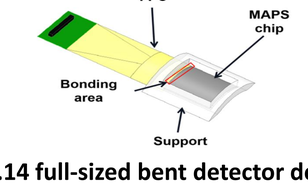

Fig.14 full-sized bent detector design

5. Summary

- From the requirements of CEPC TDR, the vertex detector consists of six layers, with the innermost four layers using stitched chip.
- A full-sized VTXD prototype model was designed, with a low material budget of about 0.1068% X_0 per layer.
- Key components were designed and produced, optimizing the VTXD assembly process.
- The tensile results before and after bending are consistent.
- The performance of the bent detector is consistent with that of the planar detector. The next step is to enhance the performance testing of the long-readout bent module.

Background Analysis and Digitization of CEPC Vertex Detector

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C10

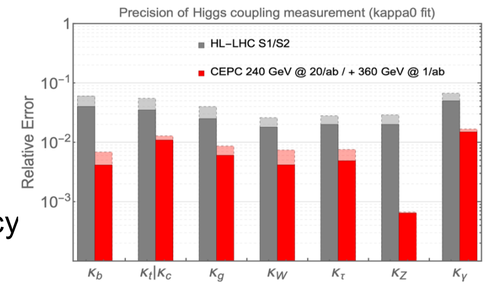
Vertex Detector

As the next generation collider, CEPC is far beyond a Higgs factory:

- Searching for exotic or rare decays of H, Z, B and τ, and new physics
- Huge measurement potential for precision tests of SM: Higgs, electroweak physics, flavor physics, QCD/Top

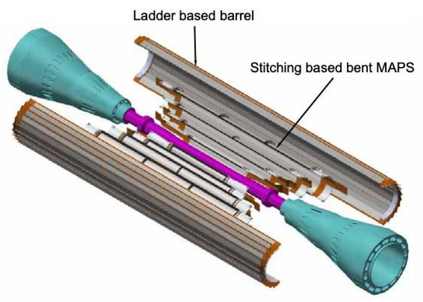
Whether it is flavor physics or Higgs physics, precise vertex measurement is an essential requirement for achieving the CEPC's physics goals.

For we have no precise digital model, the accuracy of model particularly in the forward region of the long barrel is not high, **we conducted beam test at BRSF and explored and established the TaichuPix digital model based on the results of the beam tests**.



Specification	Index
Pixel size	$25\mu m \times 25\mu m$
Dimension	$15.9mm \times 25.7mm$
Techonology	CIS 180nm
Dead time	$< 500ns$
Power density	$< 200mWcm^{-2}$
Max. Hit rate	$36 \times 10^6 cm^{-2}s^{-1}$

TaichuPix-3 Performance Index



Baseline scheme of CEPC vertex detector

Digital Model

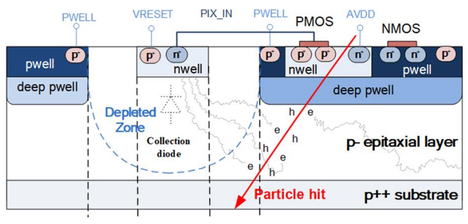
Considering the issues:

- **Low accuracy in the forward region.**
- **The performance simulation does not include the complete physical processes**

A model based on beam test result and AP2 simulation is developed to estimate cluster size.

$$C = a \sec\theta + b$$

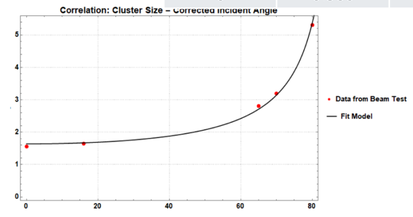
C is the Cluster Size, and θ is the incident angle

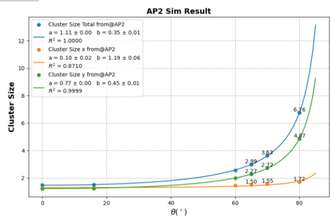


Geometry of TaichuPix

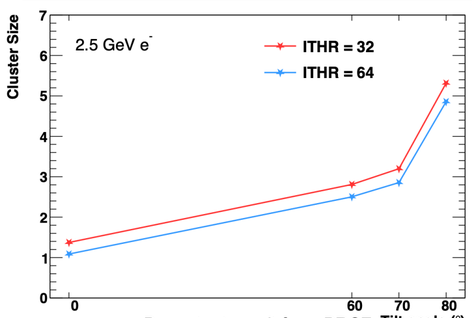
Param	Estimate	Std Error	RSquared
a	0.783	0.022	0.9995
b	0.856	0.069	

Fitting result of beamt test(left fig& table) and simulation(right fig) shows that the model is reasonbale.





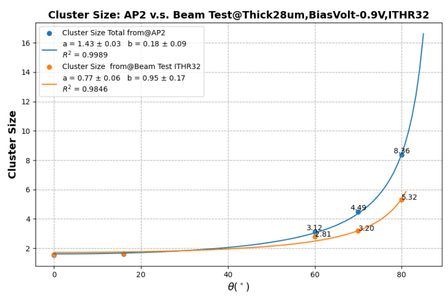
Beam Test Result v.s. Simulation

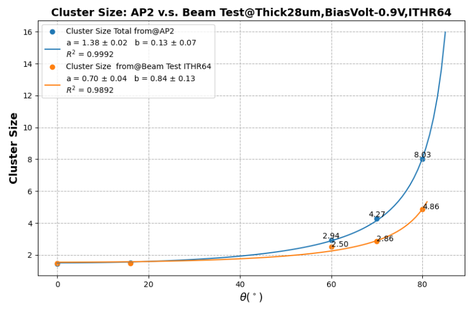


Angle	ITHR32	ITHR64
0°	1.561	1.469
16°	1.645	1.478
60°	2.809	2.504
70°	3.199	2.856
80°	5.315	4.857

from prototype beam test at DESY II

The figure above presents the results of the beam tests. To make the conclusions more reliable, we also incorporated the beam test results from DESY II. By comparing the beam test results with the AP2 simulation results, we found some significant differences when the parameter settings were the same as those in the experiments.





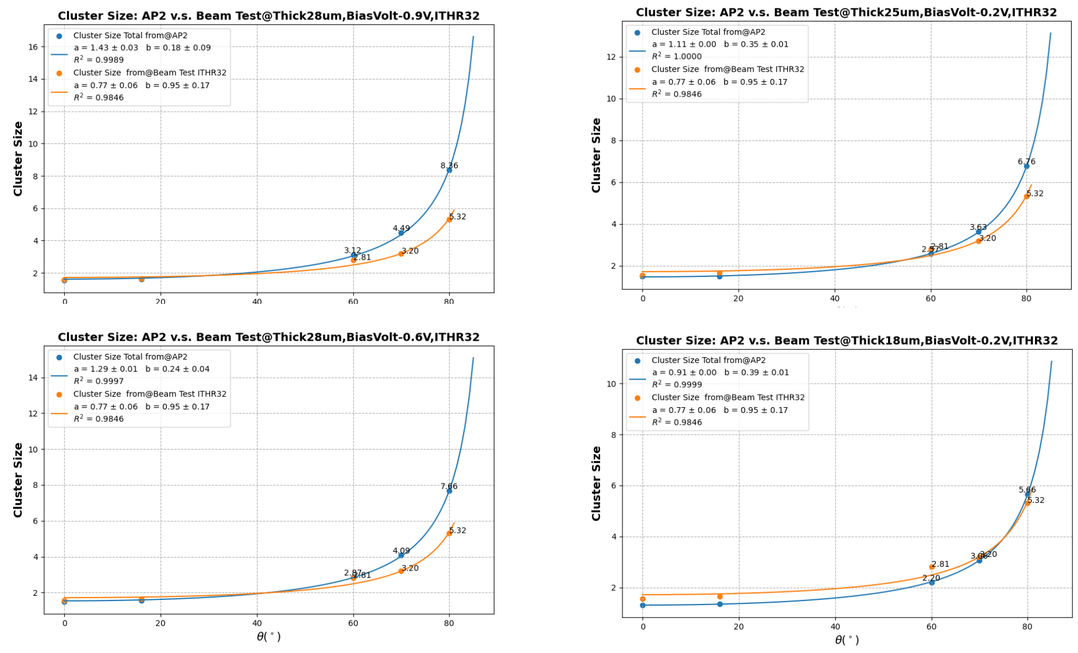
Some significant differences under large angle.

Here are some possible reasons:

- In AllPix-2, signals produced by the substrate do not contribute.
- Due to electric field distributions, the effective sensitive thickness may differ from the true thickness.

Beam Test Result v.s. Simulation

Then we try to change the parameters and results show as below.



The simulation results from AllPix-2 are acceptable in comparison to the experimental measurement results.

Beam Background Estimation

- Signal-to-noise ratio is very low, makes background analysis very important
- Provide directions for improving geometry, estimate power consumption…

Background	Generation	Tracking	Detector Simulation
Synchrotron Radiation	Geant4	Geant4	
Beamstrahlung/Pair Production	Guinea-Pig++		
Beam-Thermal Photon	PyBTH		
Beam-Gas Bremsstrahlung	PyBGB		CEPCSW/FLUKA
Beam-Gas Coulomb	BGC in SAD	SAD	
Radiative Bhabha	BBBREM		
Touschek	PyTSK with SAD		

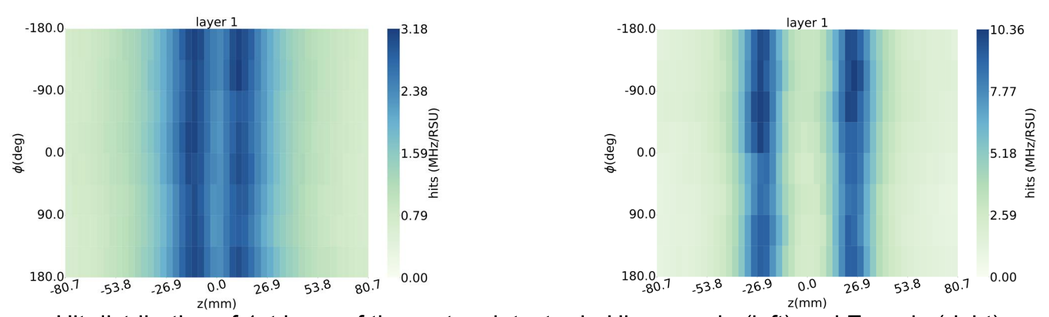
Based on the digitization model, the beam background shown as following table:

Layer	Ave. Hit Rate (MHz/cm^2)	Max. Hit Rate (MHz/cm^2)	Ave. Data Rate ($Mbps/cm^2$)	Max. Data Rate ($Mbps/cm^2$)
Higgs mode: Bunch Spacing: 277 ns, 63% Gap				
1	6.2	12	760	1500
2	0.84	1.6	87	160
3	0.17	0.36	19	38
4	0.067	0.16	8.4	19
5	0.017	0.037	2.1	4.2
6	0.013	0.026	1.6	3.7
Low-luminosity Z mode: Bunch Spacing: 69 ns, 17% Gap				
1	15	39	2700	8100
2	1.7	2.6	240	400
3	0.72	1.2	110	240
4	0.43	0.94	70	210
5	0.10	0.19	14	31
6	0.078	0.15	11	23

No trigger and error window here.

Threshold has been taken into consideration. (ITHR 32 = 368e, 1.3keV/pixel)

$$\text{Data Rate} = \text{Hit Rate} \times 32\ \text{bit} \cdot \text{pixel}^{-1} \times \text{Cluster Size}$$



Hit distribution of 1st layer of the vertex detector in Higgs mode (left) and Z mode (right)

Summary

To verify the performance of TaichuPix at different incident angles and provide a reference for future digitization, we conducted beam tests and established a cluster size model based on the current beam test results.

- Cluster Size at large incident angle approximately equals to 5 (3 after thined), and normal incident equals to 1.5.
- After making appropriate adjustments, the AP2 simulation results align well with the experimental results.
- The beam background was estimated based on the digital model we established.

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The Impact of Beam-Induced Backgrounds on the CEPC Vertex Detector Performance

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1. Nankai University 2. Institute of High Energy Physics, CAS

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Abstract

The identification of heavy-flavored quarks and τ leptons is a key physics goal of the CEPC. As a crucial component of the tracking system, the CEPC Vertex Detector (VTX) demands exceptional spatial resolution for vertex reconstruction and flavor tagging, with the impact parameter (d_0 , z_0) as its core performance indicator. Due to its proximity to the beampipe, **beam-induced backgrounds (BIBs)** may severely degrade the VTX's performance—thus, assessing such impacts is critical for advancing the CEPC's precision physics program.

Based on the **CEPCSW** simulation framework, this study compares the impact parameter resolutions (d_0 , z_0) of tracks in the CEPC Vertex Detector (VTX) under **BIB-free** and **BIB-included** scenarios (encompassing Pair production and four single-beam backgrounds: BGC, BGB, TSC, BTH) across different incident angles and analyzes the variations of these resolutions with the incident momentum of the signal particle (μ^-).

Introduction

Core Track Parameters: d_0 & z_0

- **d_0** : Signed transverse impact parameter – the closest approach to the beam axis in the r–φ plane.
- **z_0** : Longitudinal coordinate of that point of closest approach.

Extracted from helical track fits in the vertex detector, these parameters set the primary-vertex resolution and directly determine the flavour-tagging performance.

Background Category	Background Type	Abbreviation	Core Definition
Single-beam Background	Beam-Gas Bremsstrahlung	BGB	Beam particles undergo inelastic scattering with residual gas
	Beam-Gas Coulomb Scattering	BGC	Beam particles undergo elastic scattering with residual gas
	Beam-Thermal Photon Scattering	BTH	Interactions between beam particles and beam pipe thermal photons
	Touschek Scattering	TSC	Scattering of particles within the beam bunch via transverse oscillations
Luminosity-related Background	Pair Production	—	Photons from beam-beam interaction produce electron-positron pairs via strong electromagnetic fields

Beam-induced background categories accounted for in this study.

- **Pair production** dominates the beam-induced backgrounds (BIBs) of the CEPC Vertex Detector (**>90%**).
- **Single-beam backgrounds** are effectively suppressed by beam pipe optimization, W/SS shielding, and vacuum enhancement, with **relatively small proportions**.

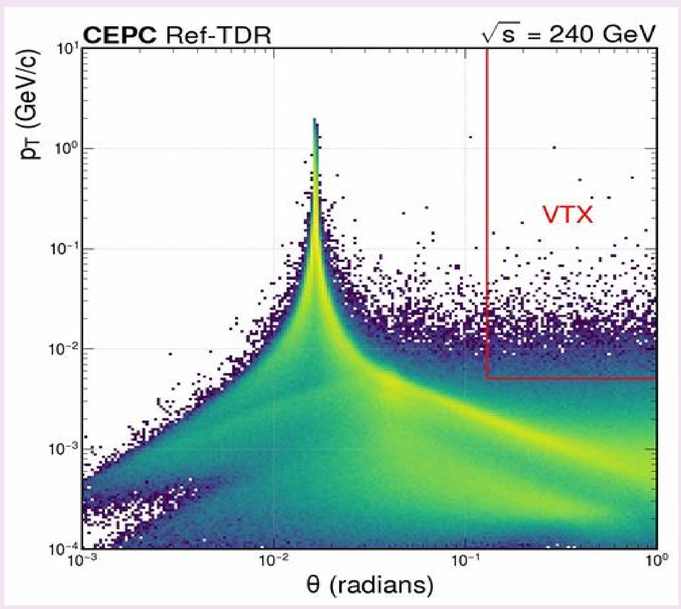

Figure 1: Energy and polar angle distribution of particles out of the pair production beam induced background at Higgs mode. VTX stands for the vertex detector.

BIB Mixing Methods

Signal events are overlaid with beam-induced backgrounds at the SimHit level, preserving energy-time-position merging within each detector cell.

Background Type	Rate ($\times 10^{-7}$ Hz)	Sampling Mode
Pair production	—	Fixed 277 ns window, 1 BX
BGB	6.67	Poisson
BGC	8.78	Poisson
BTH	40.15	Poisson
TSC	63.18	Poisson

Note: Higgs-mode BX = 277 ns beam-crossing period.
Rate data extracted from Higgs-mode background-generation configuration in CEPCSW.

Backgrounds are overlaid on signal events via Poisson sampling or a fixed 277 ns window.

BIB Mixing Results

Inner Solenoidal Magnetic Field

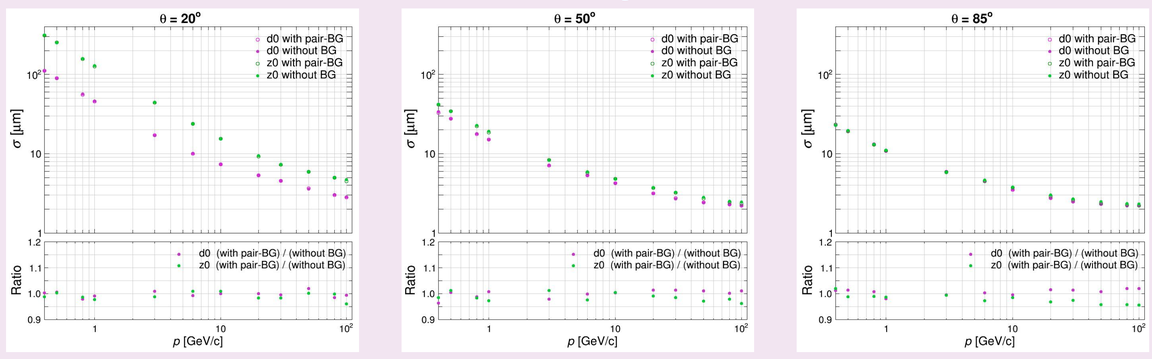

Figure 2,3,4 : d_0 and z_0 resolutions with and without **pair production** background, and their ratio "with / without" , vs. momentum at θ = 20°, 50°, 85°.

- At θ = 20° near-beam region, both d_0 and z_0 resolution ratios fluctuate around 1.0.
- In the 85° end-cap, transverse low-momentum e^+ e^- background supplements scarce Z-hits, driving the z_0 resolution ratio down to 0.95 at 10~100 GeV/c, while additional multiple scattering raises the d_0 resolution ratio by up to 2 %.
- Visible trend: Larger θ enhances z_0 resolution via extra hits but degrades d_0 resolution through multiple scattering.

Non-uniform Magnetic Field

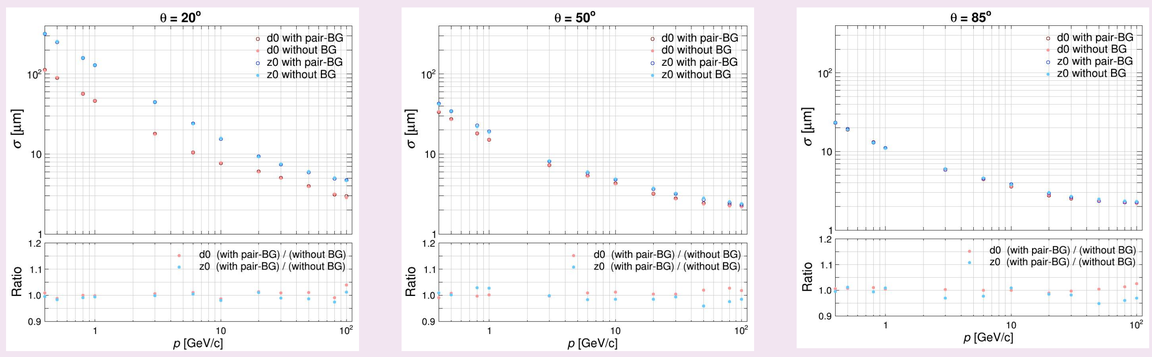

Figure 5,6,7 : d_0 and z_0 resolutions with and without **pair production** background, and their ratio "with / without" , vs. momentum at θ = 20°, 50°, 85°.

- With pair-production background, z_0 resolution improves by 0~5 % while d_0 resolution degrades by 0~4 %.
- Larger θ enhances z_0 resolution markedly.

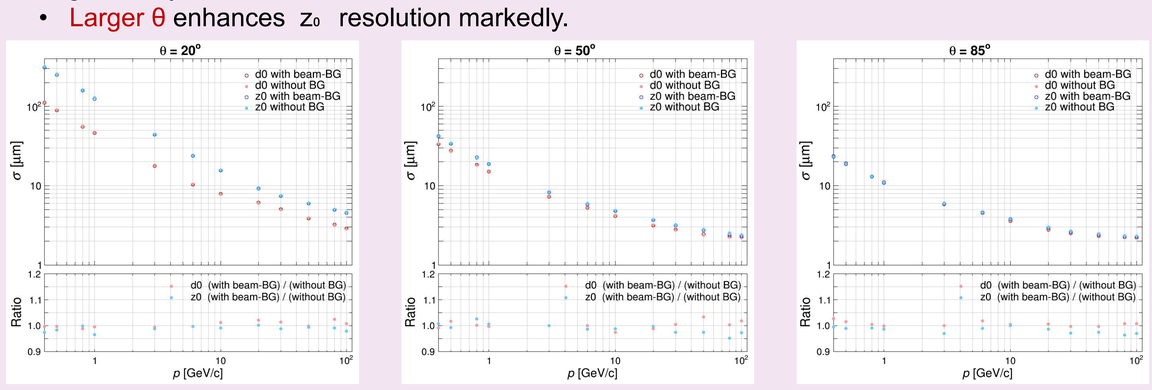

Figure 8,9,10 : d_0 and z_0 resolutions with and without **BIBs** , and their ratio "with / without" , vs. momentum at θ = 20°, 50°, 85°.

- After mixing BIBs, z_0 resolution is enhanced at all three angles, while d_0 resolution in the 85° end-cap shows only marginal improvement.

Inner Solenoid vs. Non-Uniform Field

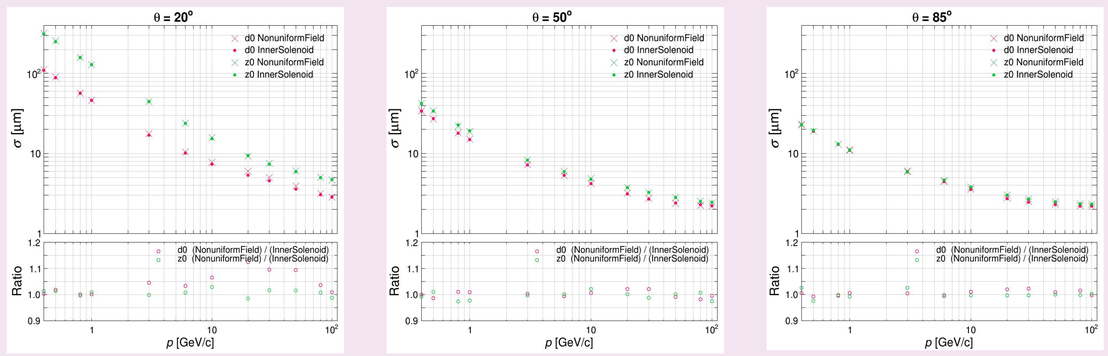

Figure 11,12,13 : d_0 and z_0 resolutions **without background** under Inner Solenoid vs. Non-Uniform Field, and their ratio (Non-Uniform / Inner Solenoid), vs. momentum at θ = 20°, 50°, 85°.

Compared with the Inner Solenoid , for the Non-Uniform Field :

- The fluctuation of z_0 resolution is controlled within ±2%.
- At θ = 20°, the degradation of d_0 resolution even exceeds 10%.
- The current helical track fitting is applicable to uniform magnetic fields, and future work will extend to track reconstruction under non-uniform magnetic fields.

Reference

[1] CEPC Technical Design Report -- Reference Detector
[2] CEPCSW, https://code.ihep.ac.cn/cepc/CEPCSW

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Geometric Optimization Simulation of the CEPC Vertex Detector

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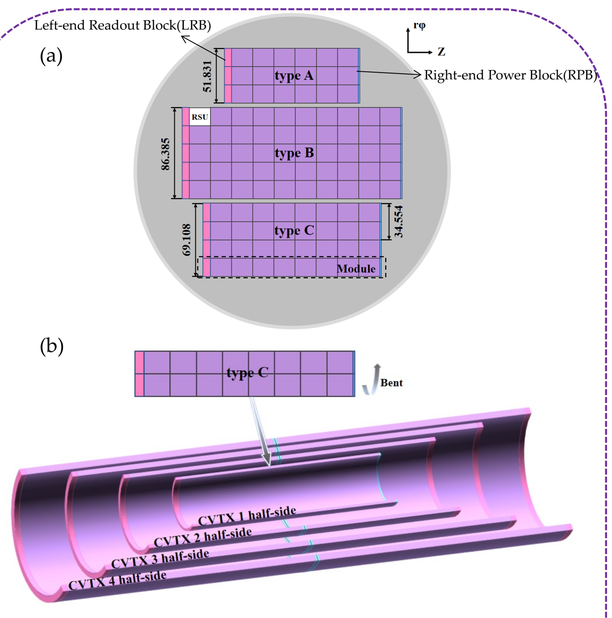
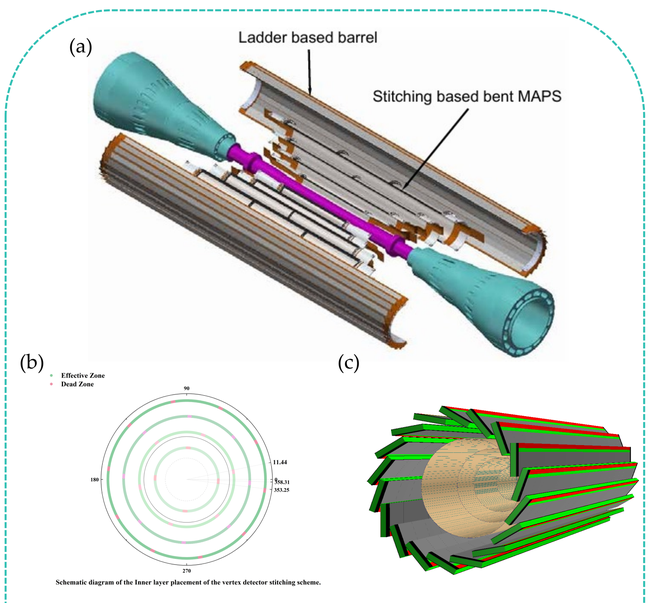
The identification of heavy-flavored quarks and τ leptons is an important physics goal of the Circular Electron Positron Collider (CEPC). The Vertex Detector (VTX) of the CEPC is capable of obtaining precise track parameters of charged particles in the vicinity of the Interaction Point to reconstruct the decay vertex of short-lived particles. The CEPC vertex detector currently employs an advanced sensor design scheme to achieve low mass and low dead zone objectives. The first four layers of the VTX are formed using stitched Monolithic Active Pixel Sensor (MAPS), while the fifth and sixth layers are constructed using traditional MAPS. This dual-sensor approach substantially reduces the detector mass to an average of 0.134% X_0 per layer while enabling stable construction for high-precision d_0 and z_0 resolution of 3.4 μm @ 10 GeV and 3.7 μm @ 10 GeV respectively. Additionally, we present the performance of the VTX under scenarios involving partial chip damage or even complete layer failure. Furthermore, considering potential deformations of the chips after the installation of the VTX, we have explored a feasible alignment solution.

Structure

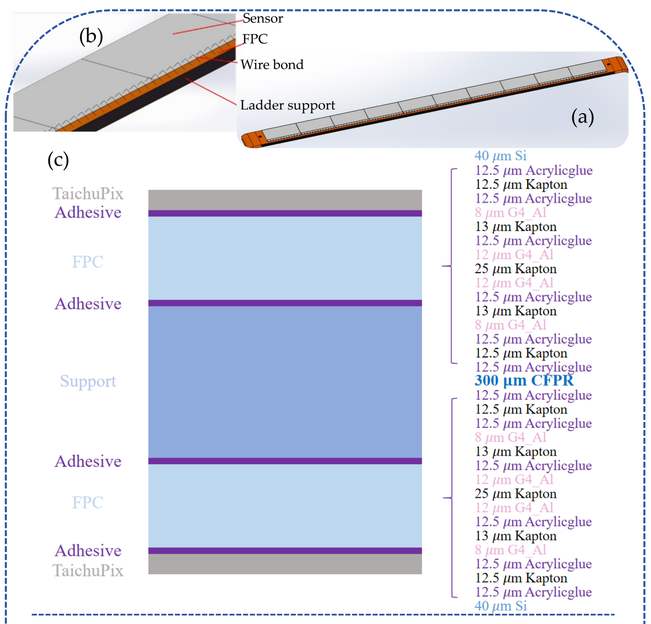


a) The arrangement of stitching frames on a 300 mm wafer. The shorted-dashed line area represents a module consisting of several RSUs, one LRB, and one RPB.
b) The Type C sensor is diced into a two-module sensor and bent along the ϕ-direction to form a semi-cylindrical structure for the Curved Vertex Layer (CVTX) 1.



Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

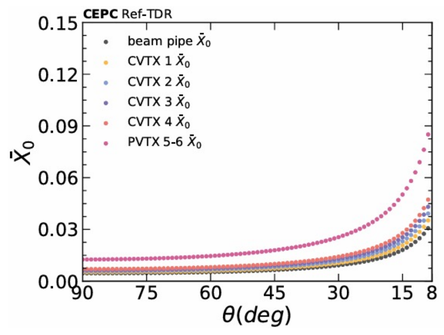
a) and c) Diagram of the VTX. The composition of the first four layers is shown on the left. The last two layers is shown on the right. Geometric configuration parameters seen in Table 1.
b) Considering the inefficient region in the ϕ direction of the stitched sensor, layers of the CVTX are rotated by an angle when mounted.



a) Full view of a ladder;
b) Close-up view of a ladder showing sensors wire bonded to the FPC.
c) Schematic transverse cross-section of a double-sided ladder structure used in layers 5 and 6, referred to as the Planar Vertex Layers (PVTXs) of the VTX.

Material budget

- Average material budget $\overline{X_0}$ as a function of the polar angle θ, averaged over the full azimuthal angle ϕ, for each layer of the VTX and the beam pipe, is shown in a stacked plot.
- As θ decreases (i.e., moving toward the forward region), the effective path length through the detector increases, leading to a higher accumulated material budget.

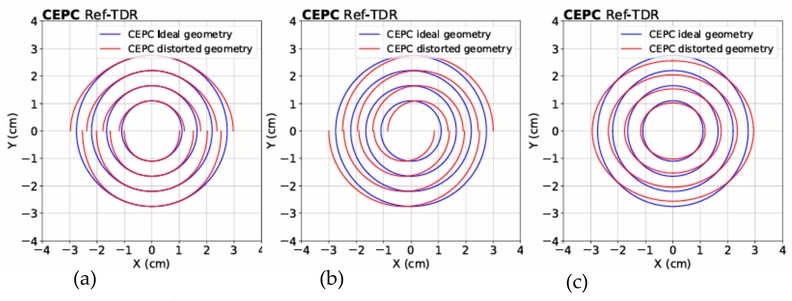


Unit	BeamPipe	CVTX 1	CVTX 2	CVTX 3	CVTX 4	PVTX 5-6
$\overline{X_0}(X_0)$	0.45%	~0.07%	~0.06%	~0.06%	~0.06%	~0.56%

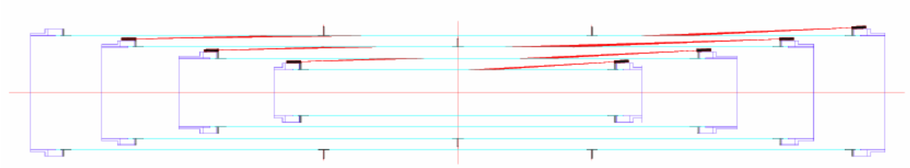
Alignment

- Illustration of hit positions in the transverse plane with ideal vertex geometry and three deformed geometry.

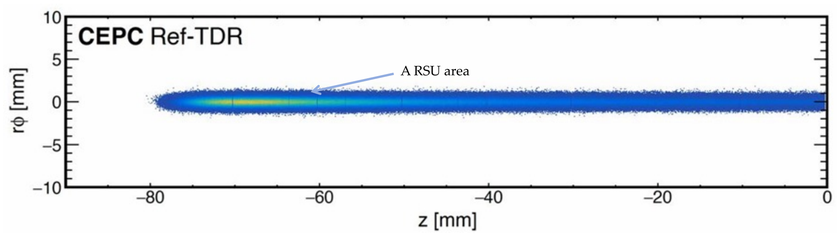
a) The radius of curvature differs from the nominal radius
b) Half-layer edge deviation from cylindrical shape
c) Compression causes cylindrical deformation into an ellipsoid



- A lased-based online alignment monitoring system



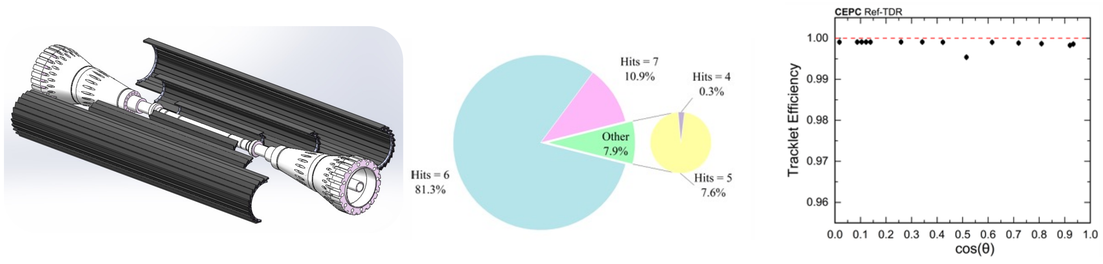
- Laser beam spot on the Layer 2 from (13 mm, 0, -85 mm) in cylindrical system.



- When simulating deformation by radially displacing the second layer outward by $d = 10$ μm, the observed difference corresponds to a distance of 50 μm, which is consistent with relationship $d/tan\theta \approx 57$μm.

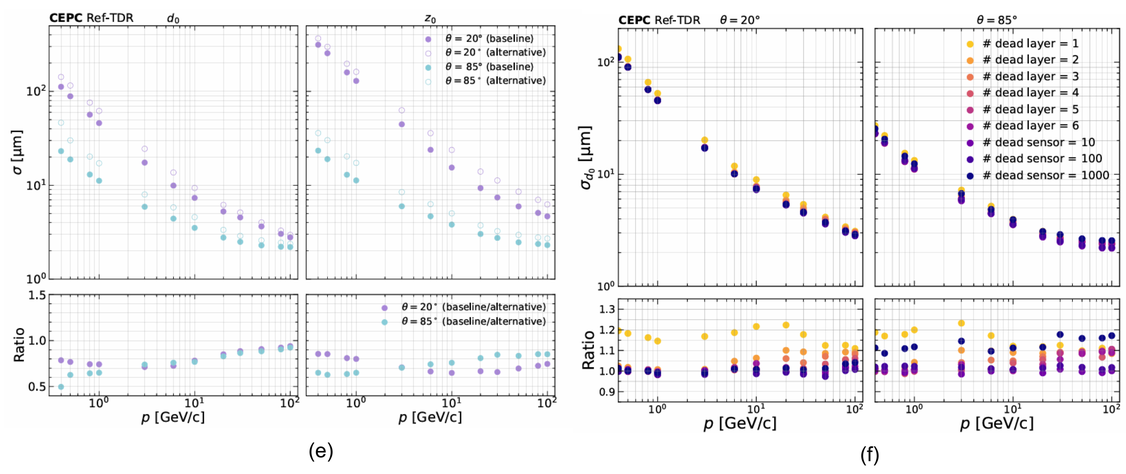
Table 1	CVTX/PVTX X	radius .mm	length .mm	arc length .mm	support thickness .μm
Baseline design	CVTX 1	11.1	161.4	69.1	45
	CVTX 2	16.6	242.2	103.7	32
	CVTX 3	22.1	323.0	138.2	31
	CVTX 4	27.6	403.8	172.8	29
	PVTX 5-6	39.5	682.0		300
Alternative design	PVTX 1-2	12.46	260.0		300
	PVTX 3-4	27.89	494.0		300
	PVTX 5-6	43.79	749.0		300

Performance



(a) (b) (c)

- Figure (a) illustrates an alternative VTX design featuring three layers of double-sided ladders with planar MAPS, with specific dimensions detailed in Table 1.
- Figure (b) shows the distribution of the number of hits per track for 10000 charged Geantinos with $p = 20$ GeV and $\theta = 20^{\circ}$.
- Figure (c) illustrates the tracklet efficiency of charged Geantino particles at 20 GeV energy, originating from the interaction point and traversing the VTX, as a function of the $cos(\theta)$.



(e) (f)

- Figure (e): $\sigma_{d_0} \approx$ 3.4 μm @ 10GeV and 85°, $\sigma_{z_0} \approx$ 3.7 μm @ 10GeV and 85°;
- The performance of baseline design is better than alternative design.
- Figure (f) demonstrates that as the number of damaged sensors increases and the damaged detector layer approaches the collision point, resolution deteriorates, with a maximum decline of 25% compared to the baseline.

Summary

- VTX achieves an extremely low material budget due to its use of stitched MAPS.
- The tracklet efficiency remains above 99.6% across all polar angles, demonstrating robust tracking performance.
- The VTX can achieve excellent resolution, and the damage to the innermost layer results in the largest performance drop, which does not exceed 25%.
- The laser calibration system can infer positional changes through the distribution of pixel IDs, and the expected precision is at the micrometer level.

Reference:

I. Chengdong Fu, "Silicon Tracking at CEPC ", The 2023 international workshop on the High EnergyCircular Electron-Positron Collider, 23-27 October 2023, Nanjing.
II. Hao Zeng, "Optimization of Silicon Pixel Vertex Detector for CEPC", Joint Workshop of the CEPC Physics, Software and New Detector Concept, 14-17 April 2021, Yangzhou.
III. http://code.ihep.ac.cn/cepc/CEPCSW