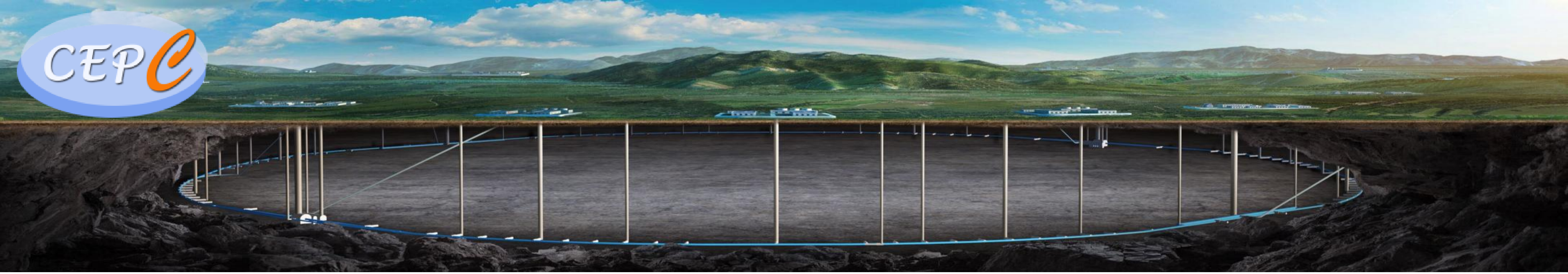


Status and plan of the TDAQ

Fei Li
On behalf of CEPC TDAQ Group

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Content

- Requirements
- Overall design
- Detailed design
- Cost
- Research team and R&D plan
- Summary

Physics Requirements

- Two upgrade for three operation phase
- Physical event rates
  - 87 Hz @ Higgs (240GeV)
  - 10.5 kHz @ Low lum. Z (91GeV)
  - 41.9 kHz @ High lum. Z
  - 56 Hz cosmic ray
  - Low energy events from $\gamma\gamma$ collision
    - 4/9 kHz @ Higgs/Low lum. Z
- The physical event rates are significantly lower than the bunch crossing rate.
  - <1/10000 @Higgs, <1/1000 @Z
- Keep physical events as more as possible
  - By a rough selection of the relevant objects (jet, e, muon, tau, γ, ...) and their combinations.
  - Required detailed signal feature extraction and simulation studies.

Table 12.1: CEPC baseline parameters

Operation phase	I			II	III
Run mode	ZH	Z	W	Z	$t\bar{t}$
SR power per beam (MW)	50	10	50		
Bunch number	446	3978	2162	13104	58
Bunch spacing (ns)	277 (x12)	69.2 (x3)	138.5 (x6)	23.1 (x1)	2700.0 (x117)
Train gap (%)	63	17	10	9	53
Bunch crossing rate(MHz)	1.33	12	6.5	39.4	0.17
Luminosity per IP (10^{34}cm^{-2}s-1)	8.3	26	26.7	95.2	0.8
Run time (years)	10	1	1	2	5
Event yields [2 IPs]	4.3x10^6	2.9x10^{11}	2.1x10^8	2.0x10^{12}	6x10^5

Table 12.2: Expected event rate at the ZH mode for 50 MW

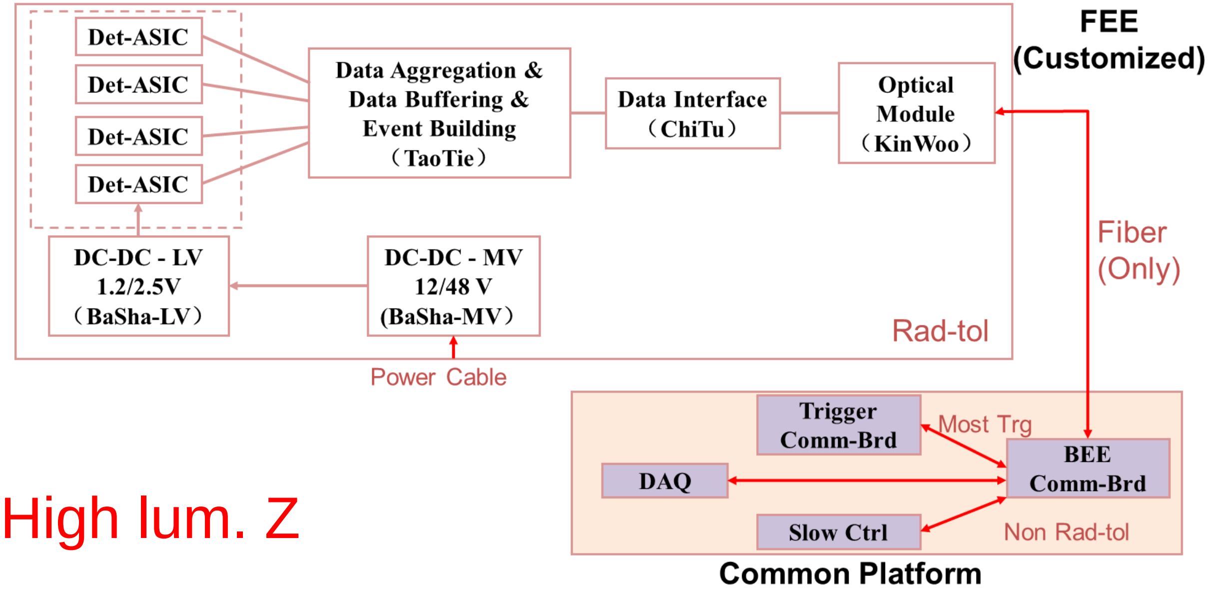
Processes	Cross section (fb)	Event rate (Hz)
ZH	203.66	0.017
Two Fermions background (exclude Bhabha)	6.4×10^4	5.3
Four Fermions background	1.9×10^4	1.6
Bhabha	1.0×10^6	80

Table 12.3: Expected event rate at the Z mode for 10 MW

Processes	Cross section (fb)	Event rate (Hz)
qq	31×10^6	7970
$\mu\mu$	1.5×10^6	400
$\tau\tau$	1.5×10^6	396
Bhabha	6.6×10^6	1714

Detector and Electronics Requirements

- Trigger, read out and reconstruction window of sub detectors
  - TPC: max draft time 34 us
    - Pileup: 123 BX/event @Higgs, 492 BX/event @Low lum. Z, 1472 BX/event @High lum. Z
    - Too slow, need special readout and trigger treatment for pileup tracks as Alice
  - ECAL & HCAL: trigger uncertainty <25 ns, readout window 100 ns
    - Pileup: 2 BX/event @Low lum. Z, 5 BX/event @High lum. Z
  - Silicon/Muon: trigger uncertainty <10 ns, readout window 10+25 = 35 ns
- Electronics framework schema
  - System clock: 43.3 MHz
  - Transmit full data from Front-End to Back-End Electronics
    - Through fiber asynchronous link
  - Trigger receive primitives from BEE
  - Trigger send L1A back to BEE
- Trigger latency
  - Millisecond data buffer @ BEE DDR
  - Possible need send trigger to FEE for High lum. Z
    - Within 6-10 us latency



Estimation of Background and TDAQ Rate

- Beam background data rate
- Readout event size
  - 1 Mbytes
  - 2 Mbytes @High Lum. Z
- Storage event size
  - 500 Kbytes
  - 1 Mbytes @High Lum. Z
- Storage event rate of TDAQ
  - Assume store physics and background events as 1:1
  - 1 kHz @ Higgs
  - 20 kHz @ Low Lum. Z
  - 80 kHz @ High Lum. Z

	Vertex	Pix(ITKB)	Strip (ITKE)	OTK	TPC	ECAL	HCAL	Muon
Channels per chip	512*1024	512*128	1024	128	128	8~16		
Data Width /hit	32bit	42bit	32bit	48bit	48bit	48bit		
Avg Data Vol @Higgs	474.2 Gbps	400.5 Gbps		277 Gbps	34.4 Gbps	710 Gbps	1348.8 Gbps	24.1 Gbps
Sum	3.2 Tbps = 400 GB/s, 300 Kbytes/BX @Higgs							
Avg Data Vol @Low lum. Z	2440 Gbps	3480 Gbps		420 Gbps	55.8 Gbps	910 Gbps	3650 Gbps	5 Gbps
Sum	10.96 Tbps = 1.37 TB/s , 115 Kbytes/BX @ Low lum. Z							
Sum	10.96x3 Tbps = 4.11 TB/s , 115 Kbytes/BX @ High lum. Z							

Background event size with readout window:

300 + 34.4/1.33/8*122 = 695 Kbytes @ Higgs

115 + 55.8/12/8*491 + (910+3650)/12/8*1 = 448 Kbytes @ Low lum. Z

115 + 55.8*3/39.4/8*1471 + (910+3650)*3/39.4/8*4 = 1070 Kbytes @ High lum. Z

Need compress event size especially for TPC with track reconstruction.

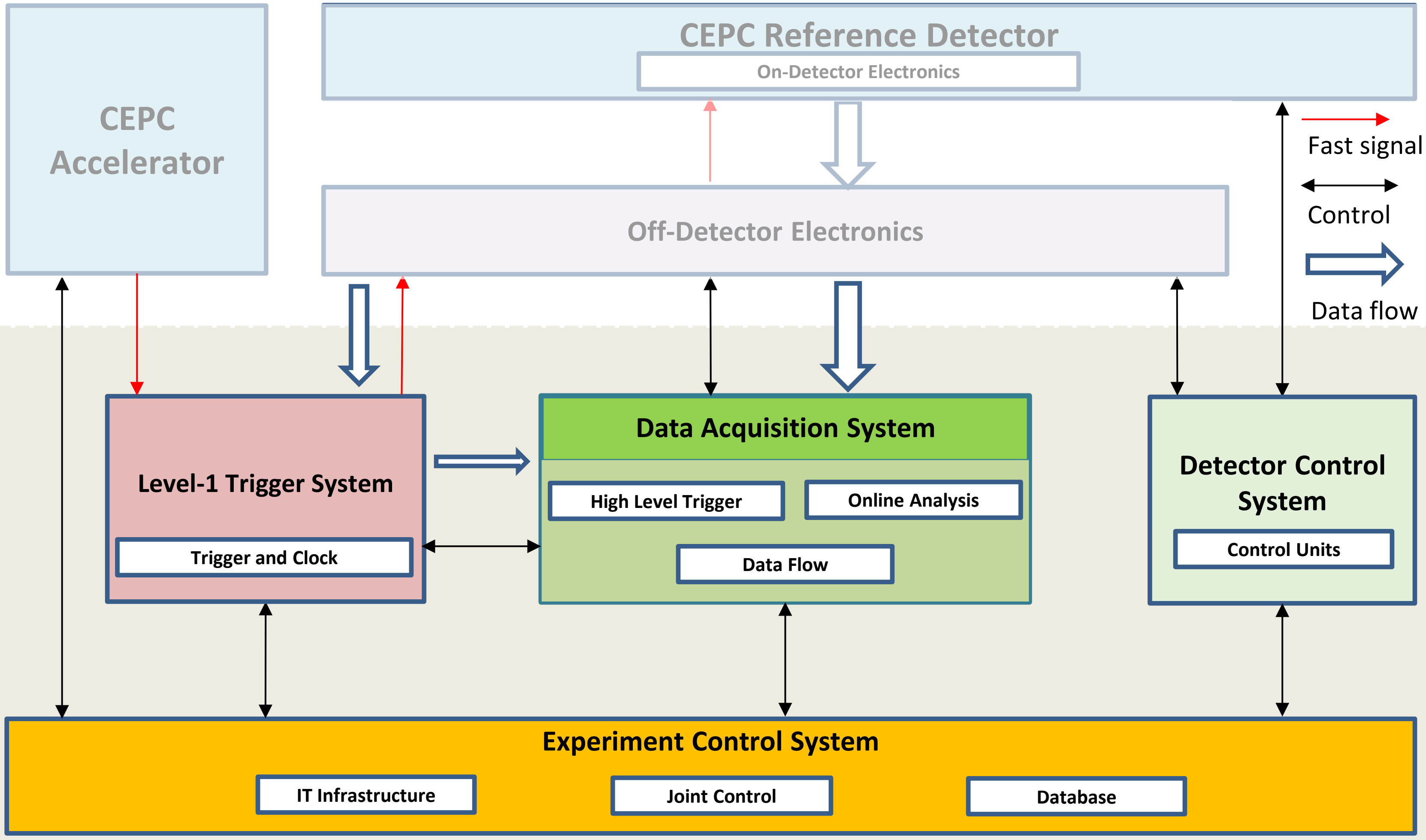
Preliminary estimation of input and output rate of TDAQ

Main Technical Challenges

- High efficiency algorithms in trigger and background compression
  - 1.3 MHz->O(1k)Hz @Higgs
  - 12 MHz->O(20k)Hz @Low lum. Z
  - 39.4 MHz->O(80k)Hz @High lum. Z
  - Trigger solution for lower-energy events, e.g. from $\gamma\gamma$ collisions
- Trigger primitive synchronization control with asynchronous data readout from subdetector electronics
  - Manage data disorder due to data transfer queuing and delay
  - Align sub-detector data of each bunch crossing within limited time and resource

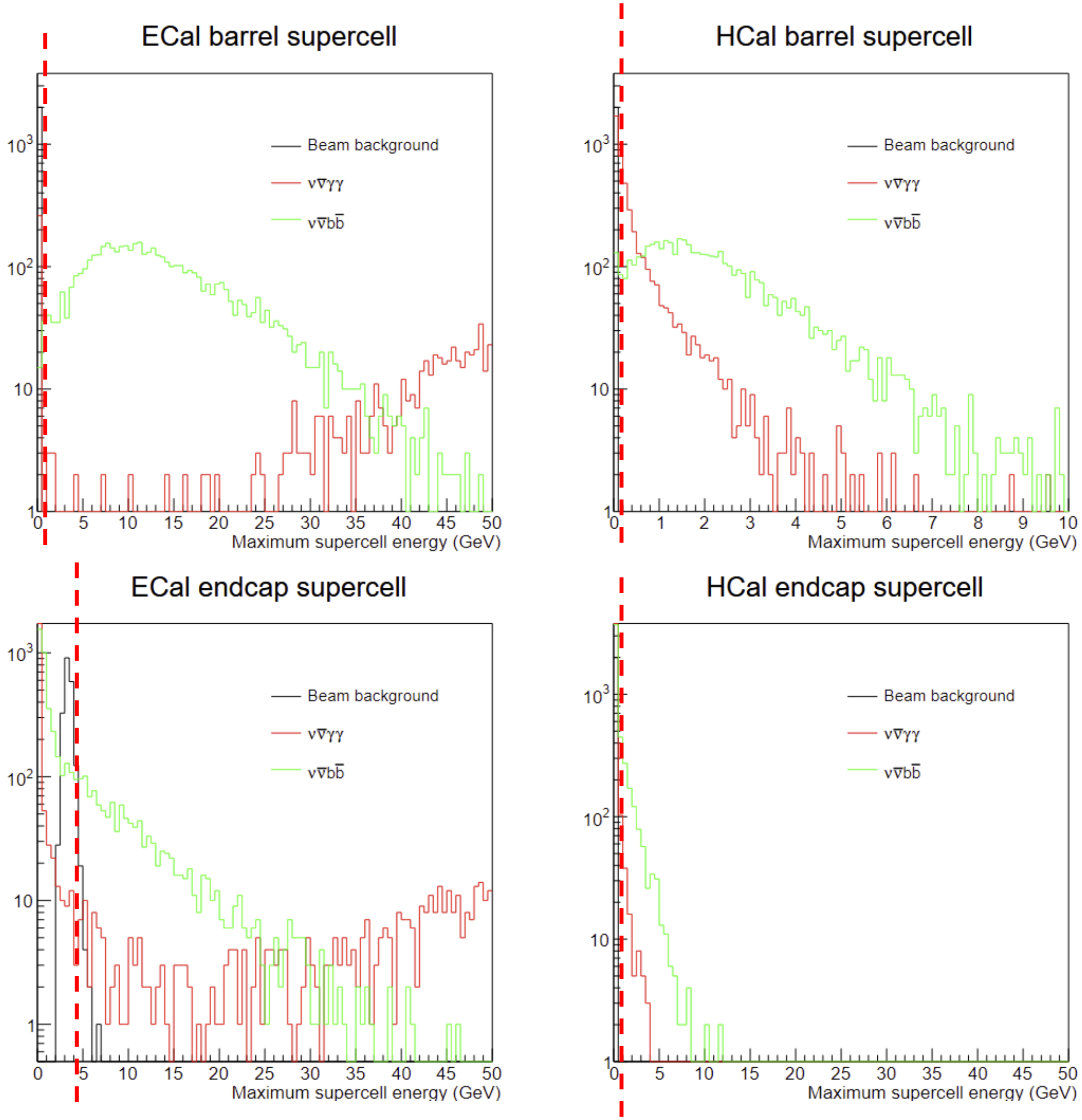
Overall Design of TDAQ and Online

- TDAQ schema
  - Level 1 hardware trigger(L1) + high level trigger(HLT)
  - Single type of common hardware trigger board
  - Ethernet readout
  - Joint control and monitoring
  - Unified online service and IT infrastructure



Overall structure of TDAQ and Online system

Preliminary Trigger Simulation



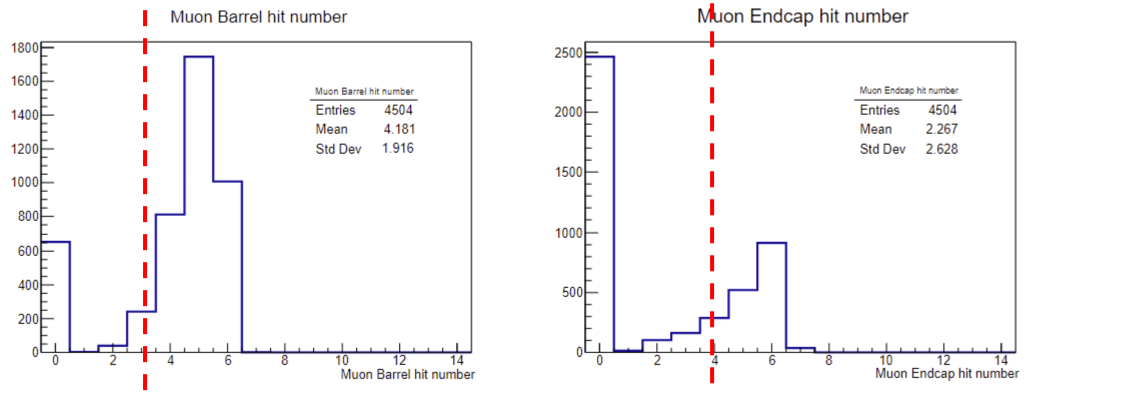


Figure 12.15: Number of hits for the $e^+e^- \to Z(\nu\bar{\nu})H(\mu^+\mu^-)$ process on the Muon Barrel(left) and Endcap(right) detector.

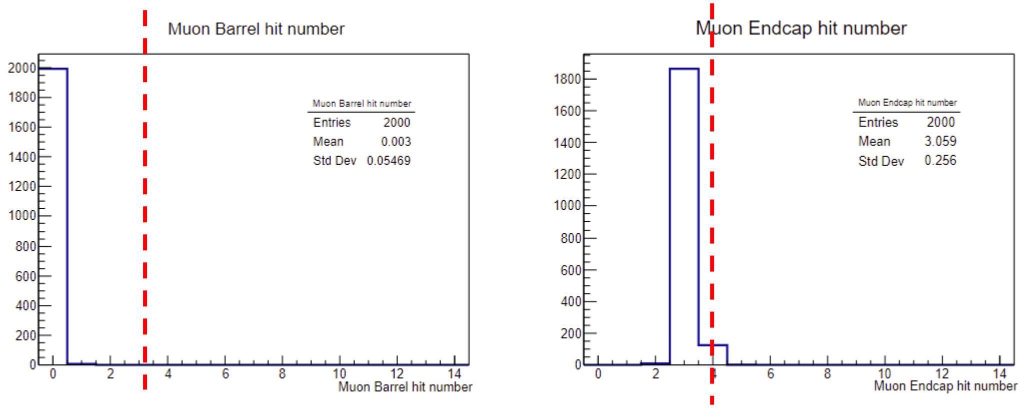


Figure 12.16: Number of hits for the beam background on the Muon Barrel(left) and Endcap(right) detector.

Trigger and background simulation with supercell energy and muon hits

Preliminary L1 Trigger Algorithm

- Good trigger efficiency
  - Physical and background event samples are separated and independent.
  - L1 trigger condition @ZH
    - ECAL Barrel supercell > 0.5 GeV
    - HCAL Barrel supercell > 0.1 GeV
    - ECAL Endcap supercell > 4.8 GeV
    - HCAL Endcap supercell > 0.1 GeV
    - Track tag Number of Muon track > 0
  - L1 trigger condition @Low lum. Z
    - ECAL Barrel supercell >0.25 GeV
    - HCAL Barrel supercell >0.1 GeV
    - ECAL Endcap supercell >2.7 GeV
    - HCAL Endcap supercell >0.2 GeV
    - Track tag Number of Muon track > 0
- Good veto efficiency with current beam background simulation
  - Need more event samples and noise studies

Table 12.8: Calorimeter threshold efficiency at the ZH mode for 50 MW

Process	Efficiency	Process	Efficiency	Background	Veto rate
$Z(\nu\bar{\nu})H(b\bar{b})$	$> 99\%$	$Z(\nu\bar{\nu})H(W^+W^-)$	$> 99\%$	Beam background	$> 99\%$
$Z(\nu\bar{\nu})H(\tau^+\tau^-)$	$> 99\%$	$Z(\nu\bar{\nu})H(ZZ)$	$> 99\%$		
$Z(\nu\bar{\nu})H(\gamma\gamma)$	$> 99\%$	$Z(\nu\bar{\nu})H(\gamma Z)$	$> 99\%$		
$Z(\nu\bar{\nu})H(\mu^+\mu^-)$	$\sim 99\%$	Bhabha	$> 99\%$		
$\mu^+\mu^-$	$\sim 98\%$				

Table 12.9: Calorimeter threshold efficiency at the Z mode for 10 MW

Process	Efficiency	Process	Efficiency	Background	Veto rate
$q\bar{q}$	$> 99\%$	$\mu^+\mu^-$	94%	Beam background	$> 99\%$
Bhabha	$> 99\%$	$\tau^+\tau^-$	$\sim 99\%$		

Table 12.10: Muon trigger efficiency at the ZH mode for 50 MW

Process	Efficiency	Process	Efficiency	Background	Veto rate
$Z(\nu\bar{\nu})H(\mu^+\mu^-)$	96.4%	$\mu^+\mu^-$	86.8%	Beam background	$> 99\%$

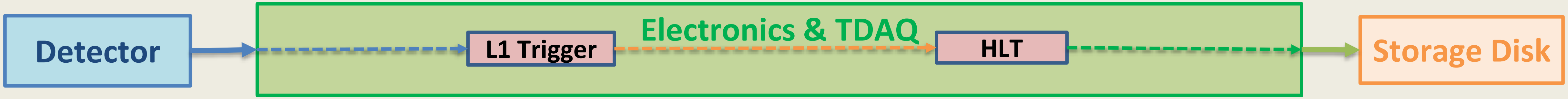
Table 12.11: Muon trigger efficiency at the Z mode for 10 MW

Process	Efficiency	Background	Veto rate
$\mu^+\mu^-$	95.3%	Beam background	$> 99\%$

Table 12.13: Expected L1 trigger rate at the ZH mode for 50 MW and at the Z mode for 10 MW. Samples are simulated with CEPCSW tdr24.12.0. Electronic noise is not added. Pile up event is not added. Beam background is using version 241227.

ZH mode	Efficiency	Z mode	Efficiency
ZH	>99%	$q\bar{q}$	>99%
Two Fermions processes (exclude Bhabha)	>99%	$\mu^+\mu^-$	>99%
Four Fermions processes	>95%	$\tau^+\tau^-$	>99%
Bhabha	>99%	Bhabha	>99%
Background	**Veto rate**	**Background**	**Veto rate**
Beam background	>99%	Beam background	>99%

Estimation of Trigger and Data Rate



Bunch crossing rate(Beam background data rate)	L1 trigger rate(Readout data rate)	HLT rate(Storage rate)
Higgs mode: 1.3 MHz (400 GB/s)	13k Hz(13 GB/s)	1k Hz(0.5 GB/s)
Low Lum. Z: 12 MHz (1.37 TB/s)	120k Hz(120 GB/s)	20k Hz(10 GB/s)
High Lum. Z: 39.4 MHz (4.1 TB/s)	400k Hz(800 GB/s)	40k Hz(80 GB/s)

- L1 trigger rate
  - Expect reduce beam background to 1%
  - 120 kHz @ Low Lum. Z
- HLT rate
  - Expect reduce beam background to 0.1%
  - 20 kHz @ Low Lum. Z
- DAQ data rate
  - Read out data rate: 120 GB/s @ Low Lum. Z
  - 1 year storage(3600h): 6.48 PB@ Higgs, 129.6 PB@ Low L. Z

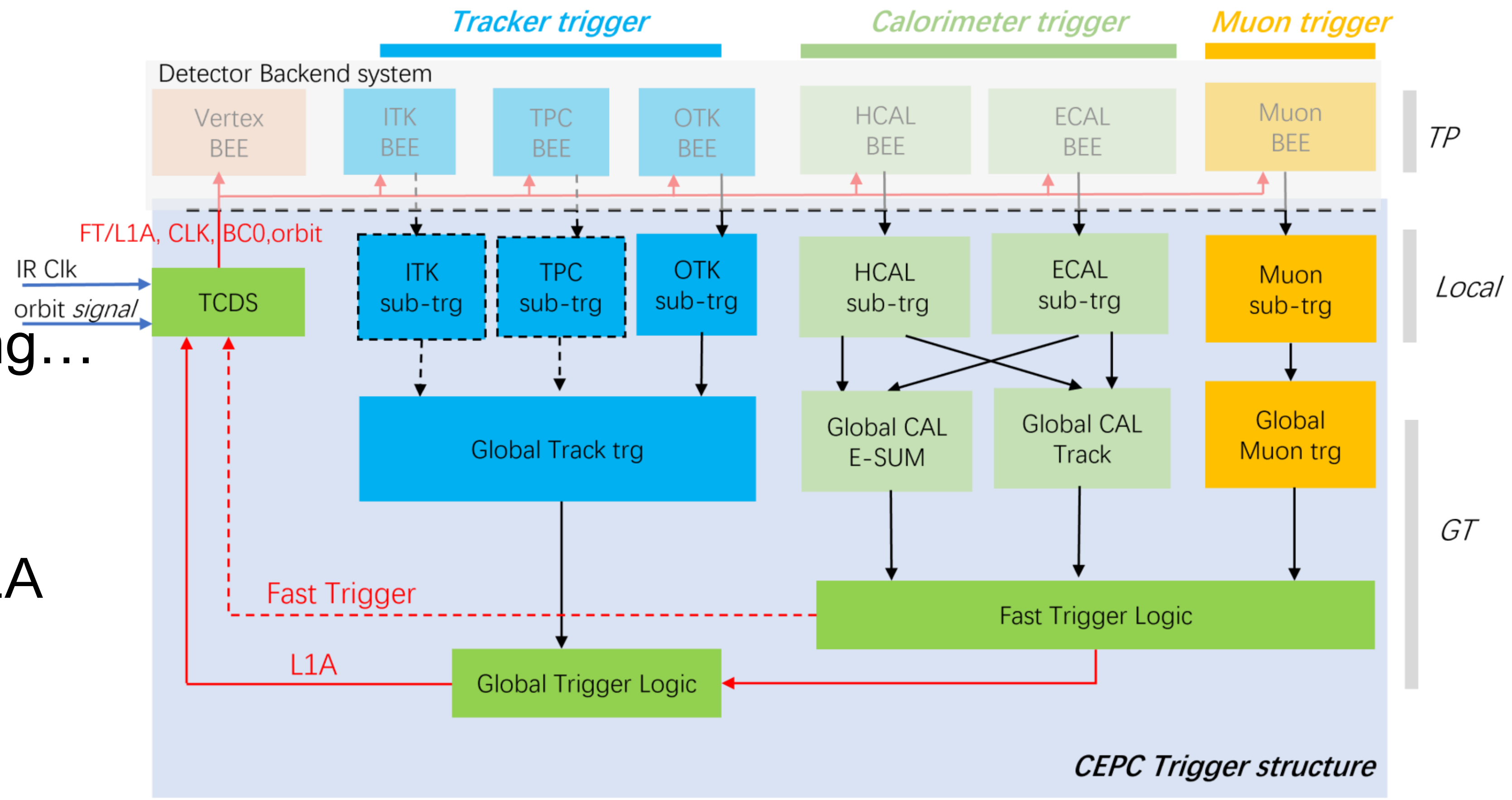
Simplify L1 trigger design to do more @HLT

Table 12.5: Trigger rate estimation table for different run conditions.

Condition	Higgs	Z(10MW)	W	Z(50MW)	$t\bar{t}$
Luminosity ($10^{34}/cm^2/s$)	8.3	26	26.7	95.2	0.8
Bunch space (ns)	277	69.3	253.8	23.1	4523.1
Bunch crossing rate (MHz)	1.34	12	6.5	39.4	0.18
Background data size/bunch crossing (kbyte)	300	162	300	162	300
Background data rate (Tbyte/s)	0.4	1.94	1.95	7.7	0.048
Physical event rate (kHz)	0.087	10.5	0.1	41.9	0.002
L1 triger rate (kHz)	13	120	65	400	2
Background event size (kbyte)	695	448	-	1070	-
Readout event size (kbyte)	1000	1000	1000	2000	1000
DAQ readout rate (Gbyte/s)	13	120	65	800	2
High level trigger rate (kHz)	1	20	6	80	1
Storage event size (kbyte)	500	500	500	1000	500
DAQ storage rate (Gbyte/s)	0.5	10	3	80	0.5

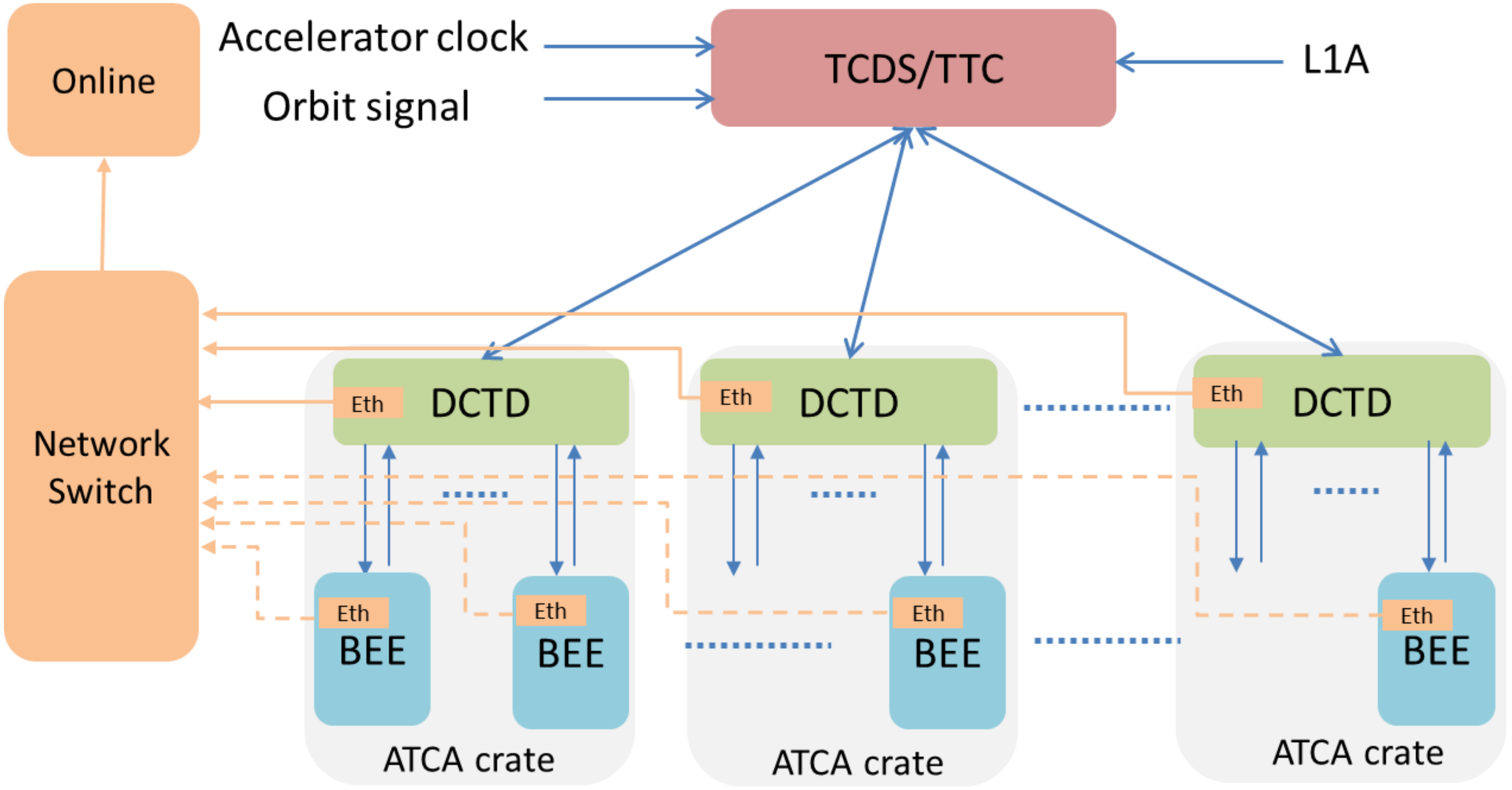
Design of Hardware Trigger Structure

- Trigger primitive(TP)
  - Extracted @ BEE
- Local detector trigger
  - Sub energy and tracking…
- Global trigger
  - E-sum and tracking
  - Fast trigger(FT) and L1A generation on demand
- TCDS (Trigger Clock Distribution System)
  - Distribute clock and fast control signals to BEE
- Which detectors participate in trigger needs to be studied



Design of TCDS and Readout Interface

- TCDS/TTC
  - Clock, BC0, Trigger, orbit start signal distribution
  - Full, ERR signal feed back to TCDS/TTC and mask or stop L1A
- Data readout from BEE
  - Read out directly or concentrated by DCTD board
  - Depending on the size of the data volume
  - Ethernet speed: 10 Gbps

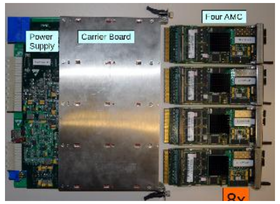


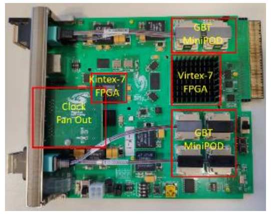
- TCDS-Trigger Clock Distribution System
- TTC- Trigger, Timing and Control
- DCTD-Data Concentrator and Timing Distribution
- BEE-Backend board Electronic

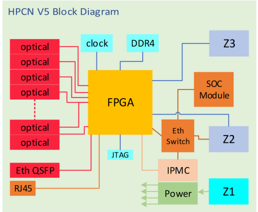
R&D Efforts and Results

- xTCA for physics standard(ATCA/MTCA extension)
  - IHEP is a founding and development lab together with DESY, FNAL and SLAC
- Developed a series of xTCA boards
  - Started the design of an ATCA common trigger board for CEPC





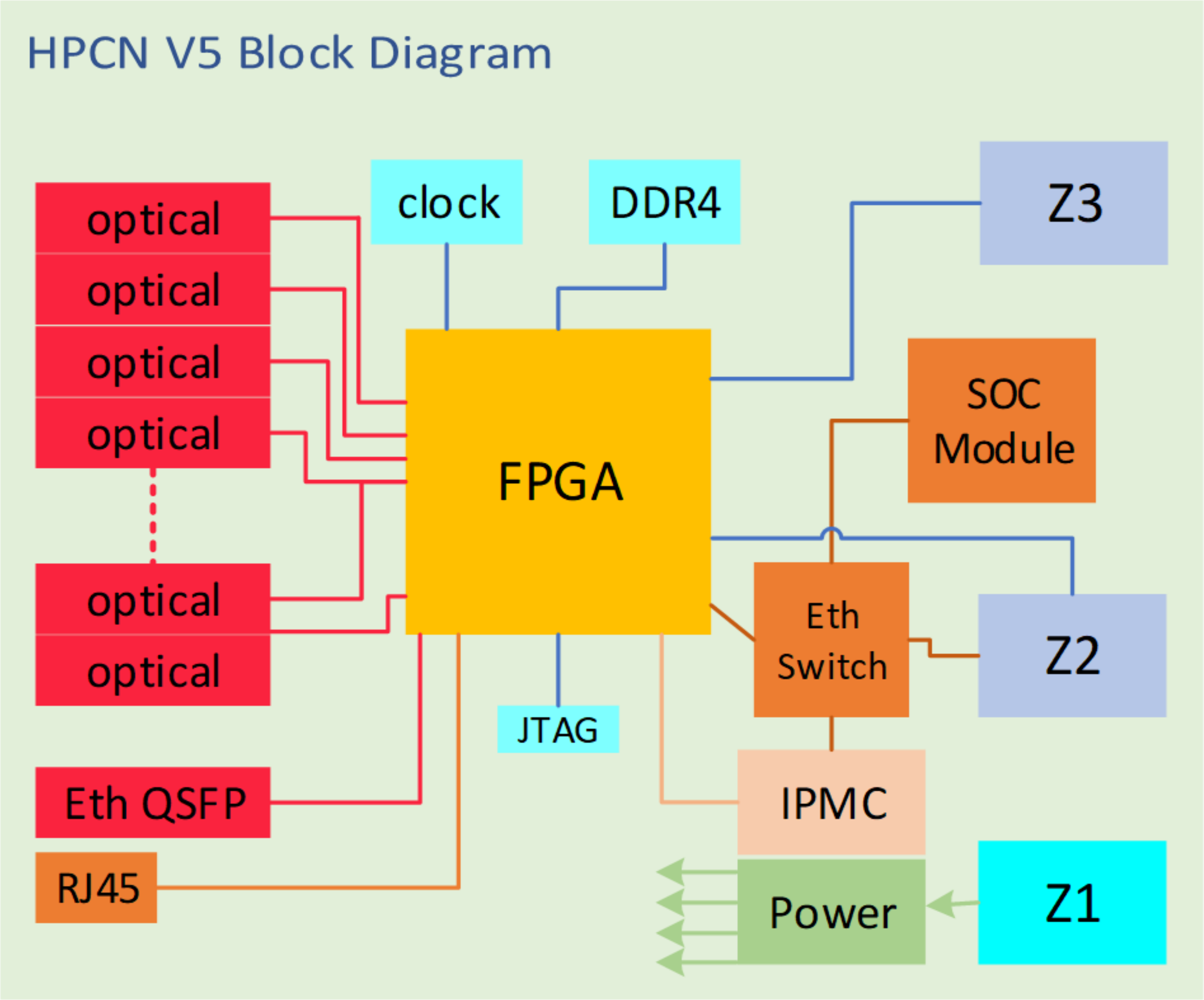


Version	HPCN V1	HPCN V2	HPCN V3	CPPF	HPCN V4	Serenity	HPCN V5
Line rate	3Gbps	3Gbps	6Gbps	10Gbps	10Gbps	25Gbps	>=16Gbps
Num. of ch	8 ch	8ch	8-16ch	36ch	48ch	124ch	36-80 ch
Buffer	2GB	2GB	4GB	—	48GB	—	TBD
Ethernet	1GbE			1/10GbE	10GbE	100GbE	40-100GbE
Aplication	PANDA		Belle II/PXD	CMS Phase-I	CMS Phase-II		CEPC R&D
Time	2006-		2009-	2013-	2017-		2024-

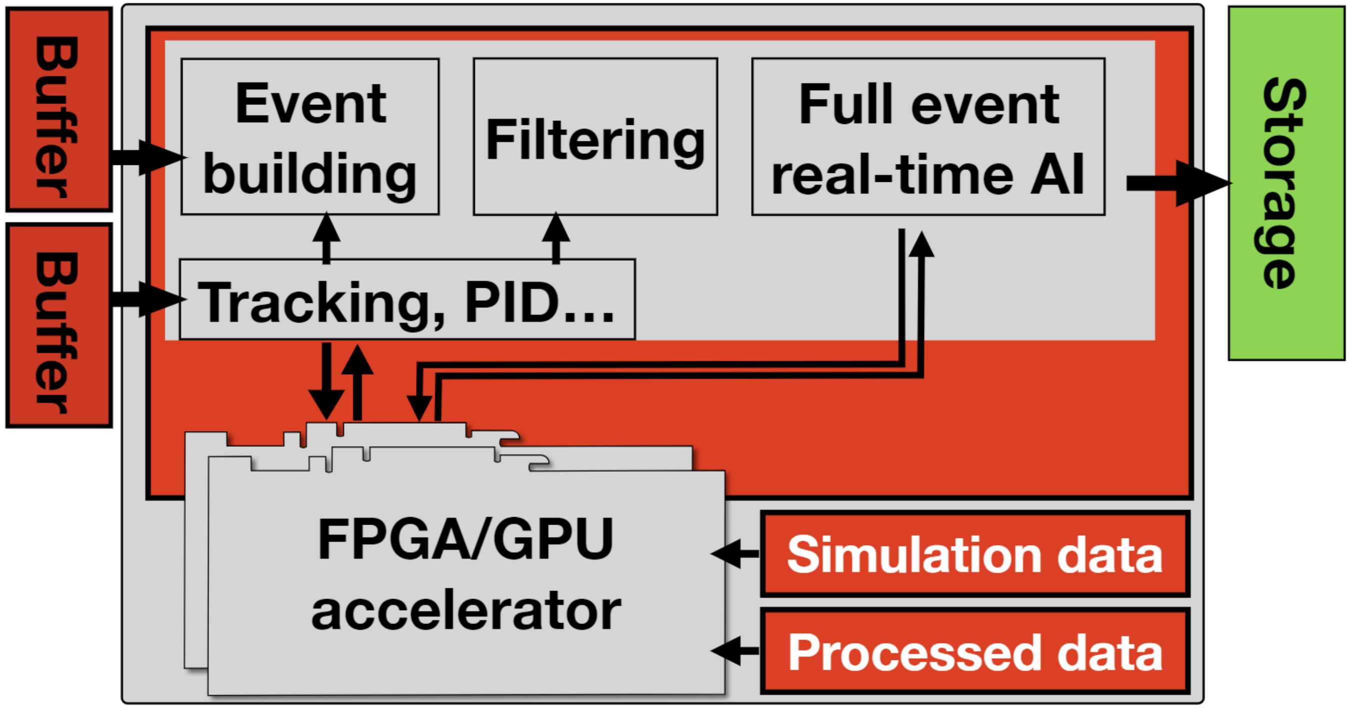
Design of the Common Trigger Board

- Common Trigger board function list
  - ATCA standard
  - Virtex-7 FPGA
  - Optical channel: 10-25 Gbps/ch
  - Channel number:36-80 channels
  - Optical Ethernet port: 40-100GbE
  - DDR4 for mass data buffering
  - SoC module for board management
  - IPMC module for Power management



High Level Trigger

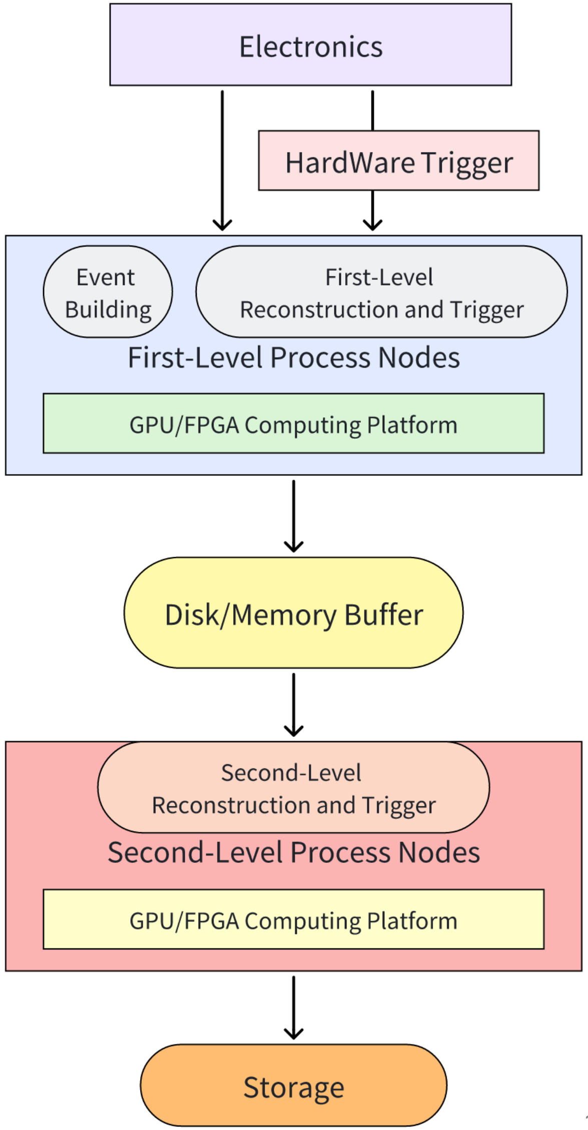
- Event selection and data reduction
  - Distributed Computing
  - Advanced Software Tools
  - Real-Time Constraints
  - Detector Limitations
- Implement feature
  - Feature Extraction
  - Track Seed Finding
  - Lightweight PID
  - Calibration
  - Physics Skim



- Need R&D a compatible and high-efficiency interface software for offline algorithm.
- CPU cores estimation
  - 1 s@Higgs for background event tracking reconstruction
  - max 6.5 s/ZH event
  - Fast reconstruction: 0.3 s/core/event, 13 kHz*0.3s=3.9 k cores, 120 kHz*0.3 s=36 k cores
- Accelerated by GPUs and FPGAs in addition to CPUs

Architecture Design of DAQ

- Compatible design with or without HW trigger
- Full COTS(commercial-off-the-shelf) hardware
- R&D RADAR software framework
  - Heterogeneous computing
  - GPU/FPGA acceleration for HLT
- R&D disk or memory buffer architecture
  - Decouple computing environments
  - Easy to run complete offline algorithm at online



DAQ Readout Interface and Protocol

- Readout data rate
  - 13 Gbytes/s@Higgs
  - 120 Gbytes/s@Low lum. Z
- Interface
  - 10 Gbps Ethernet
  - 10 Gbps per BEE or create
- Protocol
  - TCP default
  - RDMA over FPGA
    - Under R&D
- Readout full TPC data
  - 34 us window
  - Overlap among many events
  - Assemble data by time fragment according to bunch crossing id

Table 12.14: Requirements for Detector Readout. L1 trigger rate is 1%.

Detector	Avg Background Data Vol after L1-Trigger (Gbps) @Higgs	Avg Background Data Vol after L1-Trigger (Gbps) @Low Lumi Z	BEE Number	Data rate per BEE (Gbps) @Low Lumi Z
Vertex	4.7	24.4	6	4.07
TPC	34.4	55.8	32	1.74
ITK	4.0	34.8	245	0.142
OTK_B	2.5	3.8	34	0.084
OTK_E	0.3	0.4	45	0.009
ECAL_B	4.6	12.8	60	0.213
ECAL_E	1.9	5.4	34	0.159
HCAL_B	8.1	56.8	346	0.164
HCAL_E	5.4	16.2	192	0.084
Muon	0.2	0.05	24	0.002
Trigger	-	-	150	-
Sum	66.1	210.45	1168	

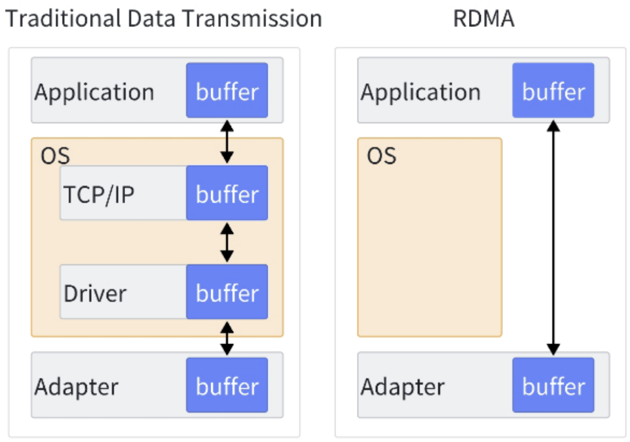


Figure 12.24: Traditional Data Transmission vs RDMA.

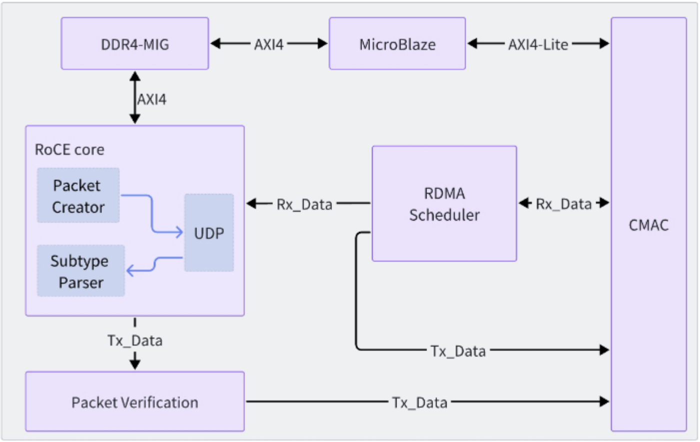
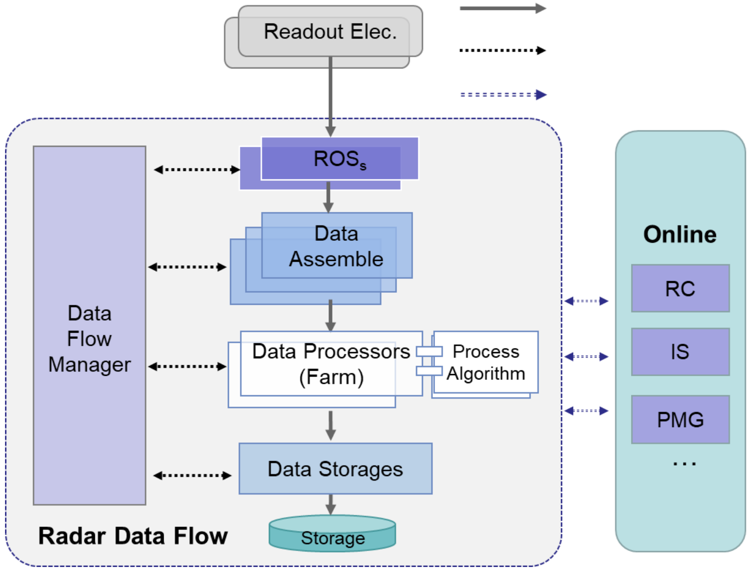


Figure 12.25: RDMA Firmware Design.

Streaming Software Framework – RADAR

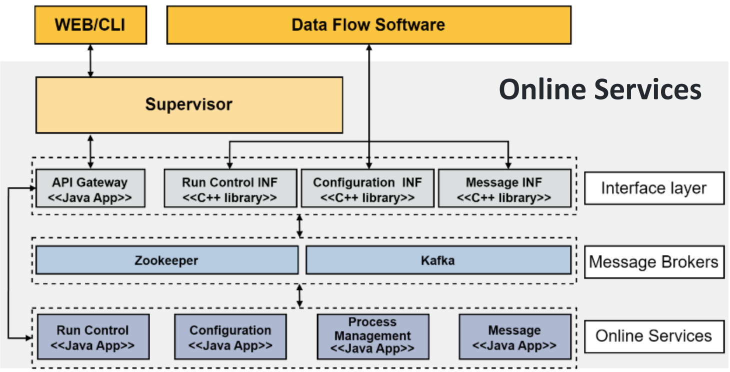
heteRogeneous Architecture of Data Acquisition and pRocessing

- **V1:** deployed in LHAASO (3.5 GB/s data rate), *software trigger mode*
- **V2:** upgraded for JUNO (40 GB/s data rate), *mixed trigger mode*
  - Containerized running
- **V3: CEPC-oriented** (~ TB/s data rate) , under development



- **General-purpose distributed framework**
- **Lightweight structure**
- **Plug-in modules design**
- **Microservices architecture**

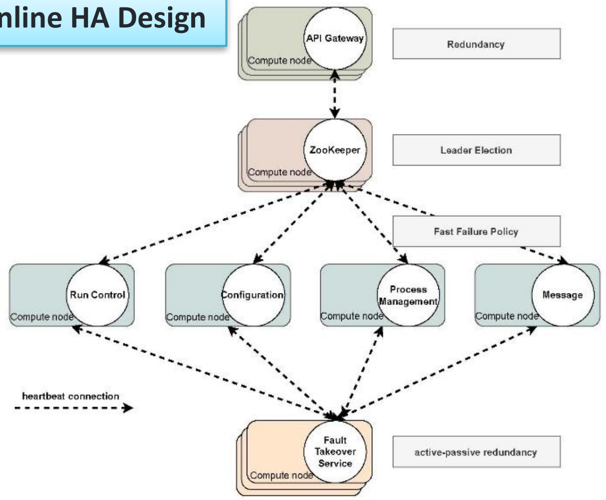
- **Motivation:**
  – High-throughput data acquisition and processing
- **Current Status:**
  – Over a decade of work led to significant progress, validated through experiments
- **Recent Focus:**
  – **Heterogeneous online processing platforms with GPU**
  – **Real-time data processing acceleration solutions**
- **Expansion:**
  – **Application across various domains** (DAQ, triggering, control, etc.)
  – **Integration of AI technologies** (ML, NLP, expert systems, etc.)



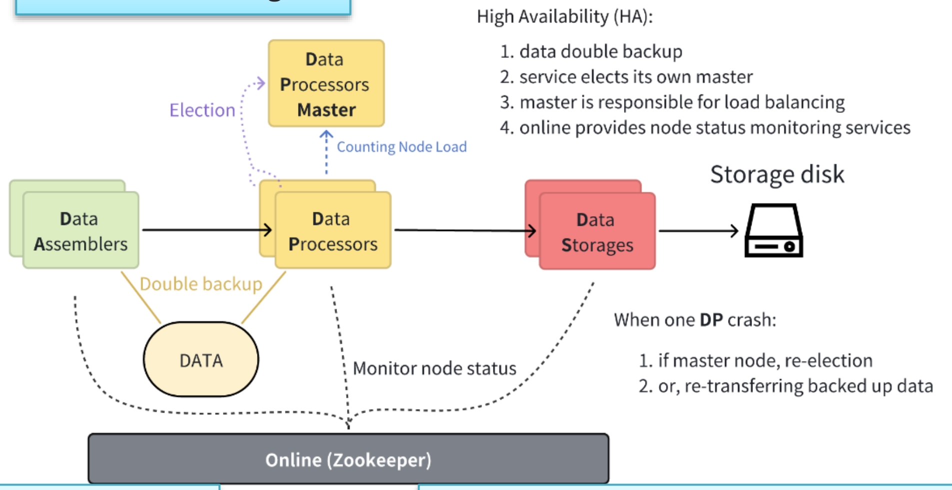
Start to develop new version with GPU acceleration.

R&D Efforts and Results

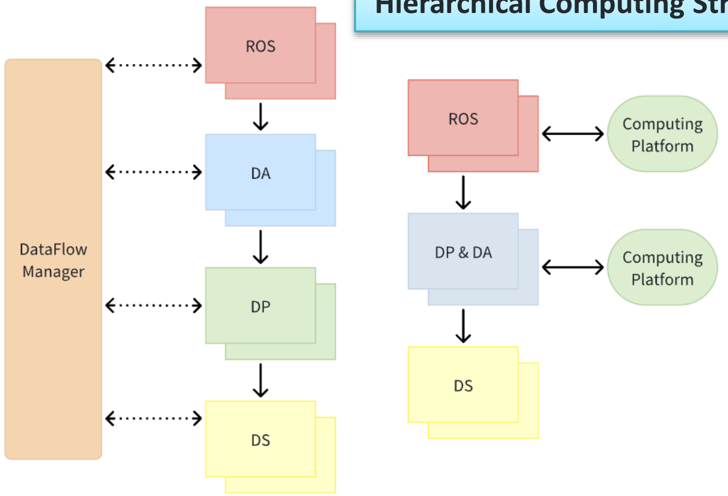
Online HA Design



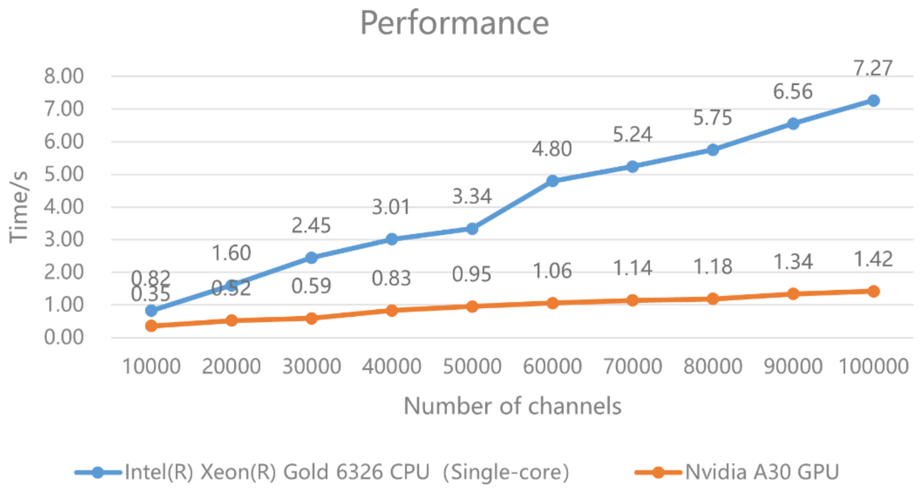
Dataflow HA Design



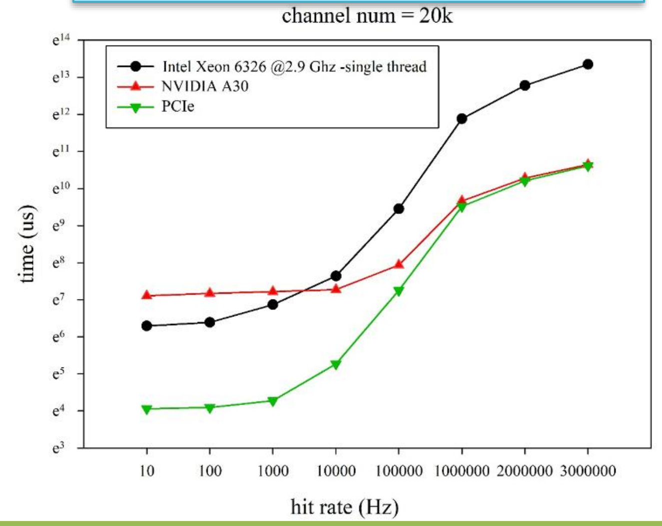
Hierarchical Computing Strategy



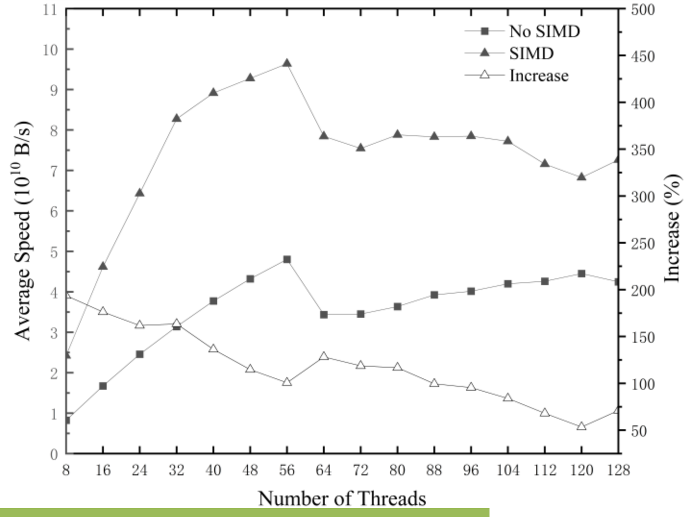
GPU based online waveform reconstruction in JUNO



GPU based nHit trigger algorithm study

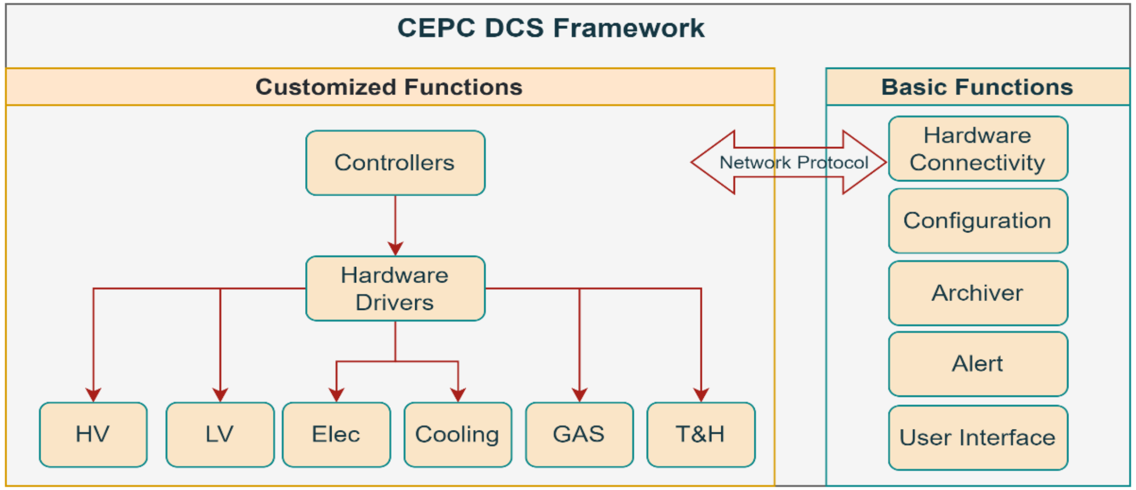


SIMD based CPU processing acceleration



Acceleration progress for waveform reconstruction and software trigger algorithm.

Design of Detector Control System



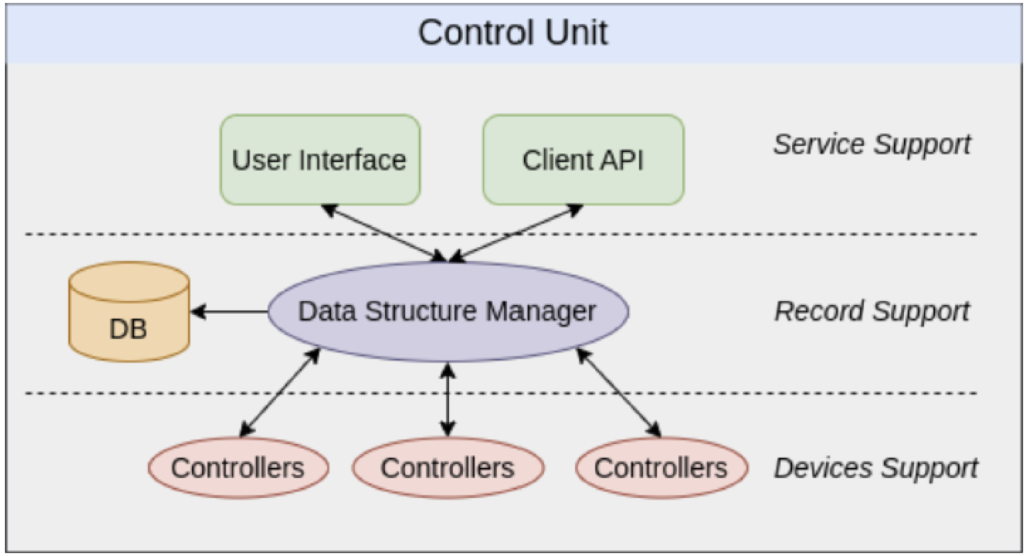


Figure 12.29: Software architecture of the control unit.

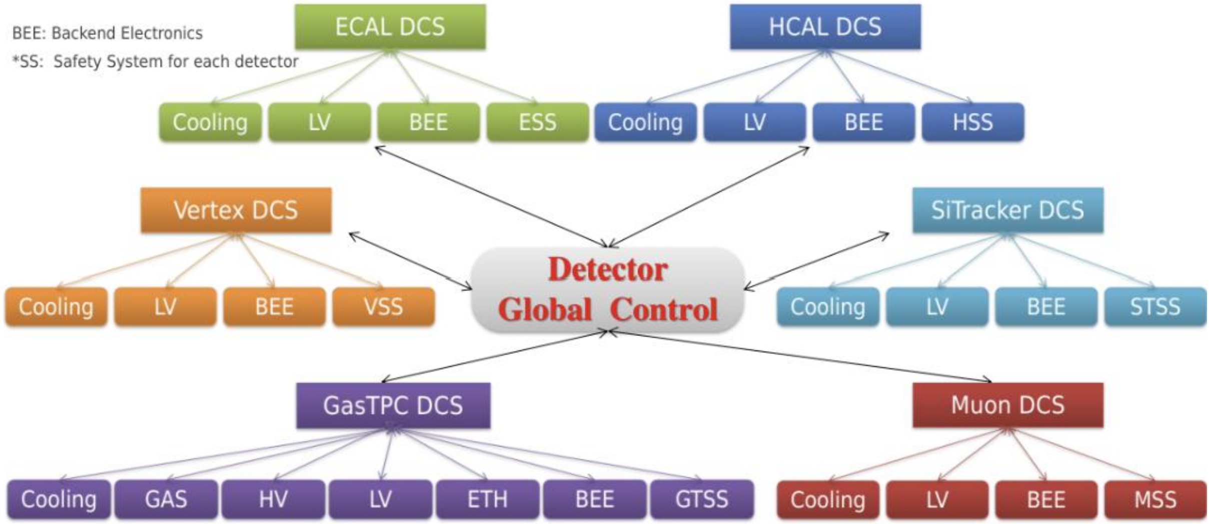


Figure 12.28: CEPC DCS requirments overview.

Table 12.16: Summary of detector control and monitoring quantities

Equipment	Channel Number	Control and Monitoring Items	Total Count
AC-DC Crate	55	Switch, voltage, current, etc., about 6 items	330
AD-DC Channel	550	Switch, voltage, current, etc., about 6 items	3300
FEE Power Crate	390	Switch, voltage, current, etc., about 6 items	2340
FEE Power Channel	17946	Switch, voltage, current, etc., about 6 items	~110,000
FEE Board	27984	Voltage, current, temperature, etc., about 10 items	~280,000
BEE Crate	180	Switch, fan, status, etc., about 10 items	1800
BEE Board	1749	Switch, voltage, current, etc., about 6 items	~10,000
Trigger Crate	21	Switch, fan, status, etc., about 10 items	210
Trigger Board	161	Switch, fan, status, etc., about 10 items	1610
HV Crate	77	Switch, fan, status, etc., about 10 items	770
HV Channel	8896	Voltage, current, status, etc., about 6 items	~55,000
Cooling, Gas	12 cooling + 1 gas	Flow control, humidity, etc., about 30 items	390
Environmental	~30	Temperature, humidity	60
Total			~470,000

Designed framework based on existed solutions

Design of Experiment Control System

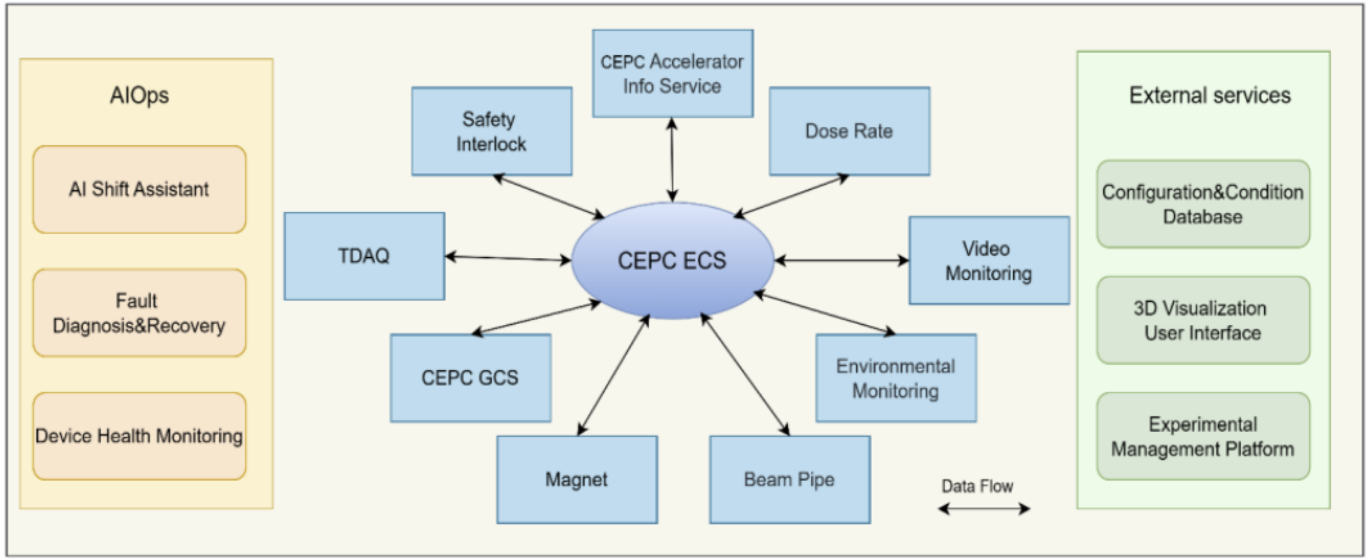


Figure 12.30: CEPC ECS structural overview.

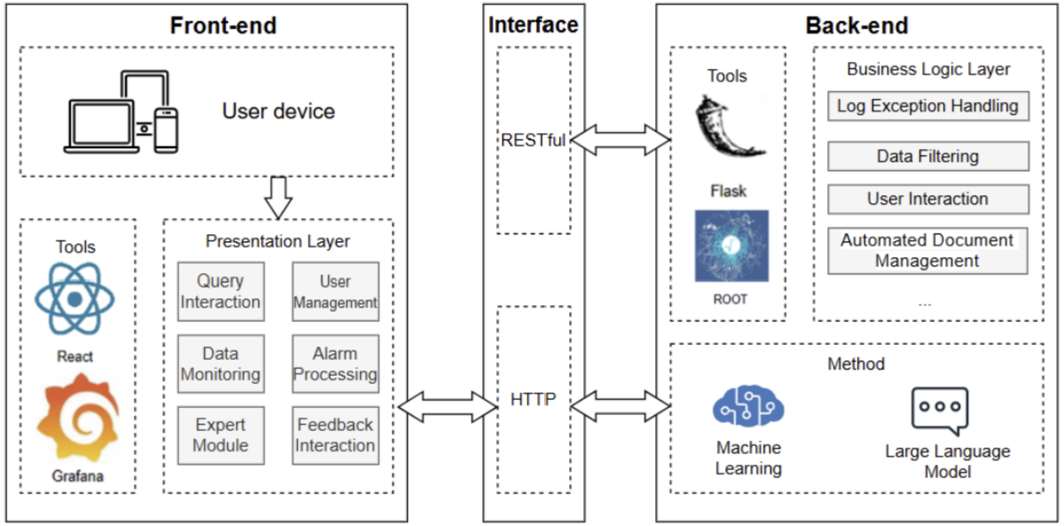


Figure 12.31: ECS software architecture.

- R&D progress from JUNO and BESIII
  - 3D Visualization Monitoring
  - AI shift assistant based on LLM+RAG (TAOChat)
  - ROOT-based Online Visualization System
- Unified control and monitoring for all system
  - TDAQ, DCS, electronics, detectors and accelerator

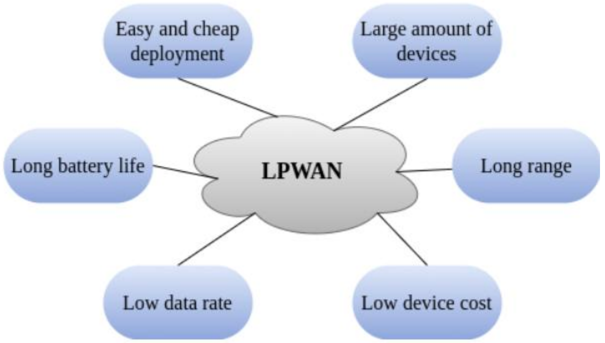


Figure 12.33: LPWAN technical advantages.

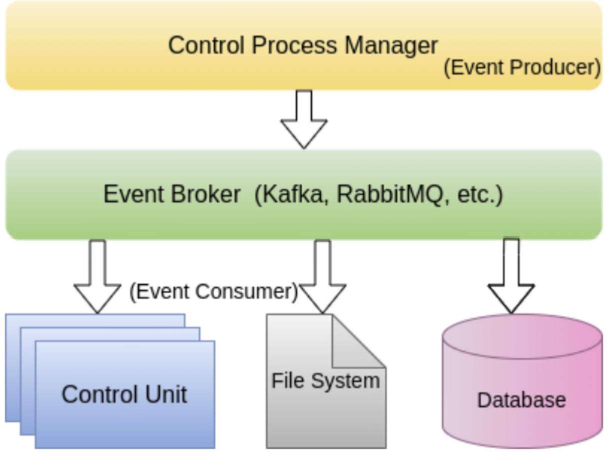


Figure 12.32: Central control software architecture.

Primary Cost Estimation(140M RMB)

Subsystem	Equipment Type	Unit	Unit Price (10k RMB)	Quantity	Total Price (10k RMB)
L1 Trigger	Trigger Electronics Board	Piece	15	150	2250
	Trigger and Clock Distribution Board	Piece	10	20	200
	ATCA Electronics Chassis	Unit	18	20	360
	Firmware Development	Man-month	2	192	384
HLT	Compute Server (32-core, 2.9GHz CPU)	Unit	5	1125	5625
	GPU/DCU Server	Unit	50		
	Core Switch (32x100GbE)	Unit	15	40	600
	Algorithm Software Development	Man-month	2	192	384
DAQ	Compute Server (32-core, 2.9GHz CPU)	Unit	5	128	640
	Storage Server (32-core, 2.9GHz CPU / 1PB SAS)	Unit	50	10	500
	Management Server (32-core, 2.9GHz CPU / 10TB SSD)	Unit	15	10	150
	Readout Switch (48x10GbE + 6x100GbE)	Unit	5	30	150
	Core Switch (32x100GbE)	Unit	15	8	120
	Software Development	Man-month	2	240	480

DCS&ECS	Online Computer Room and Control Room	Set	500	1	500
	Control and Management Server (32-core, 2.9GHz CPU / 10TB SSD)	Unit	15	20	300
	Storage and Database Server (32-core, 2.9GHz CPU / 0.5PB SAS)	Unit	30	6	180
	GPU/DCU Server (8-card DCU / 0.5PB SAS)	Unit	50	6	300
	Control and Management Switch (48x1GbE + 4x10GbE)	Unit	0.5	50	25
	Control Aggregation Switch (48x10GbE + 6x100GbE)	Unit	5	6	30
	Management Core Switch (32x100GbE)	Unit	15	4	60
	Other Control Hardware and Integration (PLC/Sensors)	Set	500	1	500
	Control Software Development	Man-month	2	144	288
SUM					14026

- Firmware and software development costs are based on the engineering needs of students, post-docs, and temporary employees, excluding regular staff.

Research Team

- 15 staff of IHEP TDAQ group
- Trigger (4/5)
  - Zhenan Liu, Jingzhou Zhao
  - Boping Che, Sheng Dong
- DAQ (4/6)
  - Fei Li, Hongyu Zhang
  - Xiaolu Ji, Minhao Gu
- DCS/ECS (1/4)
  - Si Ma
- IHEP Students(5/20)
  - 2 PhD and 3 master
- New member planned
  - 1 staff
  - 2 postdoc

- Collaborators
  - Qidong Zhou (SDU)
  - Yi Liu (ZZU)
  - Junhao Yin(NKU)
  - Miroslav Saur(LZU)
  - 4 students planned
- Adviser
  - Wolfgang Kuehn (JLU, Giessen, Germany)
- We're looking for more collaborators

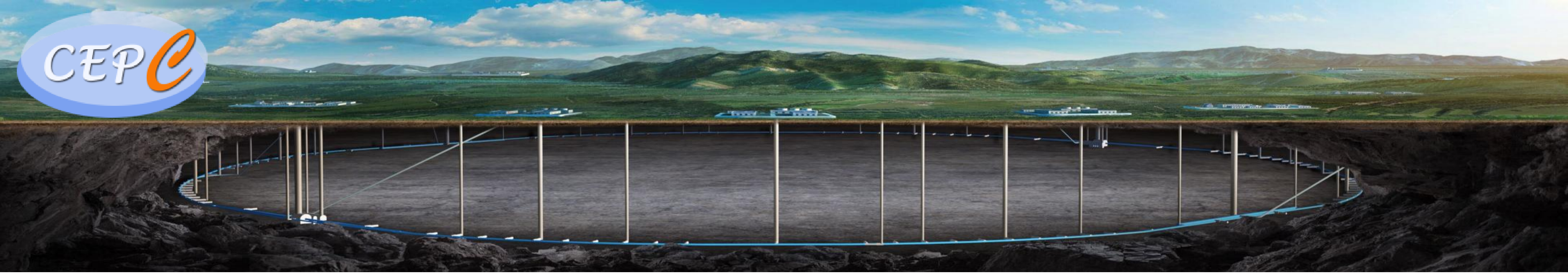
Gathering manpower for R&D, 9 staff and 5 students were involved from IHEP

Working plan

- TDR related
  - Further simulation and algorithm include low energy event from $\gamma\gamma$ collisions
  - Detailed hardware trigger and interface design
  - Finalize TDAQ and online design scheme
- R&D directions (in three years)
  - Trigger hardware, fast control and clock distribution
  - High throughput software framework(RADAR)
    - FPGA/GPU acceleration and heterogeneous computing
    - Memory-based distributed buffer
  - Detailed trigger simulation and algorithm study
  - ML/AI algorithm application study
    - Trigger/data compression/ AI operation and maintenance
  - ROCE/RDMA readout protocol and smart NIC

Summary

- Following update of sub detectors design and simulation
- Completed major technical design scheme of TDAQ
- No critical technology risk found
  – Challenges: efficient trigger algorithm and handling data at manageable hardware scale
- Primary cost estimation for phase I
  – Free resources can be shared to offline
  – Or the L1 trigger rate can be increased for more lower-energy and new physics events study @ Higgs mode
- More detailed R&D efforts needed to move forward

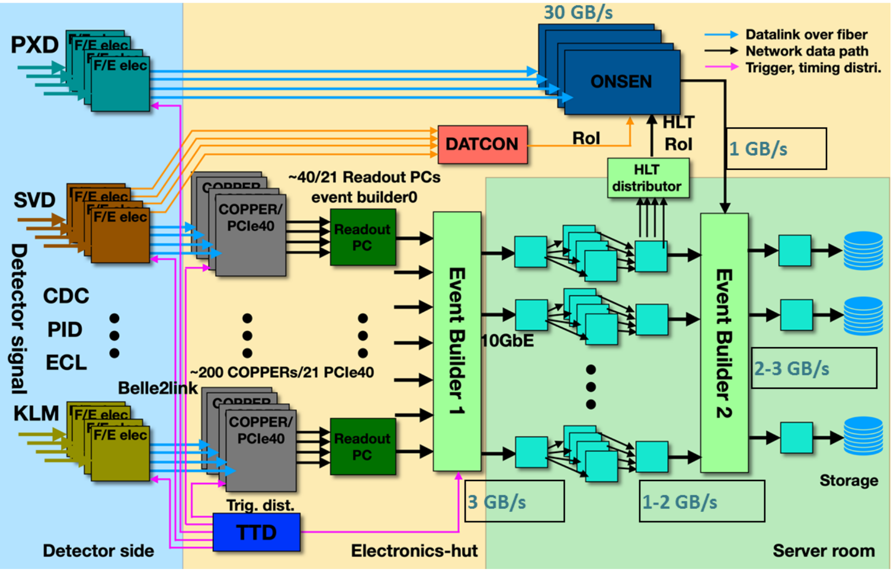


Thanks for your attention!

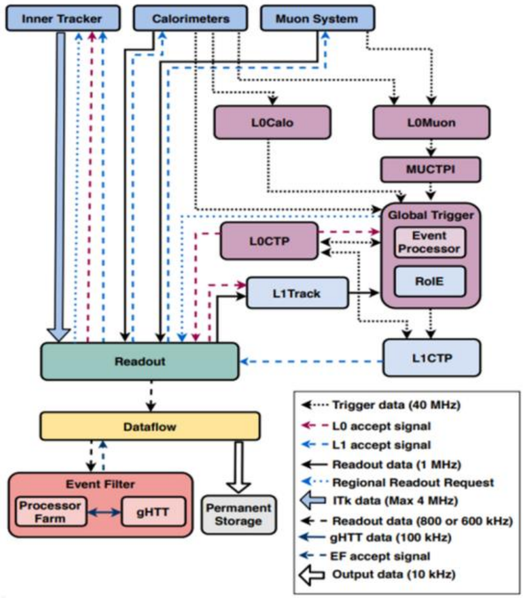
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Technology survey

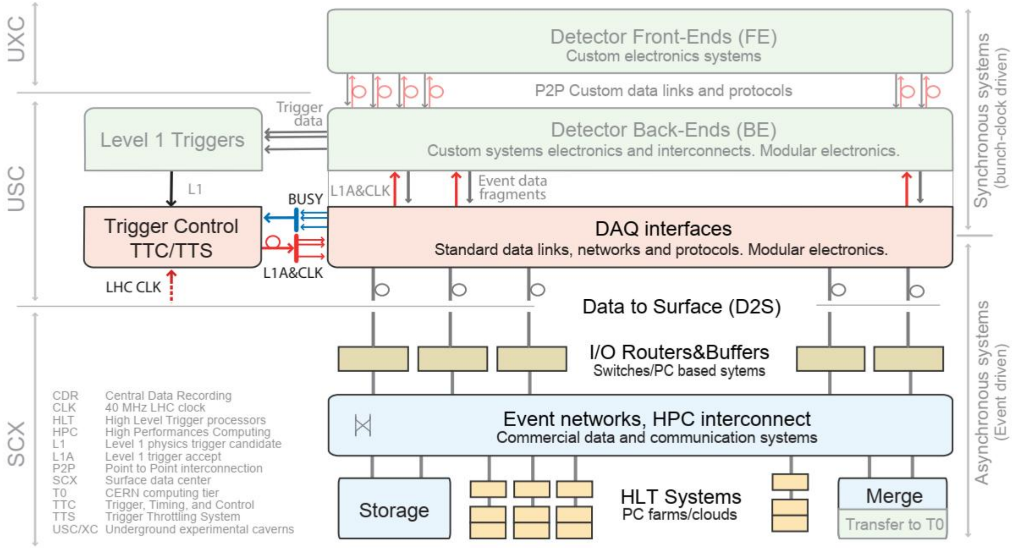
BELLE II



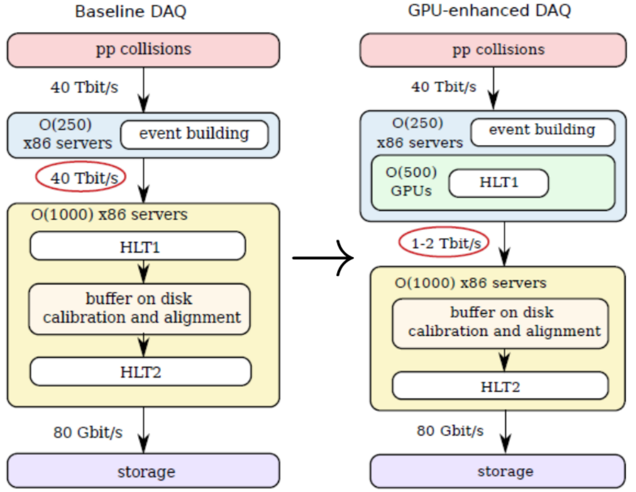
ATLAS Phase II



CMS Phase II



LHCb Phase II



- A few common backend boards (ATCA)
- Network or PCIe bus readout
- GPU/FPGA acceleration at HLT， ML in trigger
  - GPU power has increased 1,000 times in the last decade
- Full software trigger @LHCb
  - Deal with higher occupancy and more accurate tracking.

Previous experience with TDAQ Hardware

- Designed and constructed BESIII trigger system
  - Comprehensive trigger simulation/hardware design/core trigger firmware development
- GSI PANDA TDAQ R&D
  - High performance computing node (HPCN) board
- Designed and constructed for Belle II DAQ
  - Belle2Link and HPCN V3 as ONSEN
- Constructed CPPF system for CMS Phase-I trigger
  - MTCA board, Cluster finding for Muon/RPC
- Designing for CMS Phase-II backend and trigger
  - ATCA common board for iRPC/RPC

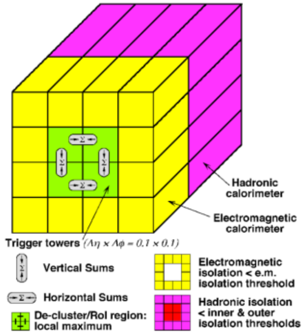
FAIR — Facility for Antiproton and Ion Research in Europe

Extensive experience in TDAQ system design, algorithm and hardware development

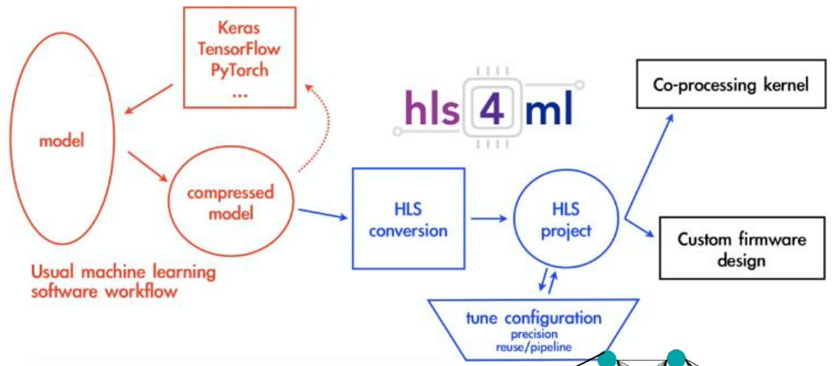
Previous experience with ML algorithm

Neural network used in ATLAS global trigger

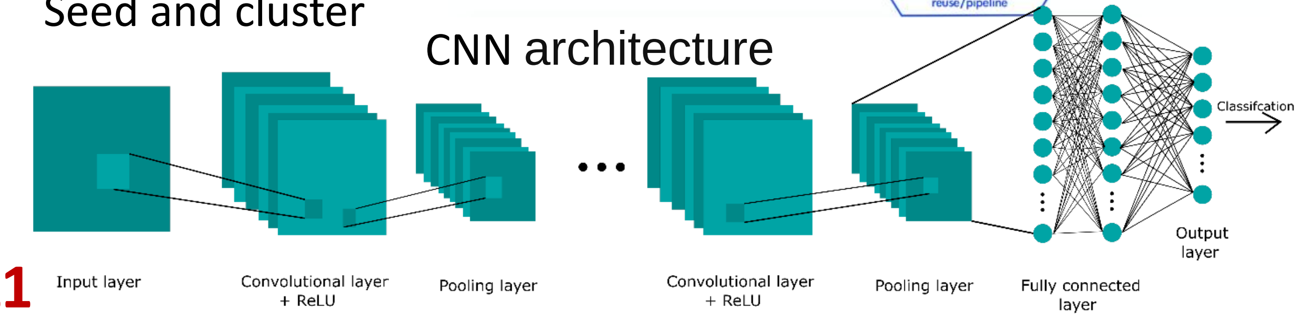
- Example: tau reconstruction at the hardware trigger level
- Train the neural network (NN) with ROI
- Use hls4ml to convert NN model to hls project



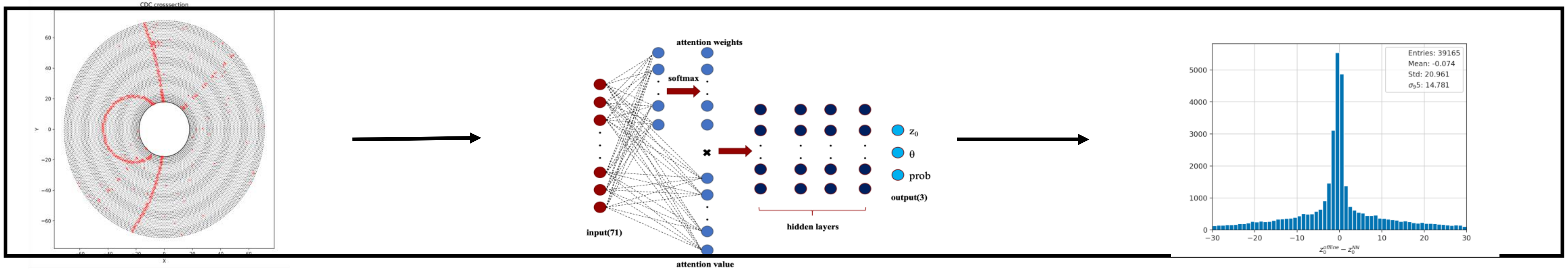
Seed and cluster



CNN architecture



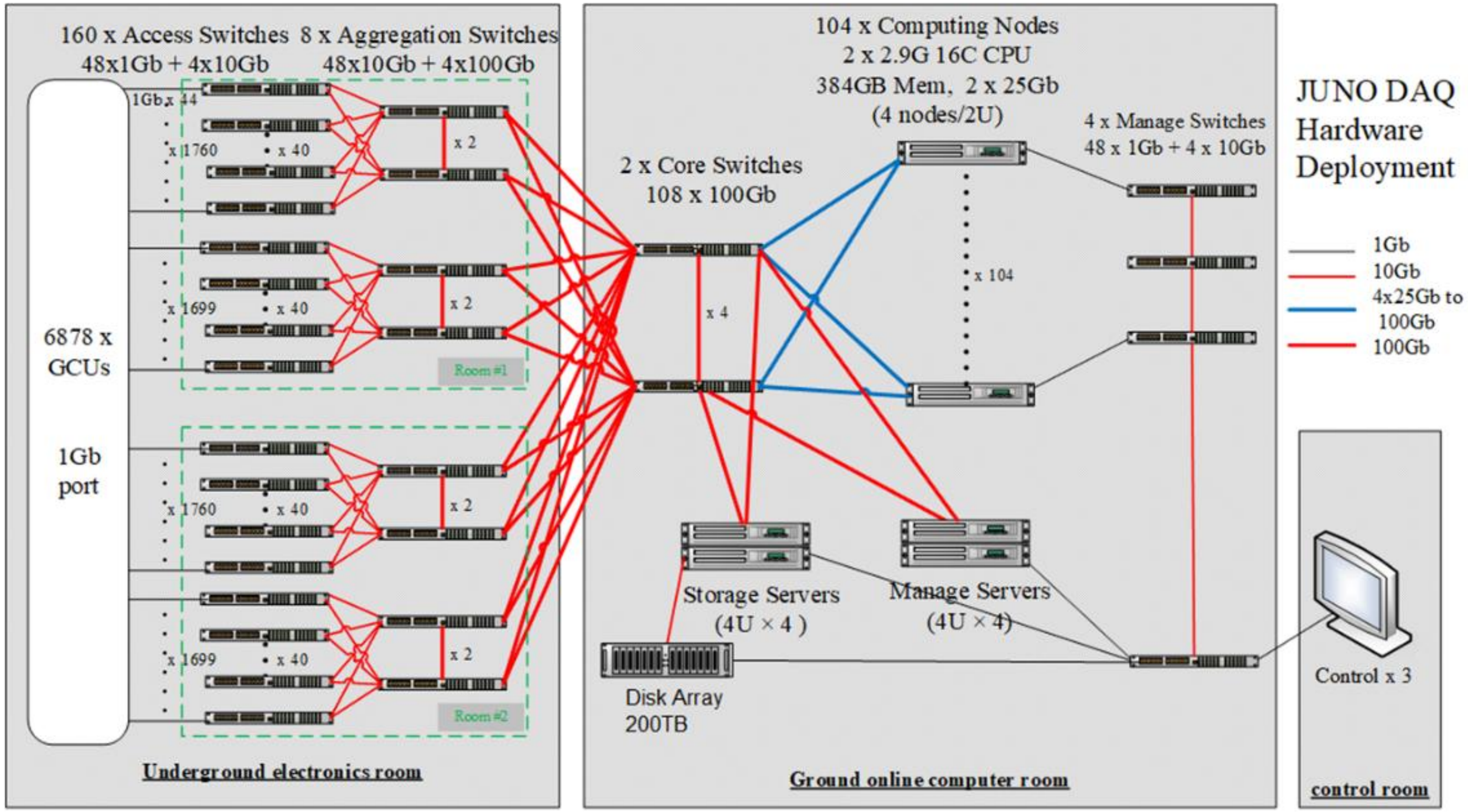
DNN based tracking algorithm for Belle II L1



Some experience in ML algorithm development at L1 trigger

Previous experience with DAQ&DCS

- BESIII DAQ & DCS
  - Running since 2008
- Dayabay experiment DAQ&DCS
  - Operated from 2011 to 2020
- LHAASO DAQ
  - Operated since 2019
  - Full software trigger
- JUNO DAQ&DCS
  - Two types of data stream
    - HW trigger for waveform
    - Software trigger for TQ hits
  - Online event classification



Extensive experience in DAQ&DCS development and operation, including software trigger