# Status at Feb 25

- Server for GUFI arrived just before lunch
  - Setting up in process, thanks to Tingxuan and other engineer for initial setup with management IP
- Finalized test of the CHECK with FANOUT
  - Logic Algorithm:
    - 256 trigger arrives
    - Check arrives
    - An active high "CHECK\_RECEIVED" flag is then transmitted to the GEMROC until the end of the next trigger: the GEMROC interpret the trigger marked by the "CHECK\_RECEIVED" flag as the first trigger of the next batch of 256.
  - Logic is working properly when run is ongoing
    - Check is readout at a trigger number that is always the same (modulo 256)

### Status at Feb 25 - II

🔝 auto_s	ignaltap_0 Not running ✔ 7675 cells 643072	bits NA	NA	NA							USB-Blasterii [USB-1]	Setup
										Device:	@1: 5AGT(FD3H3 MD3G3 *	Scan Cha
										>> SOF	Manager:	
	2025/02/24 15:57:04 (0:0:0.2 elapsed)	-	05								+795	
Type Alias		-128 -9		9 6,4	128 192	256 32	0 384	448 512	576 640	704	768 832	896
	BESIII_CLK_IN					AN INCOMENDATION OF A DESCRIPTION OF A DESC	U TUUT ILUT ILUT ILUT ILUT ILUT ILUT ILU	LAN ALUK ALUK ALUK ALUK ALUK ALUK ALUK ALUK	ALUI ULII ALUI ALUI ALUI ALUI ALUI ALUI			
*	L1_CHK_IN S	2										
	L1_TRIGGER_IN	0									-	
	L1_CHOKE_OUT	0										
	L1Chk_ARRIVED_FLAG_TOP	0.			-							
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_ARRIVED_FLAG	2										
	L1Chk_manager_2025:L1Chk_manager_2025_inst U_L1A_count[31.0]	-	055309h					0006530Ah				
	nager_2025:L1Chk_manager_2025_inst[SLV32_L1A_counter_OUT[310]	0000						00065309h				
	manager_2025:L1Chk_manager_2025_instjU_L1A_count_at_CHK[310]	0000	5209h					00065309h				
	L1Chk_manager_2025:L1Chk_manager_2025_inst synch_reset	0		-								
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_mismatch	1			0							
*	L1Chk_manager_2025:L1Chk_manager_2025_inst L1A_falling	0		I								
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1A_rising	0		0								
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_rising	0										
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_coherence_failed	1										
	B-SLV32_L1A_counter_at_CHK_TOP[31.0]	-					00000000h					
	status_port[310]			-			00000000					
	a5gx_bes_iii_qsys_no_tcpip:u0 roc_ctl_export[31]		nnnnn									
	T1_T0_SPI_CLK											
	T3_T2_SPI_CLK											
	T5_T4_SPI_CLK											
	T7_T6_SPI_CLK		HUUUUUU	mmmm					nnnnnnnnnnnnn	n n n n n n n n n		INNNNN
	T0_nSEL S	0			-							
	T2_nSEL S	0										
*	T4_nSEL S	0										
	T6_nSEL S	0			_							
	T1_nSEL S	0.										
	T3_nSEL S	2									-	
	T5_nSEL S	2										
	T7_nSEL	0										
	T0_SPI_MISO	1										
	T2 SPI MISO	1	11	1								
🇯 Data												

#### L1\_CHK\_IN is received, the end of the next L1\_TRIGGER\_IN reset it

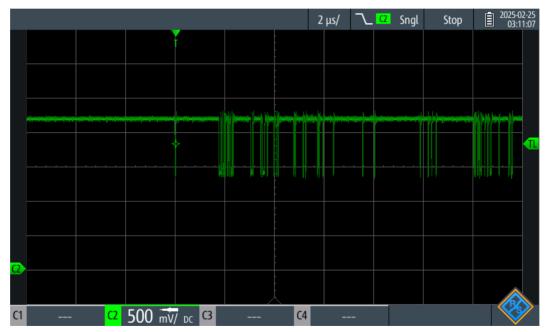
# Issue at the start of the run

- We then proceed to test the synchronization at the test of the BESIII DAQ run.
- Issue arises in both trigger and check lines

Type Alias	Name	-128 -94 9	6,4		192	256		384	448	512		640 79		832 89
*	BESIII CLK IN							mmmn		החנטונטונטונטונט	ແບບການການການການ	ແບບບານການການການ	ານທານການການການການການ	ປຸກມານພາຍພາຍພາຍພາຍພາຍພາຍພາຍພາຍພາຍພາຍພາຍພາຍພາຍພ
	L1_CHK_IN		L	1				mu		_1	۱			
*	L1_TRIGGER_IN					ທີ່	1				۱			
	L1_CHOKE_OUT													
4	L1Chk_ARRIVED_FLAG_TOP													
*	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_ARRIVED_FLAG													
<b>a</b>	■ L1Chk_manager_2025:L1Chk_manager_2025_inst[U_L1A_count[310]		00000000h							0000000	21h			
	nager_2025:L1Chk_manager_2025_inst SLV32_L1A_counter_OUT[310]		0000000	Oh						00	000001h			
<b>a</b>	manager_2025:L1Chk_manager_2025_inst U_L1A_count_at_CHK[310]		0000000	Oh						00	000001h			
*	L1Chk_manager_2025:L1Chk_manager_2025_inst synch_reset													
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_mismatch													
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1A_falling		1		[		_1				_1			
*	L1Chk_manager_2025:L1Chk_manager_2025_inst L1A_rising													L1
	L1Chk_manager_2025:L1Chk_manager_2025_inst L1Chk_rising						L							1
	L1Chk_manager_2025:L1Chk_manager_2025_instjL1Chk_coherence_failed													
<b>a</b>	SLV32_L1A_counter_at_CHK_TOP[310]						000	00000h						
	■ status_port[310]						000	00000h						
	a5gx_bes_iii_qsys_no_tcpip:u0 roc_ctl_export[31]													
	T1_T0_SPI_CLK		mm	www	mmm	www	mmm	m	www	mm	mmm	www	www	hunn
	T3_T2_SPI_CLK	mmmm	mm	mmm	ากกากกา	www	mmm	m		mm	mmm	www	mmm	hunn
	T5 T4 SPI CLK		mm	www	mmm	www	mmm	mm	mmm	mm	mmm	www	mmm	hunn
*	T7_T6_SPI_CLK	mmmm	mmm	mmm	ກກາກການ	www	mmm	m		mm	เกิดการเกิด	wwww	www.	hunn
*	T0_nSEL Q													
4	T2_nSEL Q													
	T4_nSEL 0													
4	T6_nSEL Q													
	T1_nSEL Q													
	T3_nSEL Q													
	T5_nSEL Q													
	T7_nSEL Q													
	TO_SPI_MISO 1													
	T2 SPI_MISO 1													
	T4_SPI_MISO 1													
	T6_SPI_MISO 1													
	T1_T0_TPULSE													
	T3_T2_TPULSE													
*	T5_T4_TPULSE							i						
*	T7 T6 TRUE 66	1 i												
Data	Jan Setup													

# Issue at the start of the run

• Similar behaviour in the oscilloscope when looking at the negative output of the CHECK (or L1) of the MTI board



• Jingzhou, Wenxuan and Sheng are working on it