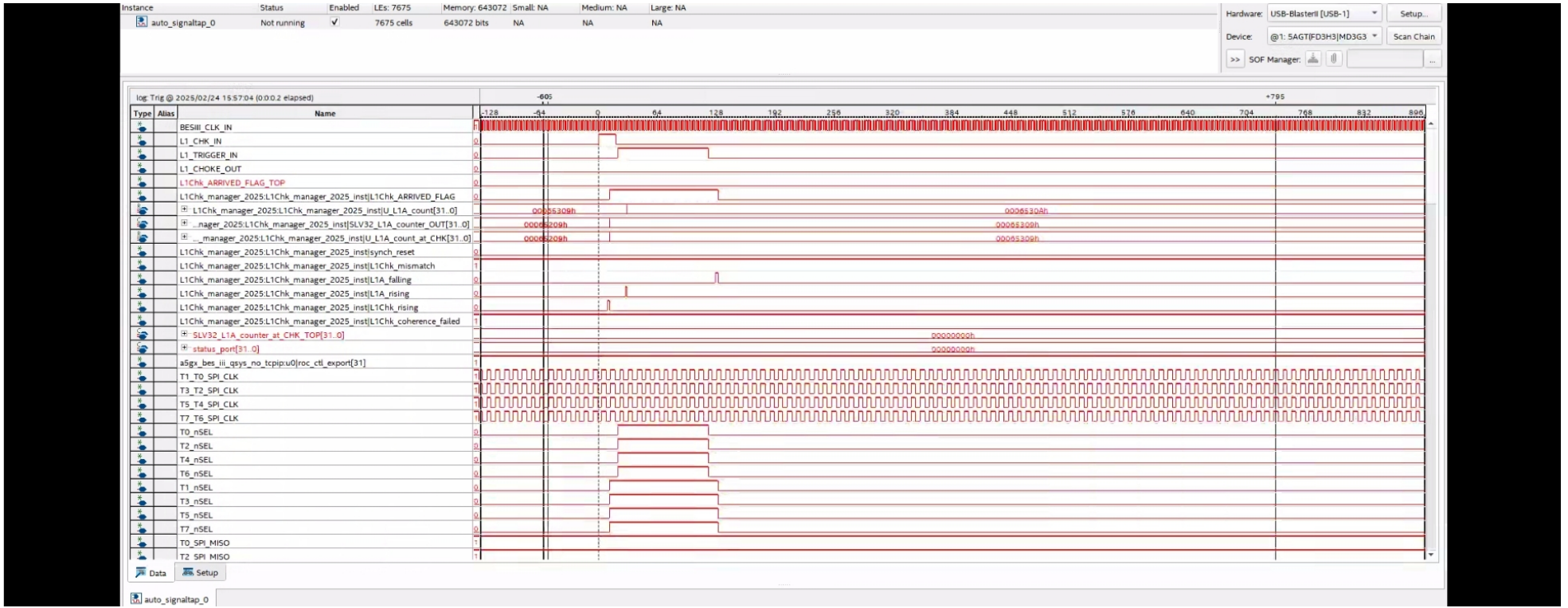
Status at Feb 25

- Server for GUFI arrived just before lunch
  - Setting up in process, thanks to Tingxuan and other engineer for initial setup with management IP

- Finalized test of the CHECK with FANOUT
  - Logic Algorithm:
    - 256 trigger arrives
    - Check arrives
    - An active high “CHECK_RECEIVED” flag is then transmitted to the GEMROC until the end of the next trigger: the GEMROC interpret the trigger marked by the “CHECK_RECEIVED” flag as the first trigger of the next batch of 256.
  - Logic is working properly when run is ongoing
    - Check is readout at a trigger number that is always the same (modulo 256)

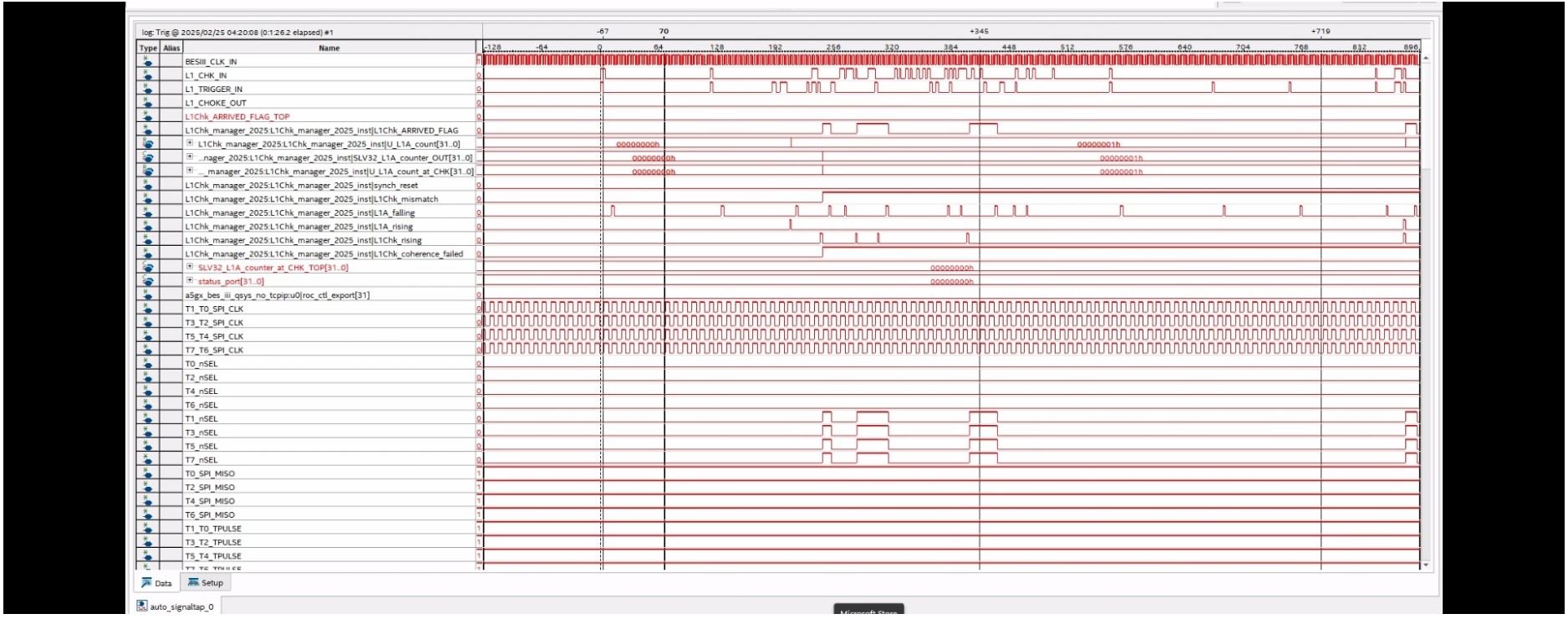
Status at Feb 25 - II



L1_CHK_IN is received, the end of the next L1_TRIGGER_IN reset it

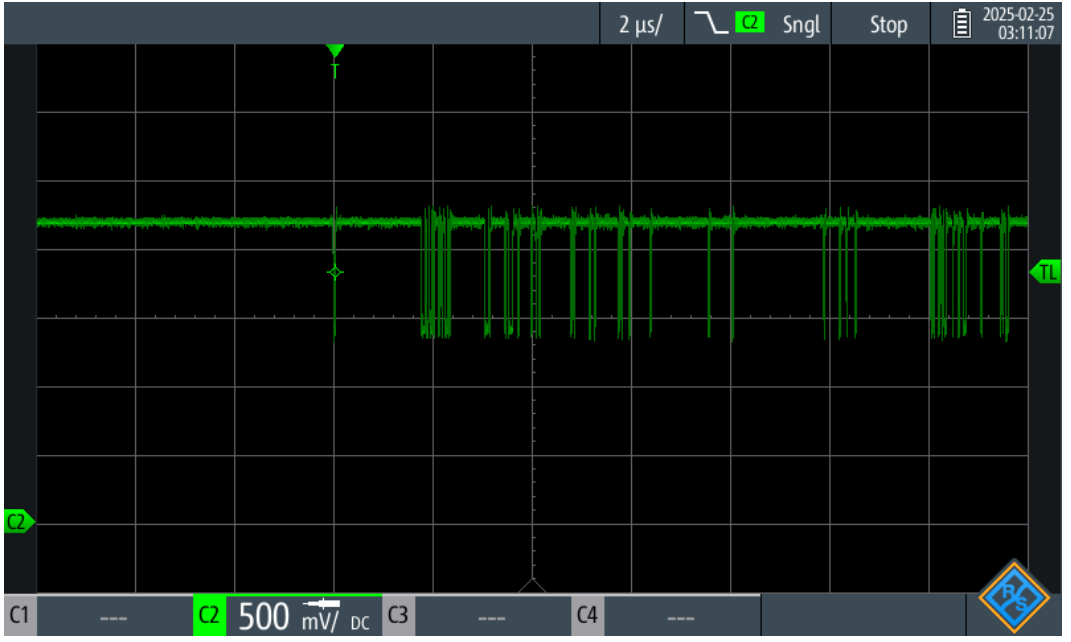
Issue at the start of the run

- We then proceed to test the synchronization at the test of the BESIII DAQ run.
- Issue arises in both trigger and check lines



Issue at the start of the run

- Similar behaviour in the oscilloscope when looking at the negative output of the CHECK (or L1) of the MTI board



- Jingzhou, Wenxuan and Sheng are working on it