Safety Interlock System for Tracker
ATLAS ITk tracker as example

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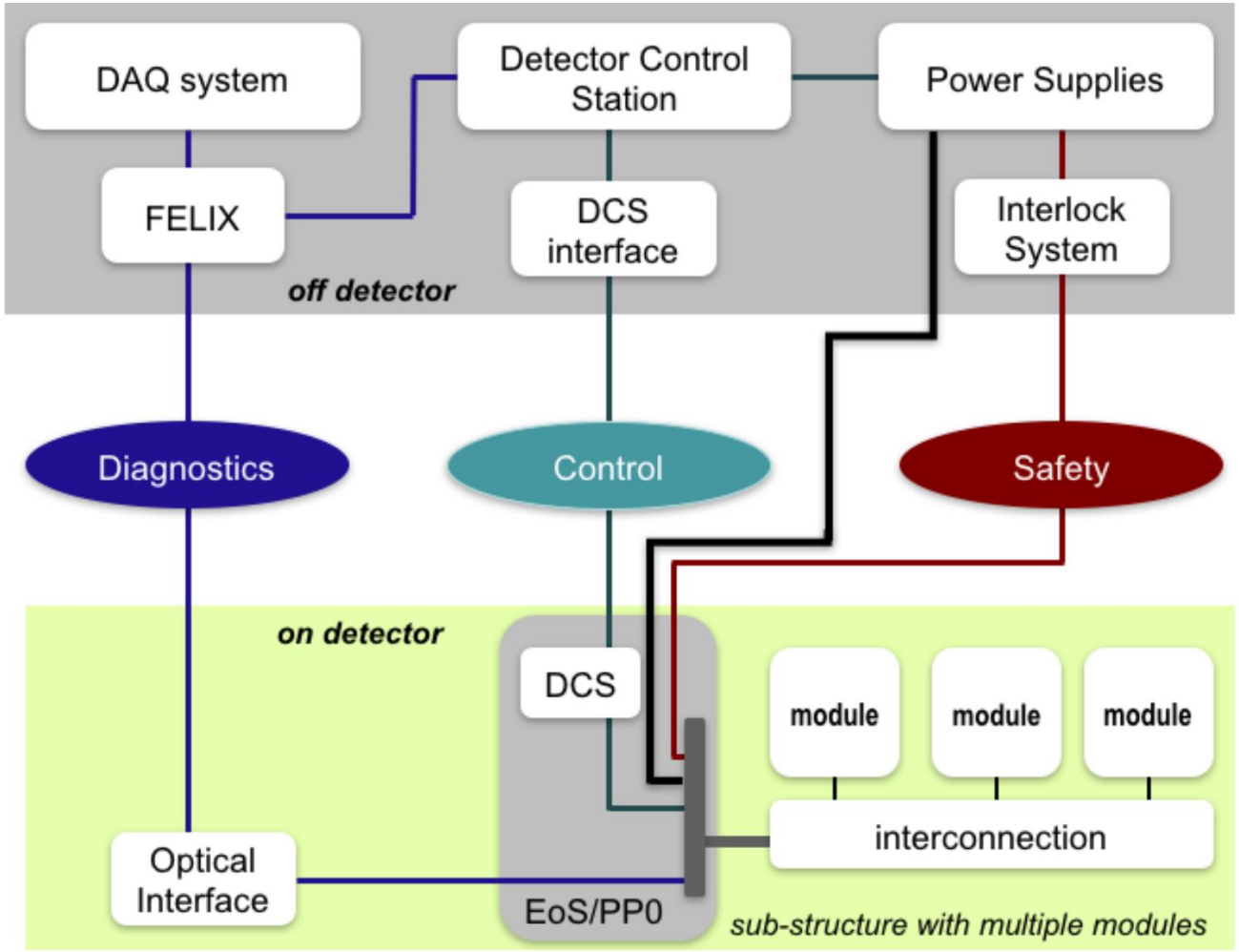
ATLAS ITk Detector Control System

- *我个人的简单总结
- Safety
  - 无论探测器是否供电，它都可以工作
  - 防止过热
- Control
  - 监控和处理探测器正常工作时的局部组件的用电异常
- Diagnostics
  - 收集探测器运行的各种环境参数，用于探测器性能研究分析



ATLAS ITk common: interlock System

- the safety path is built on a hard-wired interlock system
  - acts directly on power supplies or other equipment if the safe operation of the detector can no longer be guaranteed
  - this system must have the highest reliability, but it does not require a high granularity
  - It is always in operation, even if the detector is off. One temperature sensor per serial powering chain is foreseen, which automatically provides some redundancy
  - the Interlock system, which is built in common for all ITk Detectors, is described in more detail in Section 12.3

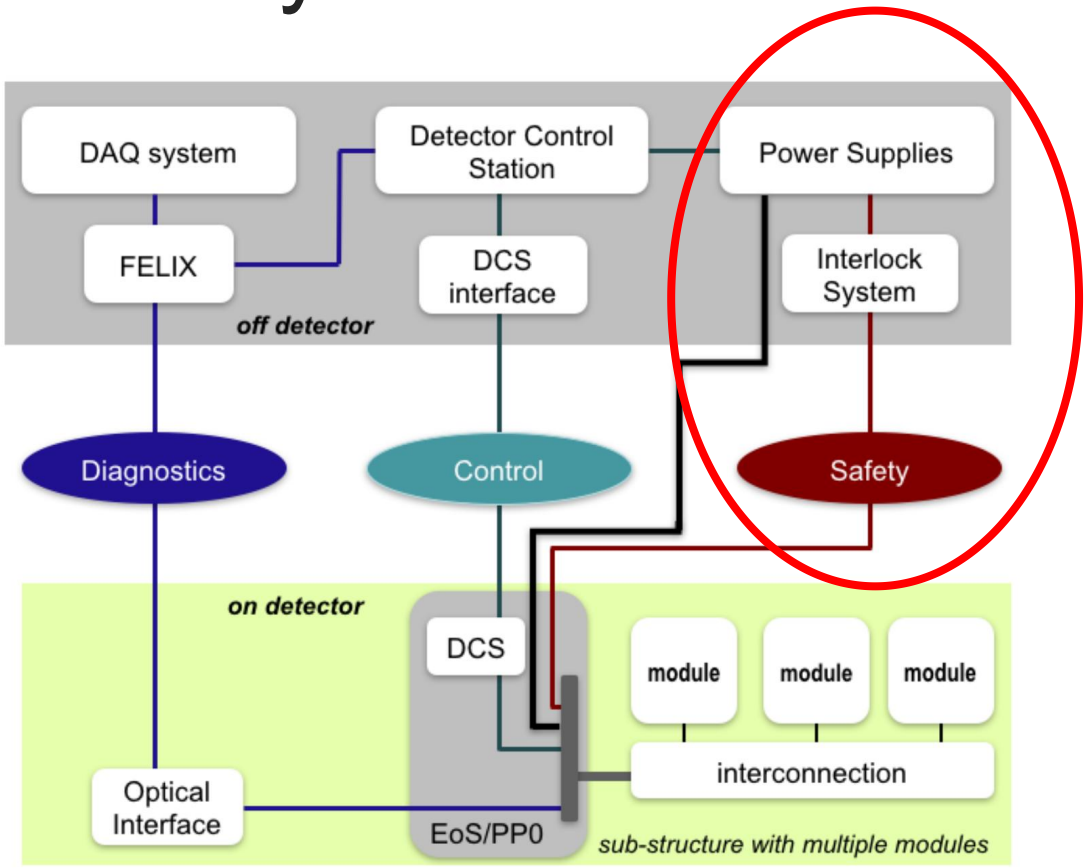


Figure 11.3: Overview on the ITk Pixel Detector Control System.

ATLAS ITk common: Interlock System

- ITk Common Interlock System is a safety system which protects both the detector and personnel against any risks which may arise
  - completely hardwired system which acts as a last line of defense for the detector safety
  - must be running at all times, but has a coarse granularity and relatively low precision

- All signal processing takes place in the Interlock Matrix Crates (IMCs) located in the counting rooms
  - In addition to temperature information, signals from the ATLAS Detector Safety System (DSS) providing information such as the status of the accelerator or of the ITk cooling plant are also fed into
  - Risks to human beings caused by lasers

The concept of the Interlock Matrix Crate can be seen in Figure 12.2.

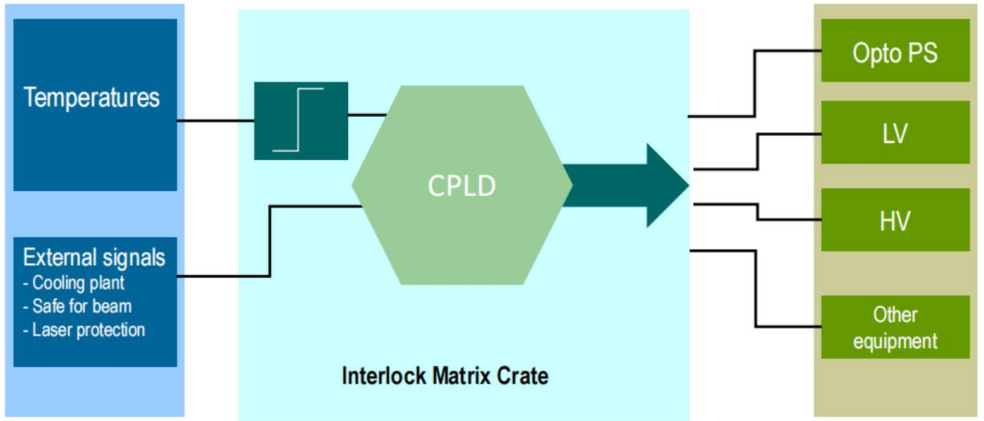


Figure 12.2: Schematic view of the Interlock Matrix Crate.

ATLAS ITk common: Interlock System

- overheating is one of the main risks to all silicon detectors, temperature sensors are located at critical points of the ITk
- ATLAS ITk Pixel Detector
  - each serial powered chain is equipped with a 10 kΩ NTC
  - always more than one serial powered chain per cooling circuit, redundancy is provided everywhere
  - NTCs are chosen due to their high radiation hardness and their large signals (dR/dT) which permit the use of two-wire read-out and routing of signals back to the counting rooms

The concept of the Interlock Matrix Crate can be seen in Figure 12.2.

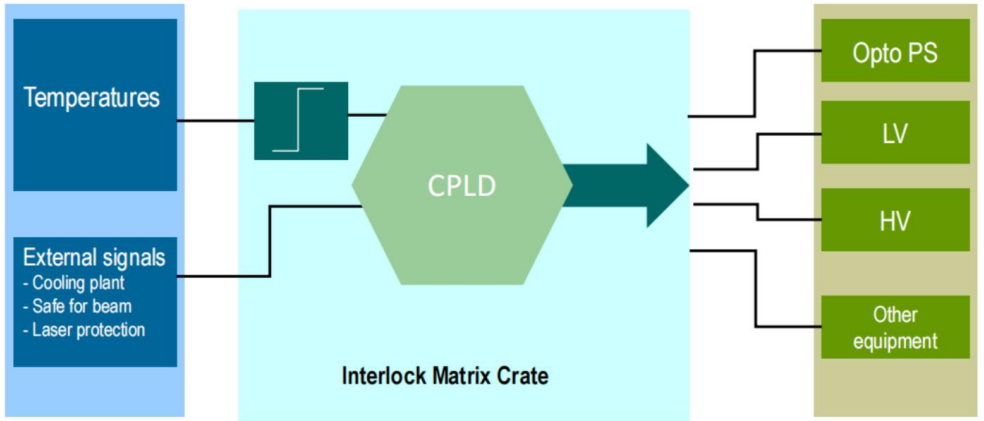


Figure 12.2: Schematic view of the Interlock Matrix Crate.

ATLAS ITk common: Interlock System

- Pixels incorporate a fully hardwired interlock system
- ATLAS ITk strip detector
  - each cooling pipe outlet is equipped with dual (redundant) 10 kOhm NTC, and two-wire read-out and routing of signals back to the counting rooms

The concept of the Interlock Matrix Crate can be seen in Figure 12.2.

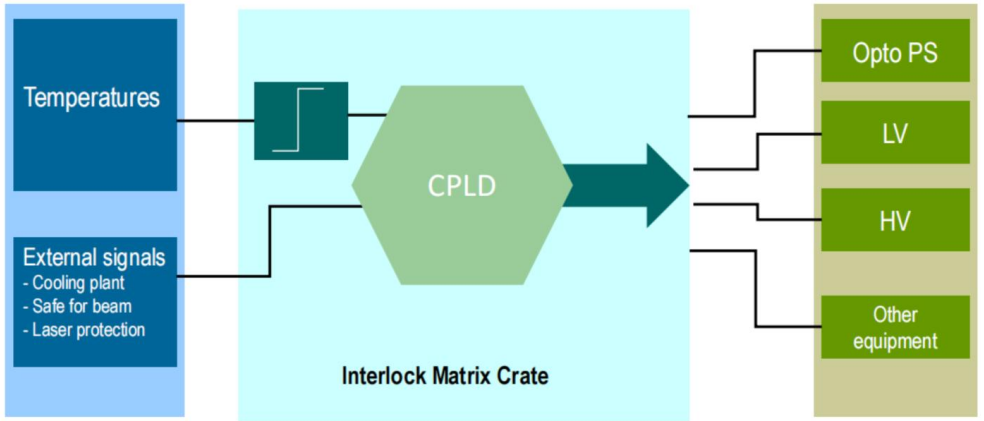


Figure 12.2: Schematic view of the Interlock Matrix Crate.

ATLAS ITk pixel: Detector Control System

- Its design is driven by the requirements of the serial powering
- It is made of the DCS network, whose main ingredients are the **DCS controllers** and the **PSPP chips**
- It has its own lines for powering and communication and is therefore independent from the other paths. It must have quite fine granularity, as individual modules must be controllable to ensure reliable control over operations

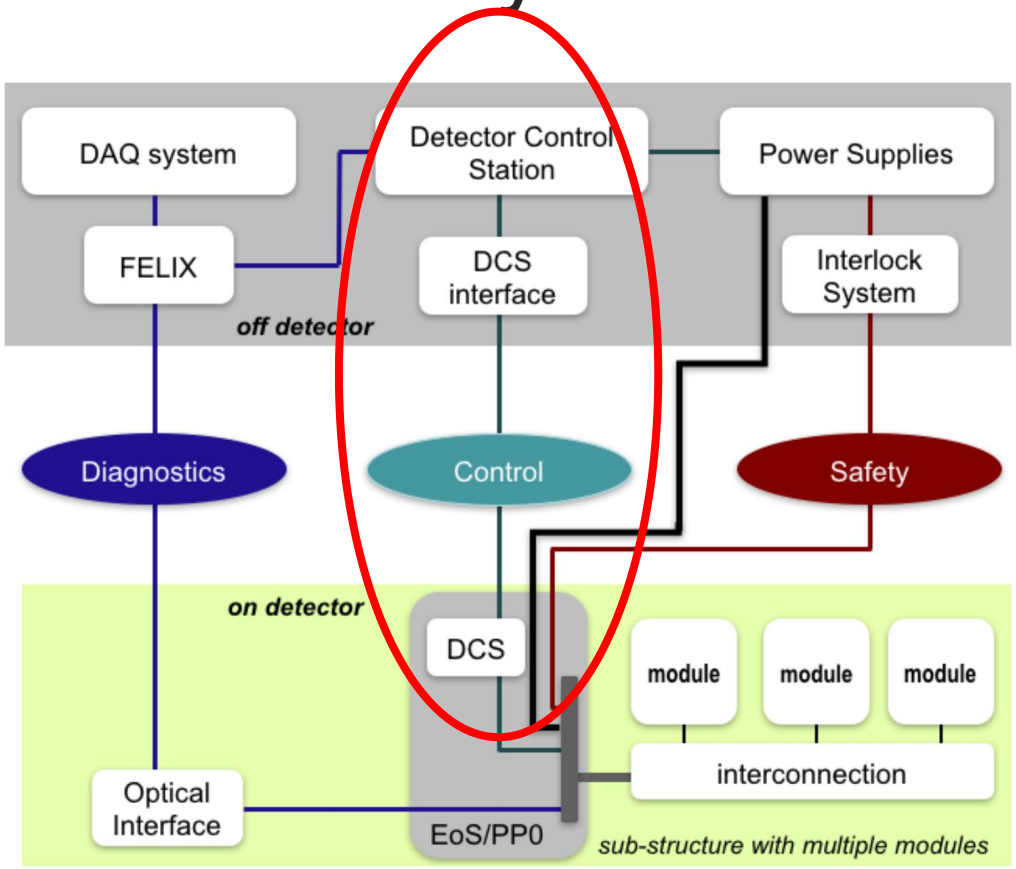


Figure 11.3: Overview on the ITk Pixel Detector Control System.

ATLAS ITk pixel: Detector Control System

- Pixel Serial Powering Protection Chip
  - A prototype of the PSPP chip has been produced in 130 nm CMOS technology
  - Its main elements are a large bypass transistor and a 10-bit ADC
  - The ADC provides monitoring of the module's voltage and temperature
  - The bypass transistor is designed to switch currents of up to 8 A to disable a single module in the serial power chain

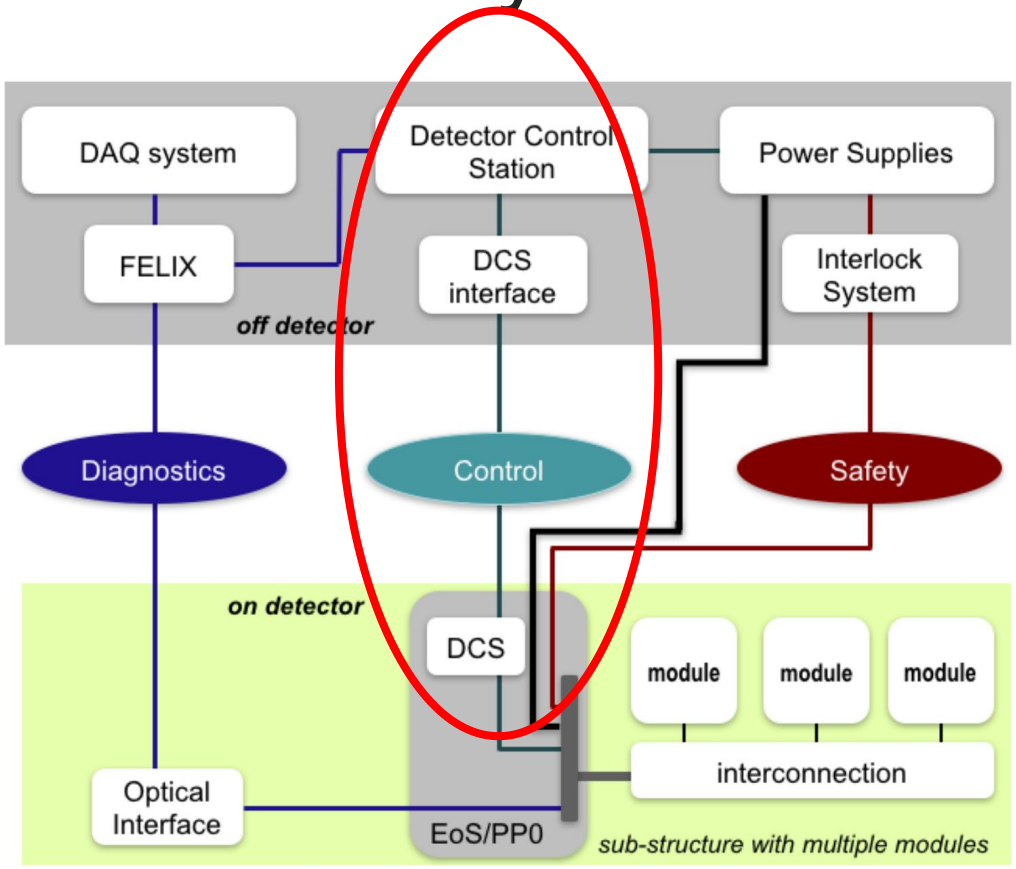


Figure 11.3: Overview on the ITk Pixel Detector Control System.

ATLAS ITk strip: Detector Control System

- ITk Strip Detector DCS comprises three main components
  - a Common **Interlock system**, shared with the Pixel Detector
  - a Common Monitoring System, also shared with the Pixel Detector
  - a Strip specific interlock and monitoring system provided by the AMAC chip

- Within each stave or petal, a local interlock system is provided by means of the Autonomous Monitor And Control (**AMAC**) chip located on the on-module power board
  - first line of defense against temperature excursions of the powered detector modules
  - AMAC chip monitors several on-module parameters such as the temperature of each hybrid and the sensor bias current. It must also be powered and configured in order to enable the two key components of the on-module power board, the DC-DC converter and the HV Multiplexer switch
  - In addition AMAC compares the digitised signals against programmable upper and lower limits: any excursion beyond these limits will, in extreme cases, result in the DC-DC converter and HV switch being disabled directly

ATLAS ITk common: Environmental Monitoring

- The Common Monitoring system monitors all environmental parameters of the ITk volume, in particular the temperature, humidity, radiation, gas flow and pressure
- the largest number of sensors is required for temperature monitoring. In the case of the ITk pixel detector, all sensors which are not directly part of the staves or ring elements are supervised by this system, for example the temperatures of air volumes or cable bundles
- CERN is developing a successor to the Embedded Local Monitor Board (ELMB)

Sensor type	Number of sensors
Temperature	1000
Humidity	30
Pressure	200
Gas flow	20
Radiation	20
Vibration	6
Strain gauges	40

ATLAS ITk Cost: Detector Control System

Table 20.1: The total costs of the ITk. The costs of the pixels, common mechanics and common electronics are detailed with the WBS number.

WBS	Description	Costs/kCHF
2.1.1	Sensors	7,339
2.1.2	ASICS	5,403
2.1.3	Hybridization and module assembly	12,325
2.1.4	Services	9,615
2.1.5	Local support	5,492
2.1.6	Global mechanics and installation tooling	2,119
2.1.7	Integration and system test	1,767
2.1.8	Off-detector electronics	2,823
Total for pixels		46,882
2.3.1	Surface assembly and commissioning	2,695
2.3.2	Integration and insertion in the pit	300
2.3.3	Common Structures including PST	2,534
2.3.4	Poly moderator	99
2.3.5	Outer Serices	387
2.3.6	CO_2 cooling plant	6,419
2.4.1	Environmental monitoring	244
2.4.2	Interlock and protection system	380
2.4.3	Grounding and shielding	14
2.4.4	Luminosity and beam protection	293
2.4.5	Phase I FELIX Read-out	777
2.5.1	Production database	303
Total Common Items		14,445
Strip Tracker		60,637
Total for ITk		**121,964**

Thank for Xiaojie Jiang and Shuqi Sheng from LHCb team

LHCb UT Tracker

Detector Control System (DCS)

- part of Experiment Control System (ECS); ECS = DCS+DAQ+HV
- normal operation of equipment
- reacts to "normal" problems

Detector Safety System (DSS)

- detects abnormal/harmful situations and takes automatic actions
- independent from DCS
  $\rightarrow$ safe even in cases of infrastructure problems

Logics for UT:

- rely on DCS for normal operation, tech. stops and shutdowns
  - safety branch of UT ECS tree for temperature, humidity
- DCS should react before DSS power cut $\rightarrow$ soft shutdown
- if DCS malfunctions, DSS keeps UT safe

CEPC Tracker Consideration

- maybe adopt the concept from ATLAS ITk detector ?
- overheating is one of the main risks to all silicon detectors
- temperature sensors are located at critical points of the tracker with some redundancy
  - each serial powered chain is equipped with a 10 kΩ NTC for ATLAS ITk pixel
  - stave CO2 cooling pipe outlet with 2x NTC for ATLAS ITk strip

The concept of the Interlock Matrix Crate can be seen in Figure 12.2.

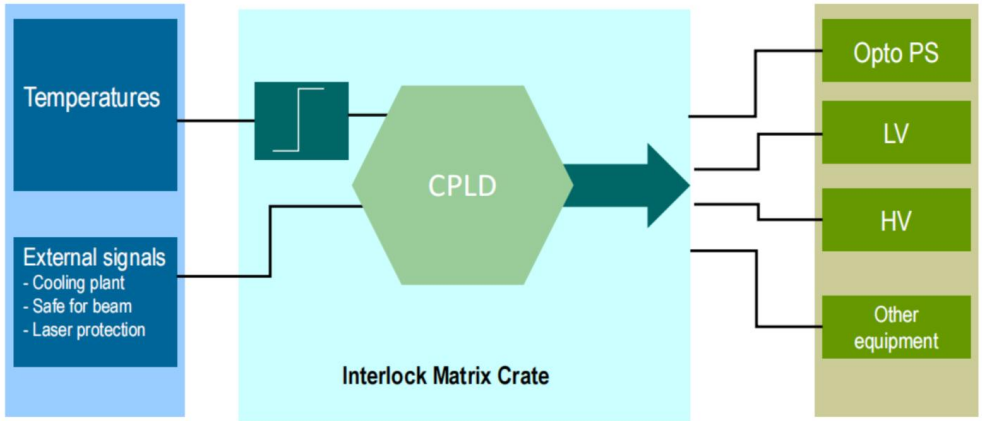


Figure 12.2: Schematic view of the Interlock Matrix Crate.

CEPC Tracker Consideration

- assuming:
  - each stave/ring/sector has 1 cooling pipe
  - each cooling pipe has 2 NTCs
- ITk: 210+(2+3+3+3)*2*2 = 254
  - *2 pipes per ring
- OTk: 110+32=142
- total 396 pipes, and 792 NTC

Information about staves, modules, and sensors used for 3 ITK barrels construction					
Barrel	Number of staves	Modules per stave	Sensors per module	Total number of sensors	Sensor area [m^2]
ITKB1	44	7	14	4312	1.72
ITKB2	64	10	14	8960	3.58
ITKB3	102	14	14	19992	8.00
Total	210			33264	13.31

Table 5.4: Information about staves, modules, and sensors used for 3 ITK barrels construction.

The Module and Sensor Layout of a Single Face of Each ITK Endcap				
Endcap	Number of module rings	Number of modules per module ring	Number of sensors per module	Total sensors
ITKE1	2	13,20	8,8	264
ITKE2	3	16,24,28	8,8,8	544
ITKE3	3	24,36,44	12,14,14	1408
ITKE4	3	24,36,44	8,14,12	1224
Total				3440

Table 5.5: The Module and Sensor Layout of a Single Face of Each ITK Endcap

(a) Nubmer of staves, modules, sensors, and readout ASICs used for the OTK barrel construction

Number of staves	Number of ladders	Number of modules	Number of sensors	Number of readout ASICs
110	880	7,040	28,160	112,640

(b) Nubmer of sectors, modules, sensors, and readout ASICs used for the construction of the OTK endcap pair.

Number of sectors	Number of 2^{nd} aggregation boards	Number of modules	Number of sensors	Number of readout ASICs
32	544	6,368	12,736	46,336

Table 5.14: Information about modules, sensors, and readout ASICs used for the OTK construction.

Backup