Status at Mar 4

- CHECK signal:
  - Angelo finished the firmware update in the early afternoon
  - Run first checks with couple of GEMROCs, then, requested access to flash all the GEMROCs
  - Acquired data with random trigger:
    - Check in the data is now sent out in the 256th trigger
    - Check is composed by a two bit word
    - We will continue testing, but so far ok!
  - We have updated the data packet format, it will be shared soon

```
]: headers[headers.gemroc==9][1020:1300]
```

	gemroc	subrun	run	l1_count	l1_ts	L1_CHK_bit	L1_CHK_error	top_L1_chk_error	header_misalignment_error	FIFO_FULL_error
1514574	9	0	1808	1021	17712	0	0	False	False	True
1514575	9	0	1808	1022	59364	0	0	False	False	True
1514576	9	0	1808	1023	35480	0	0	False	False	True
1514577	9	0	1808	1024	11596	1	0	False	False	True
1514578	9	0	1808	1025	53248	0	0	False	False	True
1514579	9	0	1808	1026	29364	0	0	False	False	True
1514580	9	0	1808	1027	5480	0	0	False	False	True

Status at Mar 4

- Trigger synchronization and data write to disk:
  - As reported by Alberto via email, yestarday we took few runs 2 kHz random trigger rate
  - Comparison between our trigger number in decoded data and number of entries in “Data size for all”
  - Number exactly the same
  - Checked also by Tingxuan

- We will take more data with 4 kHz trigger rate
  - Thanks to GONG Wenxuan for the help

- Setup cables to connect server directly to GEMROC switches

- We will meet with LI Fei for DAQ plans tomorrow morning