CPPM pixel developments R&D On Future Colliders

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On behalf of the Silicon detector FCPPN/L and CPPM Group

CPPM Chinese Cluster Collaboration

- CPPM / ACC collaboration for design and test of Front-End pixel electronics for HEP Future Colliders.

- Scientific cooperation supervised by Pr. Xinchou LOU, Dr. Zheng WANG, Pr. Wei WEI, Pr. Joao GUIMERAES and Pr. Marlon BARBERO, derived from ATLAS CPPM / ACC project (Pr. Shan JIN / Dr. Emmanuel MONNIER).

- Co-PhD Jian Liu (SDU – Pr. Meng WANG / CPPM Pr. Marlon BARBERO & Dr. Alexander ROZANOV). Tests and simulation in LFOUNDRY HV CMOS technology.

- Zhao Mei/IHEP, development work done on LF 150 nm technology in 2019 (APD, guard ring studies, etc…)

- Li Mujin/IHEP, exchange activities in 2024, participated in the design of this project ‘ITER X-Ray Crystal Spectroscopy Detector’

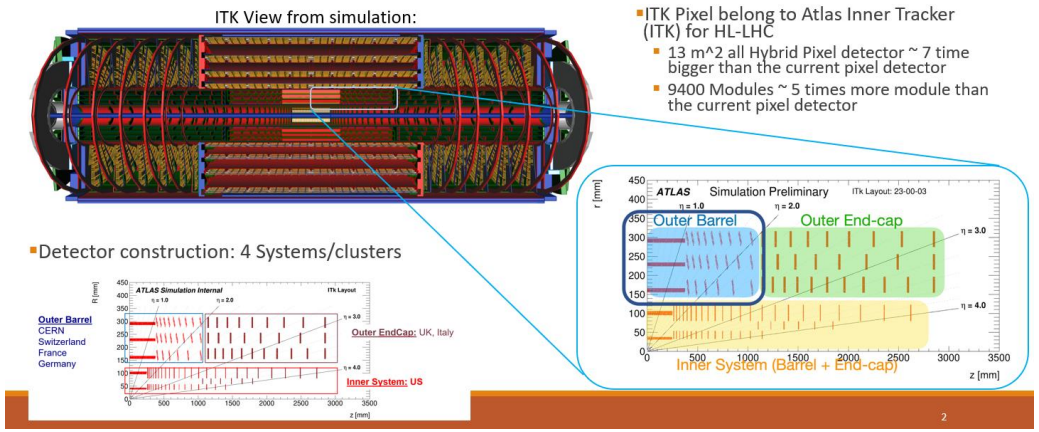
- More collaborations coming soon…

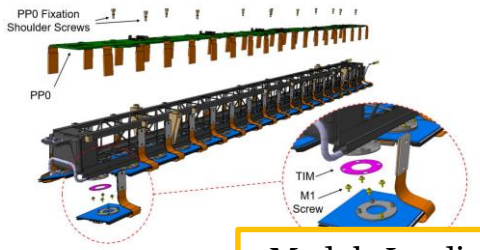
Outline

- Pixels for HEP at CPPM
- Monolithic pixels – TJ180 nm
- Monolithic pixels – TPSCo 65nm
- Hybrid pixels – TSMC 28nm
- Conclusions

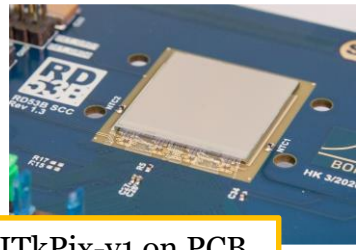
Pixels for HEP at CPPM

- ATLAS and ITk project

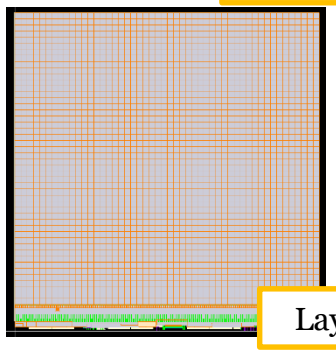




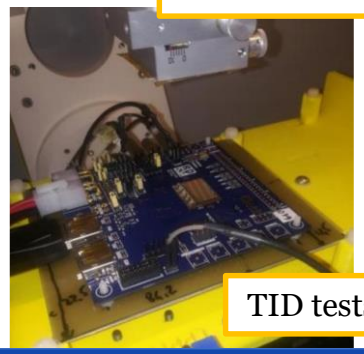
Module Loading



ITkPix-v1 on PCB

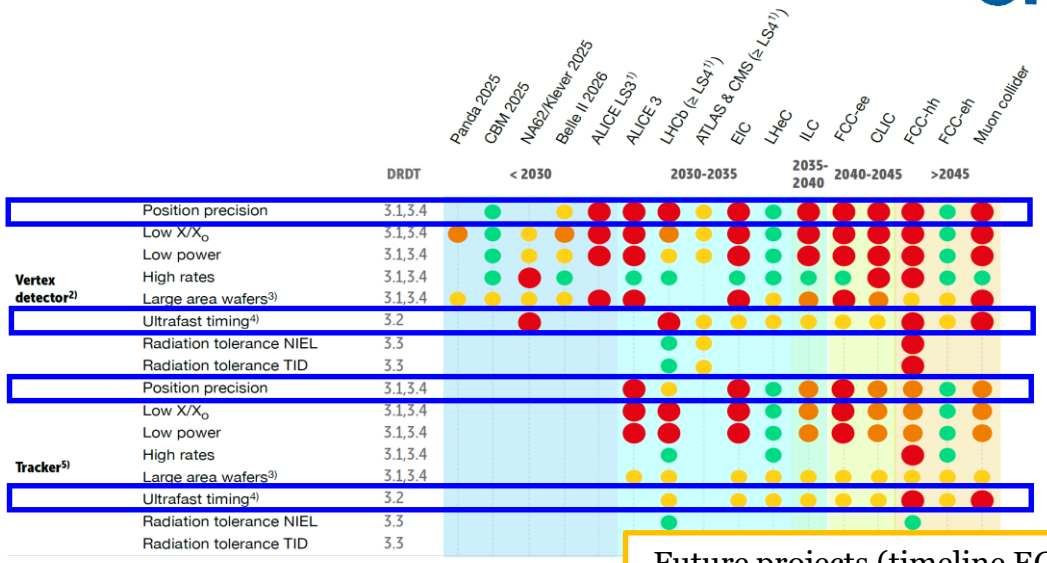


Layout ITkPix-v1

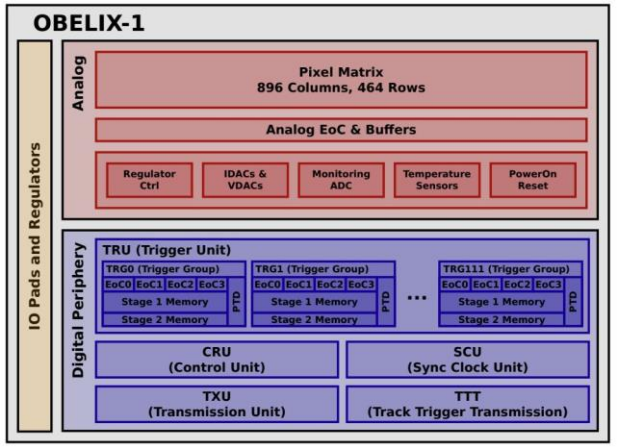


TID tests in Marseille

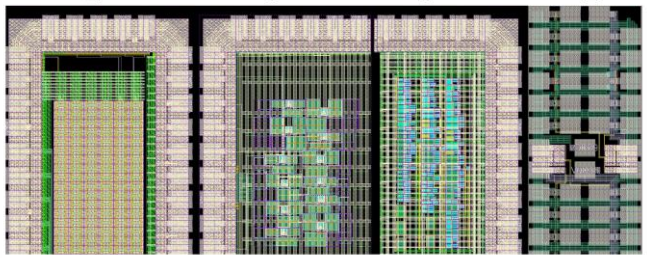
- Future Colliders and Future Projects



Future projects (timeline ECFA)



OBELIX for Belle-II upgrade

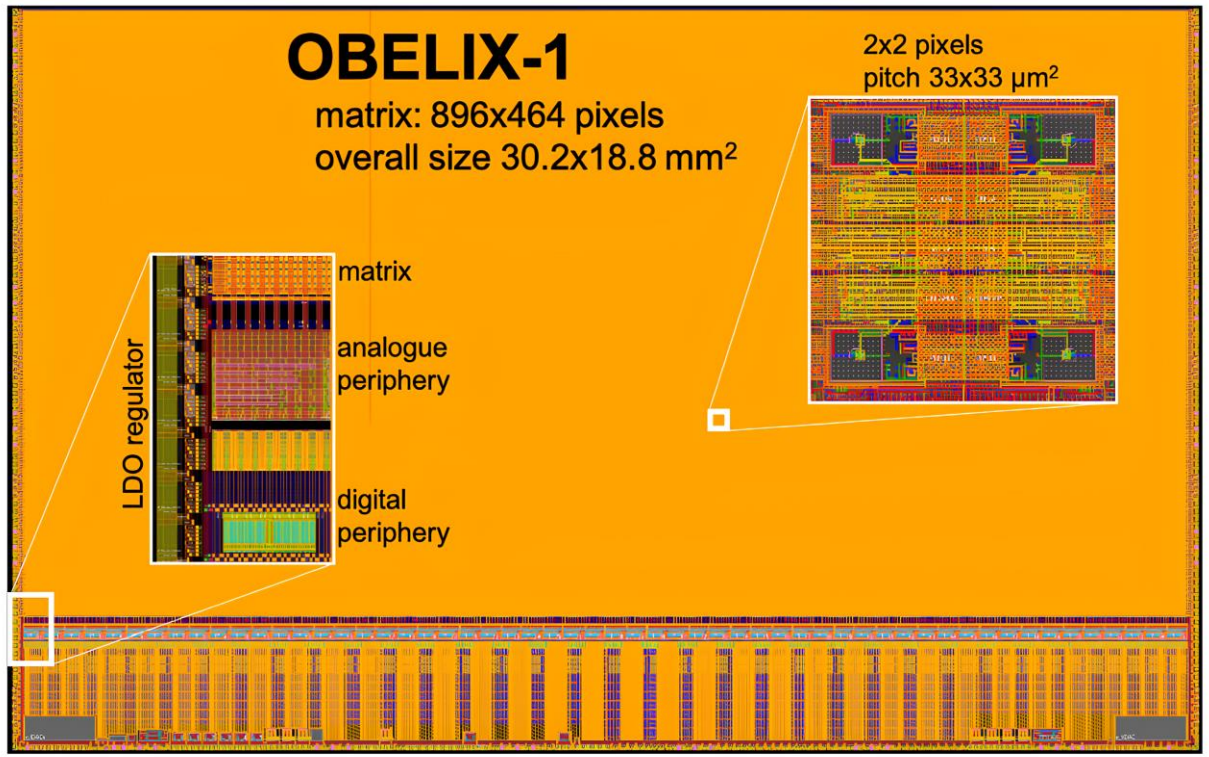


R&D activity for TSMC 28nm

TowerJazz 180nm

Have been involved in this technology-related project for a long time: ATLAS

Monolithic pixels – TJ180 The OBELIX Design

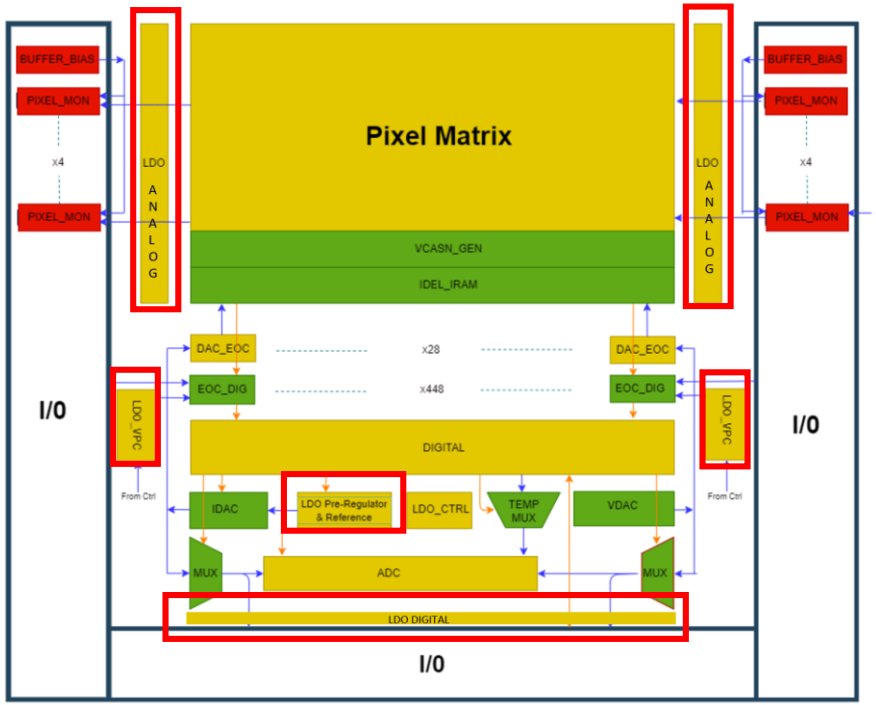


The **O**ptimized **BEL**le II p**IX**el sensor

- Main design **based on the TJ-Monopix2 chip** in TJ180 technology
- **Pixel Matrix**
  - **Hit rate up to 120MHZ/cm²**
  - TID tolerance : 10 MRad/year, NIEL tolerance: $5x10^{13}n_{eq}/cm^2/year$
  - **Power < 200mW/cm²**
  - 464 rows and 896 columns, active area 29.60 x 15.33 mm²
- **New digital periphery – CPPM**
  - New EoC adapted to Belle II trigger – average frequency 30KHz
  - Trigger latency 5-10µs
  - Main Clk at 160MHz, Single output at 320Mb/s
  - Signal digitization: ToT (7 bits, 20 MHz)
  - RD53B control protocol
- **Power Pads**
  - **Power management system added – LDO – CPPM**
  - Simplified system integration
  - **Overall sensor dimensions around 30.2x18.8mm²**

Two design key points

- **Power Management – LDO :**
  - **Power distribution** ⟹ leading to performance degradation
  - On chip regulators are developed:
    - Compensate the voltage drop
    - Simplify the power distribution
    - Two **analog LDO (Low Dropout)** regulators
    - A **digital LDO** regulator
    - A **pre-regulator**
    - A **VPC** (Voltage pre-charge) LDO

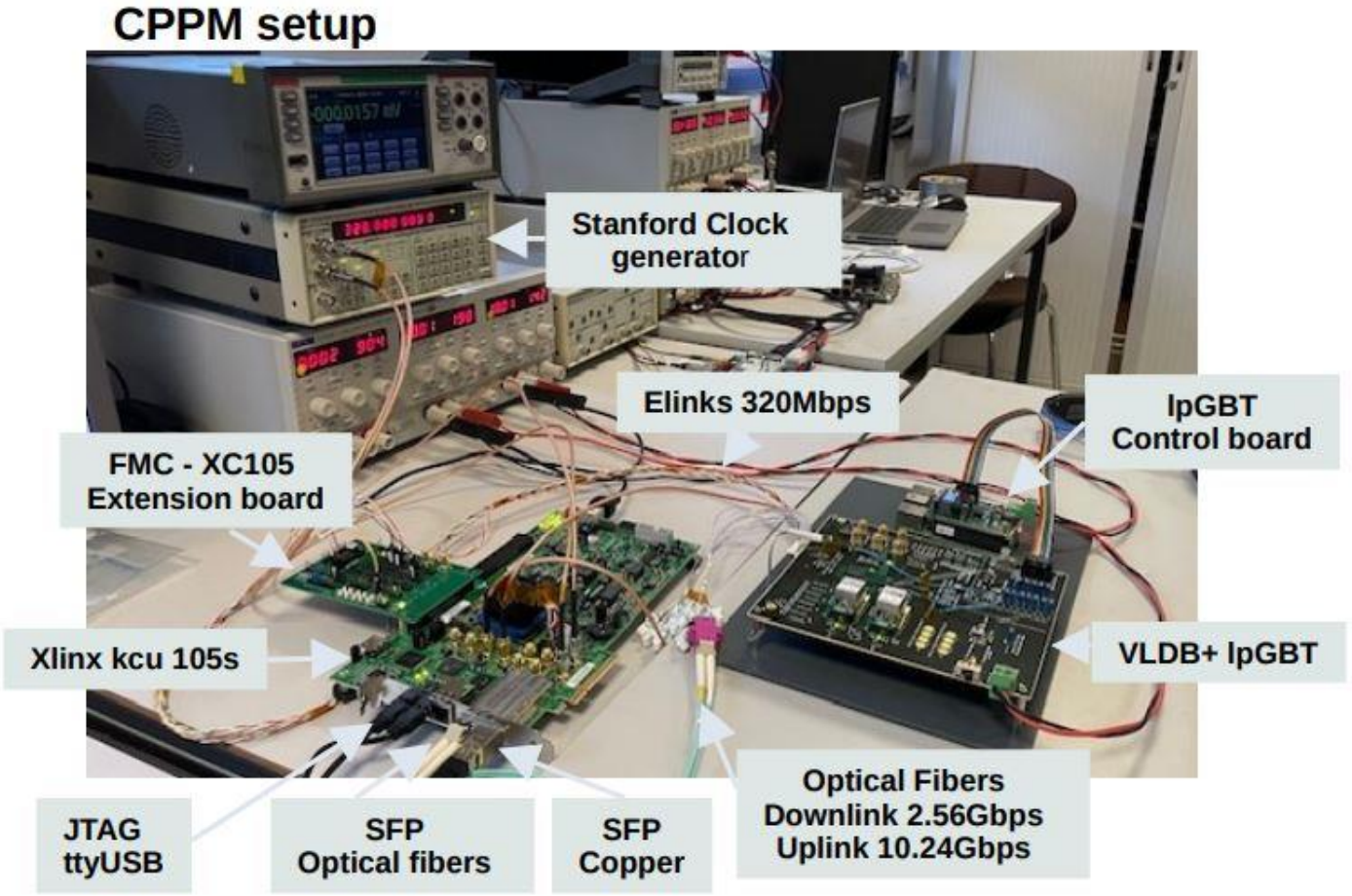


- **BCID crosstalk:**
  - Observed from the first test of TJ-Monopix2, but the cause was not understood, will change the threshold depending on the phase with respect to the hit.
  - **'Breakthrough' in issue understanding**
  - In the 2024 TestBeam, DESY/KEK, realize the effect was so important for irradiated sensors and high temperature operation
  - The amplitude of the BCID crosstalk effect **scales with the number of columns with BCID enabled**

Driver	Implementation	Comments
SYNC	Synchronous Cross-coupled inv.	Std. Cells only, need clk, 10% power increase
SLOW	Current starved output stage	Needs bias current
WEAK	Weaker output driver	Still large spikes due to high inrush current
LV	Complementary source follower	Need to verify SRAM write with low swing signals

Possible solutions for BCID crosstalk

VTX DAQ Organization



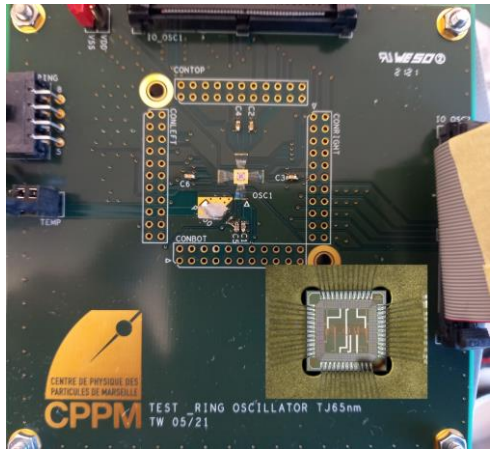
LpGBT setup status at CPPM

- Belle II VTX WG5: System Integration
- CPPM participates :
  - Work Packages: Readout
  - LpGBT evaluation HEPHY + **CPPM**
  - iVTX LpGBT integration **CPPM** + QMUL(?)
    - Chip location, PCB, cables and connectors, mechanical integration
- Interested Groups in WG5 :
  - IHEP (TDAC Group):
    - TDAC system
    - Back-End Hit data trigger readout
  - University Sciences and Tech of China
    - Test, characterization& Readout
    - Mechanic support and integration
  - Jilin University
    - Beam test
    - Run, slow control

TowerJazz – TPSCo 65nm

Monolithic pixels – Exploratory R&D TJ65

- **CPPM contributed with a series of Ring Oscillators** to study the resistance to ionizing radiation of std cells
- The chip contains 48 ring oscillators based on different standard cartridges
- 2 banks of 24 lines to test two configurations:
  - "Functional" bank with oscillation activated
  - "Static" bank with no oscillation during irradiation



DUT board

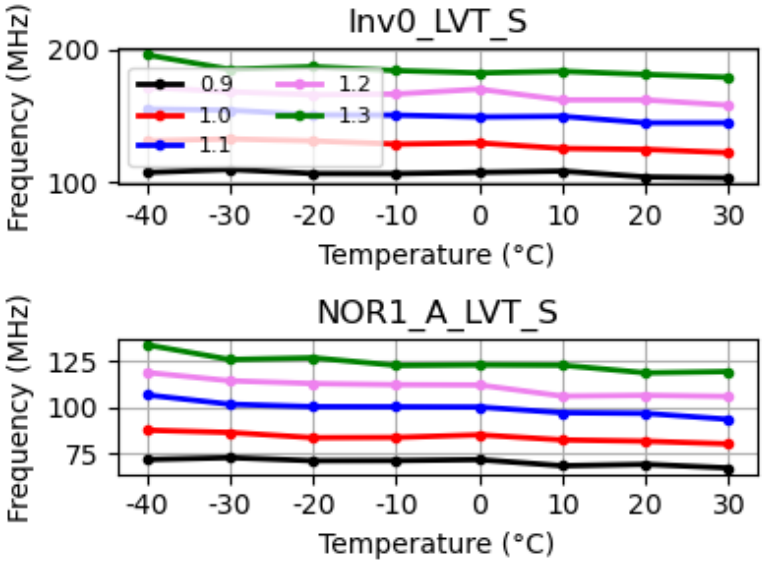
Design Requirements:

- Check basic performance
- Dedicated prototype(s) for high count rates (>> 100 MHz/cm^2)
- Temporal resolution around 100 ps
- Radio tolerance >>10^{15} neq/cm^2

1st submission: December 2020, back in summer 2021

2nd submission: June 2023, back in June 2024

3rd submission: July 2025, will be back at the end of 2025



Freq vs t°C for 2 RO and 5 Vddd (1st version)

Test results

- **Similar frequency degradations** observed for both chips
- Several weeks of annealing at different temperatures, observed:
  - **An absence of cold recovery**
  - **A slight recovery at room temperature**
  - **reverse annealing**
- **Frequency degradation is limited (12 to 25% for a total dose of 830 MRad)**
- **New production of wafers/ALICE custom standard cells** will place with a different level of metallization in 2025. **Irradiations down on 2025 to compare the two types of metallization and standard cells**

DRD3.1 Project: OCTOPUS

Optimized **C**MOS **T**echnology f**O**r **P**recision in **U**ltra-thin **S**ilicon

- Concerns monolithic fine-pitch pixel sensors implemented in the **TPSCo65 process (DRD7.6)**, targeting the vertex-detector requirements of future Lepton Colliders
- **Key final development goals** include:
  - **3µm** single-point resolution
  - Down to **5ns** time resolution
  - Average power consumption below **50 mW/cm²**
  - Minimal inactive periphery area

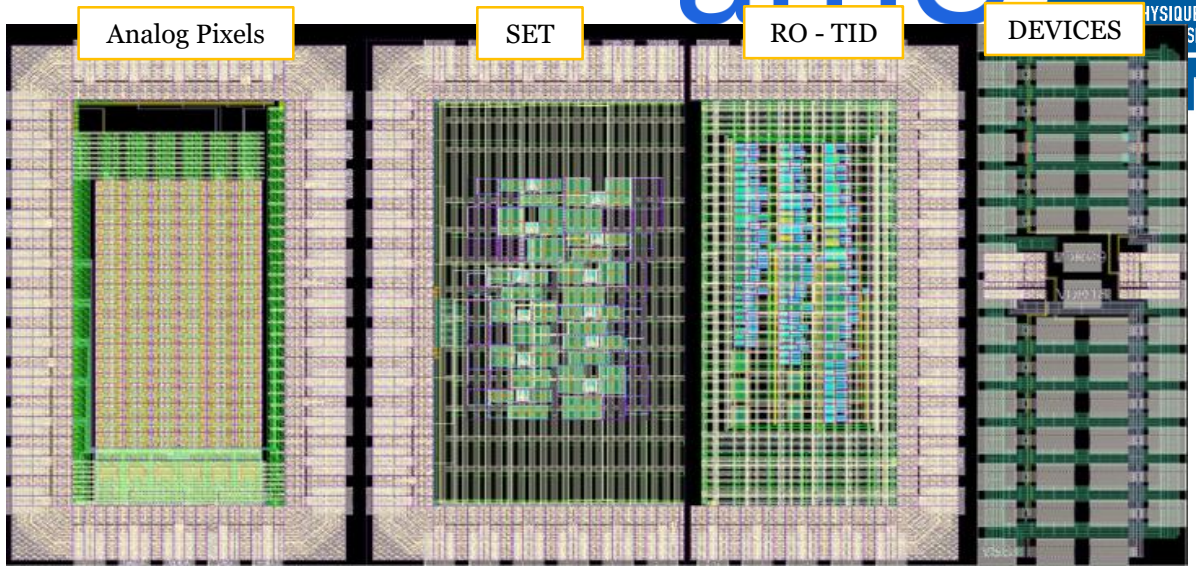
Architecture (Designs for reference):

- Front-end:
  - ALPIDE : port from 180nm to 65nm
  - **MOSAIX FE: from ALICE ITS3**
  - CSA FE 65nm
  - DPTS FE 65nm
- **Asynchronous Readout Architecture**
  - 1 readout logic: ALPIDE / Double-column: MIMOSIS
  - **Pixel grouping**
  - 1+1 readout logic / matrix (~MOSS)
  - **SPARC prototype**
- Serializer : from async to sync
- **End-of-Column**
- MAPS design: DESY
- Chip Monitoring …

TSMC 28nm

TSMC 28nm activity

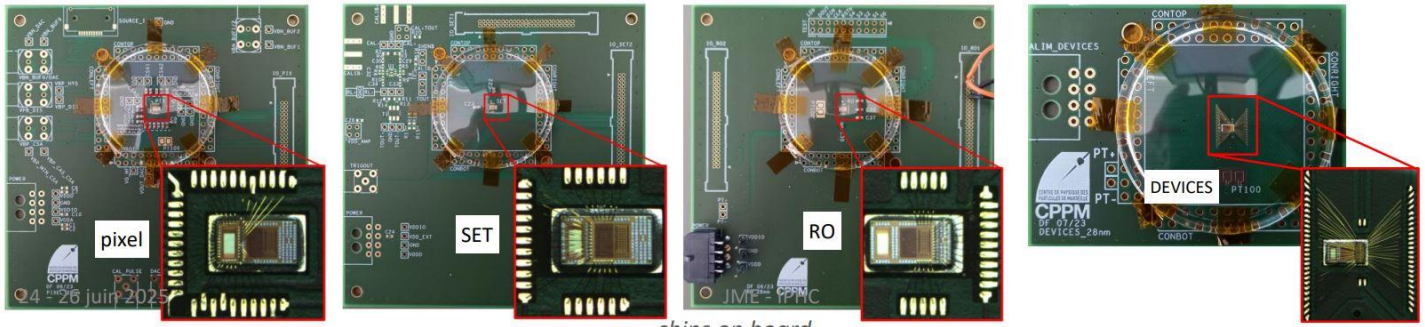
- Done **with the CERN R&D Program** on technologies for Future Experiments
- **CPPM is a member of two working groups within the DRD** (ECFA) projects: WG 7.3a & WG 7.4b
- **For future upgrades and future colliders**
- **Higher requirements**:
  - Time resolution,
  - High hit rate,
  - Larger data links,
  - Small pixel size, etc
  - New technologies need to be applied



4 sub-chips of 2×1 mm² submitted December 22

Implemented Structures:

- **Pixel_28nm**
- **RO_28nm**
- **SET_28nm**
- **DEVICES_28nm**
- **Each chip is bonded on its own board (ball bonding)**



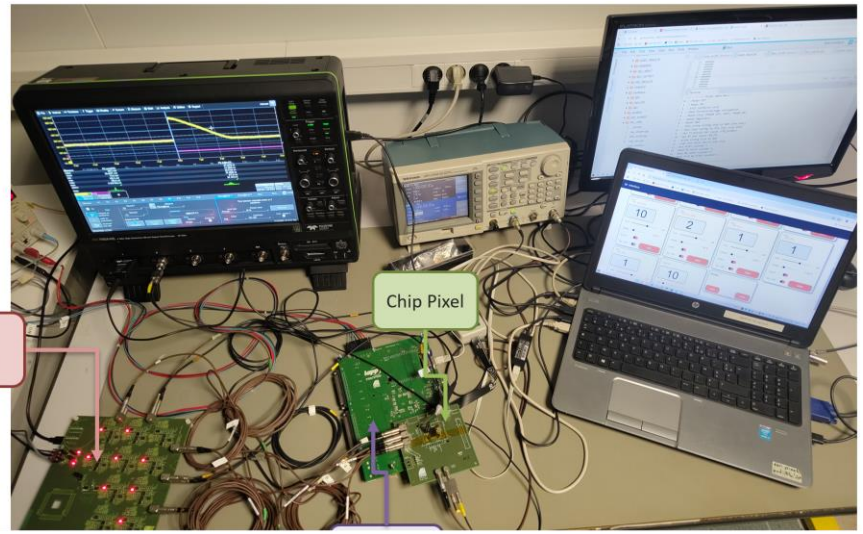
chips on board

The 28nm prototype was received in June, 2023

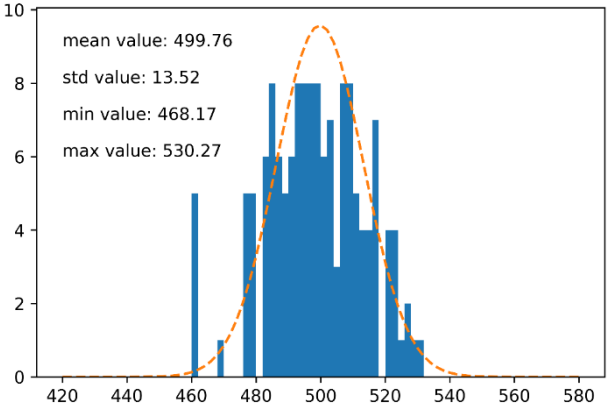
Test results for 28nm

Pixel_28nm

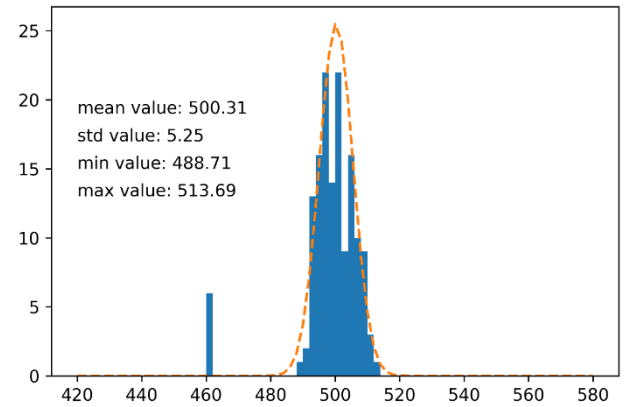
- Process qualification in terms of performance for analog, low power and low noise circuits
- **Goals of this pixel matrix design**
  - Study the limits to time resolution in analog front
  - Bandwidth, Noise, Current bias, power supply
- Threshold scan and tuning
  - CSA base line ~ 300 mV
  - After tuning : RMS value = 130 e^- -> 52 e^-
- Noise and time resolution measurement



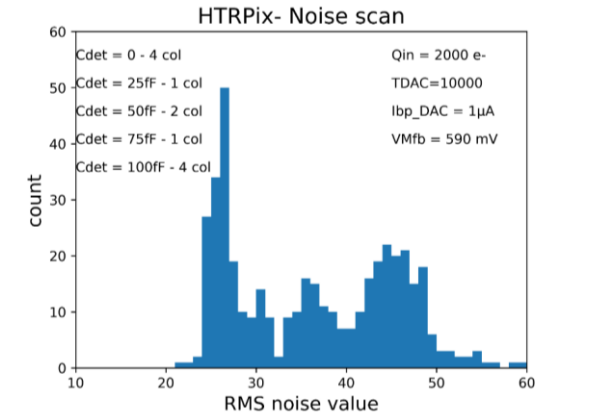
Pixel test bench



Before tuning



After tuning



•charge	•Jitter (simulated)	•Jitter (measured)
•Q > 4 ke-	•< 100 ps	•< 150 ps(*)
•Q > 10 ke-	•< 50ps	•< 100 ps(*)

Test Results for Pixel_28nm

SET_28nm

- 2 different parts in the SET chip: Target cells & Width measurement
- Same architecture used in the RD53_SEU chip
- Need a beam time (3 ~ 4 hours), test bench is ready now
- **Goal: define a time width to mask on sensitive nodes**

Test results for 28nm

RO_28nm

- **Goal: For TID effect Study of Digital Technology Cells**
- INV, NAND, NOR, and DELAY are implemented
- Bug on enable management: can't test it in static mode
- Each cell is connected to its proper counter

Time Propagation

Measurements on 10 chips

All digital cells: propagation time 5~20 ps

12T more faster than 7T (SVT)

VDD variation

Measurements on 1 chip

HVT cells more sensitive than LVT

7T cells show a VDD dependence higher than 12T

Test objects:

Cell Size 7T / 9T / 12T

Flavours SVT / HVT / LVT

Temperature variation

Measurements on 1 chip

Temp setting : -20 ~+50°C (step of 5 °C)

LVT cells show a higher variation

No difference between size

TID measurements

Measurements on 1 chip

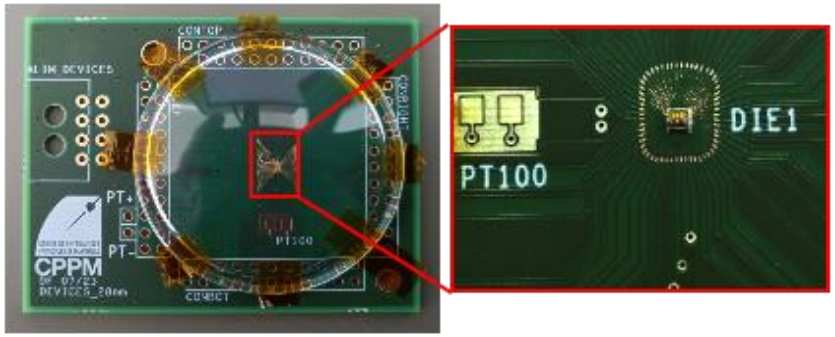
10 keV X-ray source calibrated with a PIN diode

HVT cells are more sensitive than others

Redo TID tests in 2025 on another chip

DEVICES_28nm

- **Goal: automatic extraction of transistors parameters for each channel valid**
- Transistors test bench includes:
  - 4 SMU's (Keithley - 4201+PA)
  - 4 switches matrix boards (Keithley-7174A)
- Devices implemented on the chip without ESD protections
- **New test just started from July, 2025**
- **28 chips will be tested**



Conclusions

- The CPPM team works on hybrid pixel technologies, either for the ATLAS ITk project (RD53), the upgrade of BeIIe II proposal (TJ 180nm) or in R&D for future colliders in TPSCo 65 nm & TSMC 28 nm
- Beautiful developments have occurred in Depleted MAPS technologies **in CPPM**, with prototypes produced in 10 different technologies
- CPPM is now focusing on TJ 180nm, TPSCo 65nm and TSMC 28nm
- Good developments and progress made by the CPPM group and others on **DRD3.1, DRD7.6, TPSCo 65 nm**
- Obtained good results by the CPPM group and others **in TSMC 28nm**
- **CPPM has always had very close cooperation with China. Exchange activities were resumed in 2024, and there will be more cooperation plans in the future**
- **The IHEP, SDU and CPPM have a very strong collaboration since many years, on ATLAS developments and R&D for future projects (FCC, CEPC, DRD7…)**

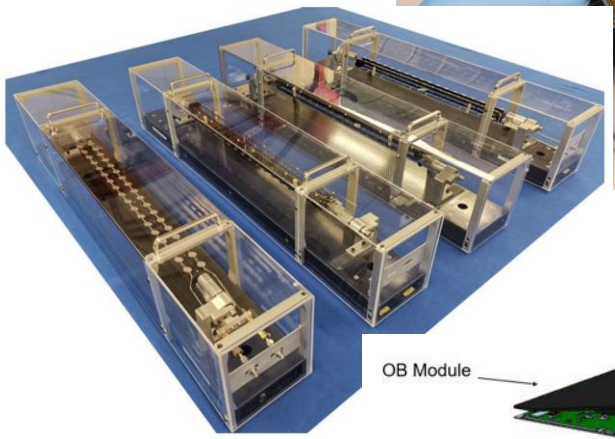
Thanks for your attention

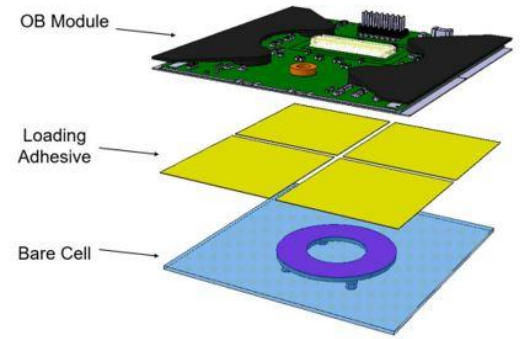
Back up slides

ATLAS and ITk detector

Mechanical activities at CPPM

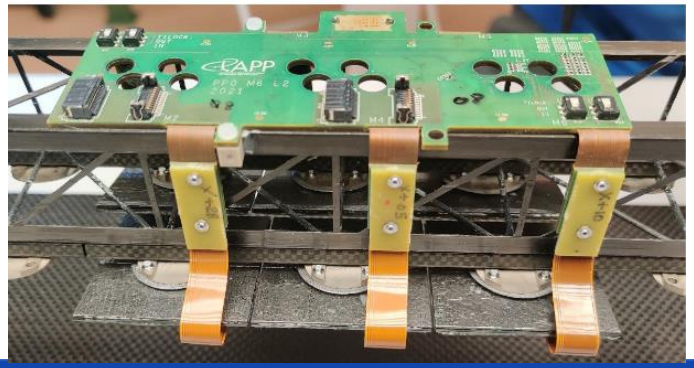
- CPPM is involved in:
  - **Designing and procuring the multipurpose tool called Handling frame**. This tool is used to handle local support all along the assembly and testing phase of the project to safe the operation and secure these fragile object up to the final integration at CERN
  - **Designing tool and qualifying the cell loading process**. This consists to define the glue deposition process and the module accurate loading on cell
  - **Designing and defining the cell integration on local support process.** This consists to set the services (pigtail and Patch panel) integration and connection, loaded cell integration into the local support
  - **Setting the testing facilities for single module at reception and loaded local support prior** to delivery to CERN





[1] A modified version developed in Japan combines 'Module Assembly' and 'Cell Loading' in a single step

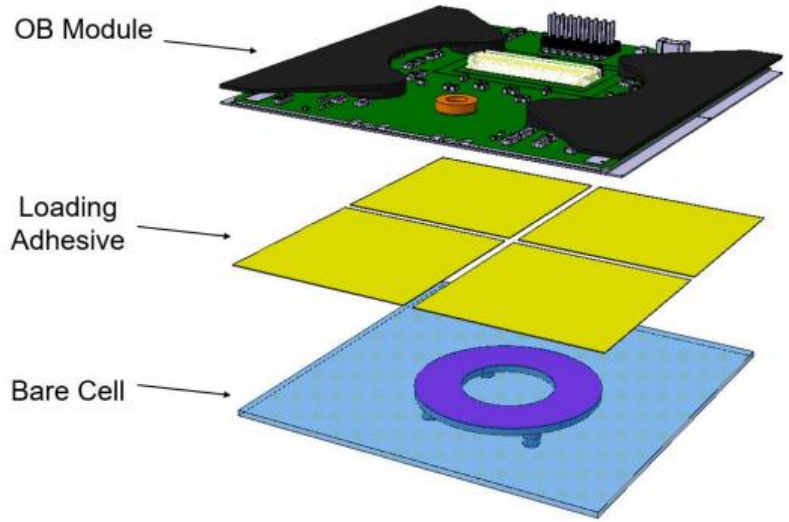
- **Outer barrel assembly and integration** will be split in 6 sites, CPPM will be one of them (~ 1500 modules to handle)→ **setting a clean room** (dust and humidity control, ESD protections, temperature control)dedicated for all construction operations
- On **local support** we will be involved in all metrological QC control of local support and procurement of the micro screws used to fix cell on local support
- CPPM is **in charge of designing the service trolley used to pack all services before ITK pixel insertion inside the strips detector**



Outer Barrel: Module Loading – Two Step Process

1. Cell Loading [1]

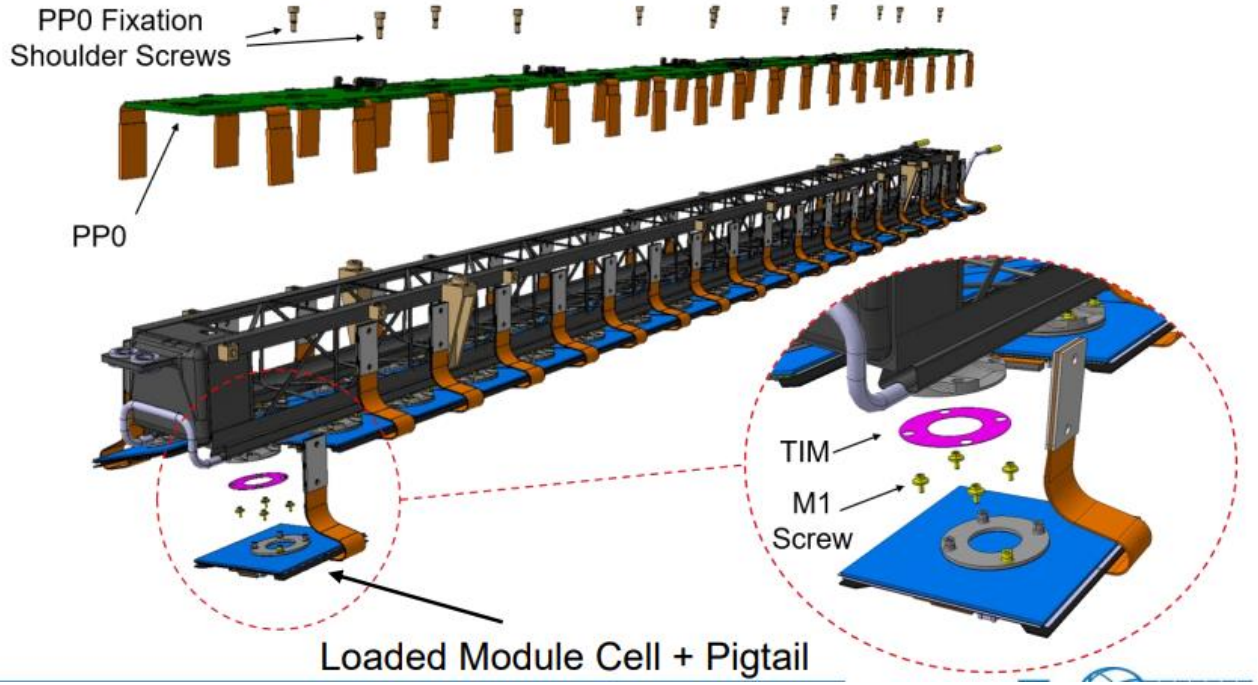
1.1 Installation of Bare Cell on loading tooling
1.2 Glue deposition
1.3 Module pick-up & placement on cell
1.4 QC testing of Loaded Cells



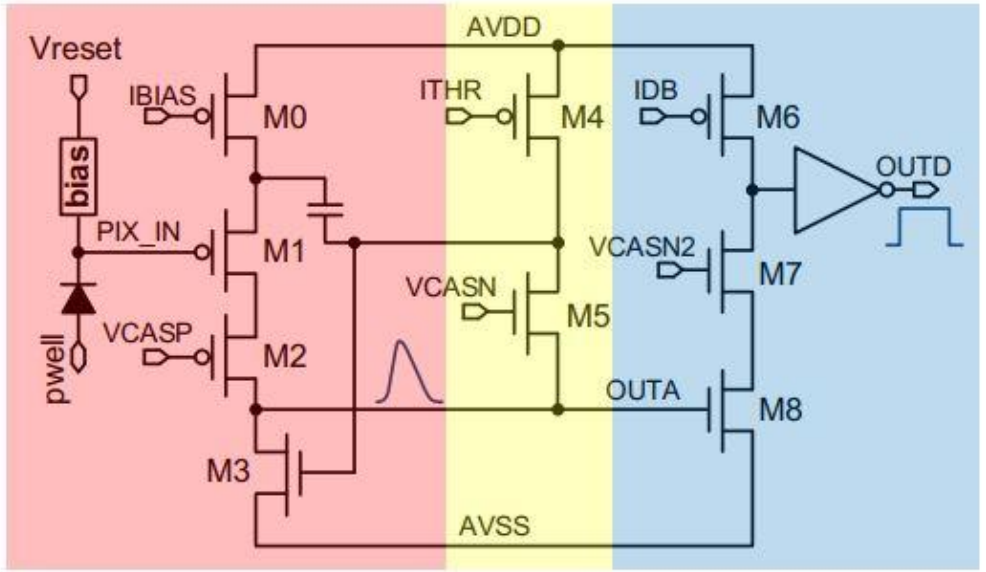
[1] A modified version developed in Japan combines 'Module Assembly' and 'Cell Loading' in a single step

2. Cell Integration

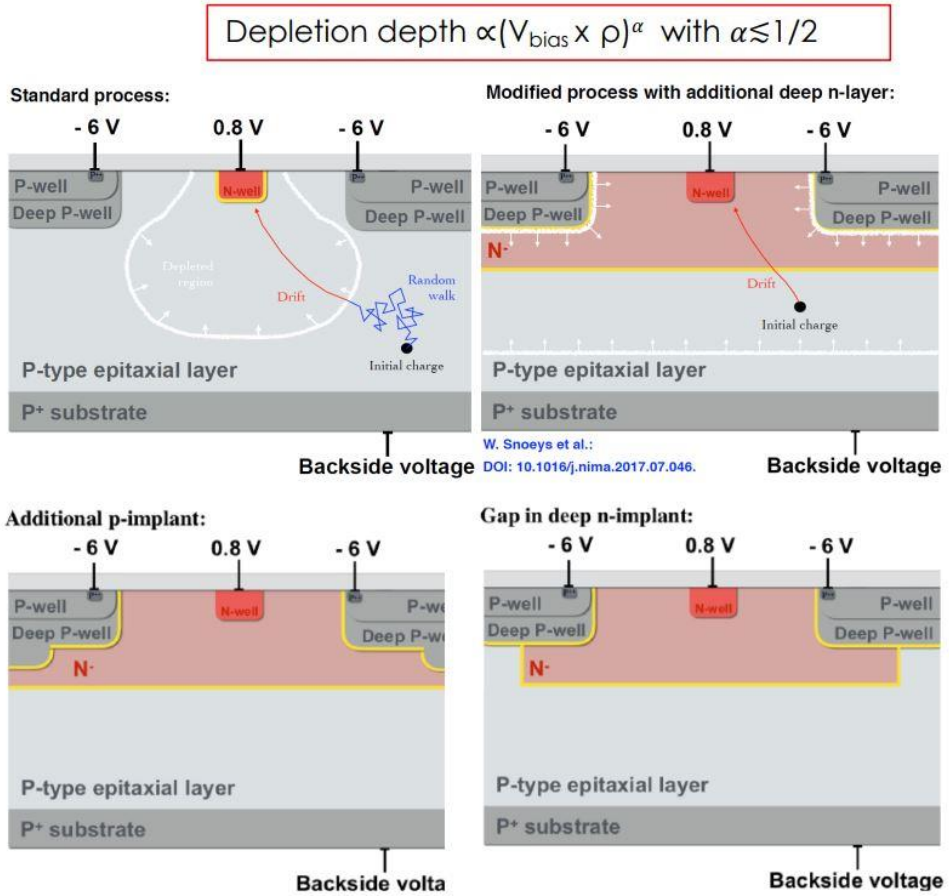
2.1 Installation of pre-bent module pigtails on Module Cells
2.2 Mounting loaded cells on the functional local support
2.3 Installation of PP0s
2.4 Module-Type-0 Connections
2.5 QC Testing of Loaded Longeron/IHR



Technology choice TJ180nm

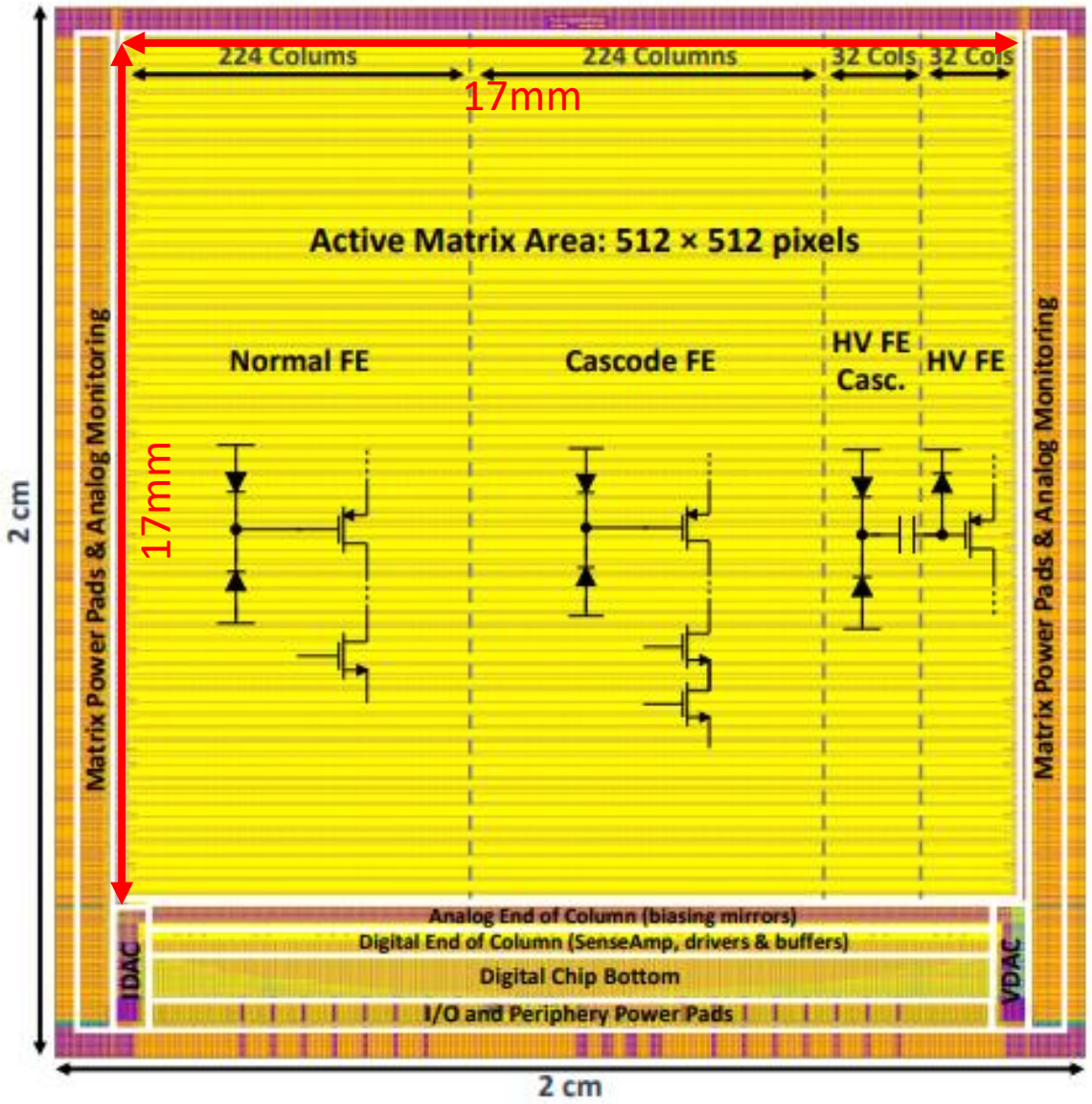


- Depleted MAPS in Tower Jazz 180nm technology.
- Large expertise in the community and many projects
- CMOS pixel sensor + electronics in same silicon die



- Small electrode concept:
  capacitance, power, Tpeak, large conversion factor
- Modified process: higher radiation tolerance

TJ-Monopix2 – pixel matrix



- 4 pixel Front-End (FE) flavors with differences in pre-amplifier, sensor coupling and biasing ;
- - Normal FE => Col_0 to Col_223

  improved TJ-Monopix I FE, DC coupled pixels
- - Cascode FE => Col_224 to Col_447

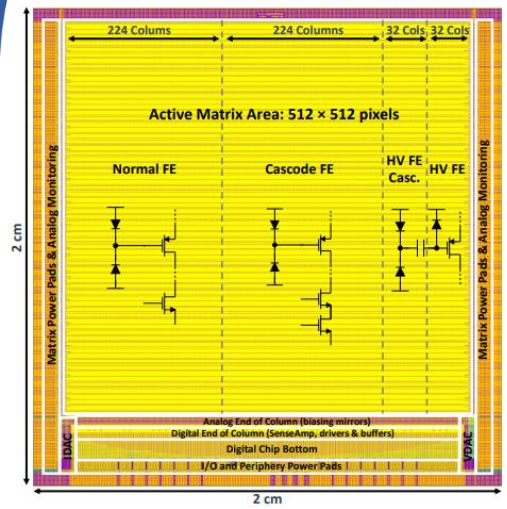
  Extra cascode transistor that increase the pre-amplifier gain, the aim is to have 50% reduction of threshold dispersion, DC coupled pixel
- - HV Cascode FE => Col_448 to Col_479

  Front side High Voltage biasing and AC coupled pixel
- - HV FE => Col_480 to Col_511

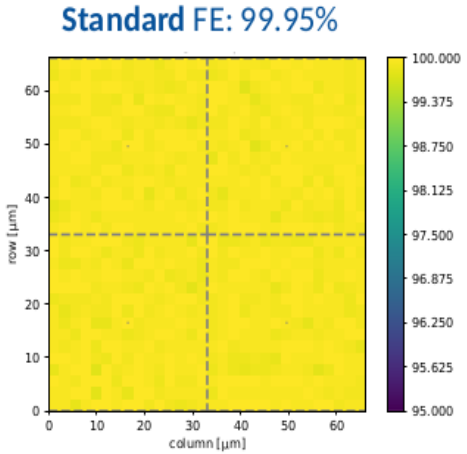
  Front side High Voltage biasing and AC coupled pixel

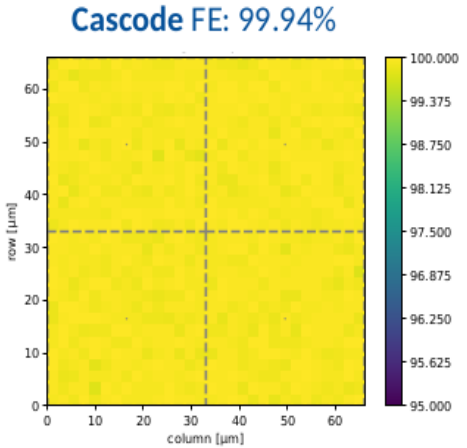
  a variation of the previous one
- Two columns for Analog Monitoring

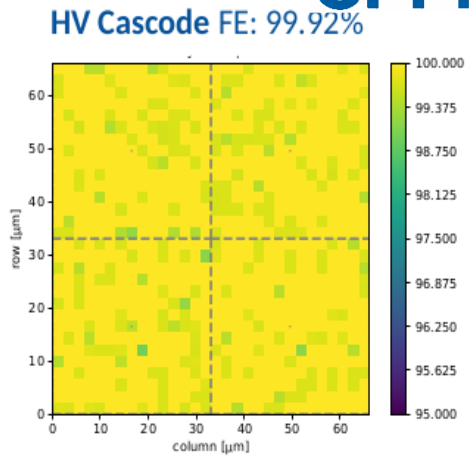
TJ180 TJ-Monopix2



- 2×2 cm², 512×512 p
- Work on implants fo
- Submitted 2021 , 2r
- Low threshold, sma
- Test done in Bonn/F
- Characterization lab
  - Threshold Scan v
  - Dispersion & Average Noise ENC
  - Beam test@DESY

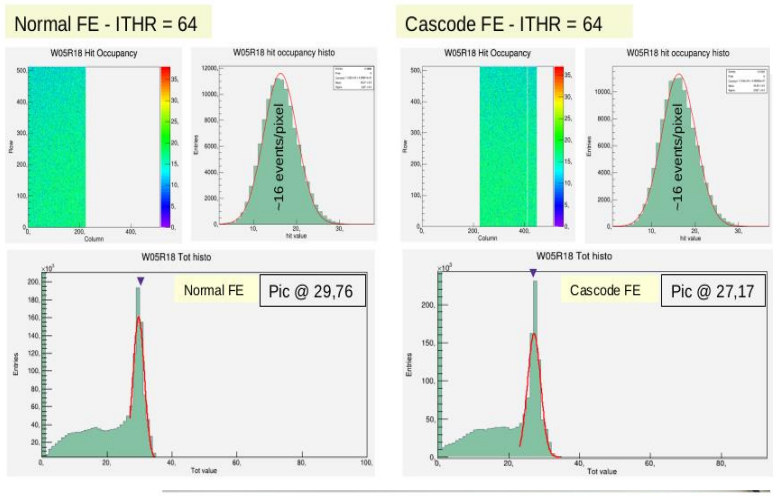






Test with a source Fe55

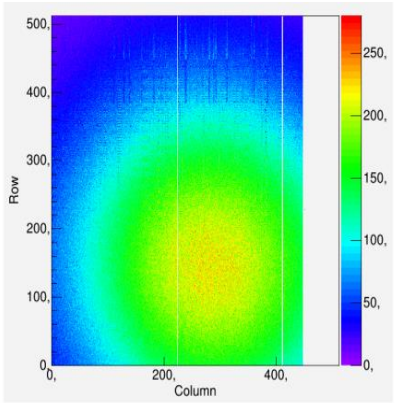
ToT Histo shows the peak energy of 6 kev



Mapping with Fe55

Source at 5cm

Exposure time 20 min



Typical characterization test results:

- Tuned threshold ~250 e- (σ ~10 e-)
- Noise < 10 e-

Beam test results :

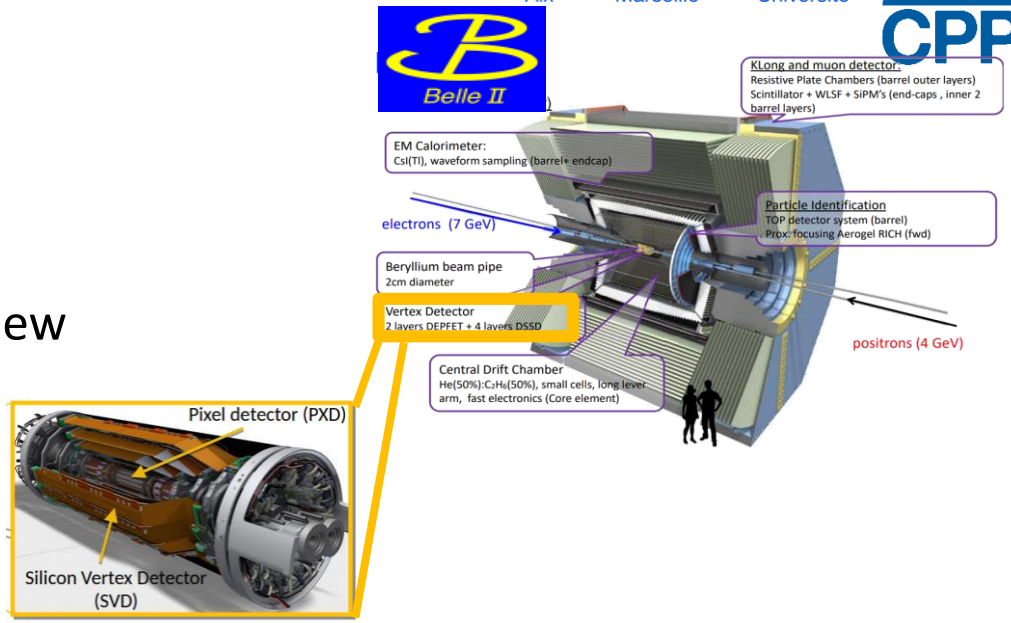
- Excellent hit detection in test beam (> 99.9%)
- Nearly 98% of hits in 25ns

Development: TJ-Monopix2 prototype -- on which **the OBELIX design for the Belle-II vertex detector upgrade project** is based

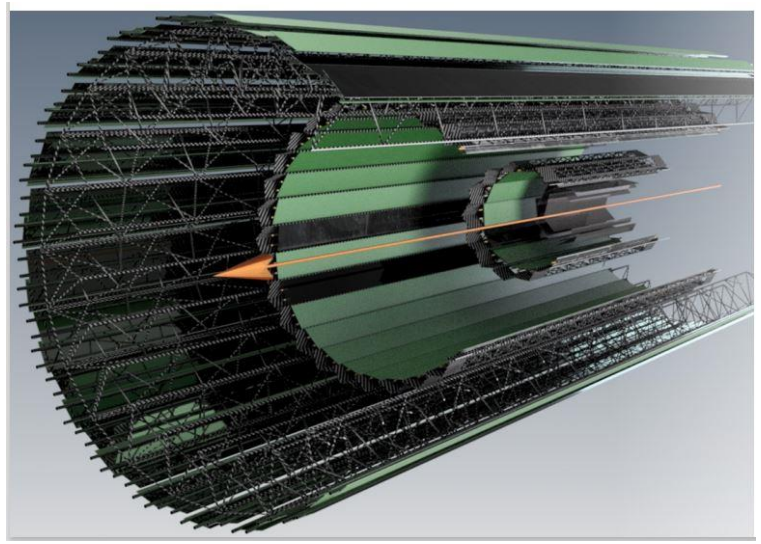
Belle II

Goal of the upgrade for Belle II:

- Cope with the higher luminosity provided by the SuperKEKB accelerator
- Be more robust against high background and match possible new interaction region

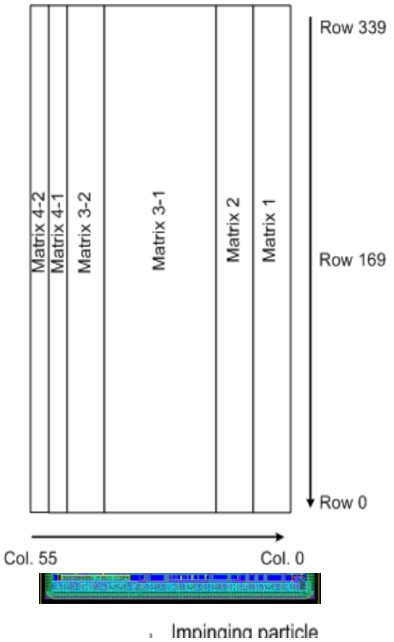


- A new fully pixelated CMOS detector to replace current VXD
- The VTX upgrade proposal
- Improved tracking resolution and space-time granuarity
- Reduced material budget less than 2%X0 instead of 3.8%X0
- 6 straight layers with **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors (DMAPS) process, 2 inner layers, 4 outer layers (???)



- Intend upgrade during Long Shutdown 2 (2032 or later)

LF150 LF-Monopix2



2×1 cm², 340×56 pixels, 50×150 µm²

6 sub-matrix
- 3 variants of CSA
- 2 Feedback Capacity values
- 2 variants of Discriminator
- 2 kinds of Logic Reset

Fast Col readout

Seuil mini :

	Vth (V)	Min thres e-	disp e-	ENC e-	bad pixel	% bad pixel
SubArray_1	0,775	1520	81	143	17/2720	0.625
SubArray_2	0,777	1437	113	127	21/2720	0.772
SubArray_3.1	0,744	1113	74	113	38/8160	0.466
SubArray_3.2	0,743	1048	72	110	15/2720	0.551
SubArray_4.1	0,768	1881	170	138	10/1360	0.735
SubArray_4.2	0,779	1611	92	136	8/1360	0.588

- Dispersion
- Medium noise

Testing with an Fe55 source

TDACs tuning :

	No tuned – TDACs = 7			Tuned		
	Vth	mean thres	disp	ENC	mean thres	disp	ENC
SubArray_1	0,79	1922	356	150	2032	62	139
SubArray_2	0,78	1969	435	137	2035	86	123
SubArray_3.1	0,76	2339	711	110	2119	85	110
SubArray_3.2	0,76	2313	707	110	2124	82	107
SubArray_4.1	0,77	2428	784	148	2077	158	138
SubArray_4.2	0,79	2184	398	148	2061	72	132

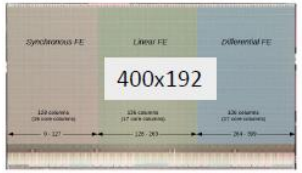
Test

- **TDACS tuning** : Apart from sub-matrix 4.1, the threshold dispersion after a TDACs tuning is between 62 and 86e-, required value 80e-. The ENC noise value is between 107 and 139 e- for all submatrix, required value between 100 and 150 e-
- **Mini threshold:** Sub-matrix 3.1 and 3.2 give the best performance in Mini threshold term, structure with CSA V1, Feedback cap 5fF, Discri Unidir

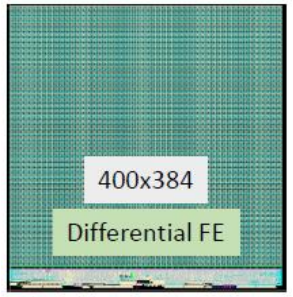
Conclusion: The performance of the technology is very **positive** (noise, threshold, radiation resistance), but a clear application has not been demonstrated for this moment -- work for the moment in the process of being finalized (then probably put on standby)

RD53 Projects

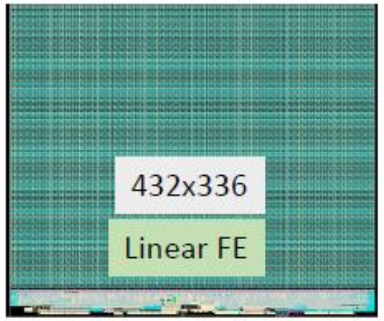
- **RD53 collaboration** was established to design and develop pixel chips for **ATLAS/CMS phase 2 upgrades**
- The RD53 project includes 24 institutes - ~20 designers
- **Extremely challenging requirements for HL-LHC**
  - **Hit rates**: 3 GHz/cm², Small pixels: 50 x 50 µm²
  - **Radiation**: **500 Mrad** - 10^{16} neq/cm² over 5 years
- Technology: **TSMC 65nm CMOS**



RD53A
Size: 20 x 11.5 mm²
submitted in August 2017



RD53B-ATLAS (ITkPix-V1)
size: 20 x 21 mm²
Submitted in March 2020

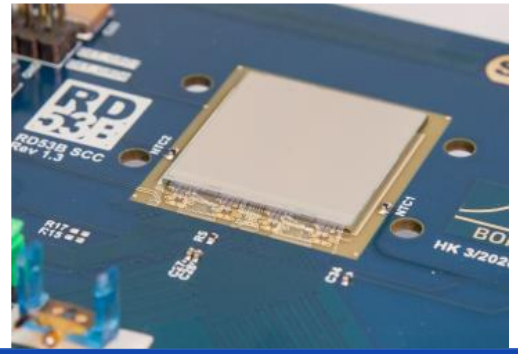


RD53B-CMS (CROC-V1)
size: 21.6 x 18.6 mm²
Submitted in May 2021

RD53C-ATLAS (ITkPix-V2)
Submitted in March 2023

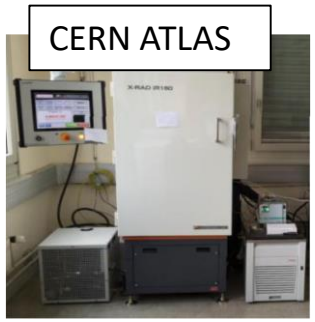
RD53C-CMS (CROC-V2)
size: 21.6 x 18.6 mm²
Submitted in Sept 2023

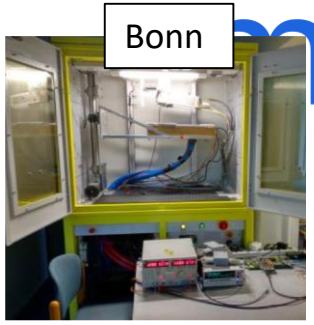
- Characterization of the TSMC 65nm process in radiat
- **Several prototypes to qualify IP blocs (Analog FE, ADC, DAC, CDR/PLL, ShuntLDO …)**
- **RD53A chip,** Large-scale demonstrator with 3 FE flavors, Submitted in August 2017 and tested in an intensive way
- **ATLAS and CMS chips** are two instances of **the same common design**, having different sizes and different Analog Front-End
- **RD53B chip (preproduction)**
  - ITkPix-V1 (ATLAS chip) submitted in March 2020
  - CROC-V1 (CMS chip) submitted in May 2021
- **RD53C chip (Production)**
  - ITkPix-V2 (ATLAS chip) received in July 2023 and is still under tests and characterization
  - CROC-V2 (CMS chip) is submitted in September 2023

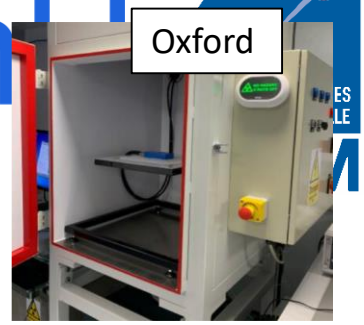


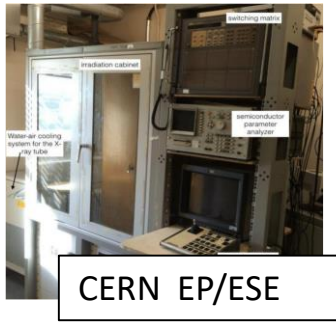
RD53 TID test

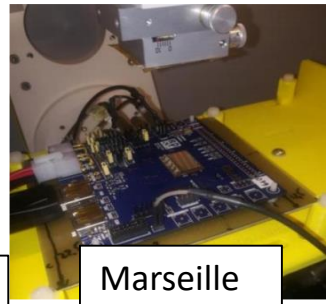
- Extensive radiation campaigns (since 2015) have been carried out to test and qualify
- **Rules followed in RD53 chip**
  - Avoid minimum size digital cells and use large area devices for the analog
  - RD53 chips are designed to meet specifications at 500 Mrad when operating at low temperature (-15 °C)
  - The chip should be maintained powered off during shut down (room temperature)
- RD53 collaboration treats radiation damage as one of the IC design corners
- Multiple irradiation campaigns for the RD53A/B chip were done at low temperature (-10 to -20 °C)
- **IJCLab-CPPM collaboration for the ITkPixV1 TID testing at low temperature**

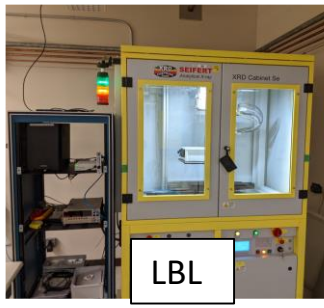


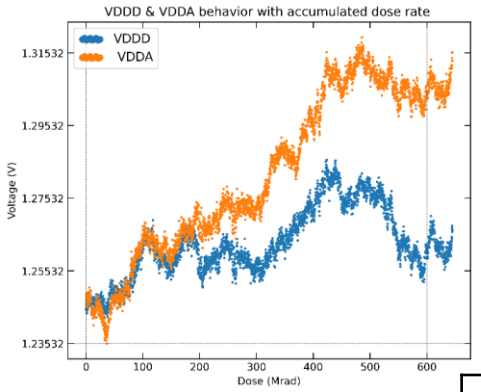


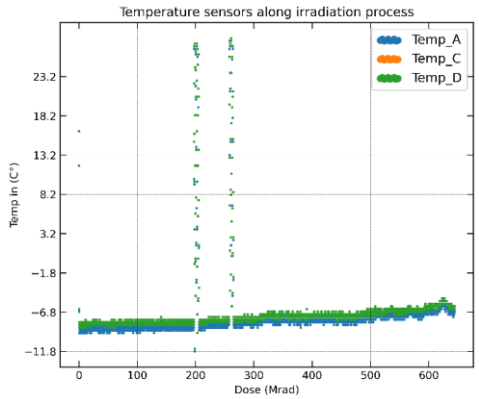


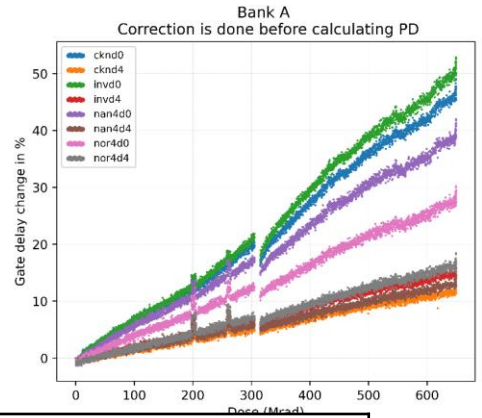












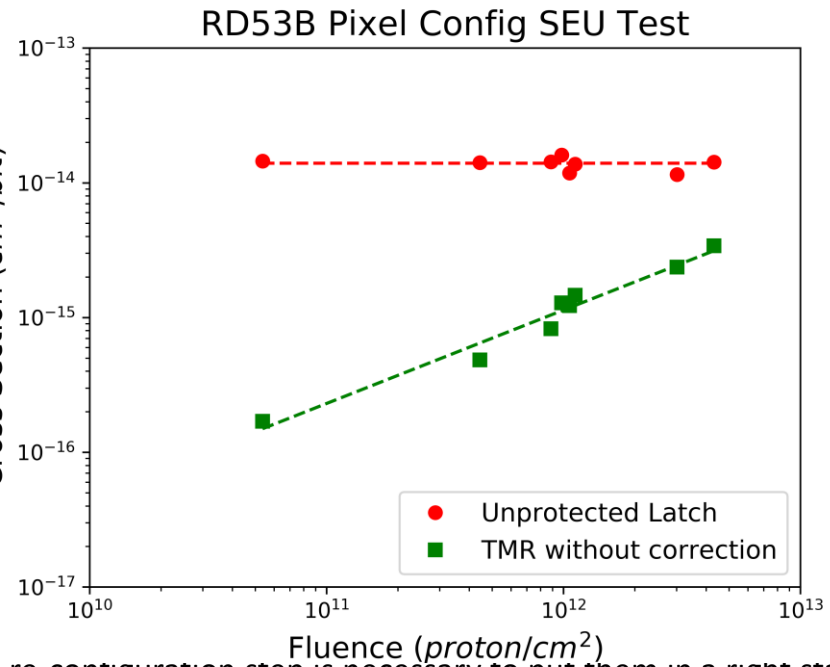
Ring Oscillator	650 Mrad
cknd 0	42 %
cknd 4	12 %
invd 0	45 %
invd 4	16 %
nand4d0	36 %
nand4d4	15 %
nor4d0	28%
nor4d4	18 %

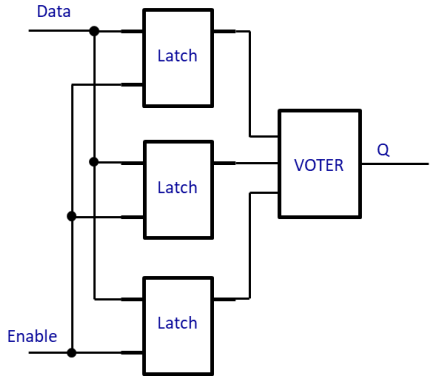
- The TID tests were conducted in strong collaboration IJCLab/CPPM
- **On chip Ring Oscillators**
  - Designed by IJCLab and used intensively for dose monitoring
  - Absolute VDDD correction applied using Freq vs VDDD slopes
  - Increase for strength 0 gates up to 45%
    - Not used in the chip
  - Increase for strength 4 up to 28%
- **The results obtained are compatible with those obtained by other institutes**

RD53 SEU configuration & test

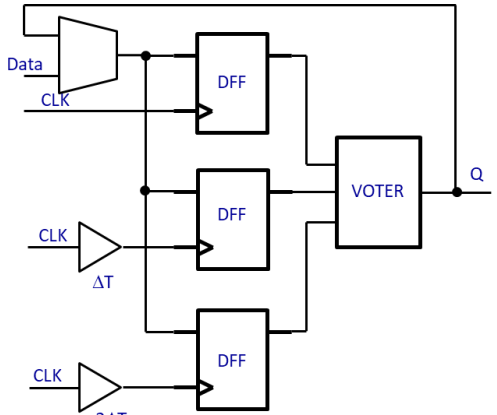
Chip Conf

- **Pixel c**
  -
  -
  -
  -
- **Global**
  -
  -
  -
- The co
  - A re-configuration step is necessary to put them in a right state





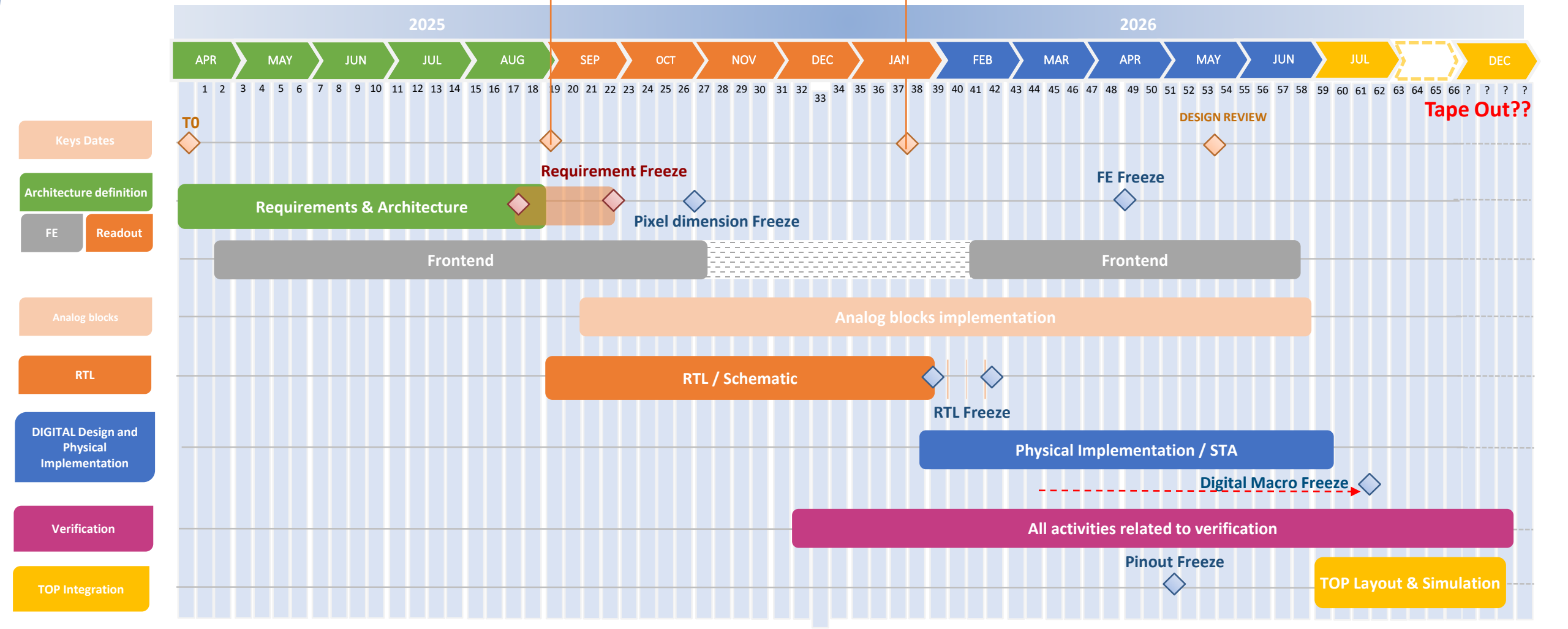
TMR latch without correction



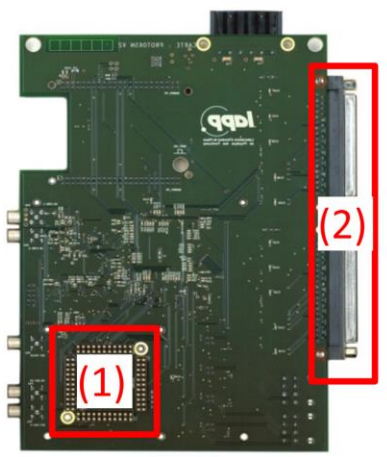
TMR with correction

- **Pixel memory size** : 8 bits per pixel -> 1.28 Mbit per FE chip
  - Unprotected latch used for 2 bits & TMR without correction used for 6 bits
- **Unprotected latch** cross section $\sigma = 1.5 \times 10^{-14}$ cm²
- **Pixel TMR latch** cross section increases with the fluence because of errors accumulation
  - **The TMR is 100 times** tolerant than the unprotected latch **for low proton fluence** (~5×10^{10} p/cm²) ,
  - **TMR is only 10 times** tolerant than the unprotected latch **for moderate proton fluence** (~1.0×10^{12} p/cm²)
  - TMR without correction is useful when considering a **regular external re-configuration**
- **Global configuration** : ~3 Kbit in total where a half is reserved only for tests
  - TMR with correction
  - $\sigma = 3.6 \times 10^{-17}$ cm²
  - The tolerance is **improved** by a **factor 400**

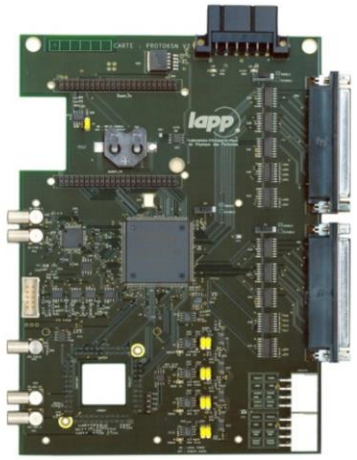
- **Tests were done with**
  - **CDR mode** : serializer and command clocks are provided by on-chip CDR
  - **Bypass mode** : both clocks are provided externally
- In PLL mode, **synchronization issues** with the BDAQ readout system have been identified

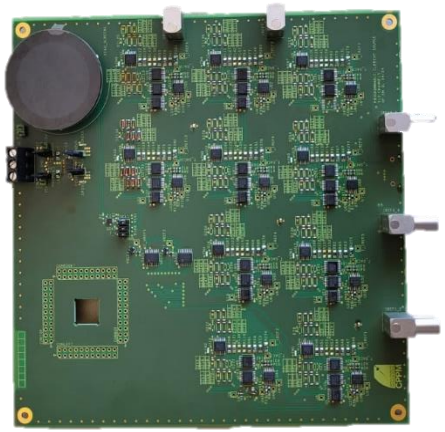

Architecture Review
Internal Design Review
2025
2026
APR MAY JUN JUL AUG SEP OCT NOV DEC JAN FEB MAR APR MAY JUN JUL DEC
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 ? ? ? ?
Tape Out??
T0
DESIGN REVIEW
Requirement Freeze
FE Freeze
Pixel dimension Freeze
Requirements & Architecture
Frontend
Frontend
Analog blocks implementation
RTL / Schematic
RTL Freeze
Physical Implementation / STA
Digital Macro Freeze
All activities related to verification
Pinout Freeze
TOP Layout & Simulation
Keys Dates
Architecture definition
FE
Readout
Analog blocks
RTL
DIGITAL Design and Physical Implementation
Verification
TOP Integration

DAQ boards for 28nm

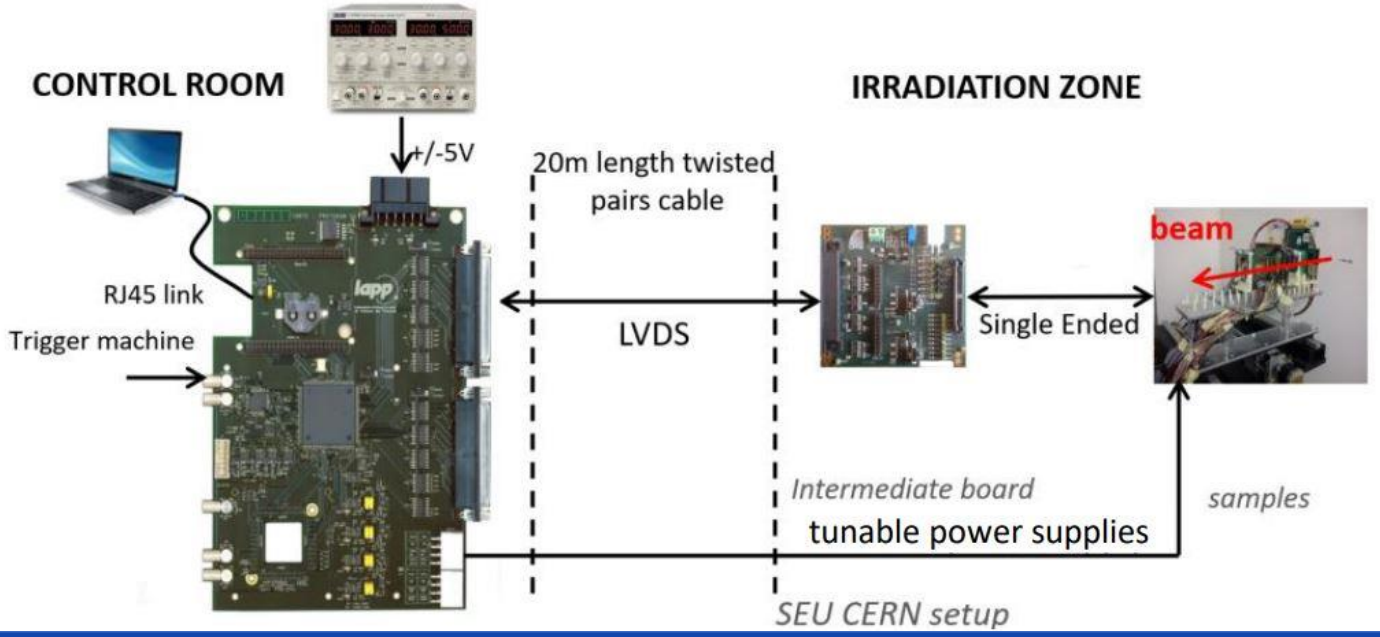


DAQ board



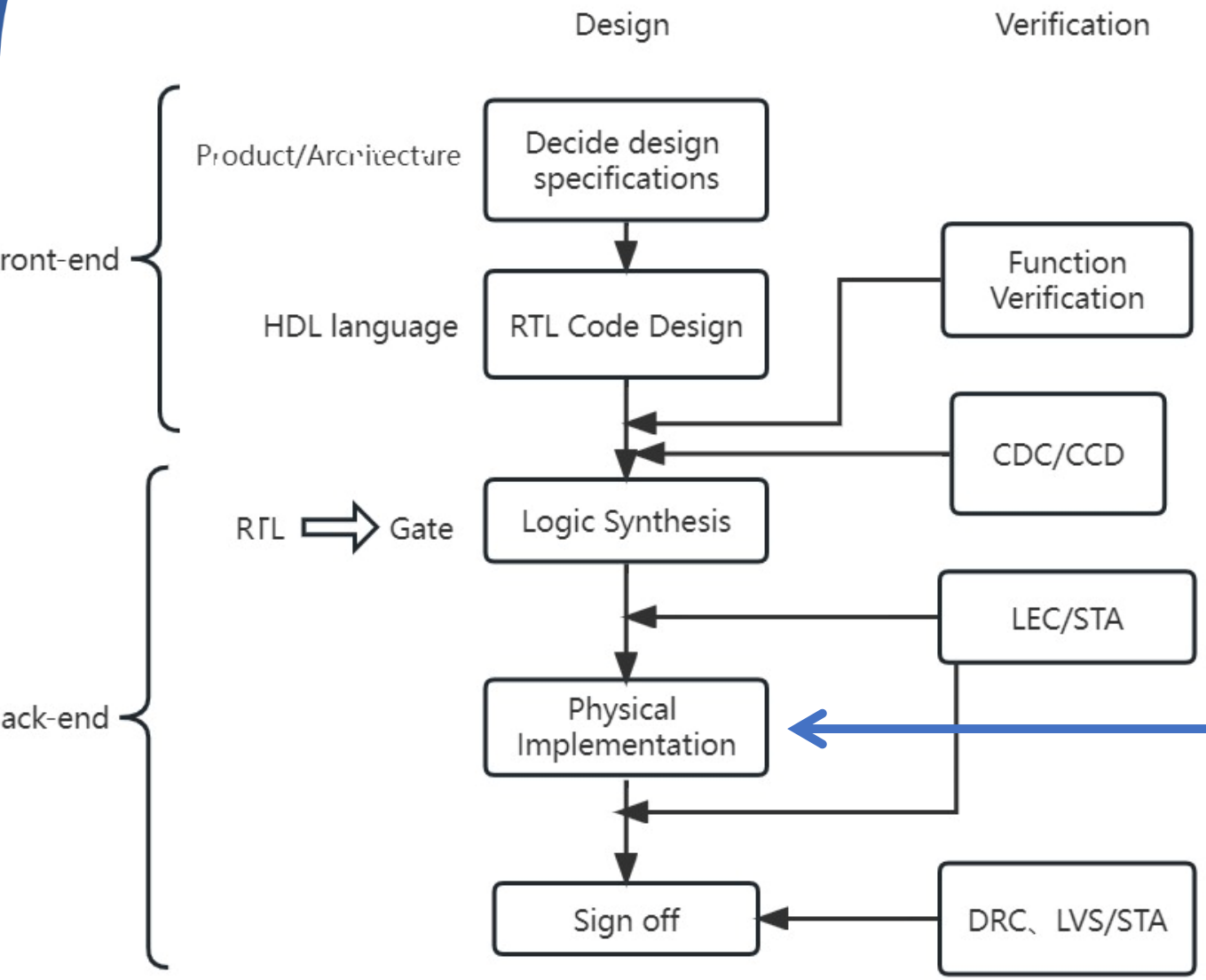


Current source board



- **DAQ board features:**
  - nanoPC BeagleBone card
  - FPGA (cyclone III – Quartus 13.1)
  - Digital signals available
    - 40TTL dignals (local mode (1))
    - 32 LVDS signals (remote mode (2))
  - Analog channels available
  - Monitoring (°C, current supply)
  - Charge injector
  - Lab tests
  - Compatible with irradiation tests
- **Current sources board features:**
  - Based on an AOP architecture (low offset, rail to rail)
  - 10 sources were implemented on an evaluation board
  - Voltage-controlled sources (12b DAC)
  - ± 1nA ↔ ± 2mA
  - Sources management thanks to an ESP32
  - user interface designed with the Node-RED framework

ASIC Digital Design Flow Method



- **General ASIC design flow**
- **Ensure design specifications**
- **RTL Code Design** : SystemVerilog, Verilog, VHDL, etc
- **Logic synthesis**: Convert logic circuits to gate-level circuits, Genus
- **Placement & Routage:** Convert ideal circuits into real production circuit designs, Innovus
- **Signoff**
- **General ASIC verification flow**
- **Logical verification**: simulation, xcelium / questa
- **CCD/CDC**: constraint check for syn , clock domain check for rtl
- **Static Timing Analysis** : check timing violation, tempus
- **LEC check**: verify design consistency, conformal
- **DRC, LVS**: design rule check & layout versus schematic, Innovus
- **Verification:** post-simulation, verification, UVM

We are now in this step !
The OBELIX design is supposed to be submitted in Q4 2023 / Q1 2024