Common R&D efforts on CMOS pixel detector system for the experiment of electron-positron colliders

16th FCPPN/L Workshop, 21 – 25 July 2025, Qingdao

Yunpeng Lu

on behalf of the FCPPN/L collaboration teams

French Groups: IPHC/IN2P3, *Jérôme BAUDOT, Christine Hu-Guo, ...*
CPPM/IN2P3, *Marlon Barbero, …*
Chinese Groups: IHEP/CAS, *Qun OUYANG, Yunpeng Lu, …*
USTC*, Lailin Xu, …*
Jilin University*, Weimin Song, …*

Outline

- Introduction
  - Overview of collaboration

- BELLE II VTX upgrade proposal
  - Backend electronics and TDAQ system

- R&D for CEPC vertex detector
  - Large area sensor design JadePix-5

- Summary

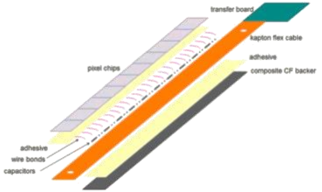
*Monolithic Active Pixel Sensor, or CMOS Pixel Sensor are used interchangeably in this talk without distinction

Overview of collaboration

- Starting from 2010, common R&D efforts of MAPS for the e^+e^- collider experiments: ***BES III upgrade, ILC/CEPC, BELLE II upgrade***

1、The prototype of CMOS pixel detector for the upgrade of BESIII-inner tracker

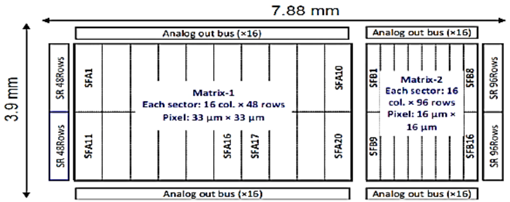
- ✓ Development of pixel detector ladder based on the MIMOSA28 sensors from IPHC
- ✓ common participation of beam test at DESY, to validate the ladder performance, space resolution, material budget, …

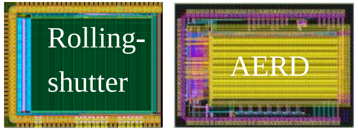


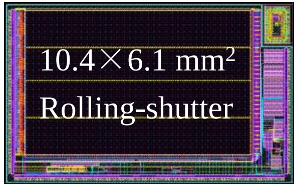
Ref.: *NIMA924(2019)287-292*, *NIMA986(2021)164810*

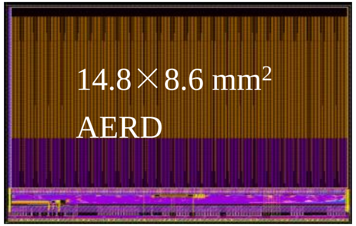
2、CMOS Pixel Sensors R&D for future $e^+ e^-$ colliders: *pixel sensor and double-sided ladder development*

Since 2015, **four engineering runs** have been shared with TJ 180 nm CIS process









2015: JadePix-1

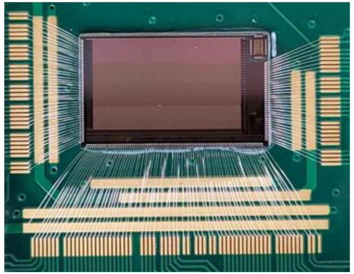
2017: JadePix-2/MIC4

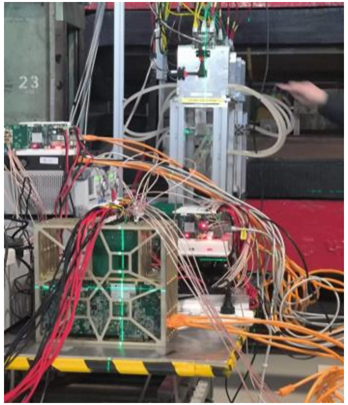
2020: JadePix-3

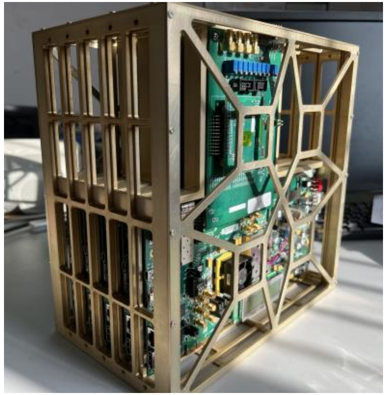
2022: JadePix-4/MIC5

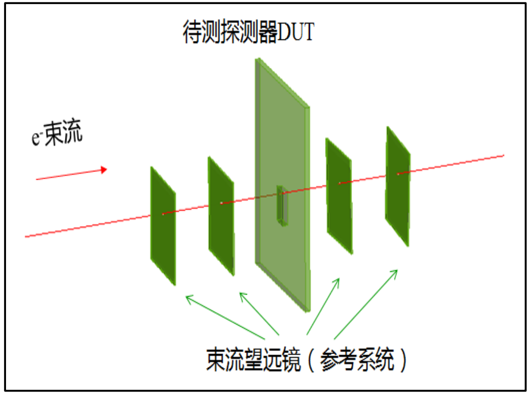
Development of CMOS Pixel Sensor JadePix-3

- JadePix-3 is a fully functional prototype chip with
  - Very compact in-pixel circuit, layout area 16 μm×23 μm
  - Low power consumption targeted on 50 mW/cm^2
- Designed by IHEP and collaborators in China
  - IHEP, CCNU, SDU, DLNU
- Extensive lab characterization and beam test
  - Electrical
  - Infrared Laser beam
  - Radiative source
  - High energy charged particle beam







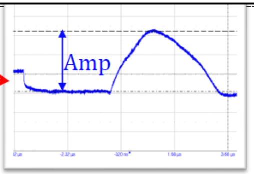


Reference:
- Design and characterisation of the JadePix-3 CMOS pixel sensor, *NIMA, 1048 (2023) 167967*
- Performance study of the JadePix-3 telescope from a beam test, *NIMA, 1065 (2024) 169551*

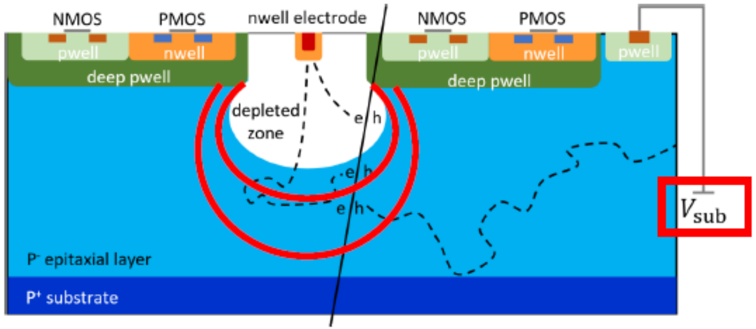
Extended collaboration among Chinese groups

- **Active participation in the JadePix-3 test study**
  - ✓ Common development of MAPS test system, used in several chip tests
  - ✓ Characterization of reverse-biased JadePix-3 sensor, research article submitted to NIMA
  - ✓ Analysis of beam test data, co-author of NIMA paper
  - ✓ 1 student graduated with master degree, “Performance Study of the JadePix-3 CMOS Pixel Detector Chip”

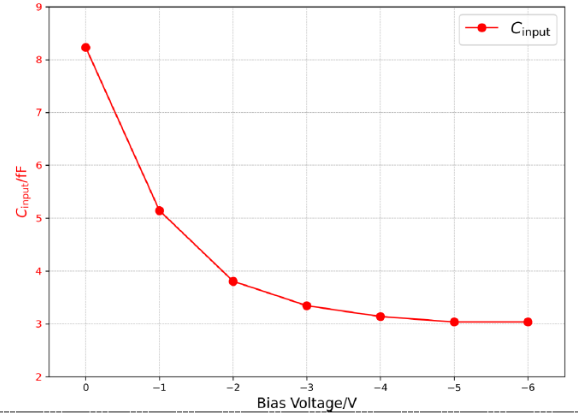
- Input Capacitance, C_{input} accessed by calculating analog response
- Smaller C_{input} increase voltage excursion and improves the SNR
- C_{input} reduced nearly **65%** as Bias Voltage increasing!



$$\mathrm{Amp} = \frac{Q_{inject}}{C_{\mathrm{input}}} \cdot f_{gain} \cdot f_{sf}$$



sensing diode of JadePix-3



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Physics program @ SuperKEKB with Belle II

- Thorough test of Std Model
- DIrect/indirect search for New Physics
- Hadronic Physics

} with billions of $B\bar{B}, c\bar{c}, \tau\bar{\tau}$ pairs
In "clean" environment of B-factory

⇒ The Belle II physics book
PTEP 12 (2019) 123C01

- Based on accumulation of 50 ab^{-1} of $e^{+}+e^{-}$ at $\sqrt{s} = M_{Y(4S)}$
  – requires instantaneous luminosity close to $6x10^{35}$ $cm^{-2}.s^{-1}$

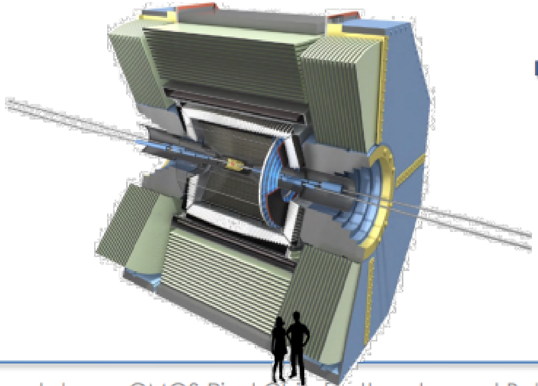
⇒ SuperKEKB collider implementing the nano-beam scheme @ high currents

⇓

High collision rate   High beam-induced bkg

The Belle II experiment

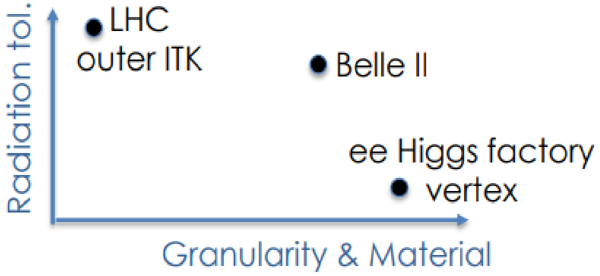
- "classical" B-factory detector + enhanced features



The vertex detector (VXD)

- Better vertexing ← lower boost
  Smarter tracking ← higher hit rate

+ Harsher radiation environment
+ Belle II trigger rate ~ 30 KHz



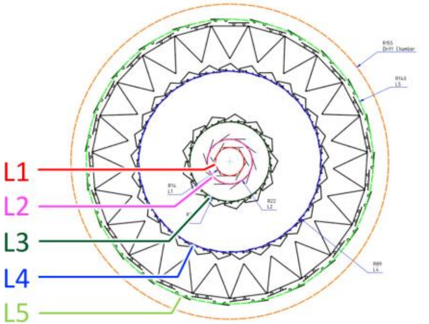
➔ Proposal for replacement of VXD = PXD (DEPFET sensors) + SVD(Double Sided Strip Detector) by VTX detector.

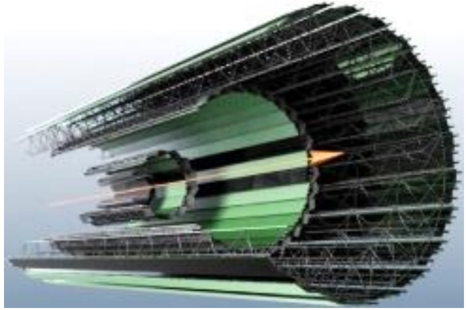
VTX proposal

Proposed BELLE II VXT upgrade scheme

- 5 straight layers with **D**epleted **M**onolithic **A**ctive **P**ixel **S**ensors
- Identical chips on all layers: Optimized BELle II pIXel (OBELIX) sensor
- ~1m² silicon surface

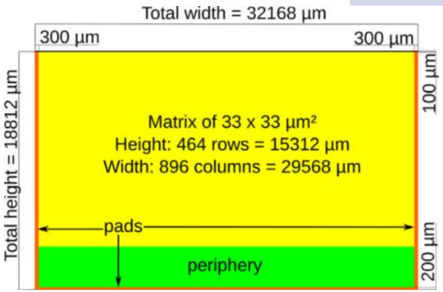
From simulations	Belle II VTX
Spatial res.	<10-15µm
Total material budget Inner-outer layers	0.1 – 0.8 %Xo
Max hit rate	120MHz/cm²
Time precision	<100ns
Trigger (freq.) (delay)	30 kHz 5-10µs
Rad. hard. (TID) (fluence)	<100 kGy/year $<50\times10^{12} n_{eq} cm^{-2}/year$
Power	<200mW/cm²





OBELIX

– Tower 180 nm process
– Extension of TJ-Monopix2
  → OBELIX sensor
– <40 µm pitch, 100 ns integration



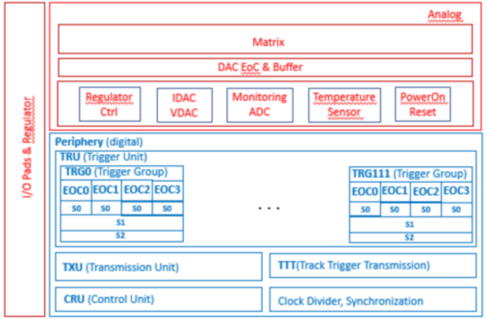
Key sensor specifications:

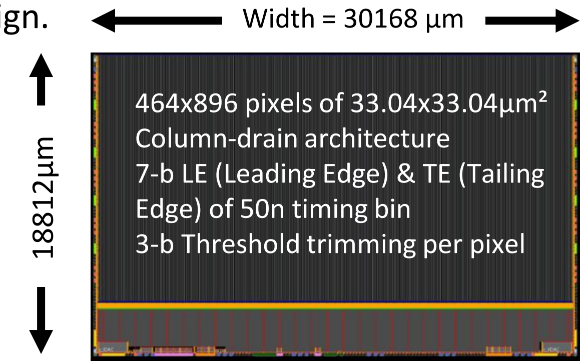
- Pixel pitch: *30-40 µm*
- Integration time: *≲100 ns*
- Power dissipation: *≲ 200 mW/cm²*

OBELIX (Optimized for BELle II pIXell)

- Developed from **TJ-Monopix2 sensor** (*Developed for ATLAS-ITK: doi: 10.1016/j.nima.2020.164460*)
- Increase **active area** from 17x17 mm² to 15x29,6 mm²
- LDO implementation on lateral sides for **power drop compensation** on ladder
- Re-design digital periphery for handling **VTX trigger requirements** with additional features: TTT (Track Trigger Transmission) & PTD (Peripheral Time to Digital)
- Additional analog functionalities for improved **monitoring and safety** : Monitoring ADC, Temperature sensor, Power On Reset

- **Design collaboration:** IPHC, CPPM, HEPHY, KEK, INFN, University of Bergamo, University of Pavia, University of Pisa, University of Applied Sciences and Arts Dormund, University of Bonn, University of Valencia
  - ✓ With their expertise in MAPS, Chinese laboratories are **candidate** for Belle II VTX contributing in different development aspects, such as chip characterization or system design.





Belle II VTX Organisation

Institutional Board

Project coordination
J. Baudot

Publications & Speakers
J. Serrano & WG leaders

WG1: Performance
V. Vobbilisetti
- Software
- Tracking
- Benchmarking

WG2: Sensor design
H. Pham
- Analog
- Digital
- Verification

WG3: Characterization and test system
G. Rizzo
- Irradiations
- Lab tests
- Beam tests

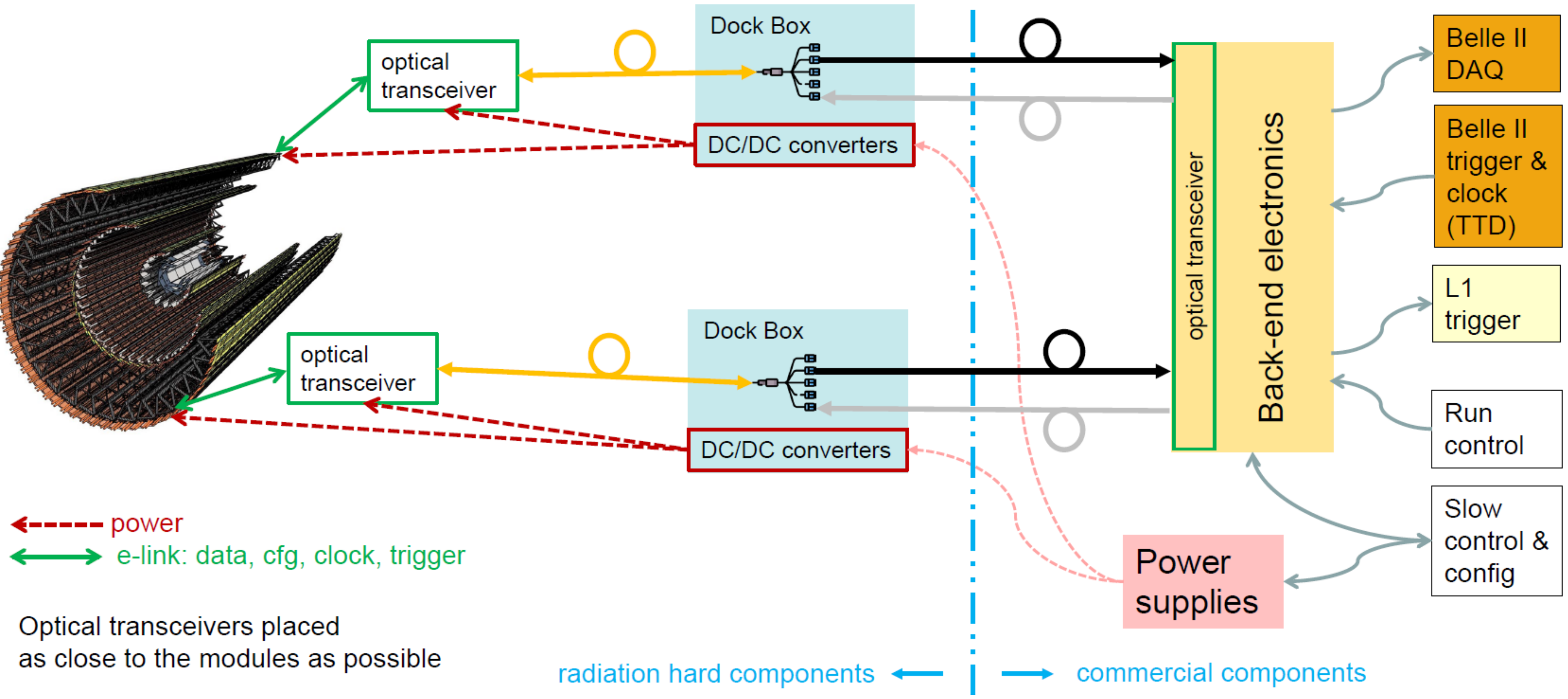
WG4: Layer development
S. Bettarini
- iVTX Electrical
- oVTX Electrical
- iVTX Thermomechanics
- oVTX Thermomechanis

WG5: System integration
C. Irmler
- Readout
- Track trigger
- Power & Grounding
- Cooling services
- Monitoring
- Slow control

WG6: Demonstrator
C. Marinas
- Full chain system
- High level tests

University of Bergamo
IHEP, Beijing
University of Bonn
University of Dortmund
University of Göttingen
DESY, Hamburg
University of Jilin
Queen Mary U., London
CPPM, Marseille
IJCLab, Orsay
RAL, Oxford
INFN & University of Pavia
INFN & University of Pisa
IFCA (CSIC-UC), Santander
IGFAE, Santiago de Compostela
IMSE-CNM-CSIC, Seville
IPHC, Strasbourg
KEK, Tsukuba
University of Tokyo IPMU, Tokyo
IFIC (CSIC-UV), Valencia
HEPHY, Vienna
ITAINNOVA, Zaragoza

VTX Readout Concept



Optical transceivers placed as close to the modules as possible

WG5: System Integration

- **Readout electronics**
  - Data readout
  - Chips configuration
  - Fast optical links
  - Interfaces to Belle II
    - DAQ
    - Trigger Timing Distribution (TTD)
    - Run / slow control
  - Track trigger
    - Transmit TTT data to Belle II trigger system
- **Powering, GND**
  - Power supplies for LV and HV, power cables
  - Grounding and shielding scheme
- **Monitoring**
  - Temperatures, voltages, currents, humidity, air and water flow, water leak, radiation, etc.
  - Hard-, firm- and software
- **Cooling services**
  - Chiller(s) and control unit for water cooling
  - Cold and dry air / N_2 supply
  - Piping (water and air)
  - Water leak detection
- **Run / slow control**
  - Entire software for control, monitoring, data acquisition and data quality monitoring
  - Server infrastructure for VTX operation

WG5 interest overview

- Dedicated WG5 meeting in May 2025
- 9 institutes interested to contribute to WG5
- USTC, Jilin University and IHEP presented activities and interests

			Interface board		Back-end electronics					
Group	Country	City	optical tranceivers for hit data readout	optical tranceivers for trigger data readout	hit data readout (DAQ)	trigger data readout (TDAQ)	Online software	Power supplies & grounding	Monitoring	Cooling services
HEPHY	Austria	Vienna	x		partially	partially	probably		partially	
CPPM	France	Marseille	x							
USTC	China	Hefei	x	x	?	x		x	x	
IHEP	China	Beijing		x		x				
Jilin University	China	Changchun					x			
IFIC	Spain	Valencia			x		x			
IFCA	Spain	Santander							x	x
IGFAE	Spain	Santiago	x		x					
ITA	Spain	Zaragoza						x		

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Physics requirements on the CEPC vertex detector

- Br (H -> cc) is extremely sensitive to the vertex design
- Br (H -> bb) is not really sensitive to the vertex design

Ref: *ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop 2019*

	Scenario A (Aggressive)	Scenario B (Baseline)	Scenario C (Conservative)
Material per layer/X_0	0.075	0.15	0.3
Spatial resolution/μm	1.4 - 3	2.8 - 6	5 - 10.7
R_{in}/mm	8	16	23

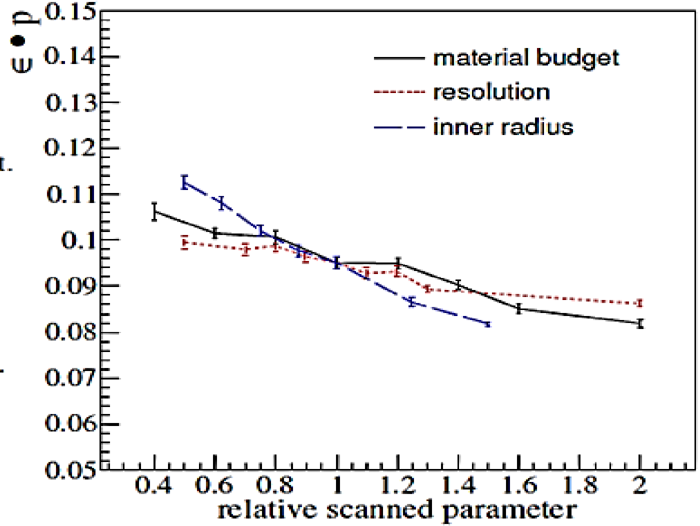
σ_{SP}< 3 μm very difficult

Table 3. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \to c\bar{c})$ measurement.

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.133 ± 0.002	0.095 ± 0.001	0.078 ± 0.001
	41%		-22%

Table 4. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \to b\bar{b})$ measurement.

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.925 ± 0.001	0.914 ± 0.001	0.900 ± 0.001
	1%		-1.5%

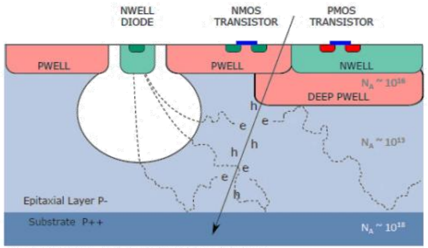


H-> ττ has similar analysis and results

$$\epsilon \cdot \mathrm{p} = 0.095(1 - 0.14\frac{\Delta x_{material}}{x_{material}})(1 - 0.09\frac{\Delta x_{resolution}}{x_{resolution}})(1 - 0.23\frac{\Delta x_{radius}}{x_{radius}})$$

Ref.: *ZG Wu et al., Study of vertex optimization at the CEPC, 2018 JINST 13 T09002*

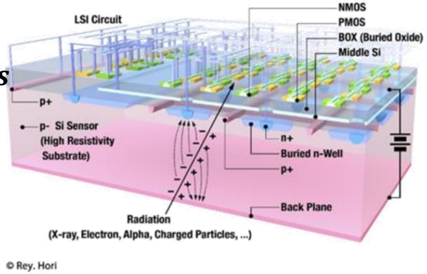
R&D for CEPC Vertex detector



pixel capacitance ≈5 fF (@ V_{bb} = -3 V)

HR-CMOS pixel sensor

- ***TowerJazz CIS 180 nm process***
- *Quadruple well process*
- *Thick (~20 μm) epitaxial layer with high resistivity (≥1 kΩ•cm)*
- *Thinning to 50 μm proved*



SOI-CMOS pixel sensor

- ***LAPIS 200 nm process***
- *High resistive substrate (≥1 kΩ•cm)*
- *Double-SOI / PDD-SOI layers available*
- *Thinning and backside process*
- *3D connection technology available*

Towards Baseline Requirements: CMOS and SOI R&D in Synergy

Fine pitch
Low power
frontend

+

Fast readout
architecture

⇓

Spatial resolution
thinning
Analog power

⇓

Readout speed
Digital power

⇓

Before 2020 ---- CPV1/2/3 (SOI)   JadePix1/2/3 (CMOS)   MIC4 (CMOS)   TaichuPix1/2 (CMOS)

2020-2025 ---------------- JadePix4/MIC5, TaichuPix3
CPV4-3D

	Pixel size	Readout Scheme
JadePix-3	16 X 23.1 μm^2	Rolling shutter
CPV-4	17 X 21 μm^2	AERD
JadePix-4	20 X 29 μm^2	AERD
TaichuPix-3	25 X 25 μm^2	Column drain

R&D for CEPC Vertex detector

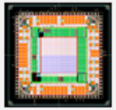
2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022

SOI pixel

Compact Pixel for Vertex

Double-SOI process

CPV1



$3\times3\ mm^2$

CVP2

SOI-PDD process

$6\times6\ mm^2$

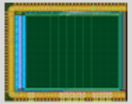
CVP3

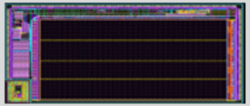
CVP4-3D

HR-CMOS pixel

Tower-Jazz CiS process

$3\times3.3\ mm^2$





Sensing node study

JadePix1

Small pixel size, in pixel digitization and low power design

JadePix2

$3.2\times3.7\ mm^2$

$10.4\times6.1\ mm^2$

JadePix3

JadePix4/MIC5

Fast readout, +time stamp (25ns)

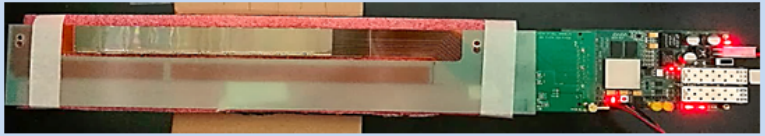
MIC4

TaichuPix1/2

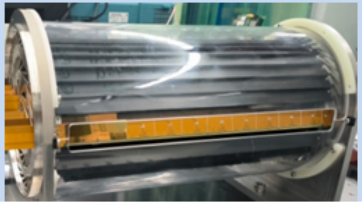
TaichuPix3

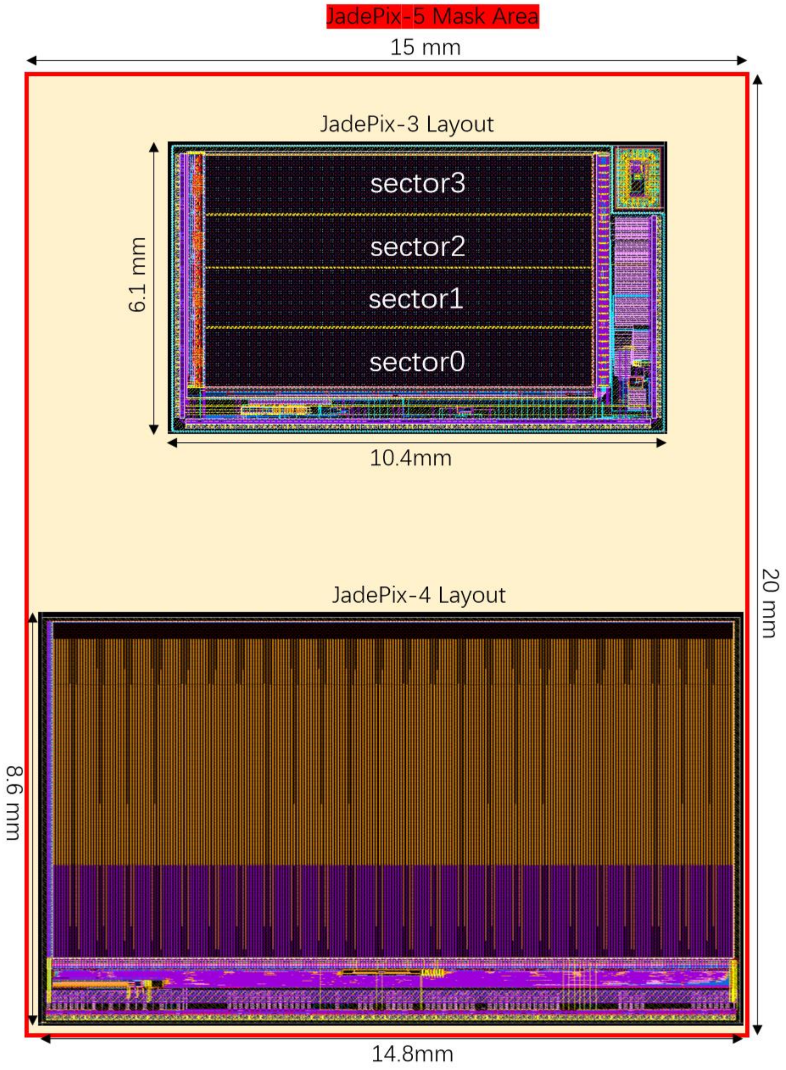
Ladder and prototype

Single-sided ladder with MIMOSA28 sensors, $0.39\%X_0$/layer



Double-sided prototype





JadePix-5

- The largest design of JadePix series
  - Pixel array 896 rows × 480 col.
  - Sensitive area 17.9 mm × 14.4 mm (86%)
- Functional blocks verified in JadePix-3/4
  - Sensing diode
  - Analog frontend
  - Pixel logic
  - AERD and DAC
- Optimizations on power distribution and signal driving
  - Voltage drop across the matrix
  - Signal transition on long metal lines
- Optimizations on peripheral readout
  - SRAM size and clock frequency

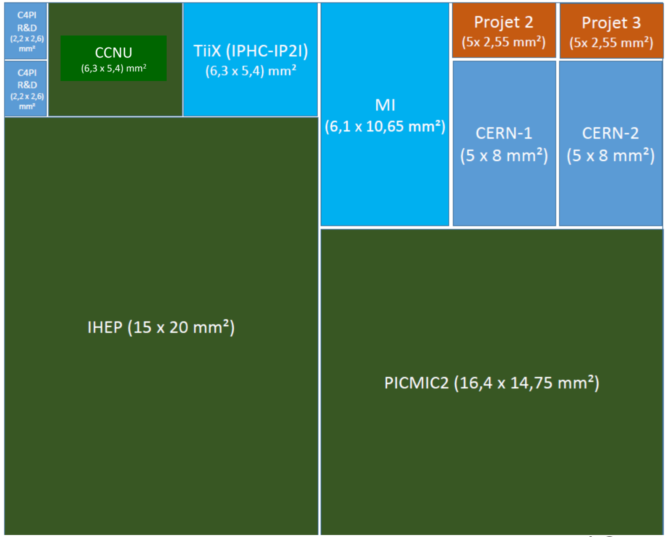
Shared submission and Technology discussion

➢ Shared submission to Tower 180 nm process (Engineering Run)

- <u>3/8 mask area </u>for IHEP team (2 cm x 1.5 cm)
- **JadePix-5 design** for CEPC R&D
- Submitted in Apr. 2025
- Paperwork for export license still ongoing with IPHC as coordinator

➢ Discussion sessions have been launched on demand and Visit in person during workshops

- Pixel 2024 workshop, Strasbourg, 18-22 Nov. 2024
- VTX workshop, Pisa, 15-17 December (to be announced)



Summary

- Common R&D efforts of monolithic CMOS Pixel Sensor for the e^+e^- collider experiments since 2010
  - BES III upgrade, ILC/CEPC, BELLE II upgrade

- 2 French groups and 3 Chinese groups involved in the BELLE II VTX upgrade
  - Chinese groups participated WG5 workshop and expressed interest on various tasks

- Large area MAPS chip JadePix-5 submitted to a shared engineering run coordinated by IPHC
  - JadePix-5 is one of two major chips on the same mask

Thank you for your time!