上海交通大学 SHANGHAI JIAO TONG UNIVERSITY | SJTUPA 上海交通大学物理与天文学院

Progress on the Hardware Development for the Timing-SDHCAL

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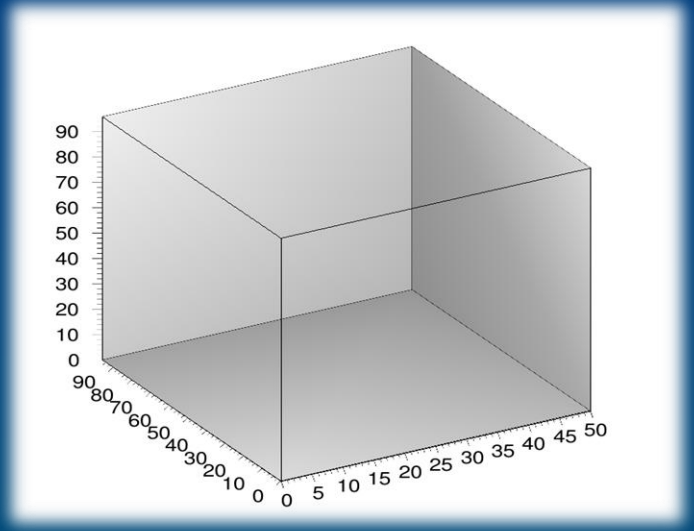
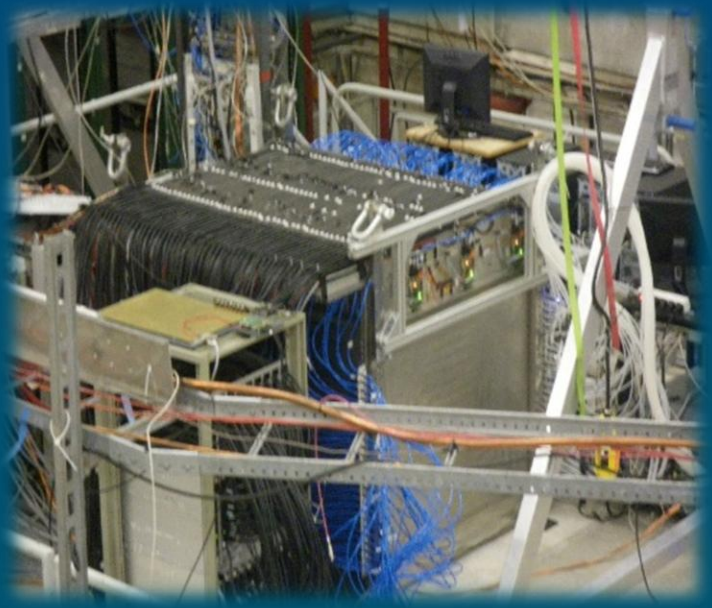
on behalf of SDHCAL Group

2025-07-24

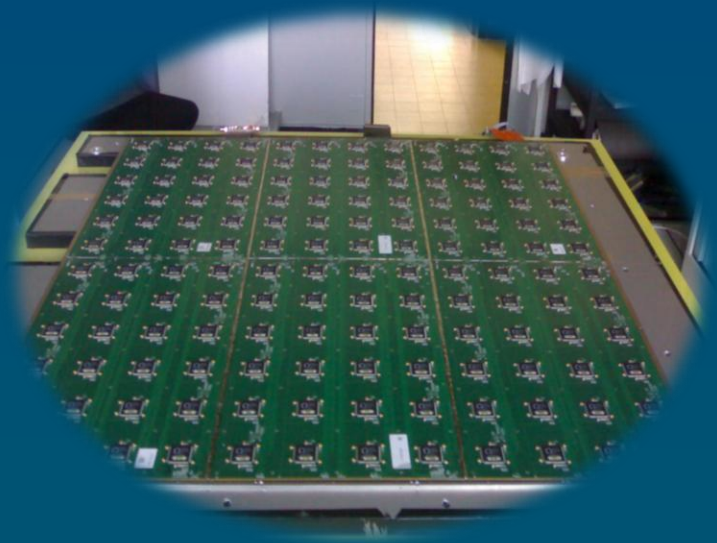
SDHCAL Main Characteristics

- SDHCAL is a high-granularity PFA (Particle Flow Algorithm) calorimeter
- Sampling calorimeter: Stainless Steel + Glass Resistive Plate Chamber
- $1m^3$ prototype has been built and tested
  - 48 layers (~$6\lambda_I$), 1 cm^2 granularity, 500000 channels





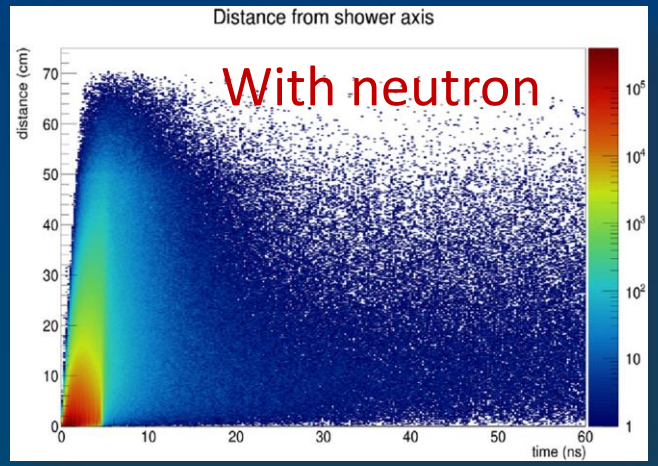
- Detector: GRPC operating in avalanche mode
- Embedded electronics:
  - PCB Top: HARDROC ASIC and related components
  - Semi-Digital Readout: 2bits - 3 thresholds (110 fC, 5pC, 15pC)
  - PCB Bottom: 1x1 cm^2 pads

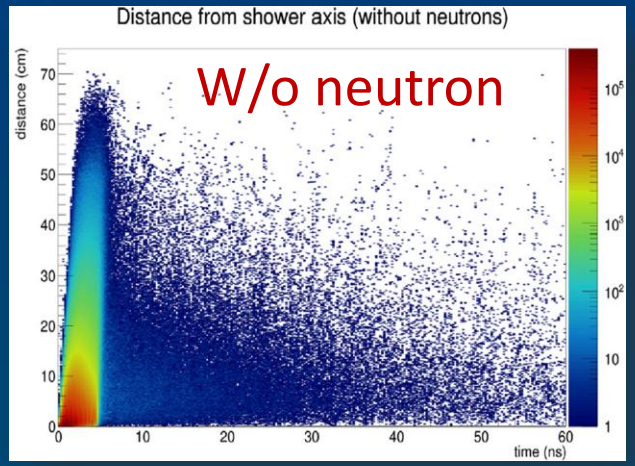


5D Calorimeter: Including Precision Time - Why?

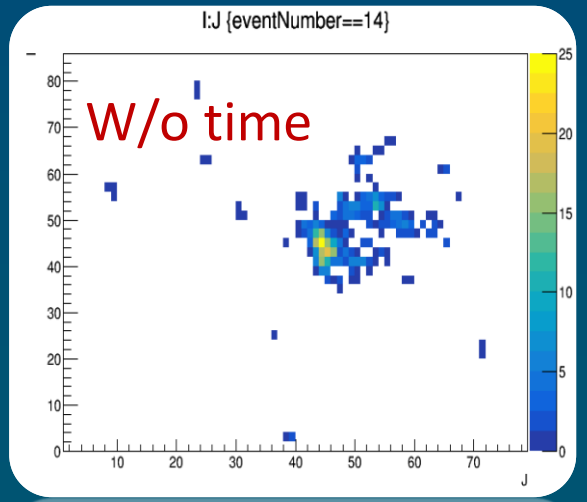
1. Precise time helps identify delayed neutron-induced showers and improve the energy reconstruction.

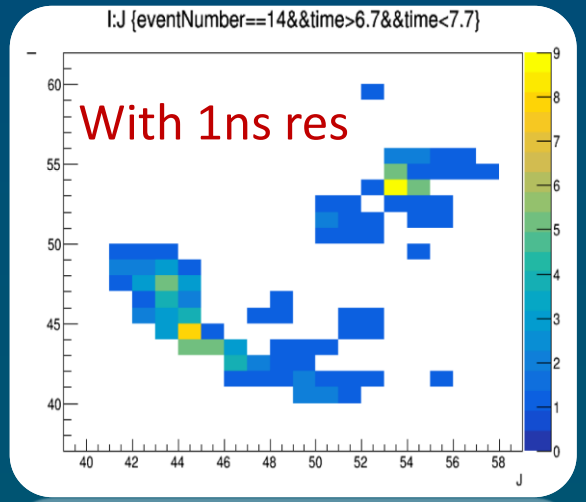
2. Precise time helps to separate nearby showers and reduce the confusion for a better PFA application.

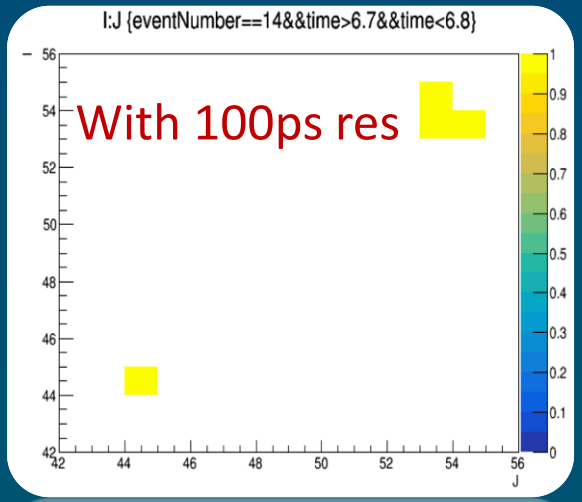




Example 1: Pi-(20 GeV), K-(10 GeV) separated by 15 cm in the SDHCAL detector(from Prof. Yong Liu @IHEP)







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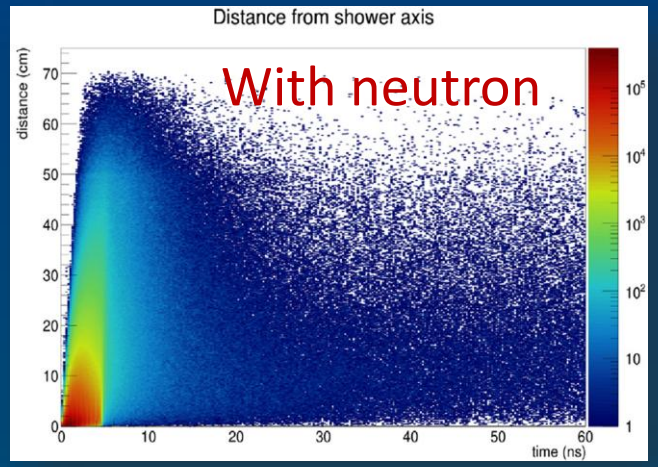
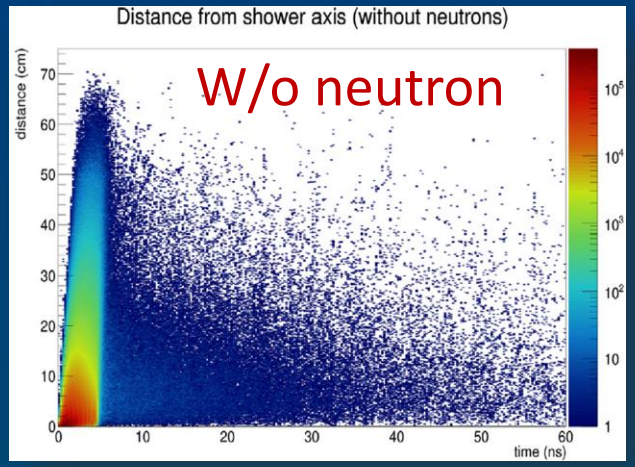
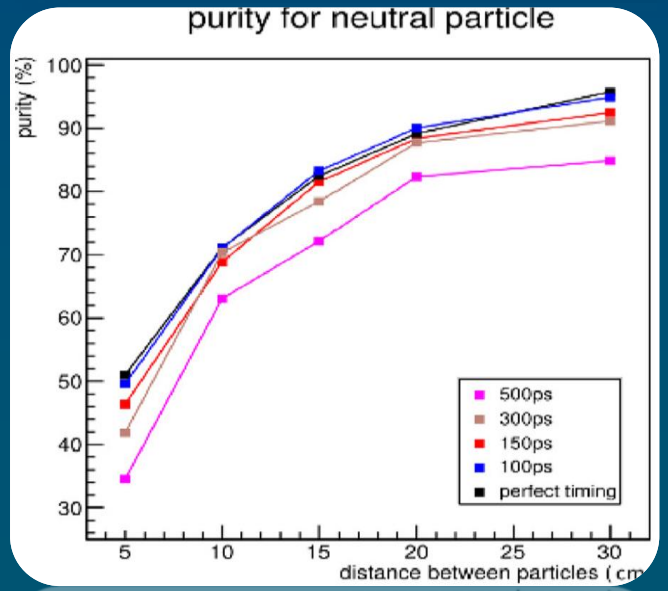
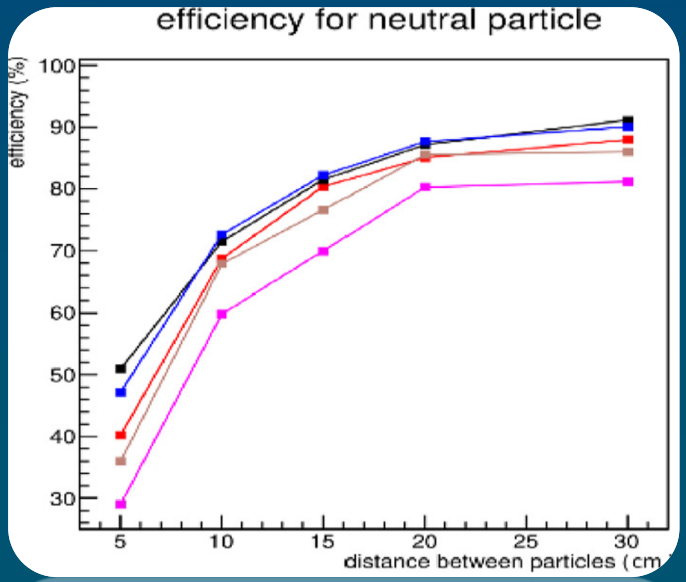




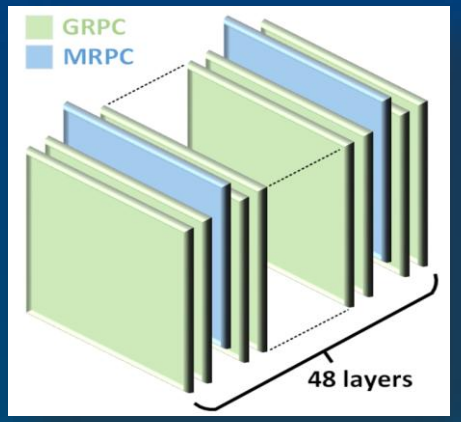
Example 2: Simulated purity and reconstruction efficiency for a 10 GeV neutral particle in the presence of a nearby 30 GeV charged particle in the SDHCAL

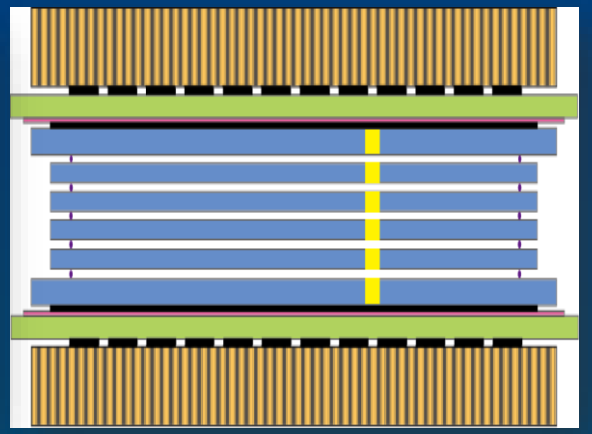


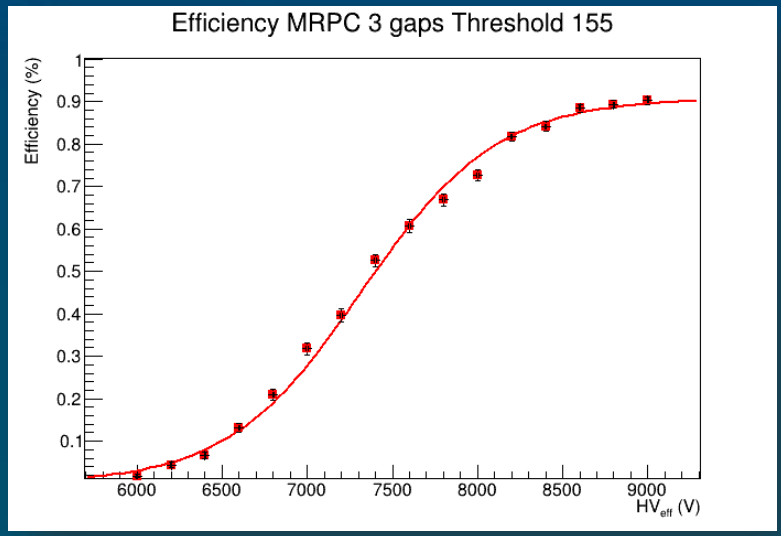


5D Calorimeter: Including Precision Time - How?

- Chambers: GRPC -> MultiGap GRPC
  - Improve the intrinsic timing of the calorimeter
  - Time resolution of better than 100 ps was obtained with 5-gap RPC by Tsinghua group
  - 3-gap MRPC detectors of 50 cm x 33 cm has been built and tested by Lyon group
  - 4-gap and 5-gap MRPC detectors have also been built and will be tested soon.

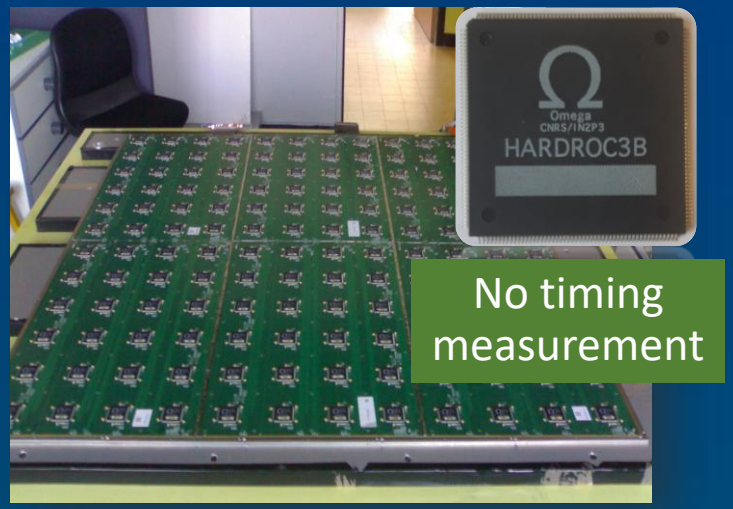






- Electronics: new front-end boards with timing ASICs
  - Timing ASIC: a fast preamplifier, precise discriminator and excellent TDC
  - High channel density, low power consumption

High Precision Time Measurement ASIC



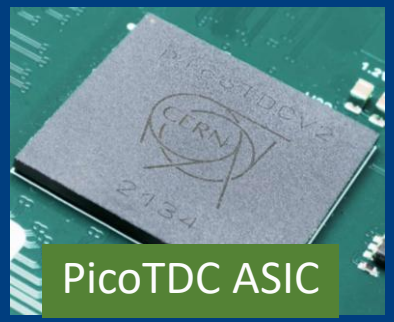
- Support high-precision timing ASICs:
  - ALTIROC, FastIC, PETIROC, TOFPET2, NINO, HRFlexToT, FlexToT et al.
- "Present" baseline: PETIROC
  - Only for exploring the MRPC performance and conception validation of the detector prototype
- Medium/long term possible option: LiROC+PicoTDC

PETIROC ASIC

- 32 channels
- Time resolution < 50ps
- Pros: On-chip TDC, QDC
- Cons: deadtime
- Power consumption: ~6mW/ch
- Developed at CNRS-OMEGA

LiROC ASIC

- 64 channels
- FWHM < 20ps



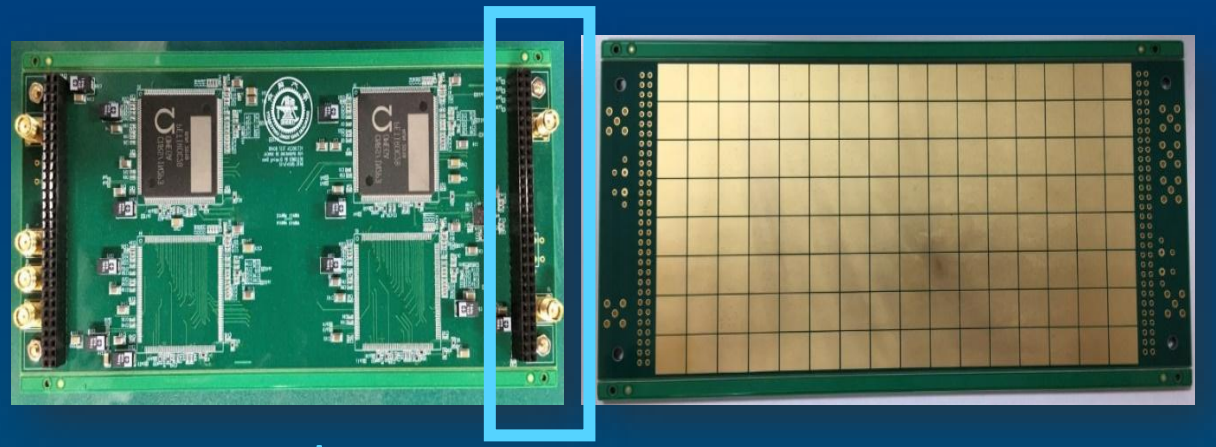
PicoTDC ASIC

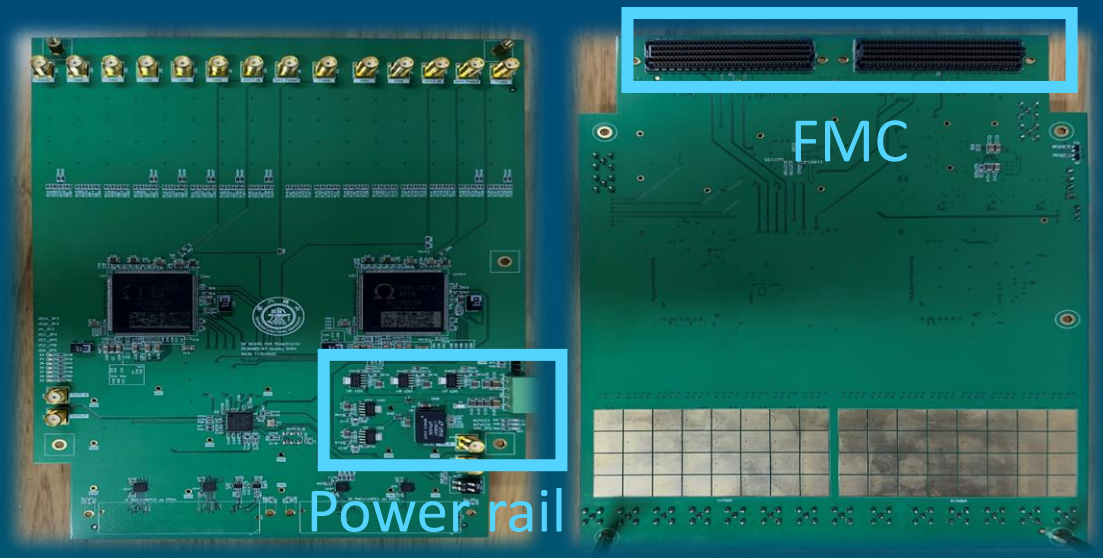
- 64 channels
- Timing res < 10 ps

Front-end Board (FEB)

- 1st-version of small FEB prototype
  - Cell size: 1cm x 1cm
  - Blind and buried vias
  - SMAs to inject signals
  - Jump cables for power &digital signals
  - Crosstalk issue in injection tests

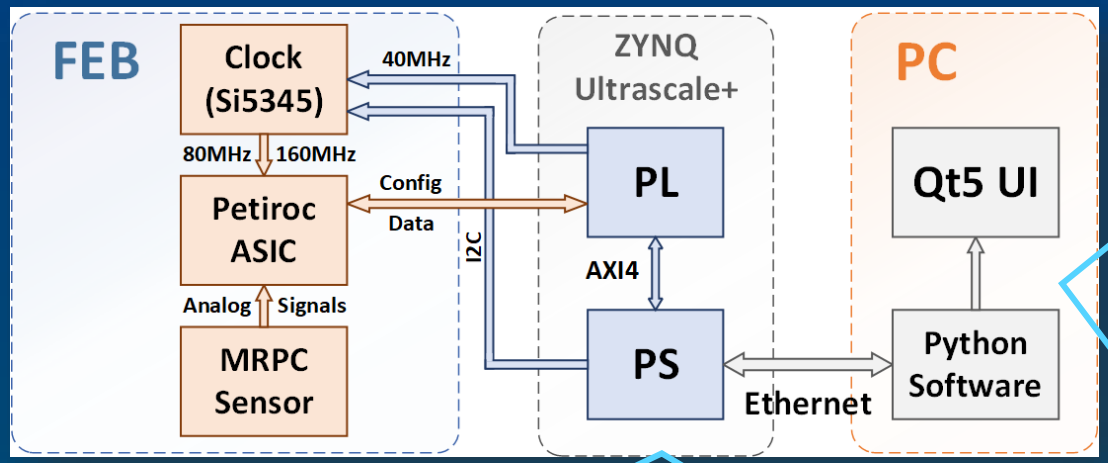
- 2nd-version of small FEB prototype
  - On-board power rails
  - Crosstalk issue fixed
  - Injection test
  - Commissioning test with MRPCs

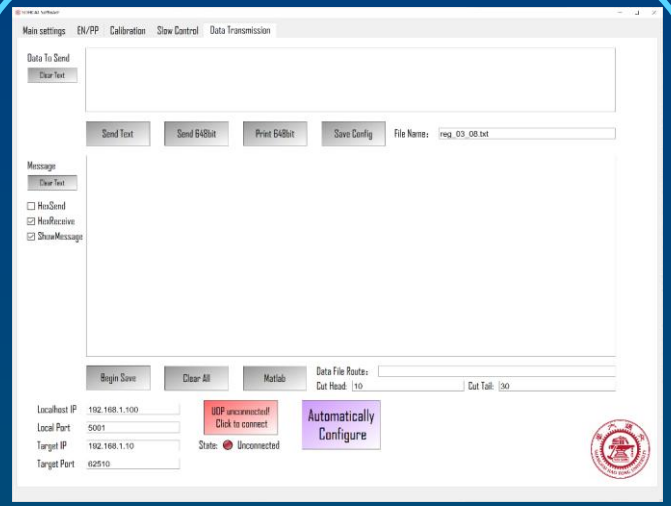


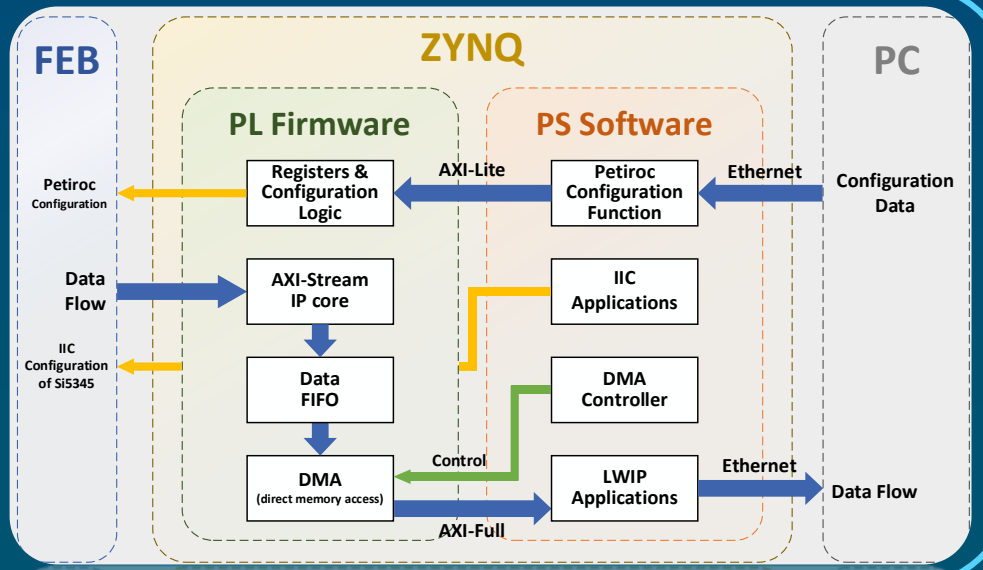


DAQ Development

A readout system has been developed based on Xilinx ZCU102 board.

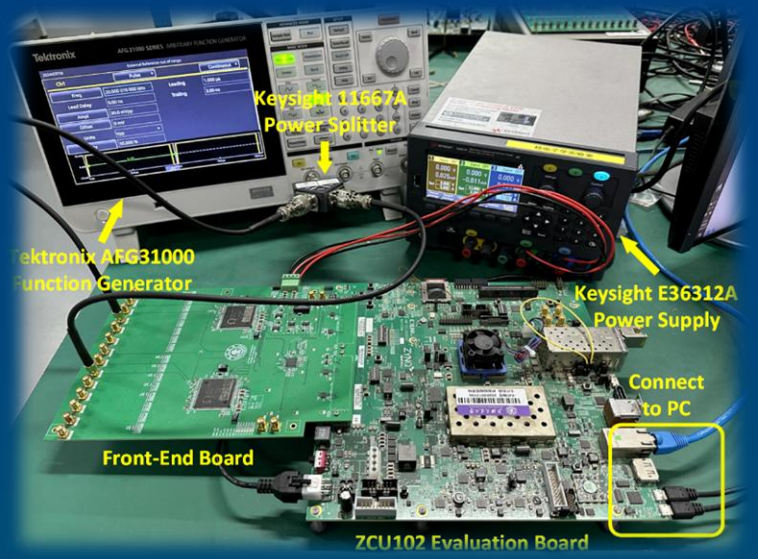


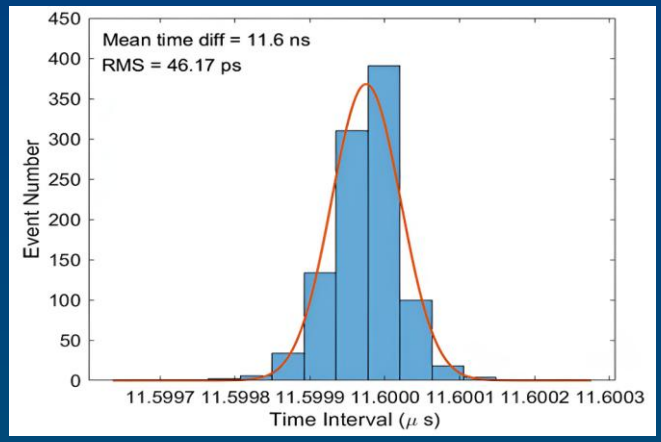


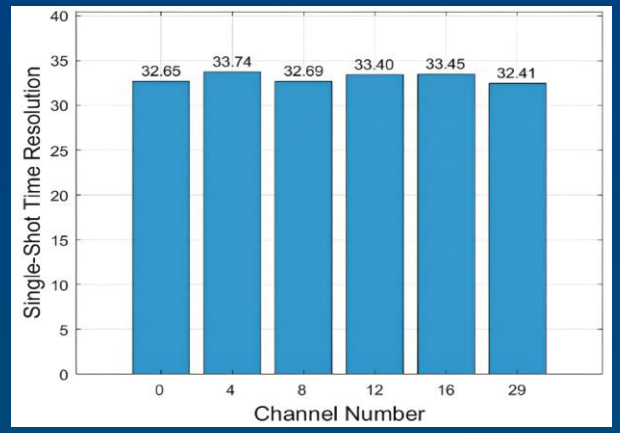


- Qt5 & PyQt
- Main functions:
  - Slow control
  - Data transmission
  - Calibration
- Multi-threading

Front-end Board (FEB) – Injection Test

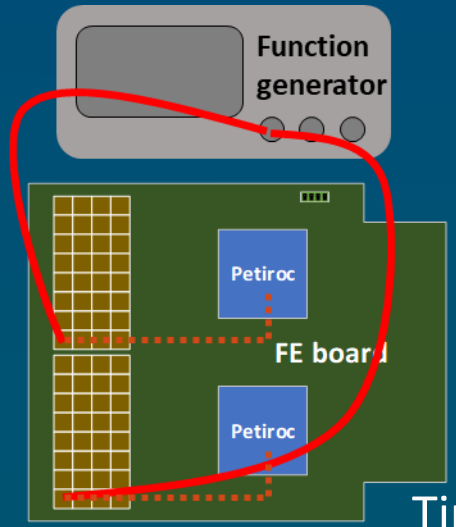


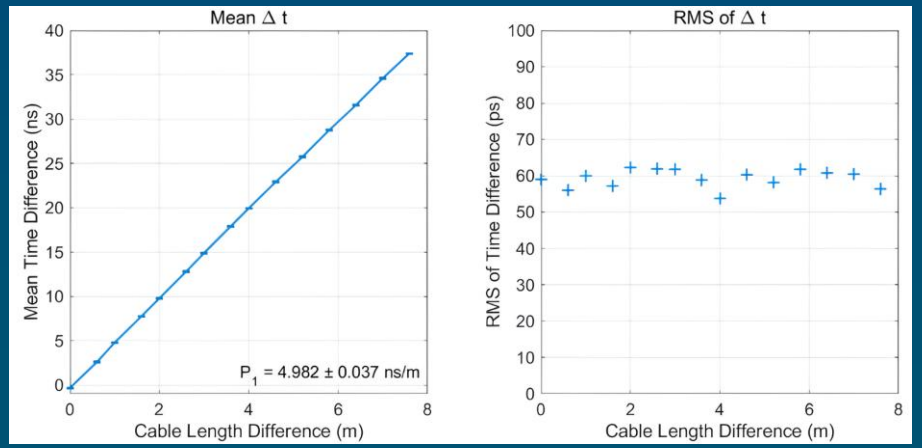




Time resolution across different channels： σ=33.06±0.54 ps

features	description
waveform	Negative pulses
frequency	20 kHz
duty	95 %
Amp	30 mVpp
rising edge	1 μs
falling edge	2 ns





Time resolution in multi-ch： $\sigma = 43.37 \pm 2.08$ ps

Front-end Board (FEB) – Cosmic Ray Test

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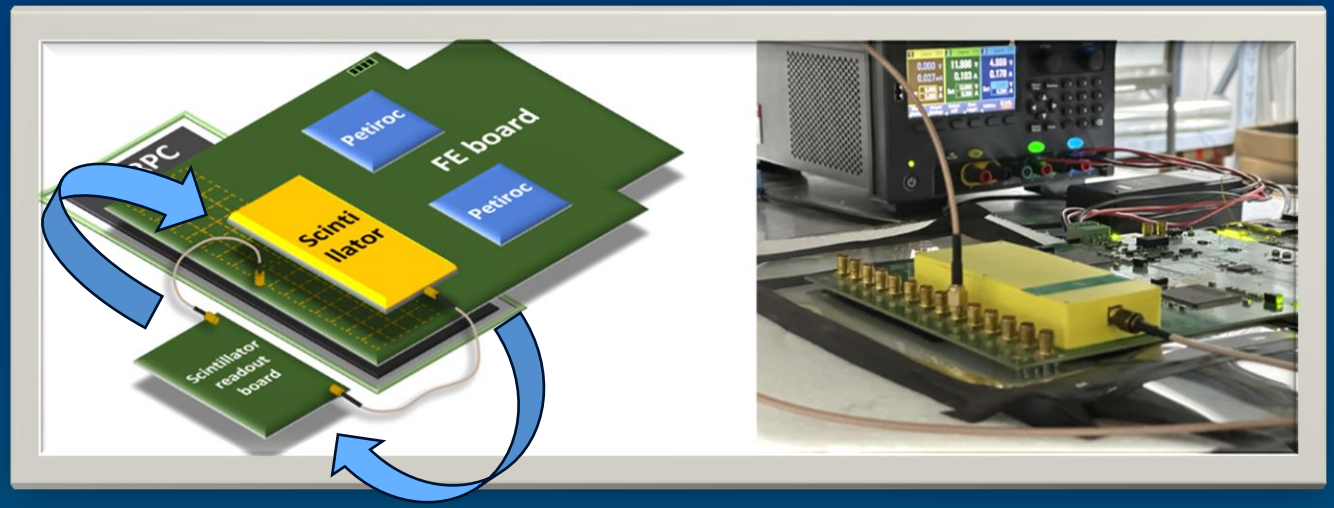
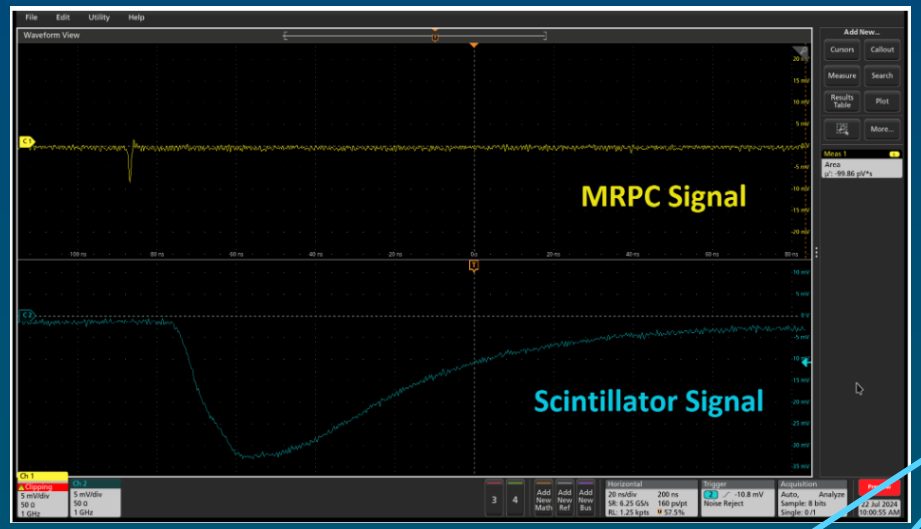
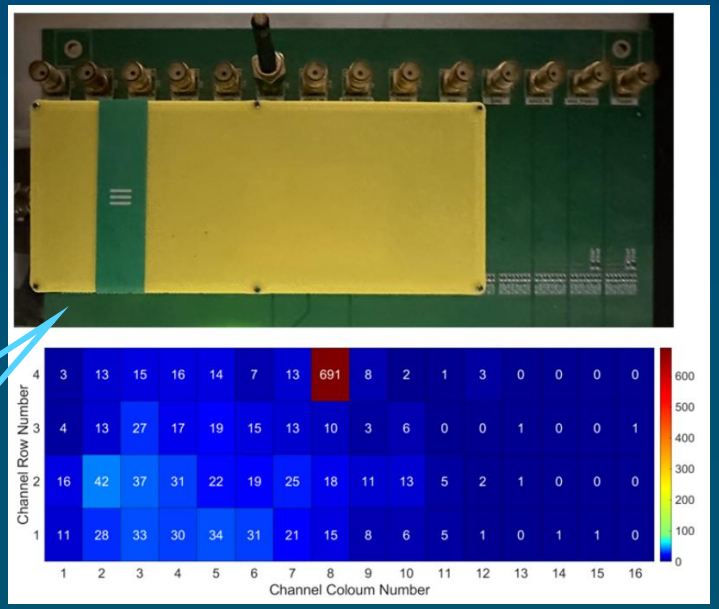
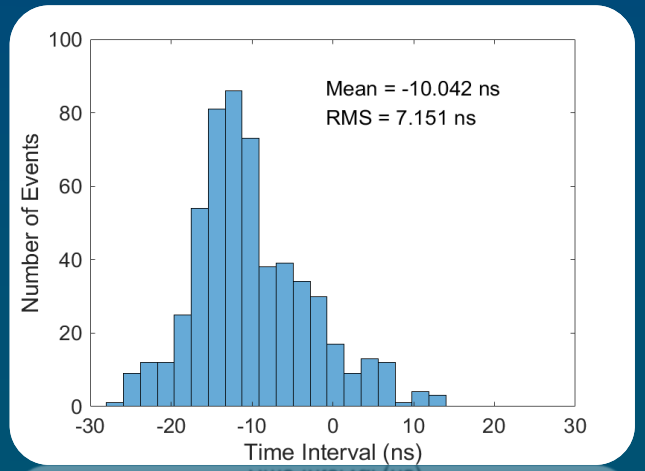
- Commissioning test with MRPCs
- Scintillator signal for specific-channel injection.
- Test time difference between scintillator and MRPC signals.



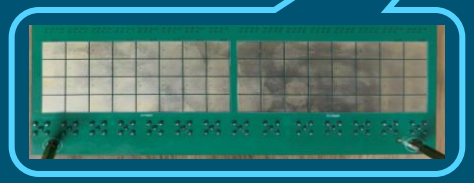






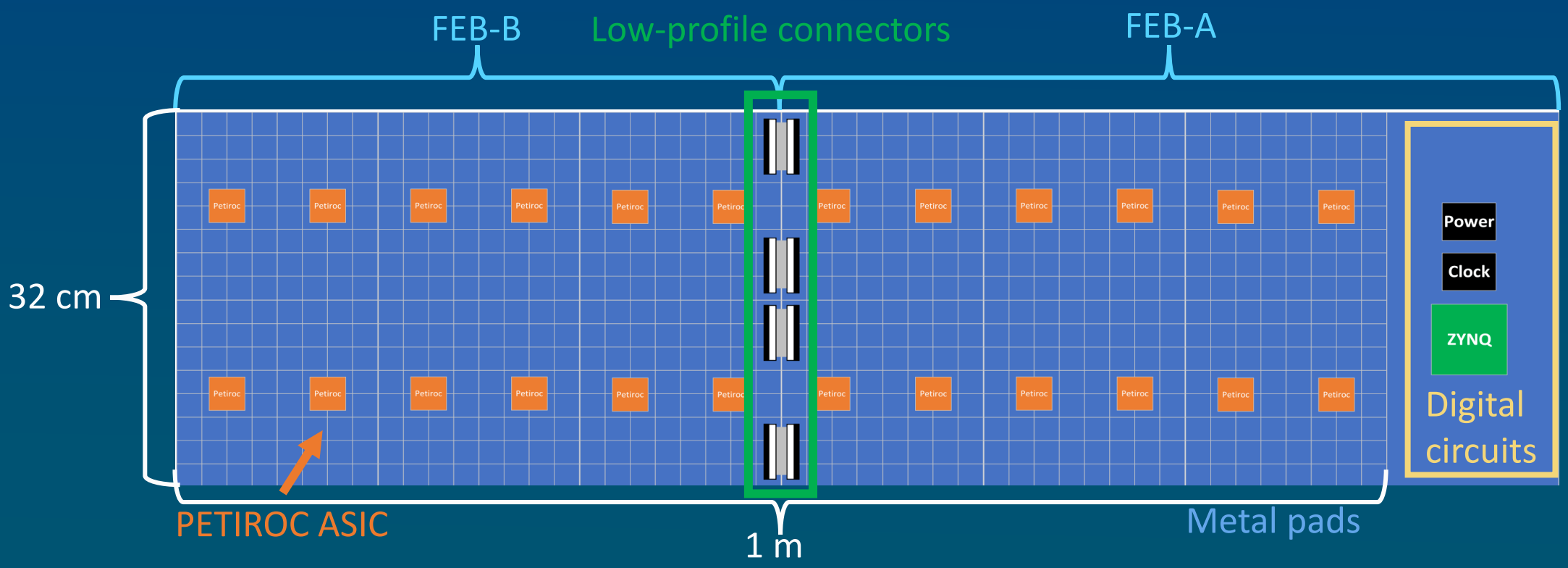
Statistical results of time differences between MRPC and scintillator signals

Metal pads on the bottom



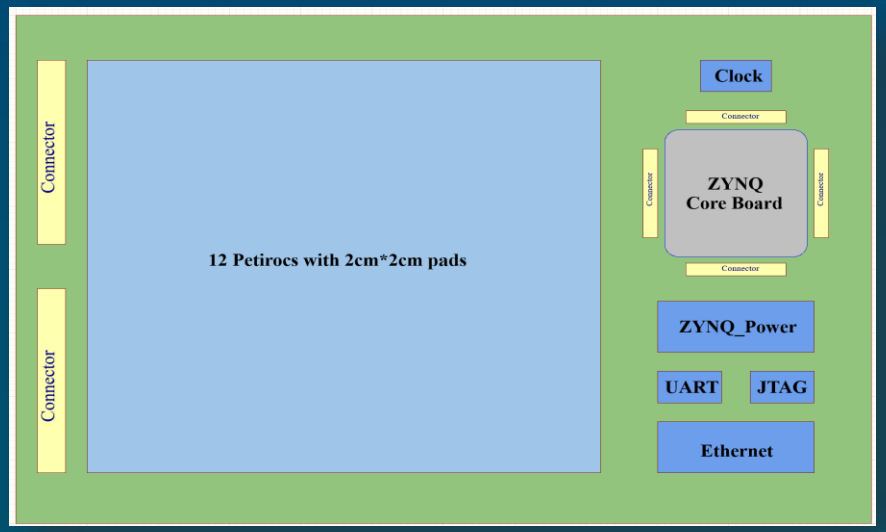
New larger FEB Development

- To match the MRPC size, larger FEB board need to be developed.
- Due to the limitation of PCB manufacturing, *two versions of the FEB* need to be designed, using high-density, low-profile connectors between them.



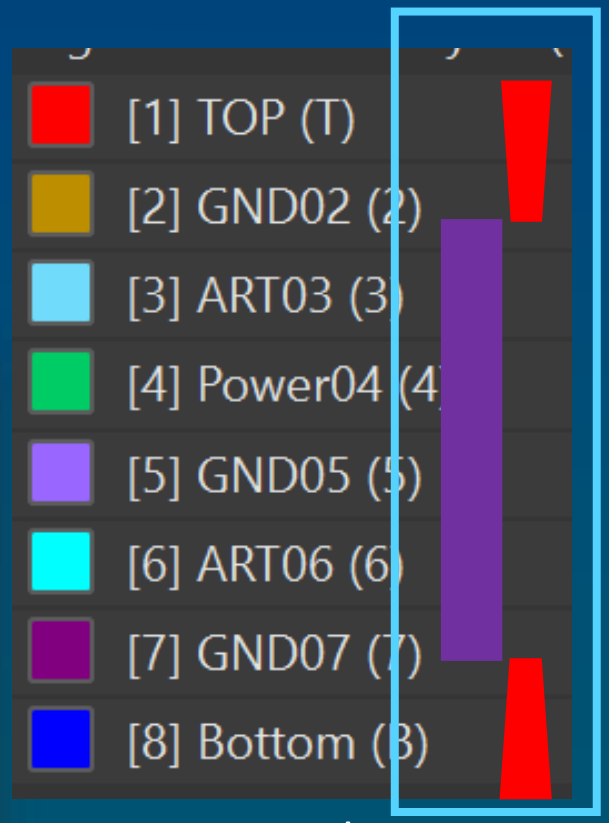
New larger FEB Development

- 1st-version of large FEB-A prototype has been designed and manufactured.
  - Size: 32cm x 50 cm
  - Cell size: 2cm x 2cm
  - Buried and laser vias
  - FPGA on board
  - Low-profile FCC connector

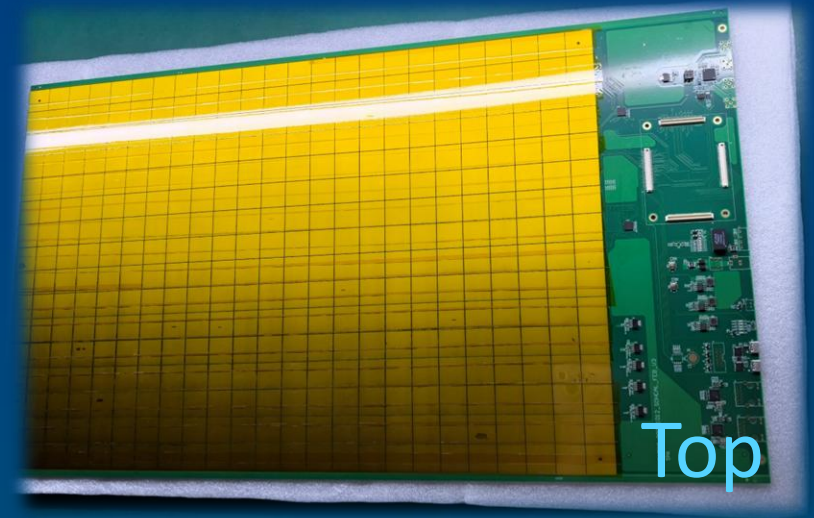


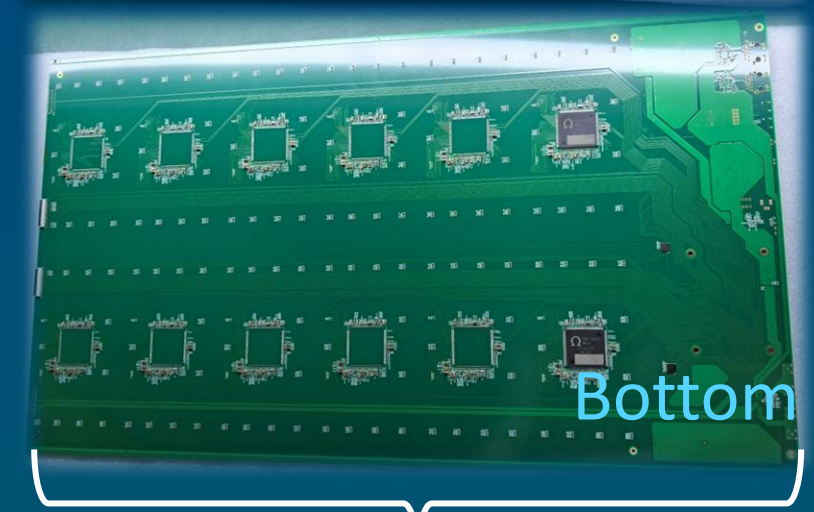
Functional block diagram

Blind and buried vias



PCB Stack-up





0.6 m

Test will be carried out soon

Summary

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- The SDHCAL is being upgraded into a Timing-SDHCAL, as precise timing is highly valuable.
- Two versions of small front-end boards (FEBs) based on the PETIROC ASIC has been developed and tested.
  - Injection tests show timing resolution < 50 ps
  - Commissioning tests have been performed with MRPC detectors
- A DAQ system based on Zynq FPGA and PyQT5 has been developed.
- A new larger-size of FEB has been developed and will be tested soon.

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T H A N K Y O U

Thank you for your attention!

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