Module Flex Update

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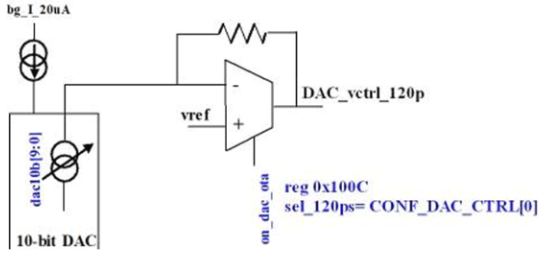
ALTIROC-A TID report

https://indico.cern.ch/event/1504990/contributions/6338792/attachments/3000670/5287693/Vctrl_External_R_22January2025.pdf

External resistors

TID tests: sensitivity of lsb with dose and dose rate, due to Vctrl variation: see Salah's presentation
https://indico.cern.ch/event/1504990/

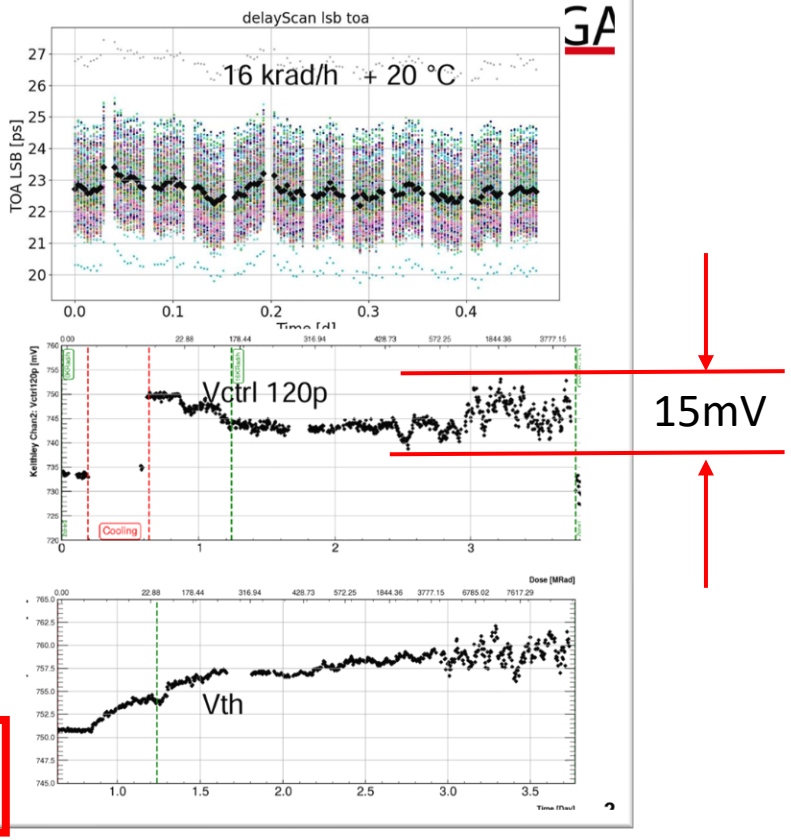
Vctrl provided by internal DAC, 2mV /DACU:



Same DAC architecture used to generate Vctrl (and Vth)
Vctrl (and Vth) voltages vary by a few mV under irrad

Large sensitivity of the toa lsb with Vctrl values : 3 mV variation => 1 ps variation

AltirocA: TDC bin with external resistors



- During TID tesing, Vctrl variation up to 15mV -> 5 ps

ALTIROC-A TID report

- Nathalie reported ALTIROC-A TID tests
  - https://indico.cern.ch/event/1518865/contributions/6391428/attachments/3021893/5331882/AltirocA_TID_ExtR_Feb2025.pdf

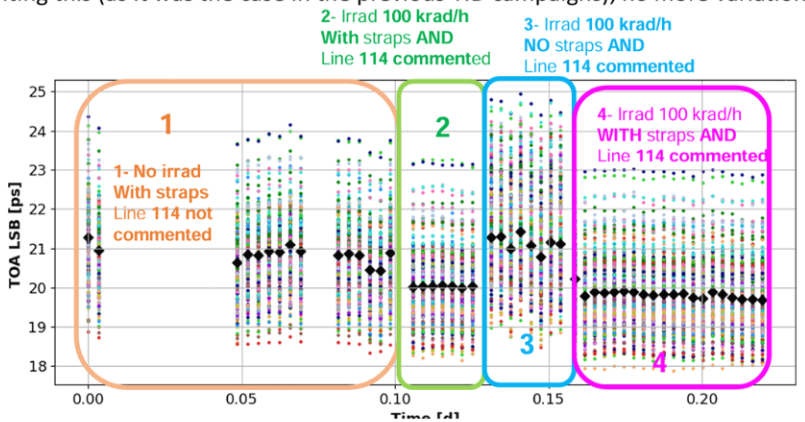
B100 TID tests: First conclusions

- External Resistors clearly help to limit the LSB variation to < 0.5 ps
- But still some variations, even without irrad
- These variations were due to a software issue: Automatic tuning of the Vctrl done for each delayScan and so Vctrl small variations

https://gitlab.cern.ch/atlas-hgtd/Electronics/FADA/-/blob/TOTRPG/firmware/FastFADA_ALTIROCA/scripts/runStability.sh?ref_type=heads#L114

```
108  ##################################
109  #monitoring probe
110  ##################################
111  echo $(date)'              monit. probe'  | tee -a $maindir"status.log"
112  sudo python3 scripts/monitoringProbe.py -b $board -o $dir --pixelOn $pixelOn --pixelInj col0 &>> $dir"/monitoringProbe.log"
113  echo $(date)'              monit. probe ana'  | tee -a $maindir"status.log"
114  sudo python3 analysis/anaMonitoringProbe.py  -i $dir/monitoringProbe/  --vctrlFile $vctrlFile  -o $dir/monitoringProbe/ &>> $dir"/monitoringPr
```

- After commenting this (as it was the case in the previous TID campaigns), no more variation when no irrad and also with 100 krd/h



Remarks: measurements on Friday done with cbits_slow set to 1011 for col 10 to 14

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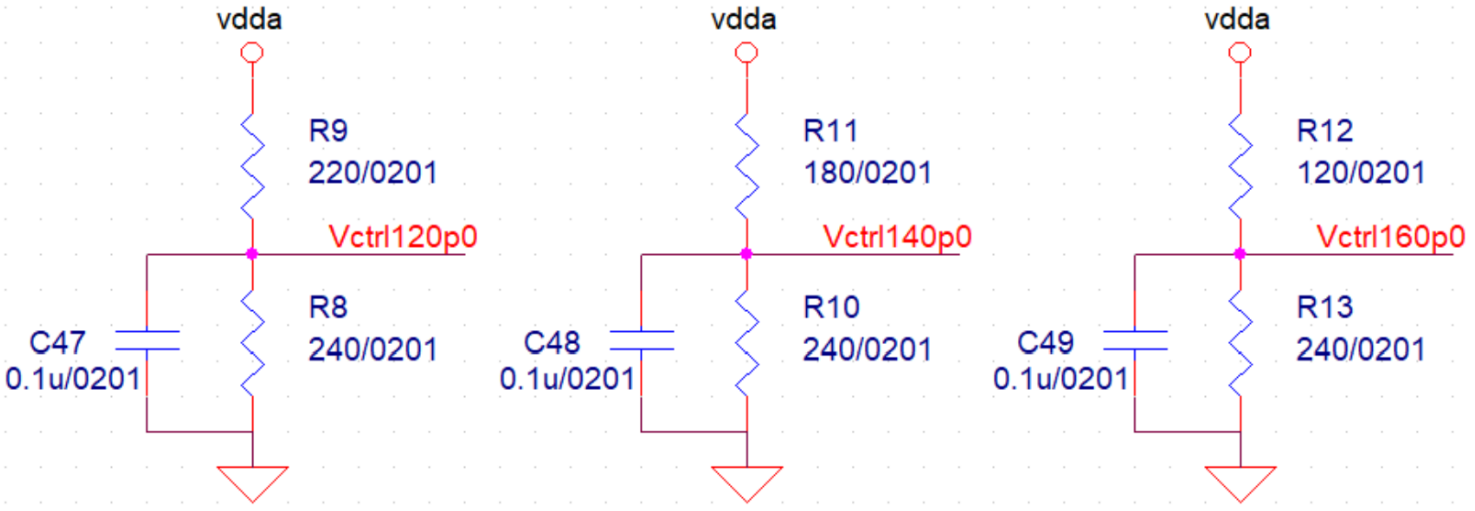
- Confirmed that need to use external resistors

Modification on the module flex

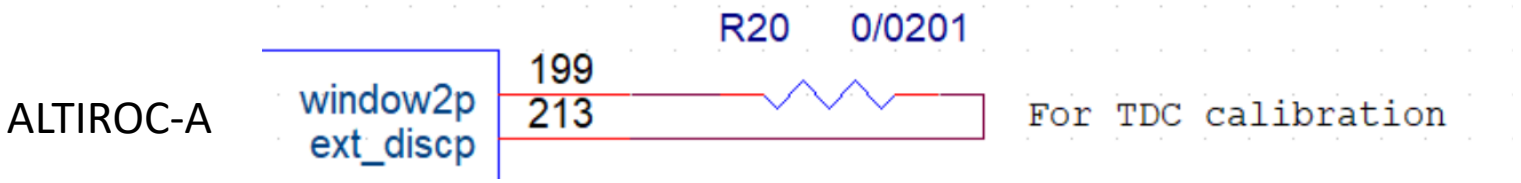
- Add 18 caps/resisters on module flex
  - 9 caps/resisters for each ASIC
    - 220 Ohm and 240 Ohm for **Vctrl120**, and 240 Ohm connects to GNDA.
    - 180 Ohm and 240 Ohm for **Vctrl140**, and 240 Ohm connects to GNDA.
    - 120 Ohm and 240 Ohm for **Vctrl160**, and 240 Ohm connects to GNDA.



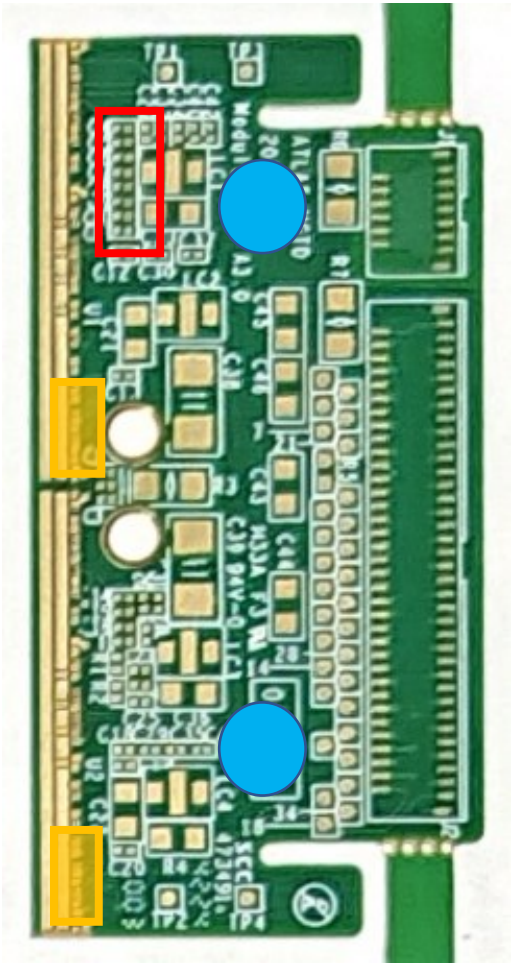
ETB scan for TDC calibration

- Joaquim reported External Time Base scan (ETBscan)
  - Correction strategy for TDC non-linearities
  - https://indico.cern.ch/event/1479316/contributions/6348416/attachments/3009907/5306548/ETBscan_v13.pdf

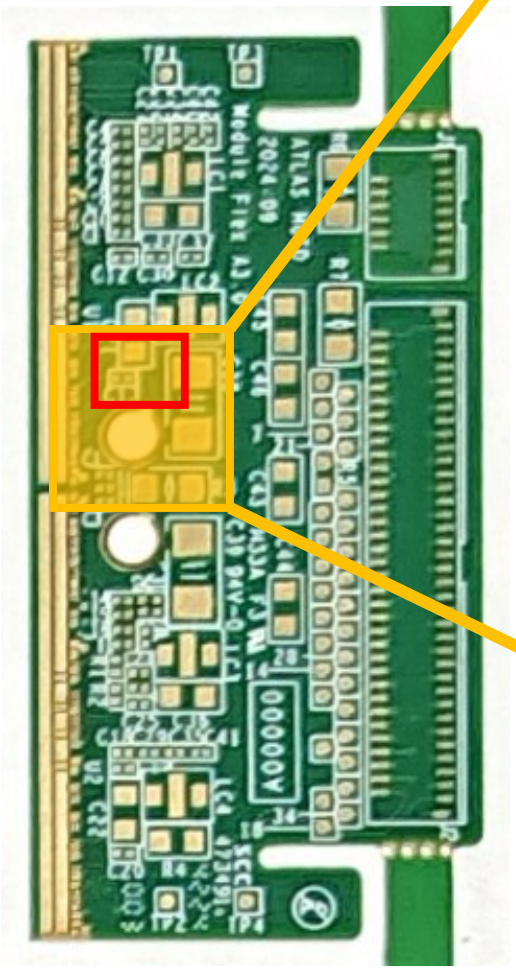
- Send “window2p” for instance into the "ext_disc_p" input through 0 Ohm

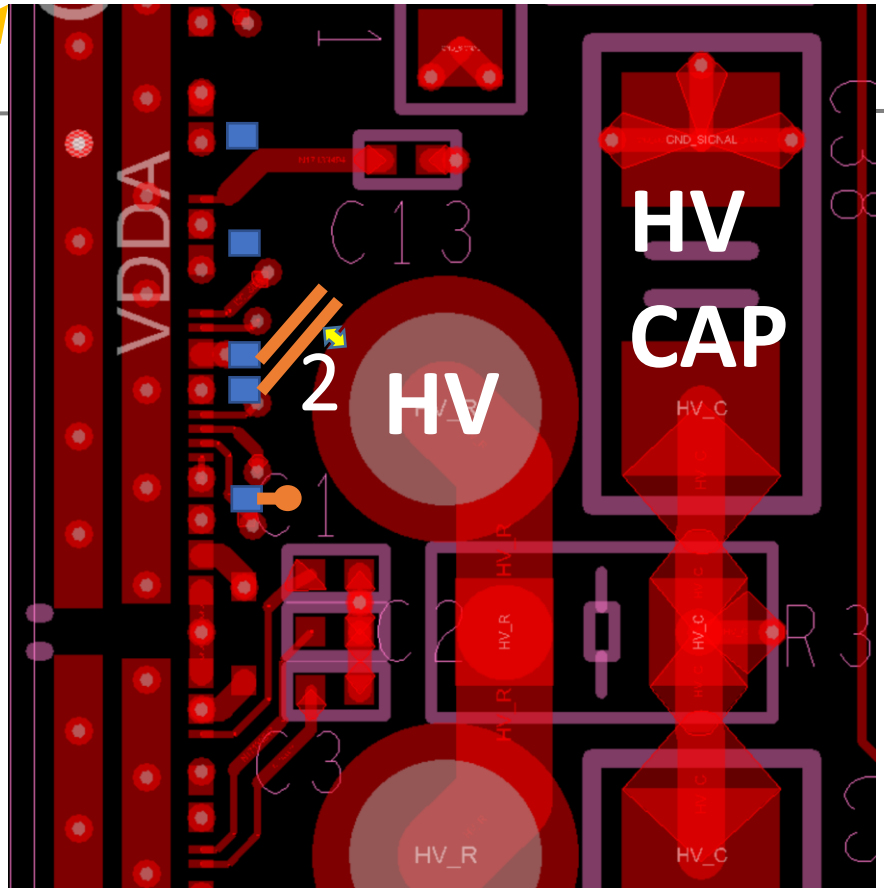


Surface occupancy for caps/resisters



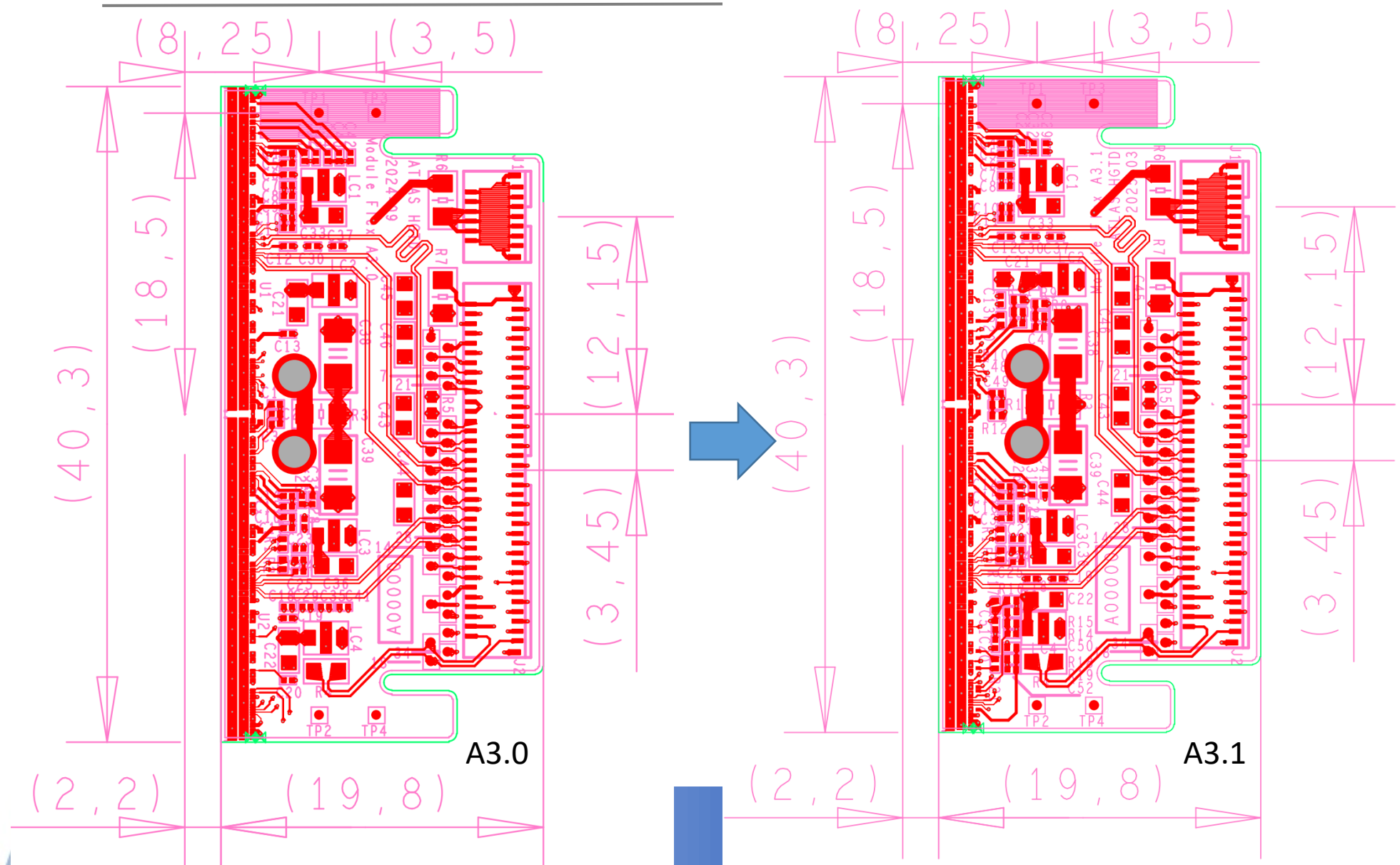
- Requested area
  - Caps/resisters size: 0201
  - Red square shows the area for 10 caps/resisters
- Orange square is the pin region to add
  - Pin 199 - windows2p
  - Pin 213 - ext-discp
  - Pin 229 - vctrl140p
  - Pin 231 - vctrl120p
  - Pin 247 – vctrl160p
  - Add the pad at the fourth column
- Other Caps changes
  - Caps for vcasc_pa, vcasc_disc, vbi_disc, vbo_disc removed
  - Cap for c_ext_por reserved
- For WB
  - Remove 4 wires
  - Add 5 other wires
- Blue circles are pick up areas for jig or SU
  - Keep as the same as before



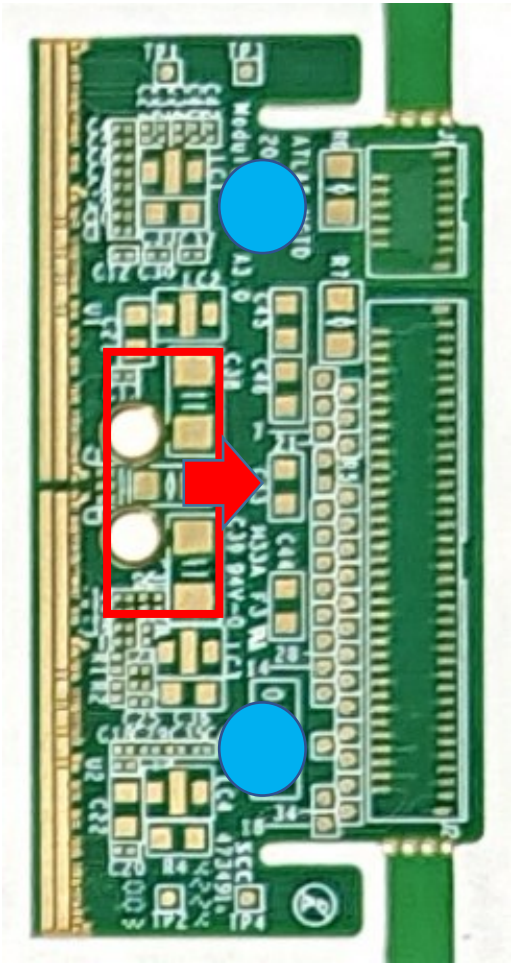


1. Need area to add 10 caps/resisters in the red square, too small
2. Safe distance between HV and the routings are too short. There is a risk of spark discharge.

PCB modification



Modification on Placement



- Move HV caps, resister and HV WB holes to right side by 0.75 mm.
  - Influence on DU design
- No changes on pick-up area

Short summary

- Finished schematics modification
  - https://gitlab.cern.ch/atlas-hgtd/module-assembly-loading/-/blob/master/hgtd-module_flex/A3_1/module_flex.pdf
- Finished wire-bonding modification
  - Add 5 pins for each ASIC at the fourth column
  - https://gitlab.cern.ch/atlas-hgtd/module-assembly-loading/-/blob/master/hgtd-module_flex/A3_1/altirocA_wb_20250305.xlsx
  - Each site of assemble group MUST check the feasibility for WB
- PCB modification
  - Move the HV caps to right by 0.75 mm (For area and HV safety)
  - Influence on DU design
  - No Influence Jig head
- New 3D model released
  - https://gitlab.cern.ch/atlas-hgtd/module-assembly-loading/-/blob/master/hgtd-module_flex/A3_1/MODULE_FLEX.stp

Thank you for your attention